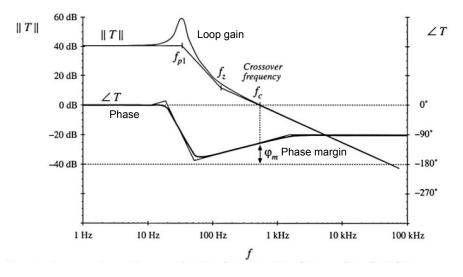
C200/C220 Compensator Design: Voltage Mode Control

Sep 2nd 2022

Bode Plot Basics

• Why compensator?

- In a Voltage regulator, the output filter (Lout, Cout) and the PWM modulator create the converter forward plant
- Bode plots (loop gain and phase) are employed to analyze the frequency response of this linear system
- In the loop, a Compensator is inserted to ensure stability and dynamic performance





Compensator Design Example

•Power component: C200/C220

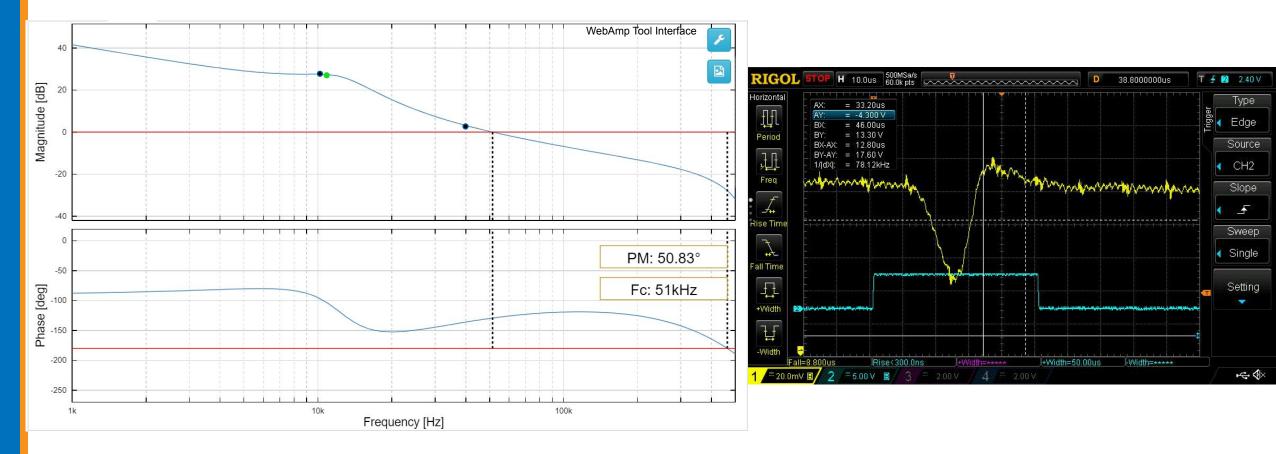
- •Vin = 12 V
- •Vout = 1.3 V
- •f_SW = 571 kHz
- •Lout, L= 1.1 uH
- •DCR = 3.15 mΩ
- •Cout, C = 4x47 uF
- •Resonant frequency f_LC=1/($2*\pi*\sqrt{LC}$) = 11 kHz
- •Load: 0 5 A

•Voltage mode compensator parameters: f_{Z1} , f_{Z2} , DC Gain



Compensator Design 1

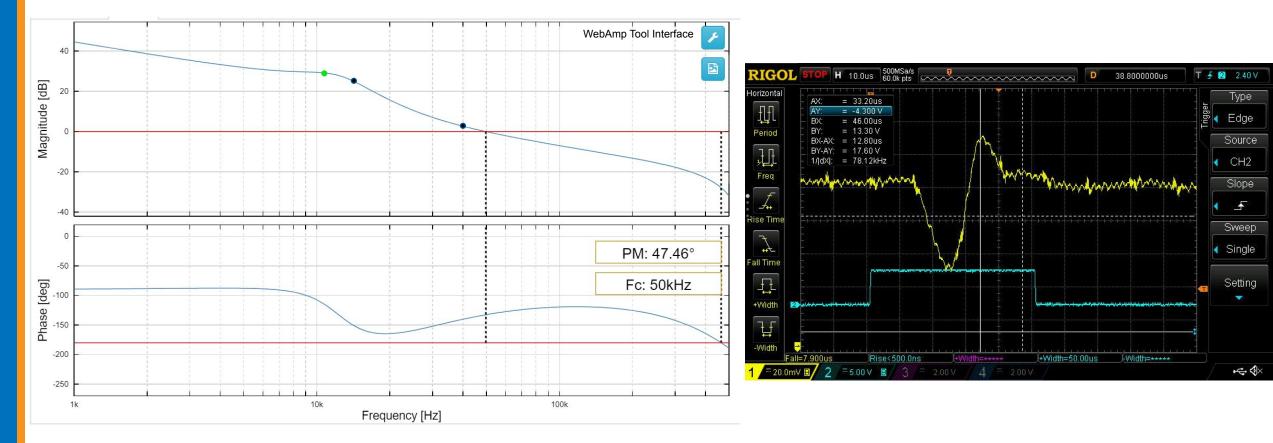
Gain = 650 Z1 = 10.6 kHz Z2 = 40 kHz





Compensator Design 2 - Increasing f₂₁

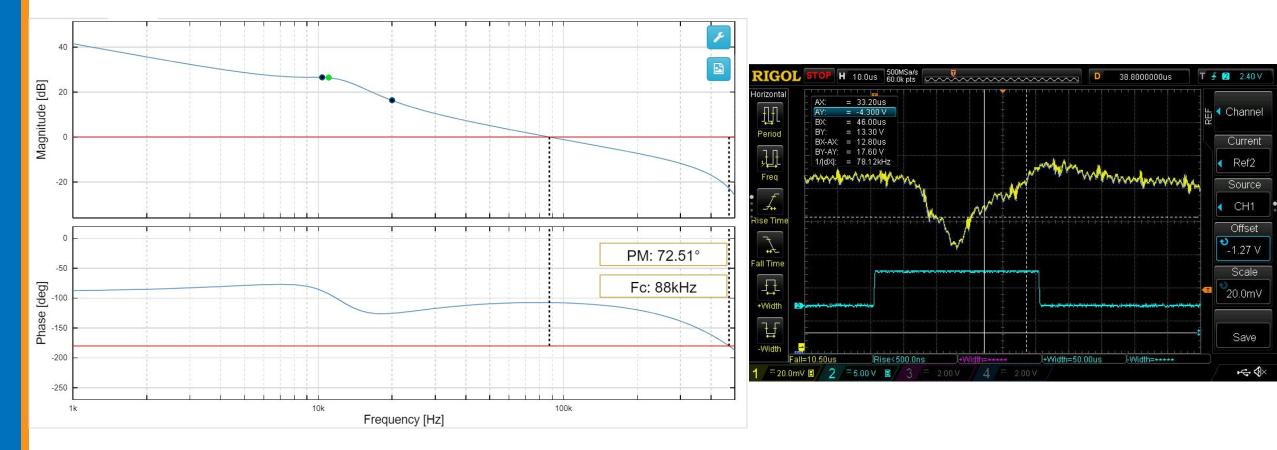
Gain = 650 Z1 = 15 kHz Z2 = 40 kHz





Compensator Design 3 - Decreasing f₇₂

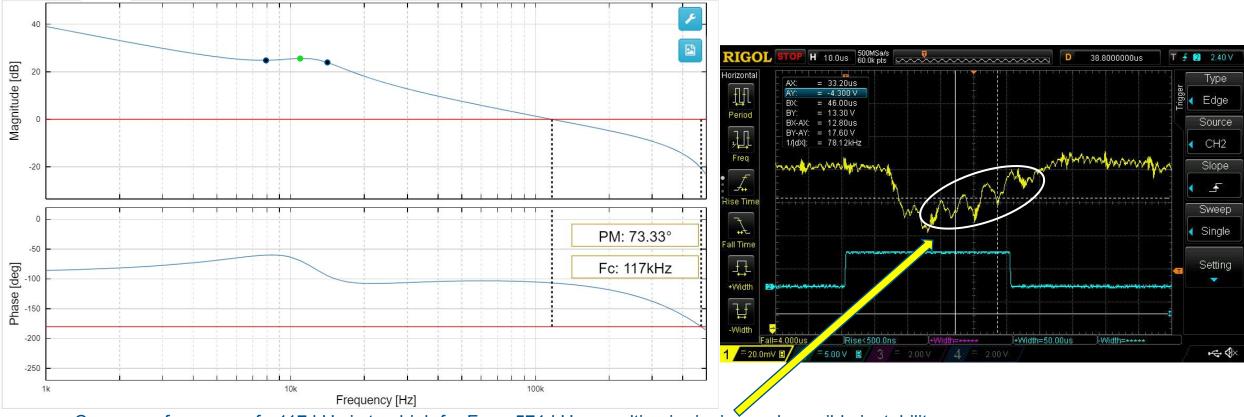
Gain = 650 Z1 = 10.6 kHz Z2 = 20 kHz





Compensator Design 4 - Decreasing f₇₁ and f₇₂

Gain = 650Z1 = 8 kHzZ2 = 15 kHz



- Crossover frequency, $f_c = 117$ kHz is too high for $F_{sw} = 571$ kHz, resulting in ringing and possible instability
- Thumb-rule: choose $f_c \leq F_w/10$ Bode plot is based on linear modeling, PCB parasitics and other non-linearities affect Bode plot accuracy beyond frequencies = $F_w/5$

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Effects of different Gain settings

Z1 = 10.6 kHz Z2 = 40 kHz

Gain	PM (deg)	Fc (kHz)
650	51	51
800	54	60
950	57	70

• Increased DC Gain increases crossover frequency, f_C



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Compensator Design Steps

- 1. Place first zero, f_{Z1} , slightly below filter's resonant frequency, $f_{LC}=1/(2*\pi*\sqrt{LC})$
- 2. Place second zero, f_{z_2} at around $f_{sw}/12$
- 3. Modify DC gain to obtain desired crossover frequency
- Recommendations:
 - Crossover frequency (F_c):
 - Optimal: $0.05*f_{sw} < F_c < 0.1*f_{sw}$
 - Acceptable: $0.03*f_{SW} < F_c < 0.12*f_{SW}$
 - Phase Margin (PM):
 - Optimal: PM>45°
 - Acceptable: PM>35°