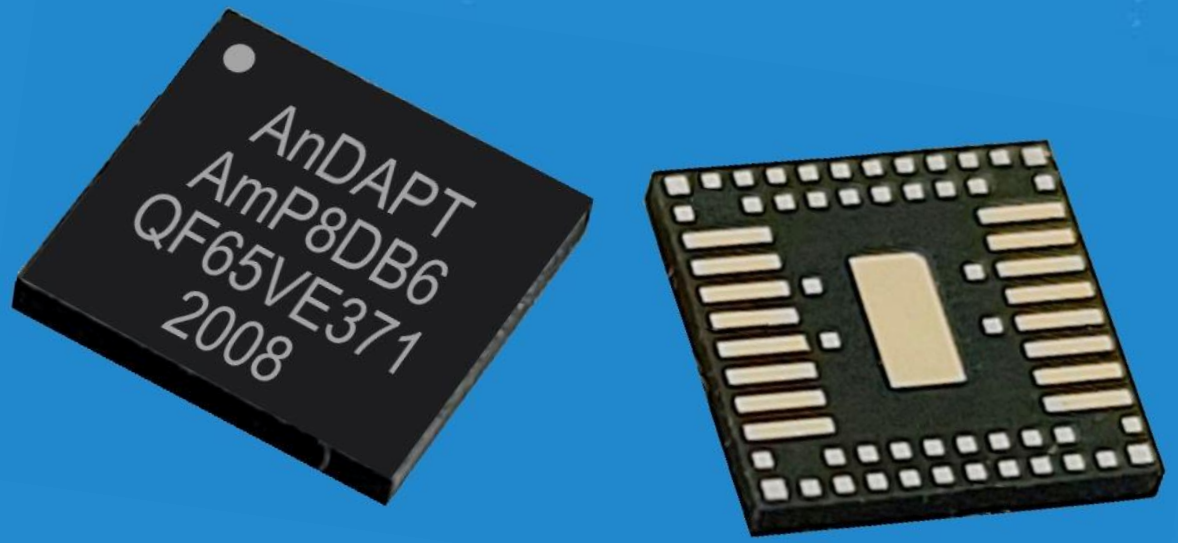


AnDAPT Power Solutions for Microchip PolarFire FPGAs/SoCs Use-case:

Ease-of-Use

ARD_M_MPF_A3

Bench Data

AnDAPT

Microchip PolarFire Power Specifications*

#	sequence	Rail	Power Component	Input Voltage (V)	Output Voltage (V)	Full Load (A)	DC tolerance (±)	AC Tolerance (±)
1	1	VDD	C200 (Sync buck)	12	1	6	1 %	2 %
2	3	VDDA	C200 (Sync buck)	12	1.05	2	30 mV (total)	
3	2	VDD25 (VDD25, VDDA25, VDD_XCVR_CLK)	C200 (Sync buck)	12	2.5	2+0.2*	1 %	2%
4	4	VDDAUXX	C150 (Async buck)	12	3.3	4	5 % (total)	
5	5	HSIO_GPIO (VDDIX_GPIO, VDDIX_HSIO, VDD18)	C710 (SIM LDO)	2.5	1.8	0.2	5 % (total)	

* 0.2A for LDO output #5

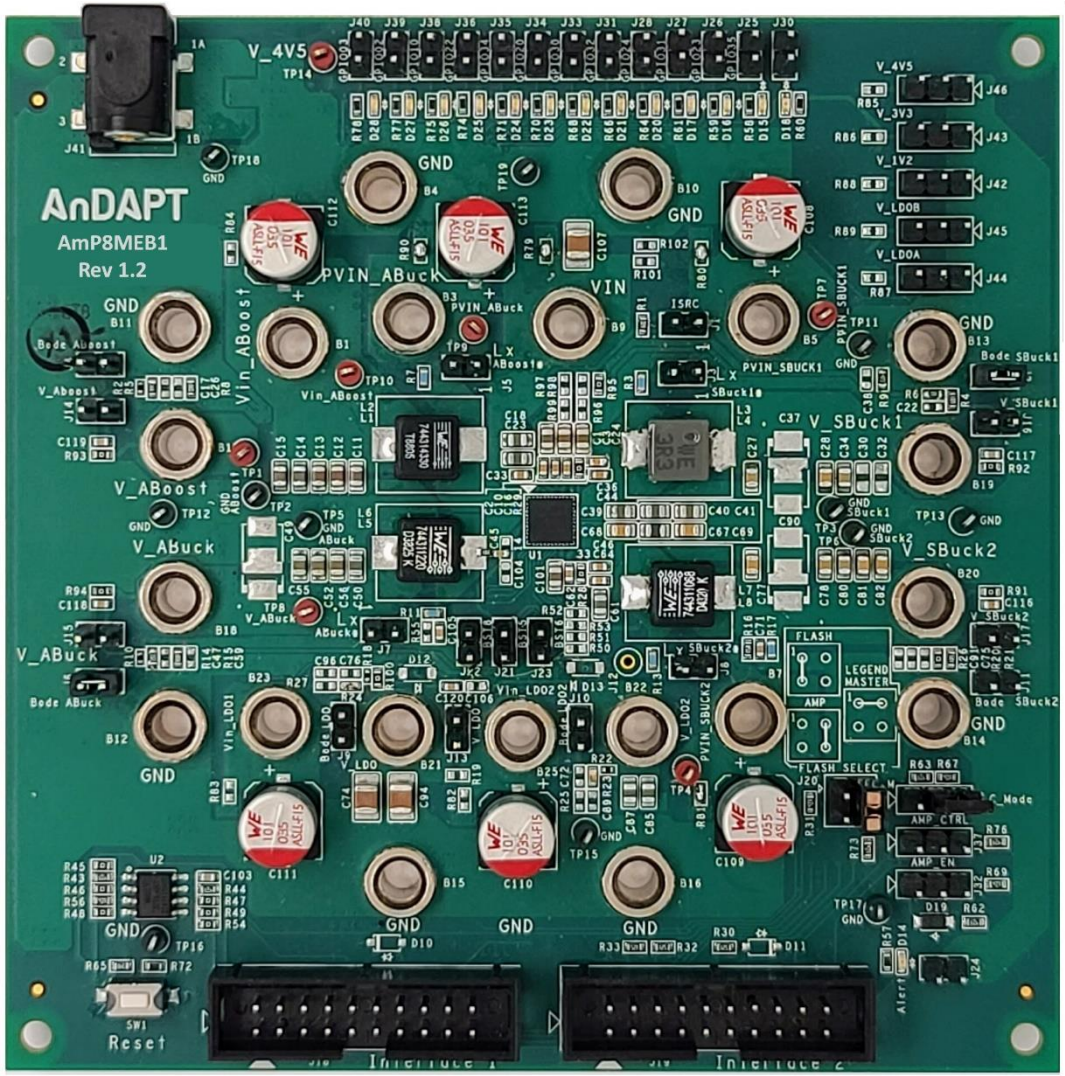
- Ripple: ±1% pk-pk
- Transient conditions
  - Step 25 % of full load @ 10A/us for non-core rails
  - Step 25% of full load @ 100A/us for core rails (using Xilinx spec here since no data from Microchip)

* Source: https://ww1.microchip.com/downloads/en/DeviceDoc/20006361C.pdf

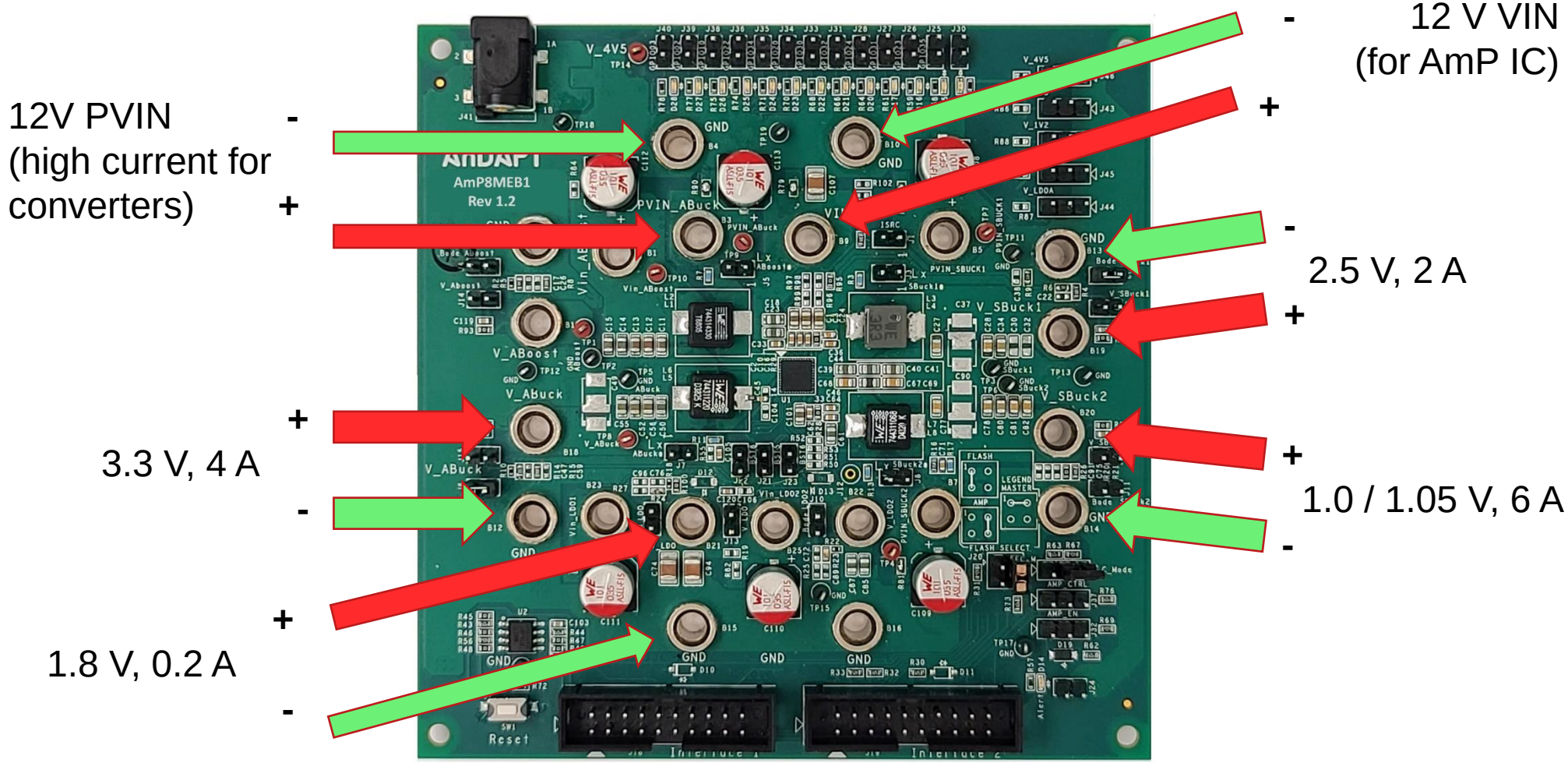
Evaluation Hardware: AmP8MEB1

- Implements 4 of 5 outputs
  - Custom PCB will cover all 5
- 2 configuration (.JSON) files:
  - 1.0 / 1.8 / 2.5 / 3.3 V outputs

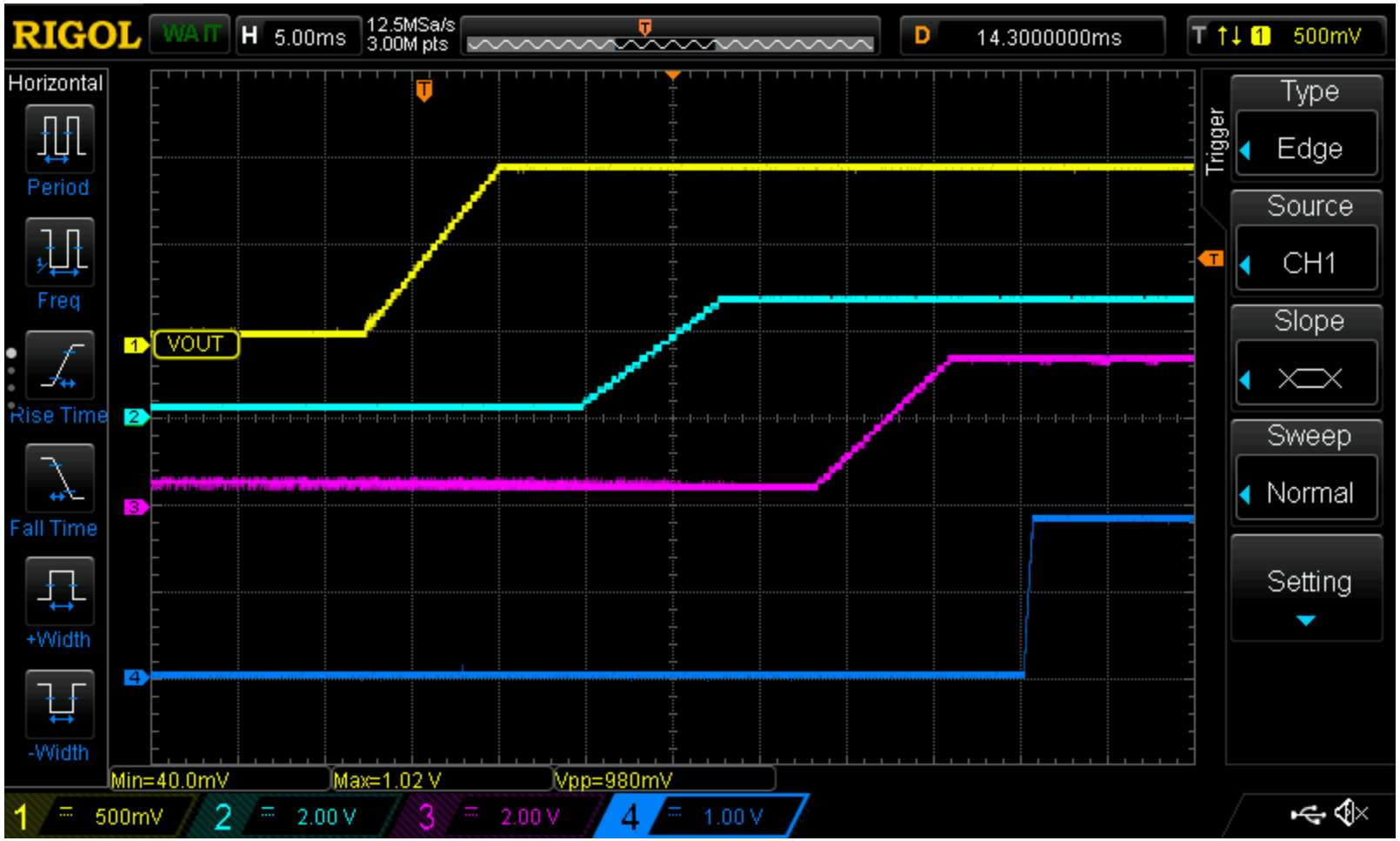
    - or -
  - 1.05 / 1.8 / 2.5 / 3.3 V outputs
- Download jsons here:
  - https://www.andapt.com/docs/WebAmP_RD/Microchip/zip/ARD_M_MPF_A3.zip



Power Inputs and Outputs



Startup Sequencing



1.0 V

2.5 V

3.3 V

1.8 V

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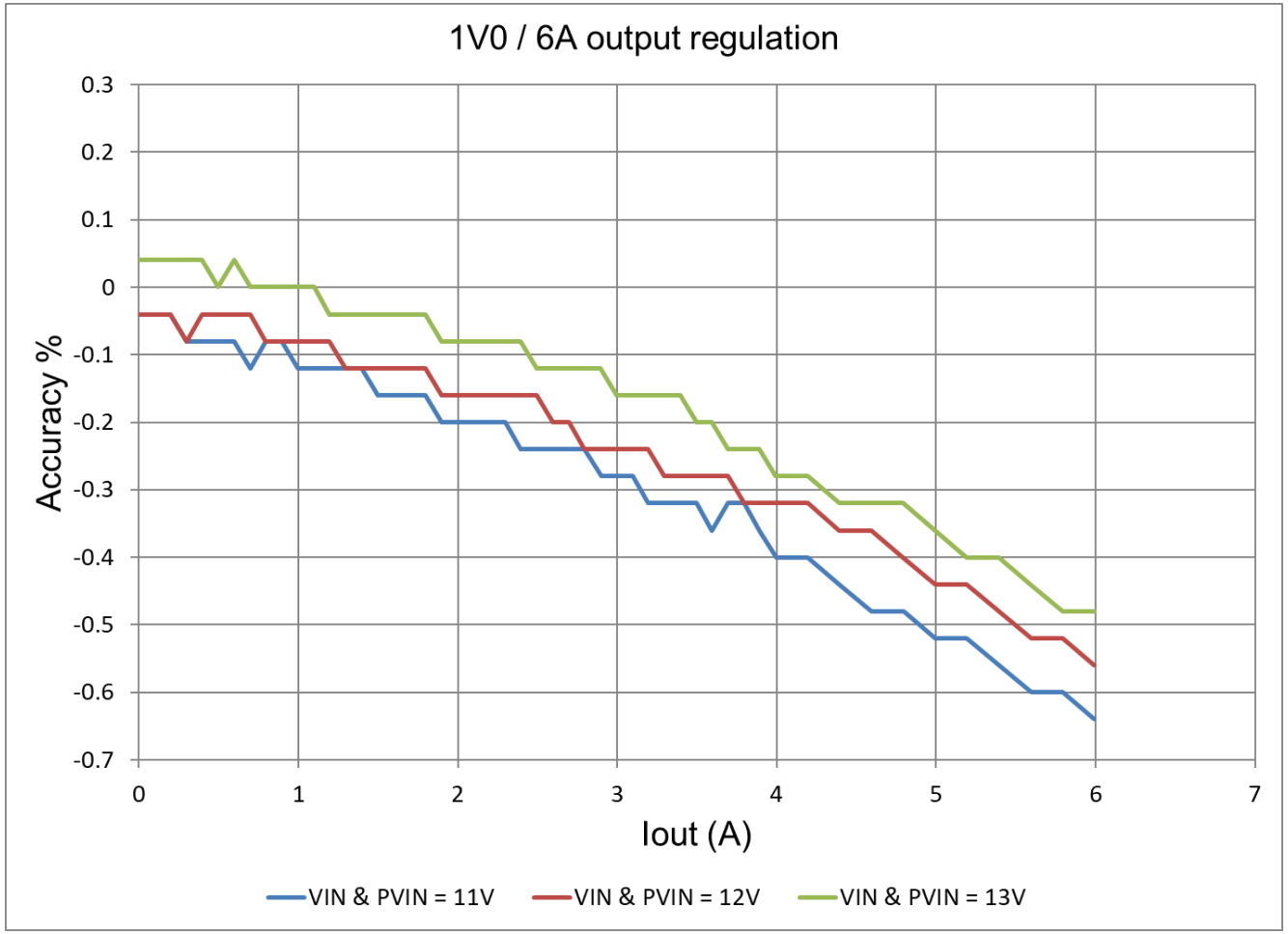
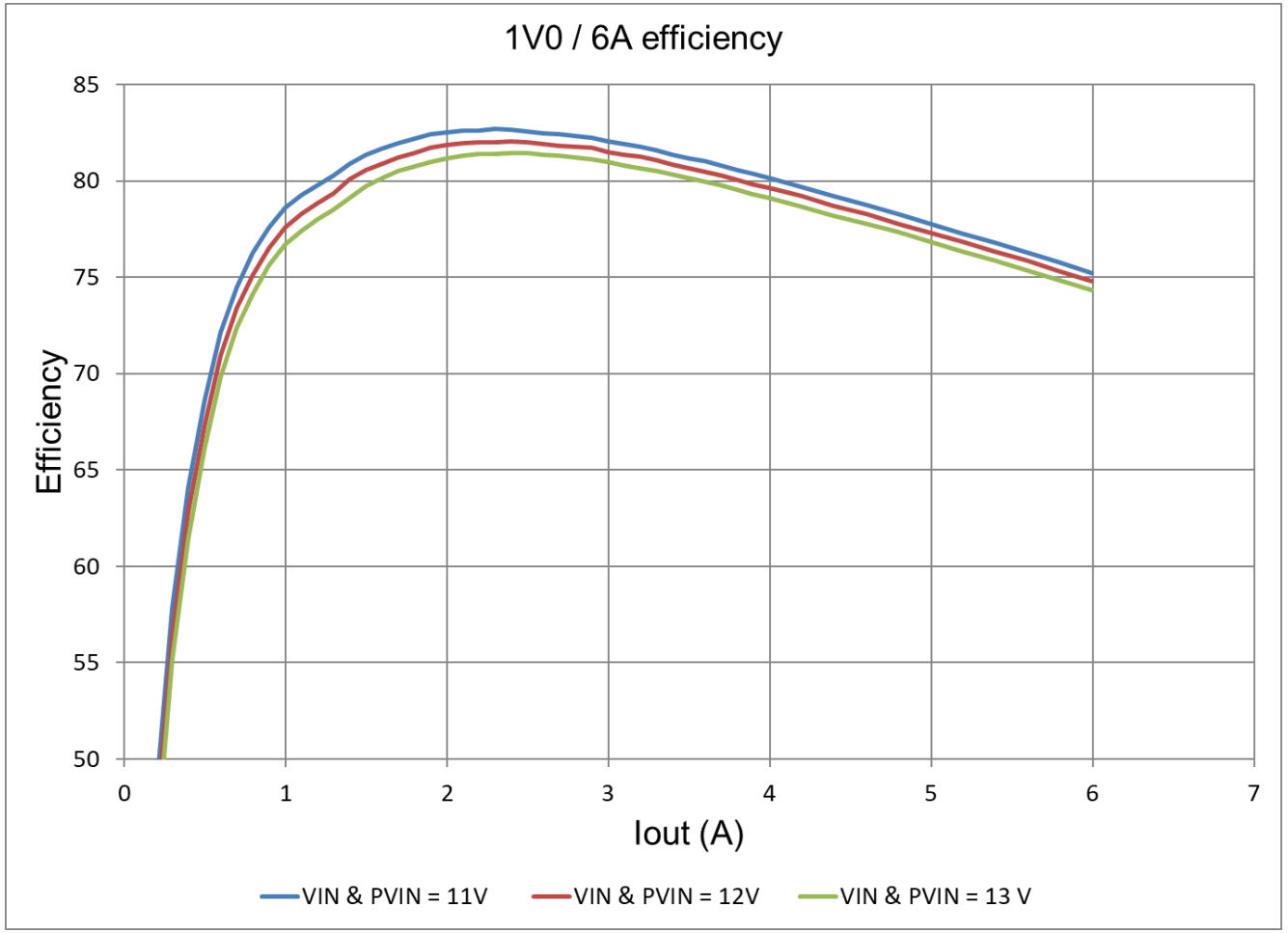
1.0 V / 6 A (VDD Rail)

- C200 (Synchronous buck)
- 1 MHz
- L = 680 nH
  - Wurth 744311068
- C = 7 x 47 µF

1V0 Load Regulation at 11, 12, and 13 V input

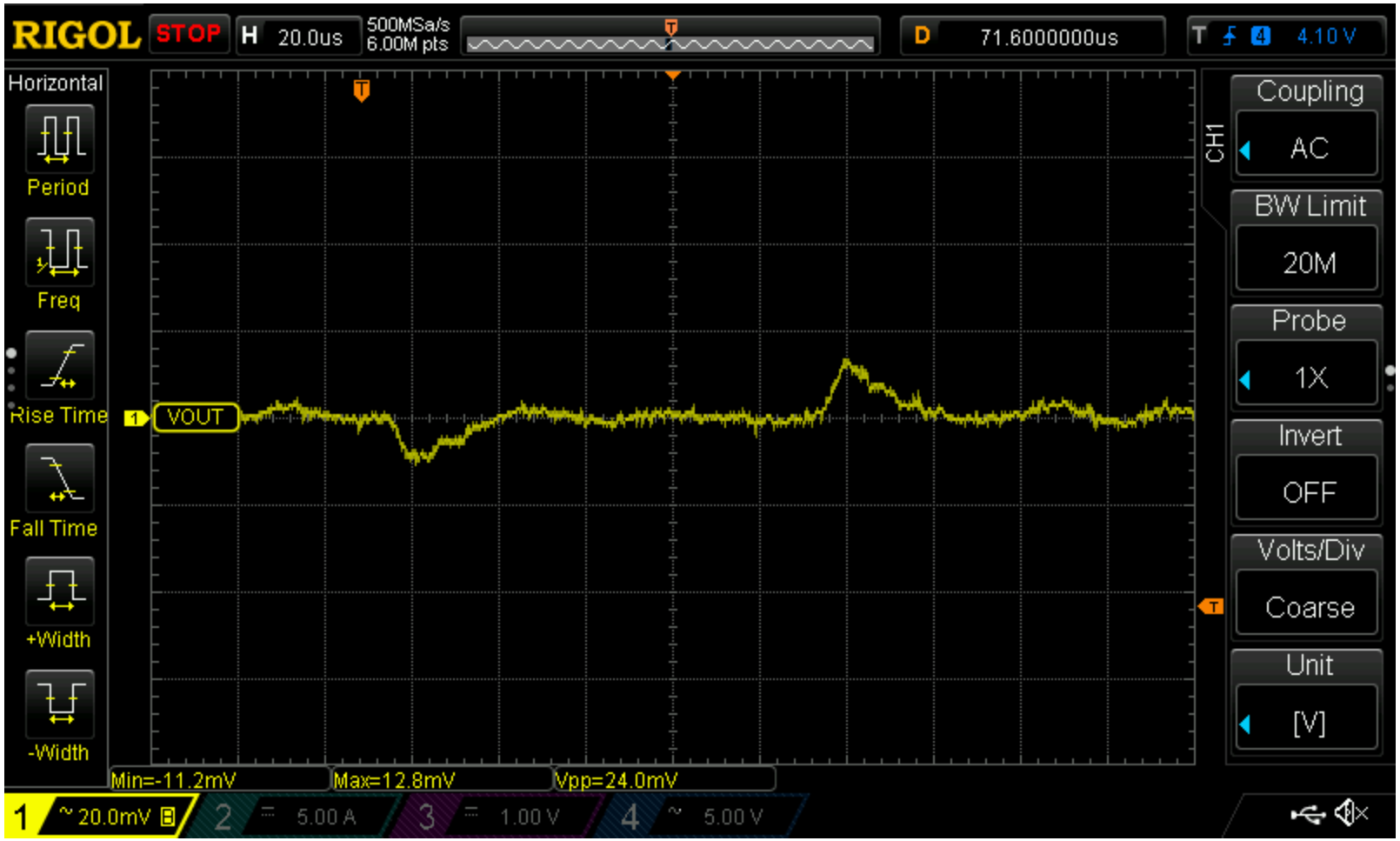


1V0 Efficiency Curves at 11, 12, and 13 V input



1V0 4.5 A → 6 A Load Step Response

- 10 A/µs
- Vp-p = 24 mV
- spec = 40 mVp-p



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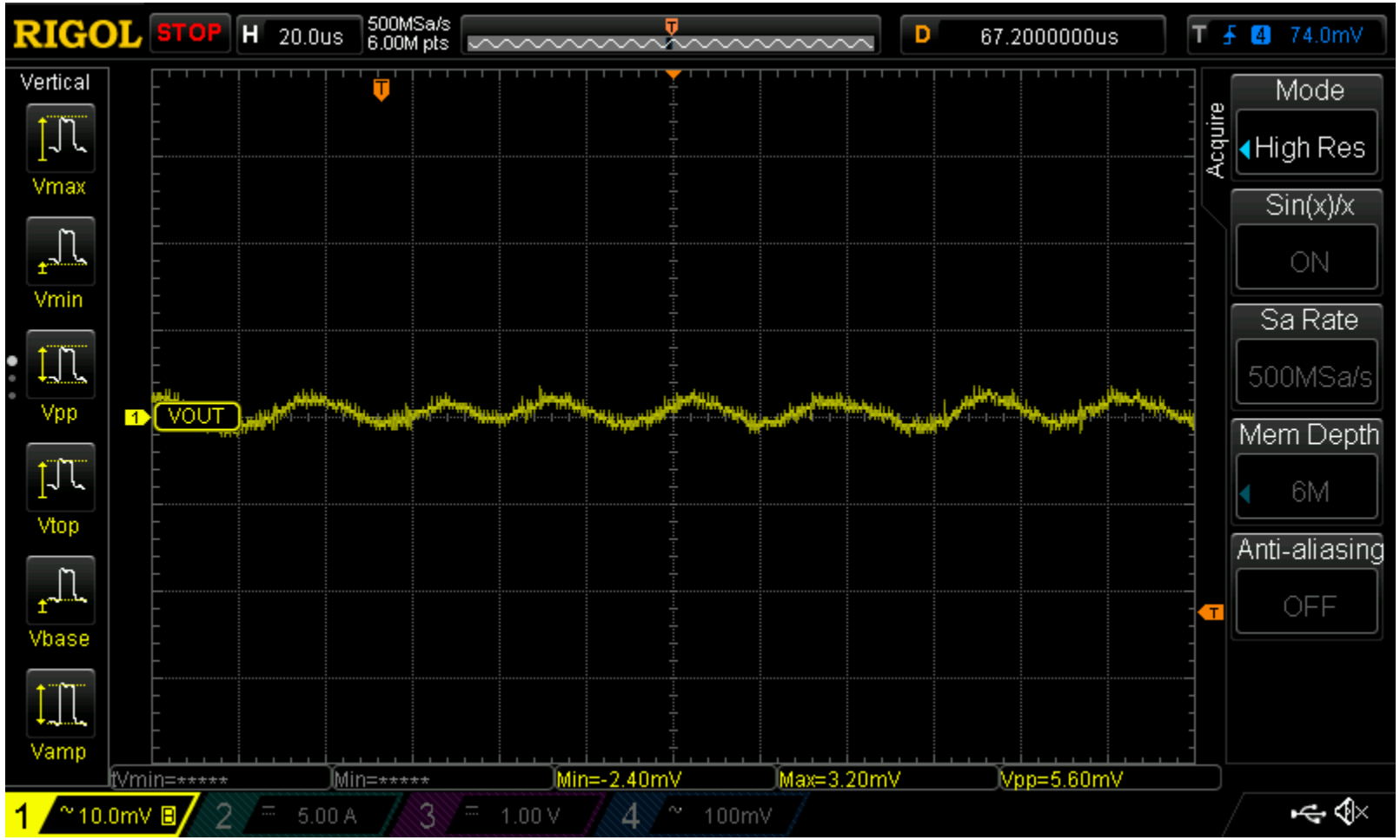
1V0 Output Ripple at 6 A

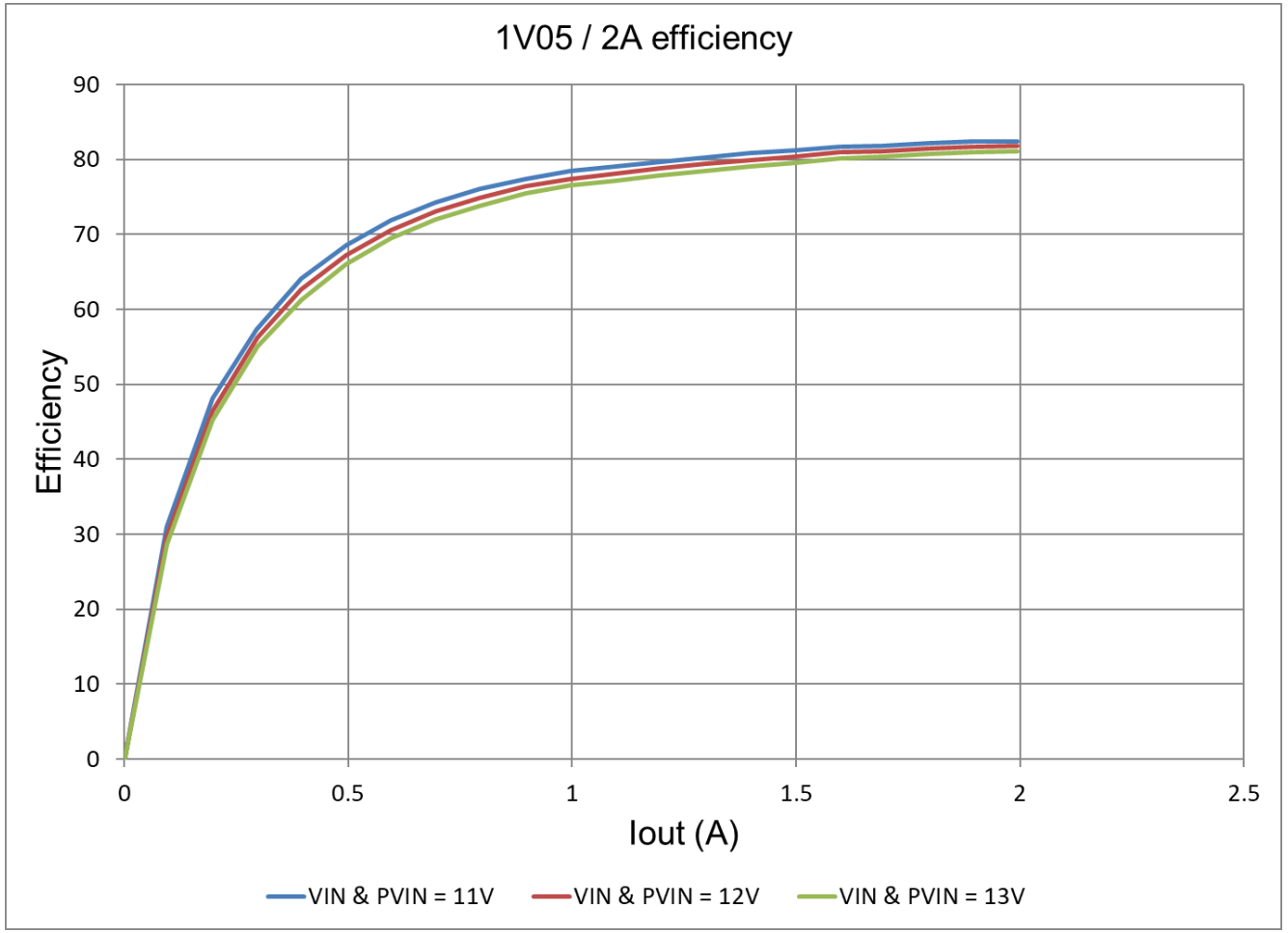
- 10 A/µs
- Vpp = 5.6 mV
- spec = 20 mVp-p



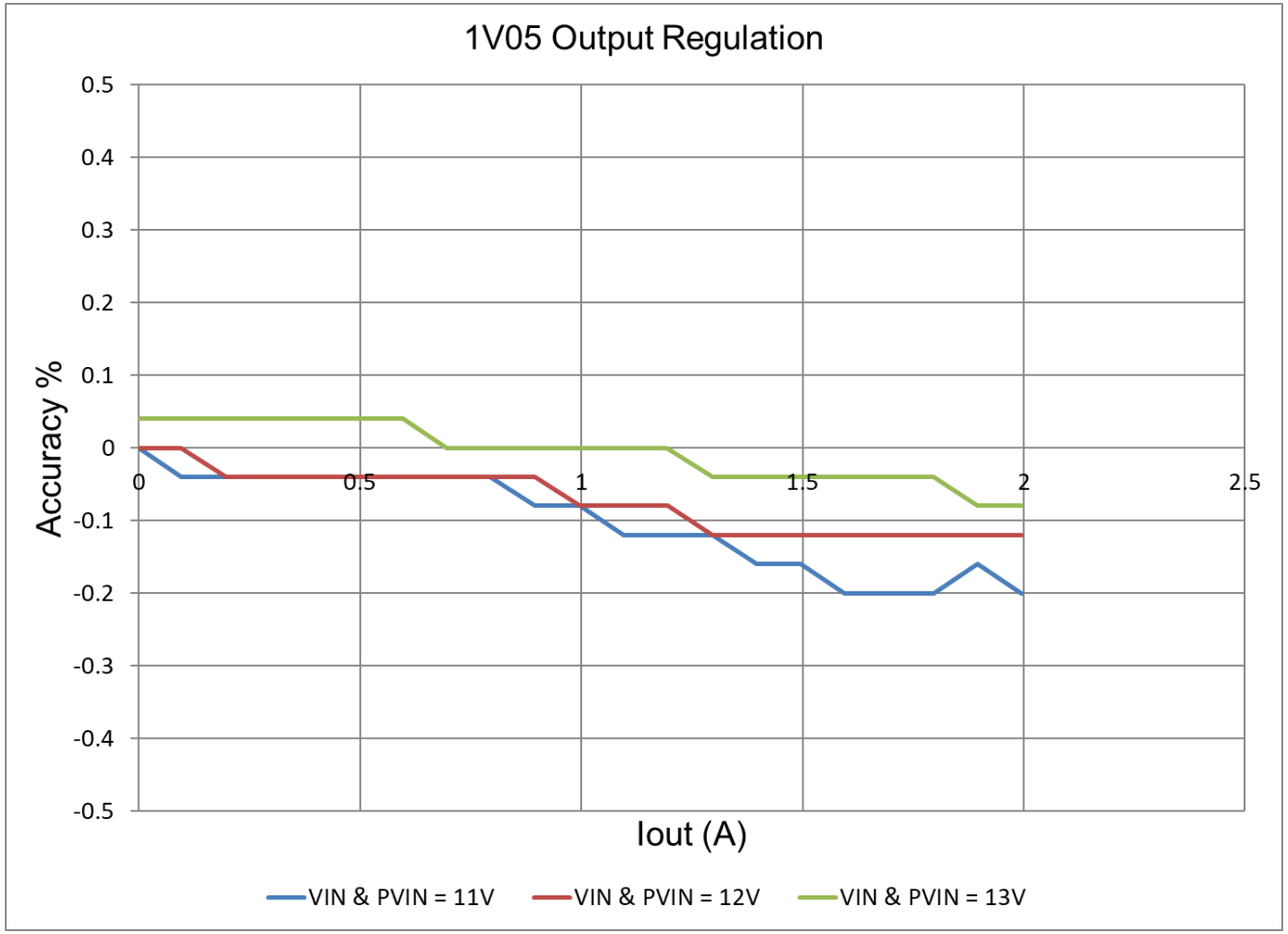
1.V05 / 2 A VDDA Rail

- C200 (synchronous buck)
- 1 MHz
- L = 680 nH
  - Wurth 744311068
  - A lower current inductor can be used for a custom design – this board uses the same hardware as the 1V0/6A rail
- C = 7 x 47 µF

1.05 V Efficiency

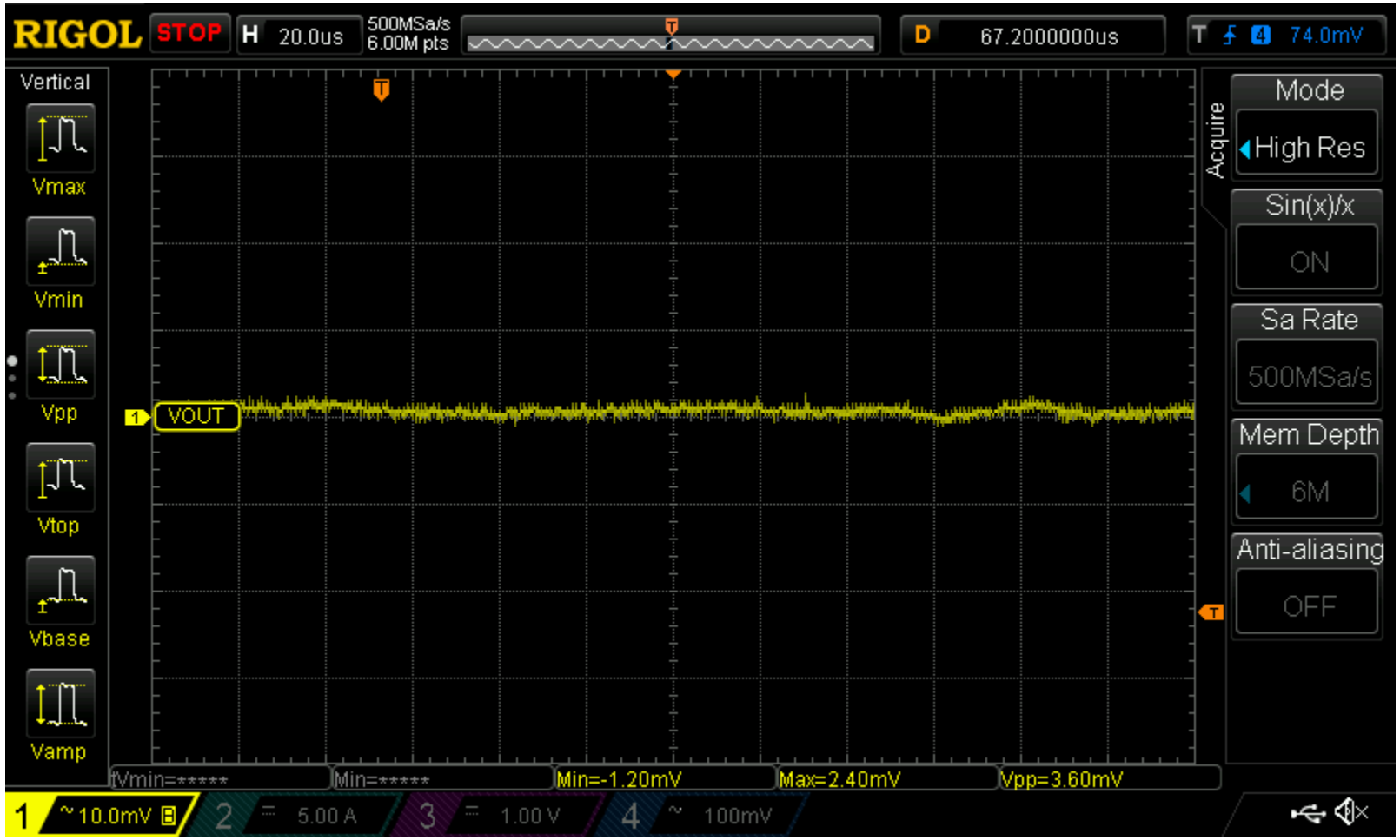


1.05 V Regulation



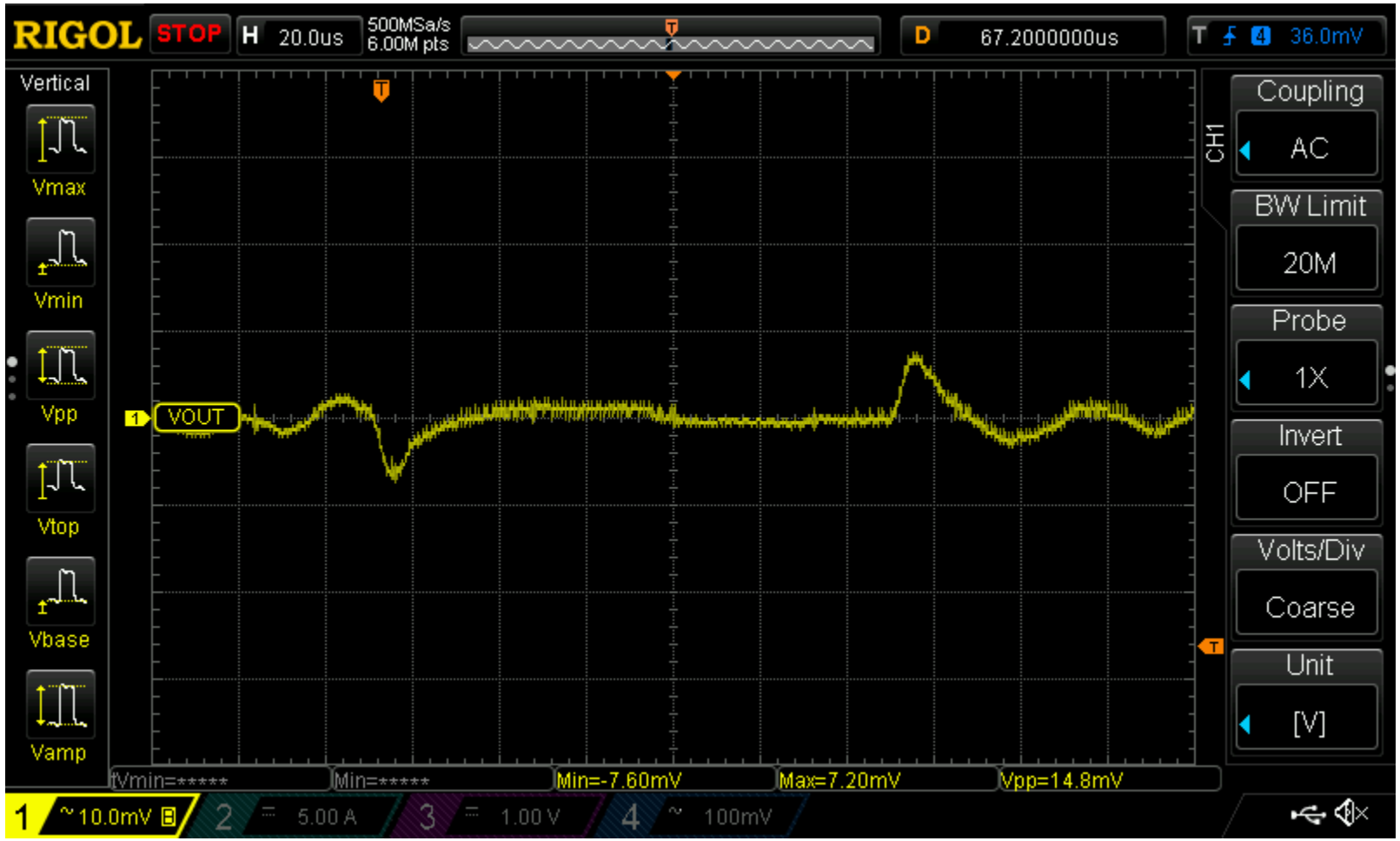
1V05 Output Ripple at 2 A

- Vp-p = 3.6 mV + 3 mV regulation window
- spec = 30 mVp-p including load regulation



1V05 1.5 A→ 2 A Load Step Response

- 10 A/µs
- Vp-p = 14.8 mV
- spec = 30 mVp-p



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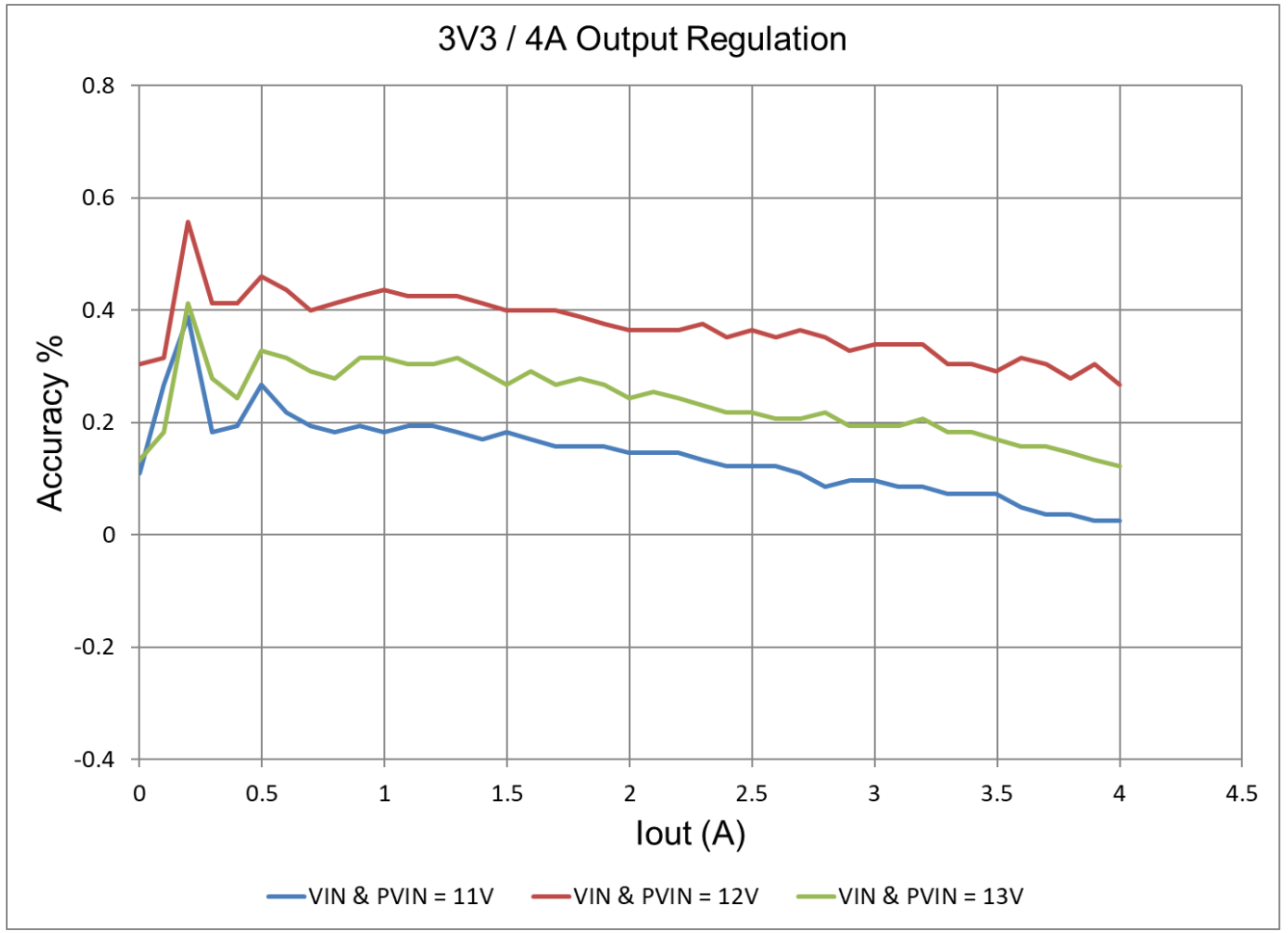
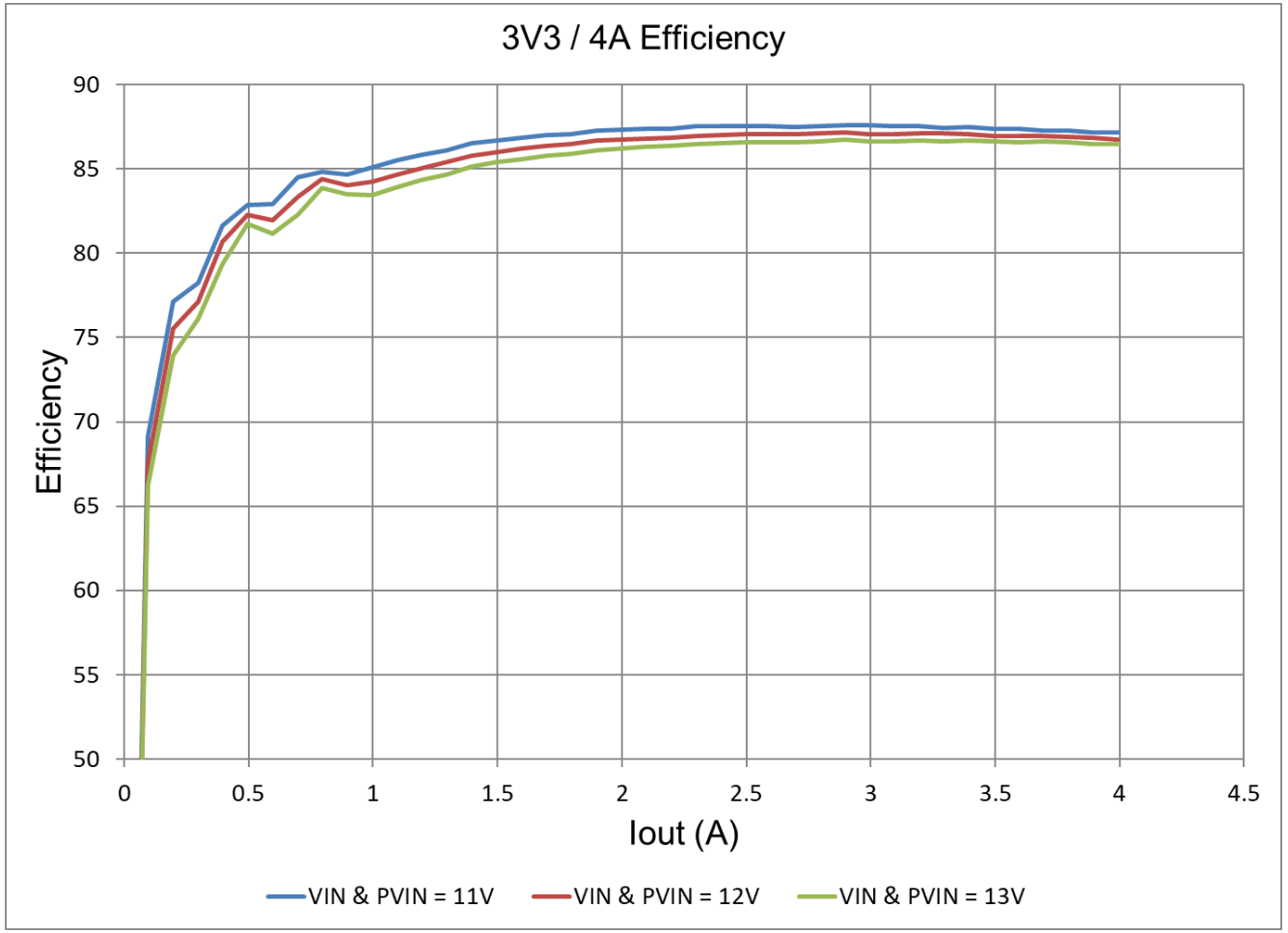
3V3 / 4 A
VDDAUX Rail

- C150 (Asynchronous buck)
- 571 kHz
- L = 2.2 uH
  - Wurth 744311220
- C = 4 x 47 µF

3V3 / 4 A Output Regulation

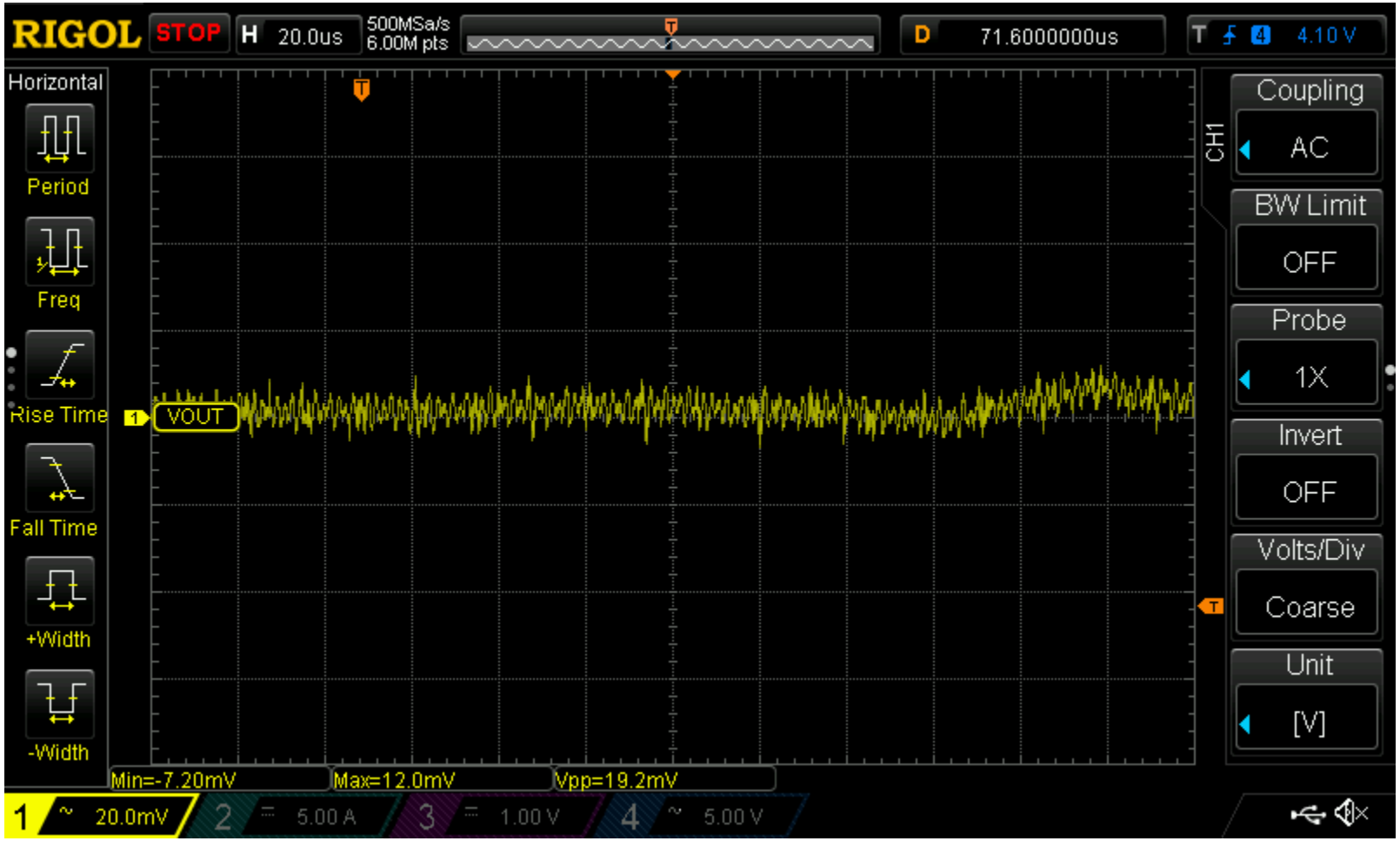


3V3 / 4 A Efficiency



3V3 / 4 A Output Ripple

- Vp-p = 19.2 mV
- Spec = 60 mVp-p



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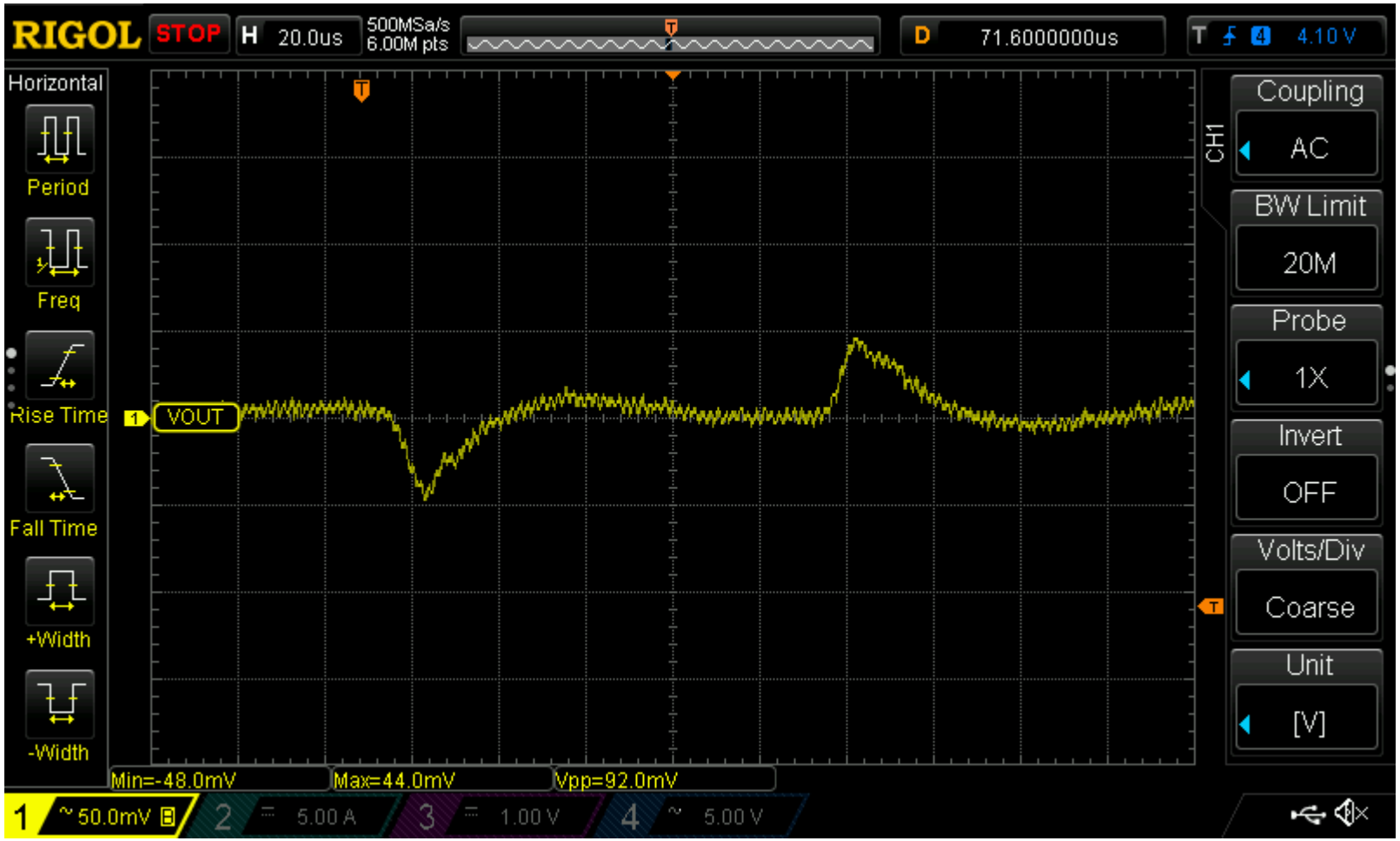
3V3 3 A→4 A Load Step Response

- 10 A/µs
- Vpp=92 mV
- spec = 330 mVp-p

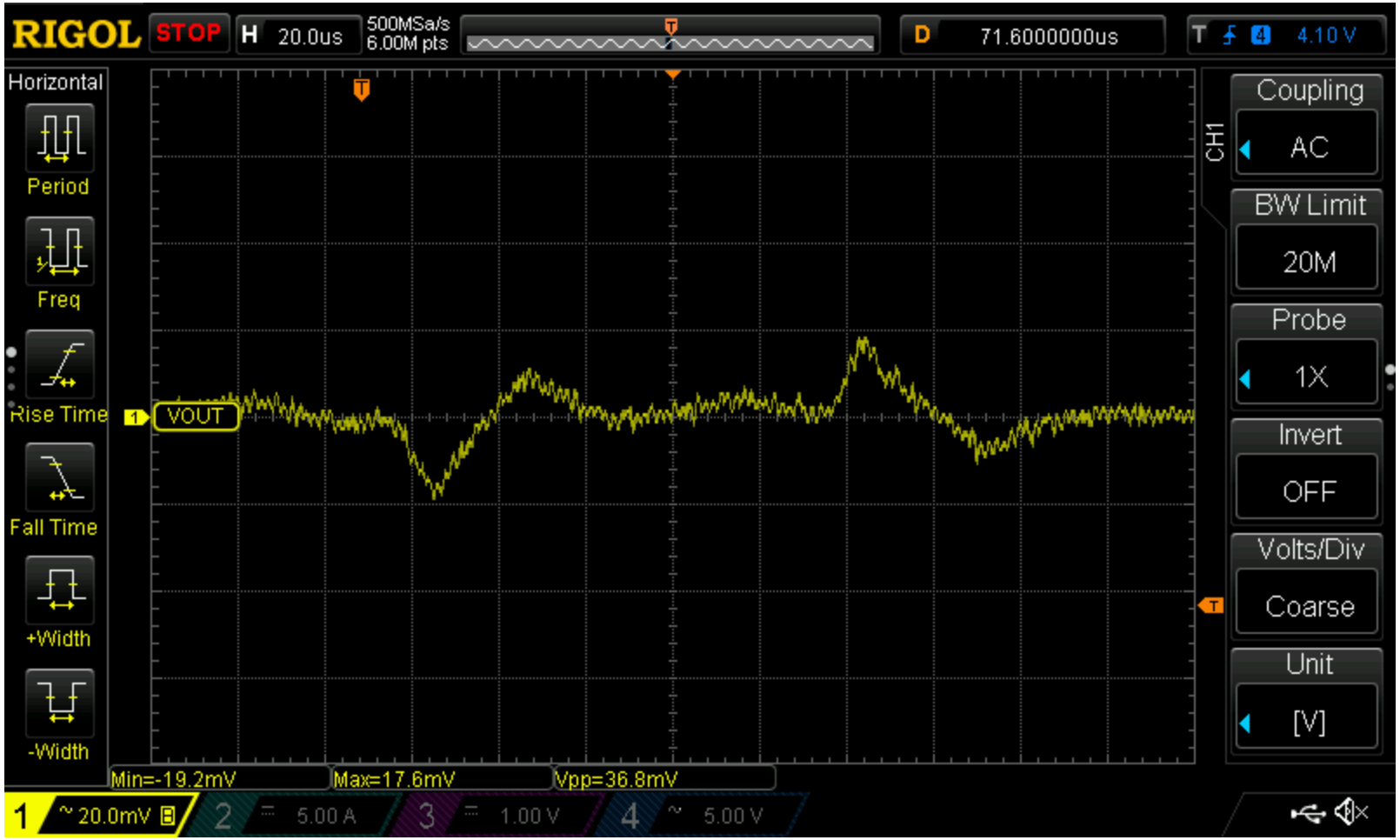


2.5 V / 2 A VDD25 Rail

- C200 (synchronous buck)
- 571 kHz
- L = 3.3 uH
  - Wurth 74439344033
- C = 4 x 47 µF

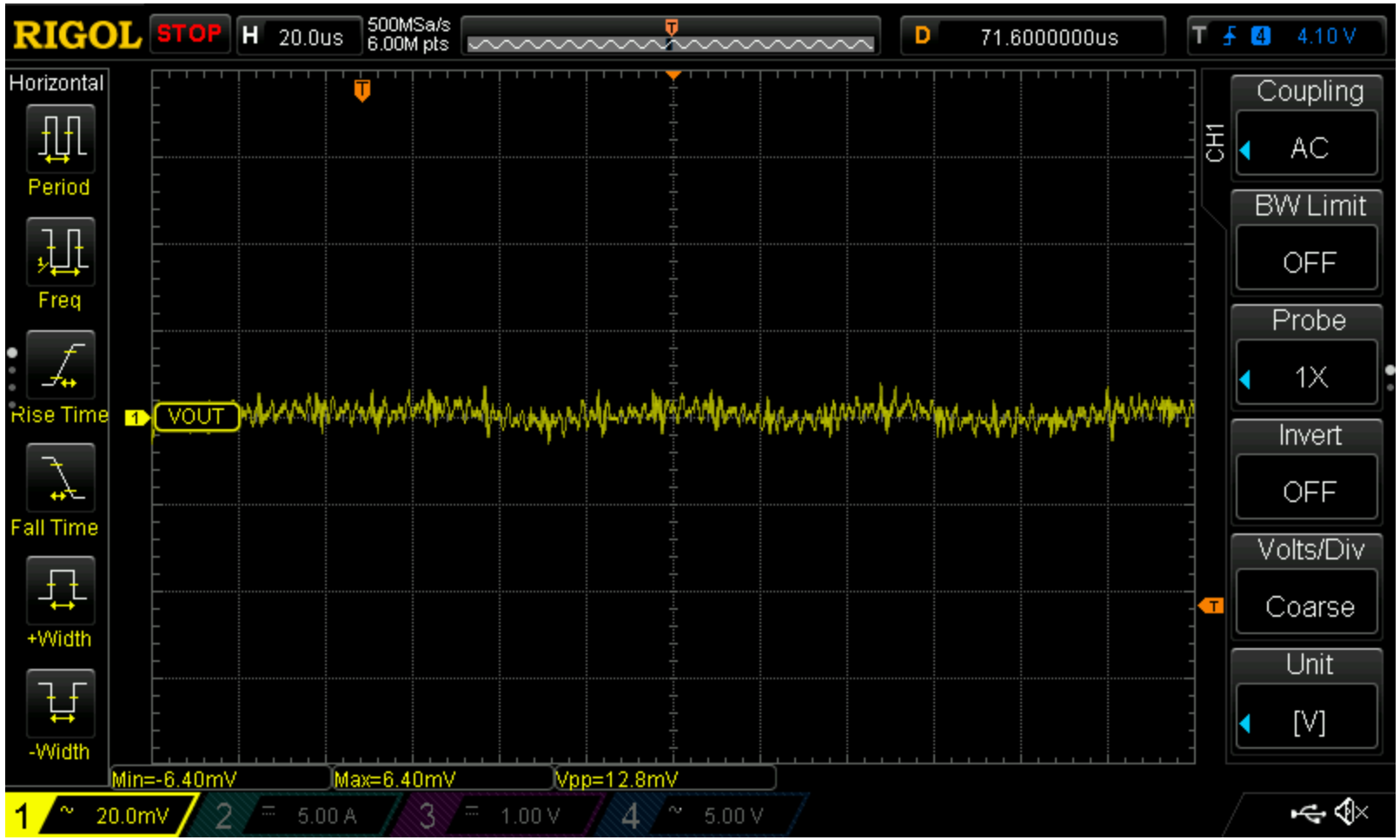
2.5 V / 2A 1.5 A→2 A Load Step Response

- Vpp = 36.8 mV
- spec = 50 mVp-p

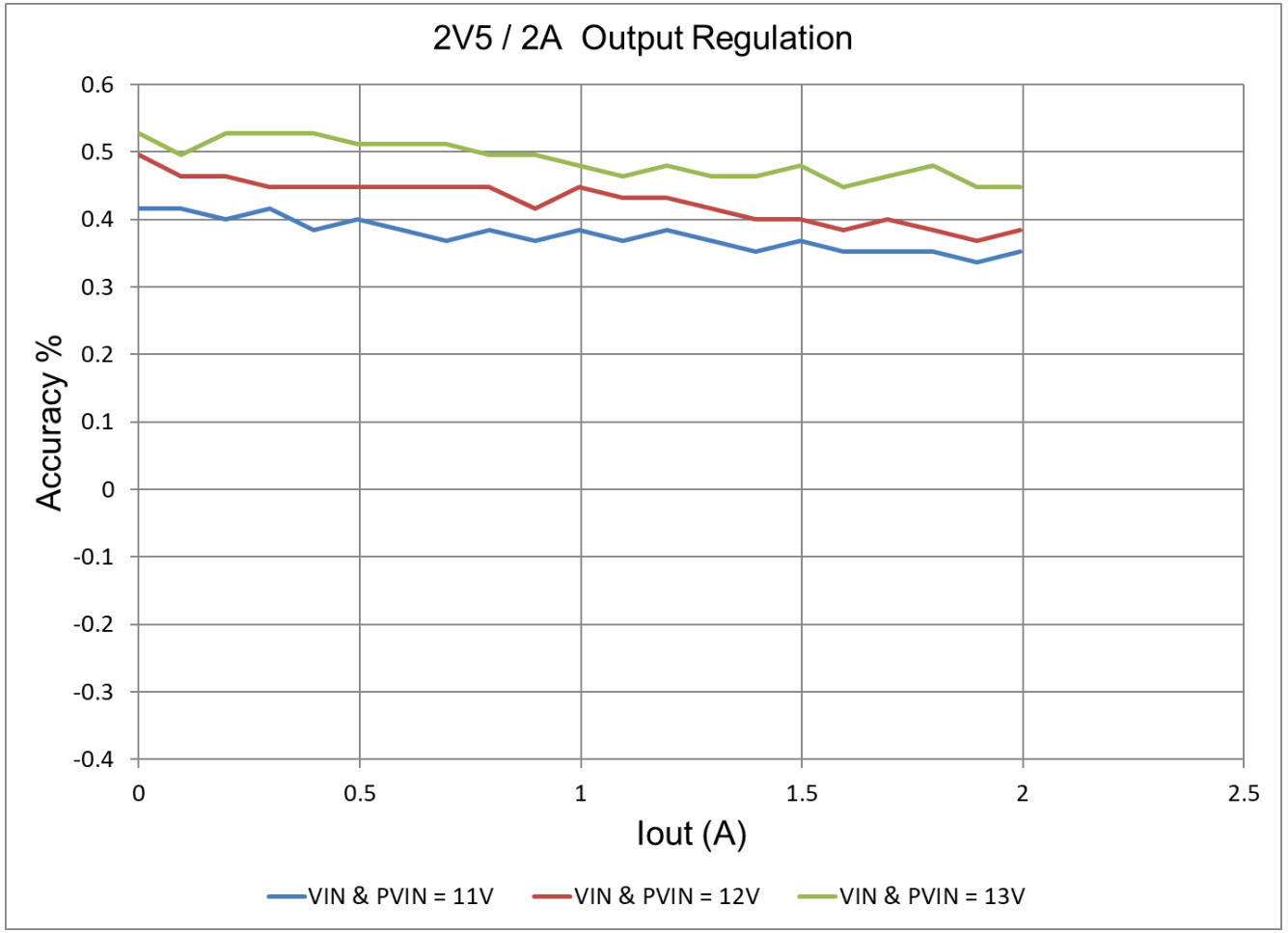


2V5 / 2 A Output Ripple

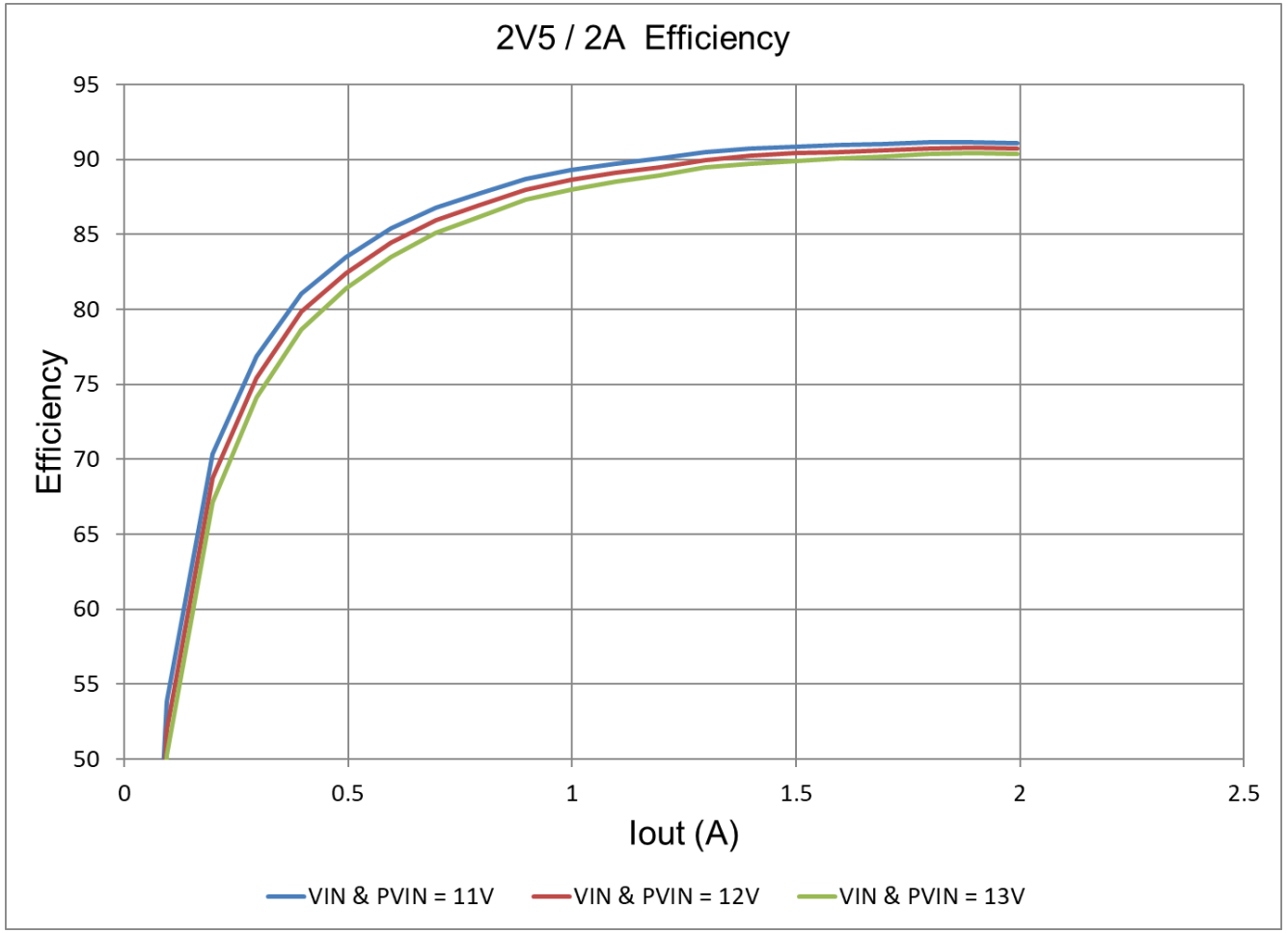
- Vpp = 12.8 mV
- Spec = 50 mVp-p



2V5 / 2 A Output Regulation



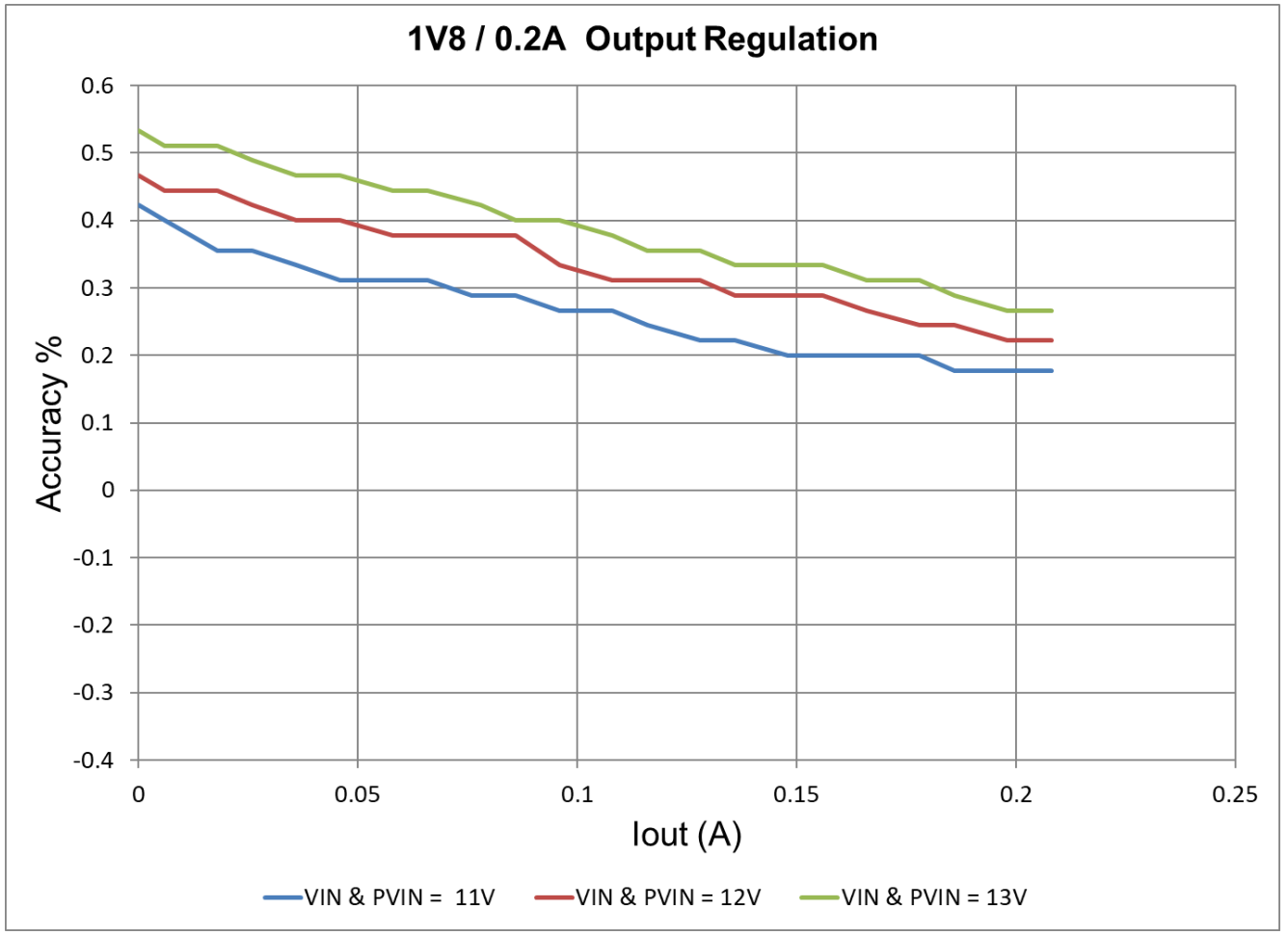
2V5 / 2 A Efficiency



1.8 V / 0.2A
HSIO_GPIO Rail

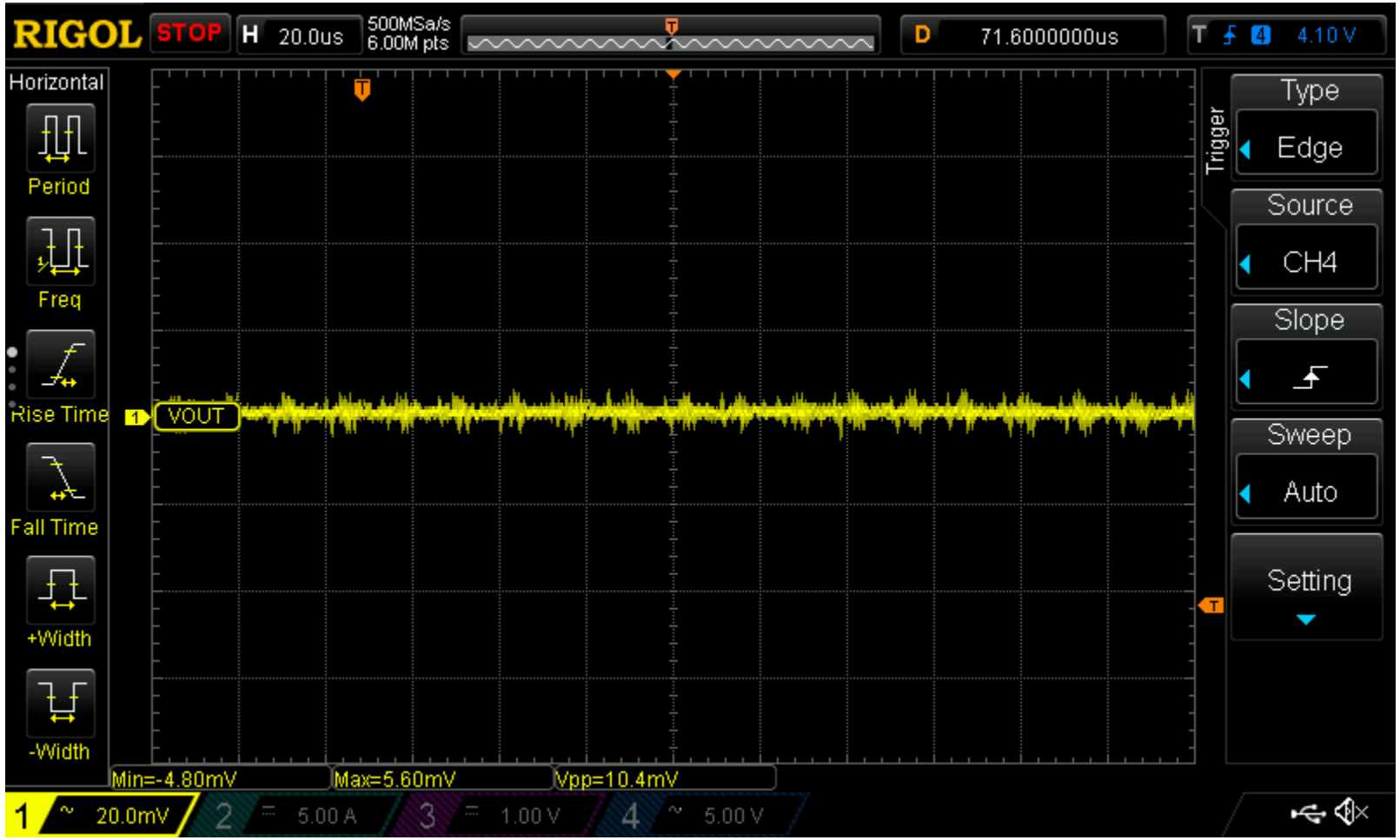
- C710 (SIM LDO)
- PVIN = 2.5 V
- C = 2 x 47 µF

1V8 / 0.2 A Output Regulation



1V8 / 0.2 A Output Ripple at 0.2 A

- Vpp = 10.4 mV
- Spec = 36 mVp-p



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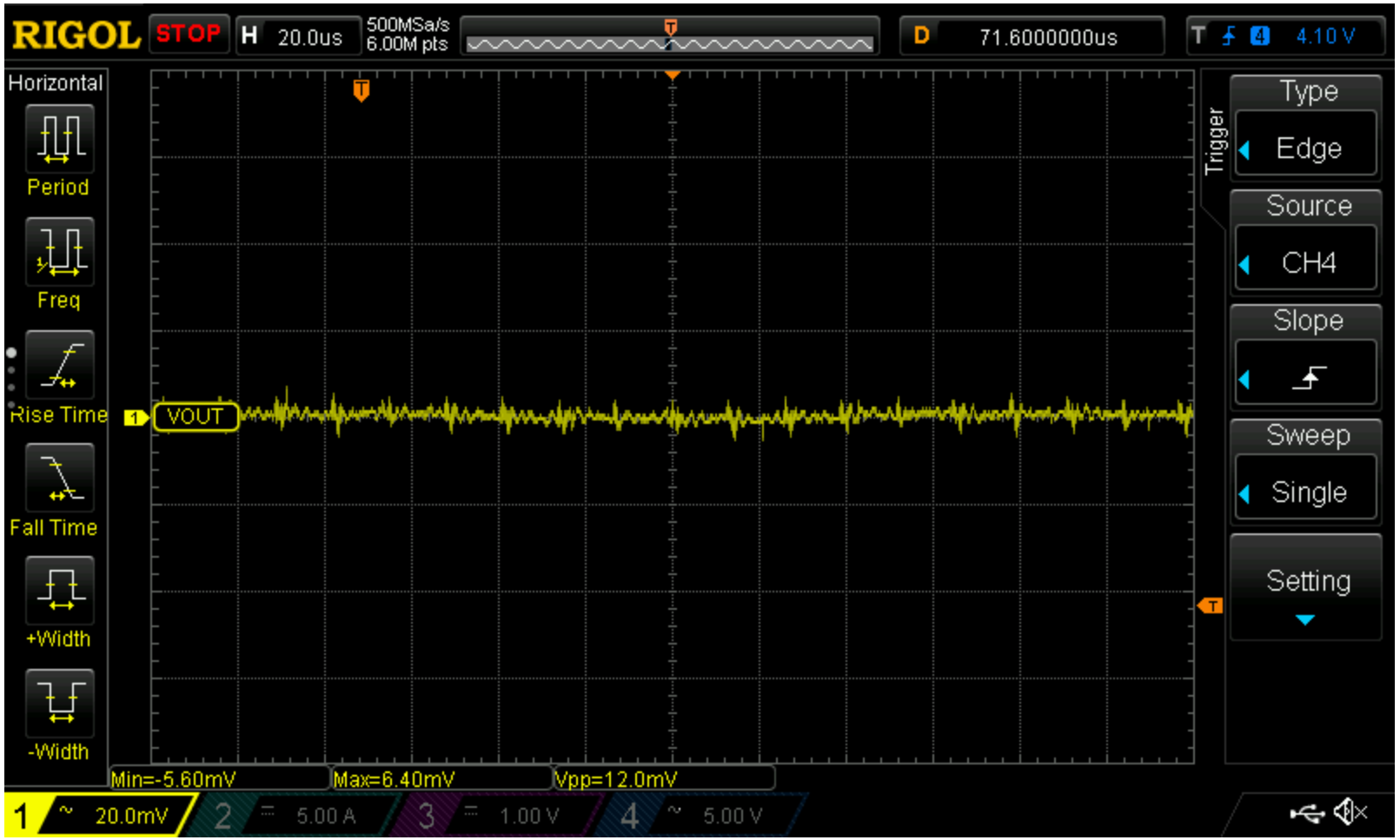
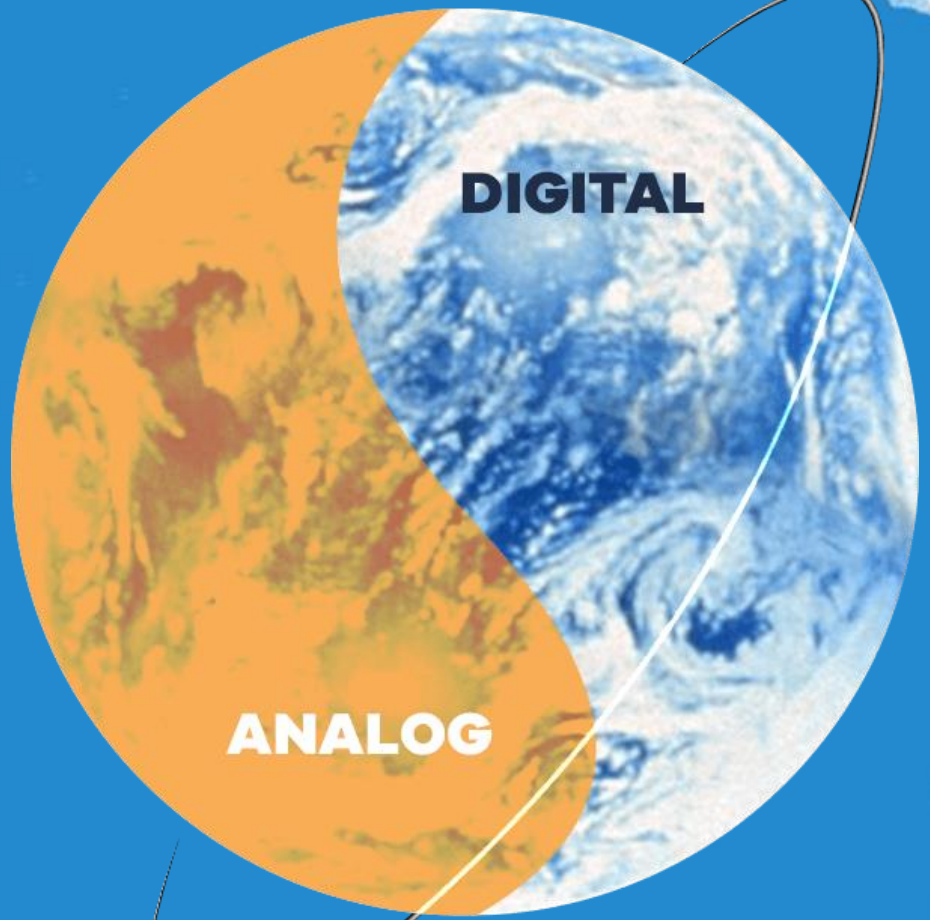
1V8 / 0.2 A 0.15 A→0.2 A Load Step Response

- 10 A/µsec
- No measurable response because of the small current, and the 2 x 22 µF output capacitors





Thank You

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