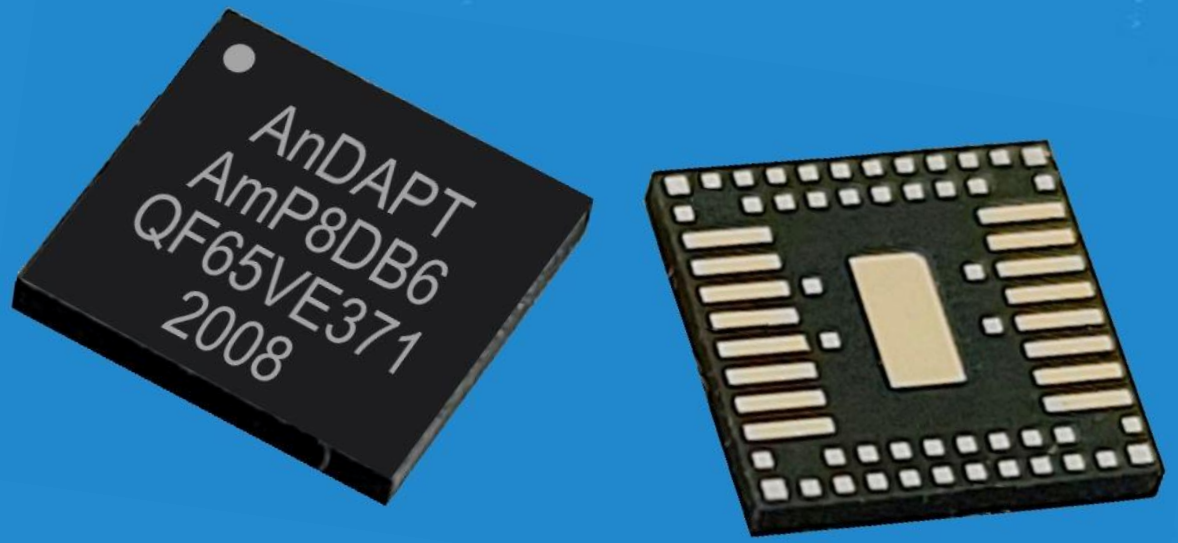

Artix UltraScale+ (Medium Power)

Mappings & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Artix UltraScale+ family of devices SKUs (medium power)
- Artix US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Artix US+ family FPGAs

*Xilinx document: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Artix UltraScale+ (US+) Device SKUs Covered

Supported SKUs
AU10P
AU15P
AU20P
AU25P

Artix UltraScale+ (Medium Power)

Can be combined if voltage same

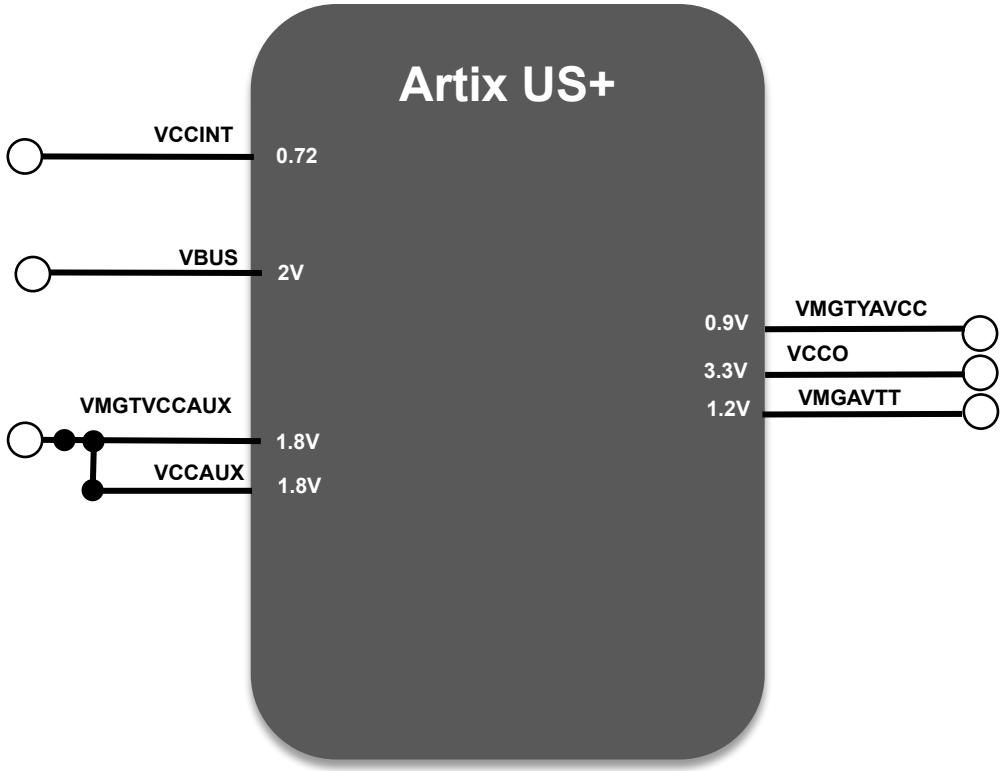

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

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Power Tree: Artix UltraScale+ (Minimum Rails)

PVIN = 12V/2V/1.2V

#	Rail	Seq	Vin (V)	Vout (V)	Iout (A)
1	VCCINT	1	12	0.72/0.85	1.2
2	VCCAUX	2	2	1.8	0.35
3	VBUS	1	12	2	0.5
4	VMGAVTT	3	12	1.2	3.75
5	VMGTVCCAUX	4	2	1.8	0.15
6	VMGTYAVCC	5	1.2	0.9	0.75
7	VCCO	6	12	3.3	1.5

Power Tree Mapping: Artix UltraScale+ (medium power)

PVIN = 12V/2V/1.2V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, BRAM, VCCINT_IO	1	C150	Async Buck	PVIN	12	0.72/0.85	1.2	ARD_X_AUP_A2
2	VCCAUX, VCCAUXIO, VCCADC	2	C710	LDO	VBUS	2	1.8	0.35	ARD_X_AUP_A2
3	VBUS	1	C150	Async Buck	PVIN	12	2	0.35 + 0.15	ARD_X_AUP_A2
4	VMGAVTT	3	C200	Sync Buck	PVIN	12	1.2	3 + 0.75	ARD_X_AUP_A2
5	VMGTVCCAUX	4	C710	LDO	VBUS	2	1.8	0.15	ARD_X_AUP_A2
6	VMGTYAVCC	5	C710	LDO	VMGAVTT	1.2	0.9	0.75	ARD_X_AUP_A2
7	VCCO	6	C150	Async Buck	PVIN	12	1 – 3.3	1.5	ARD_X_AUP_A2

Estimated total area estimated = 599.41 mm^2

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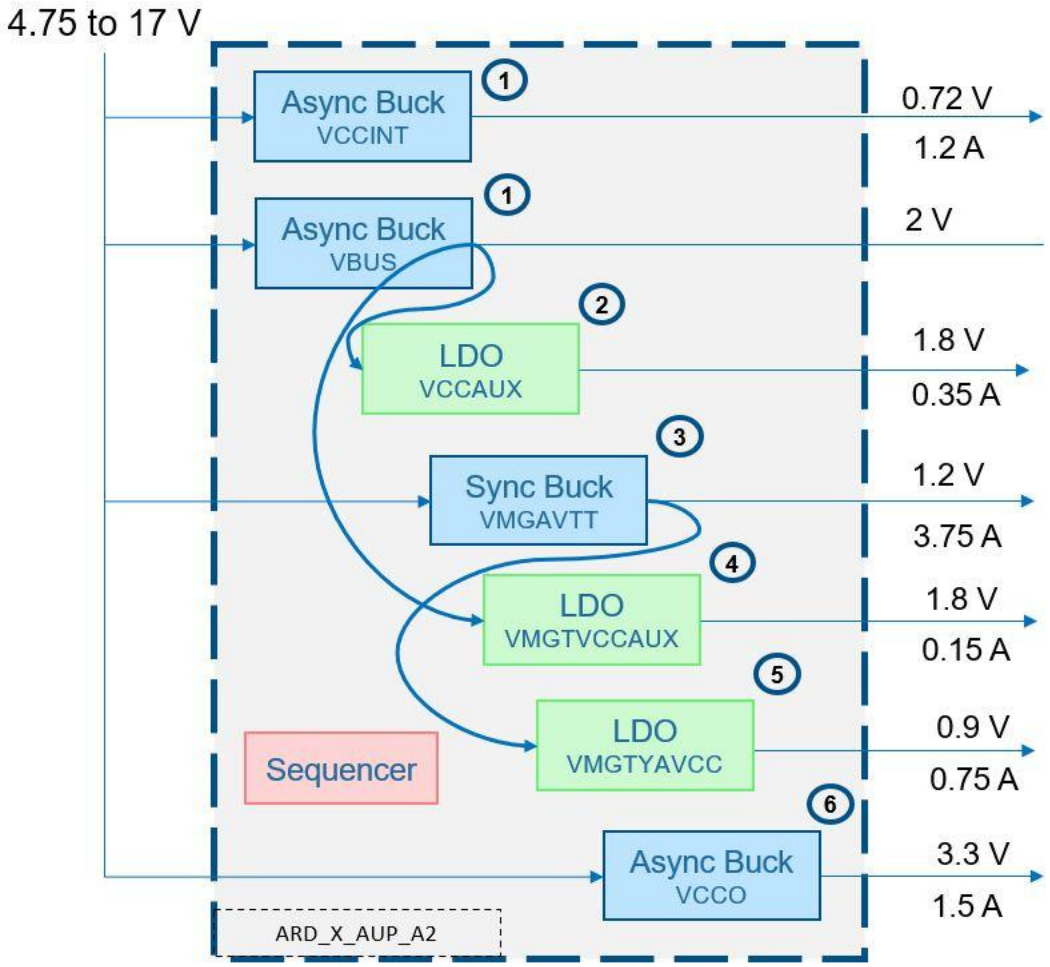
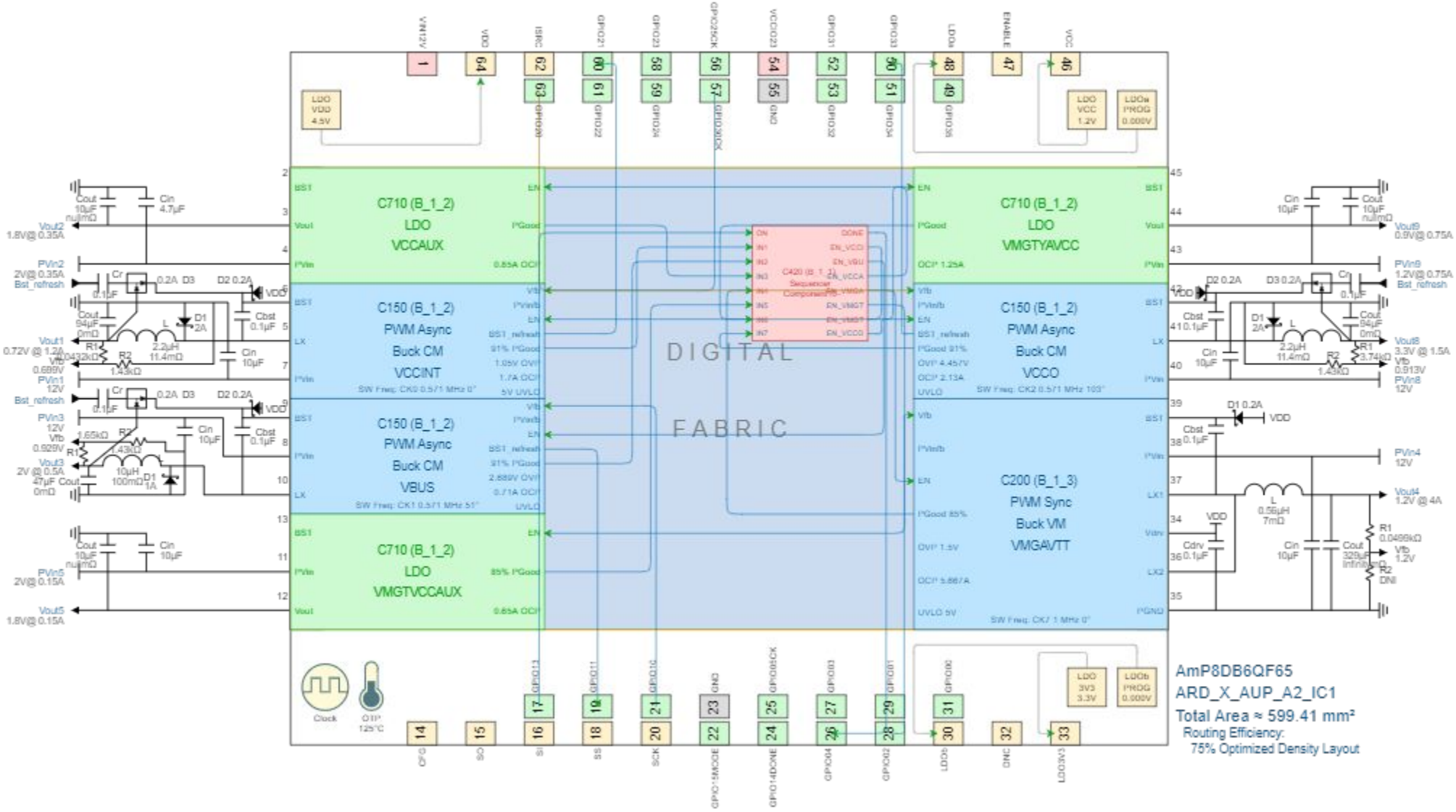
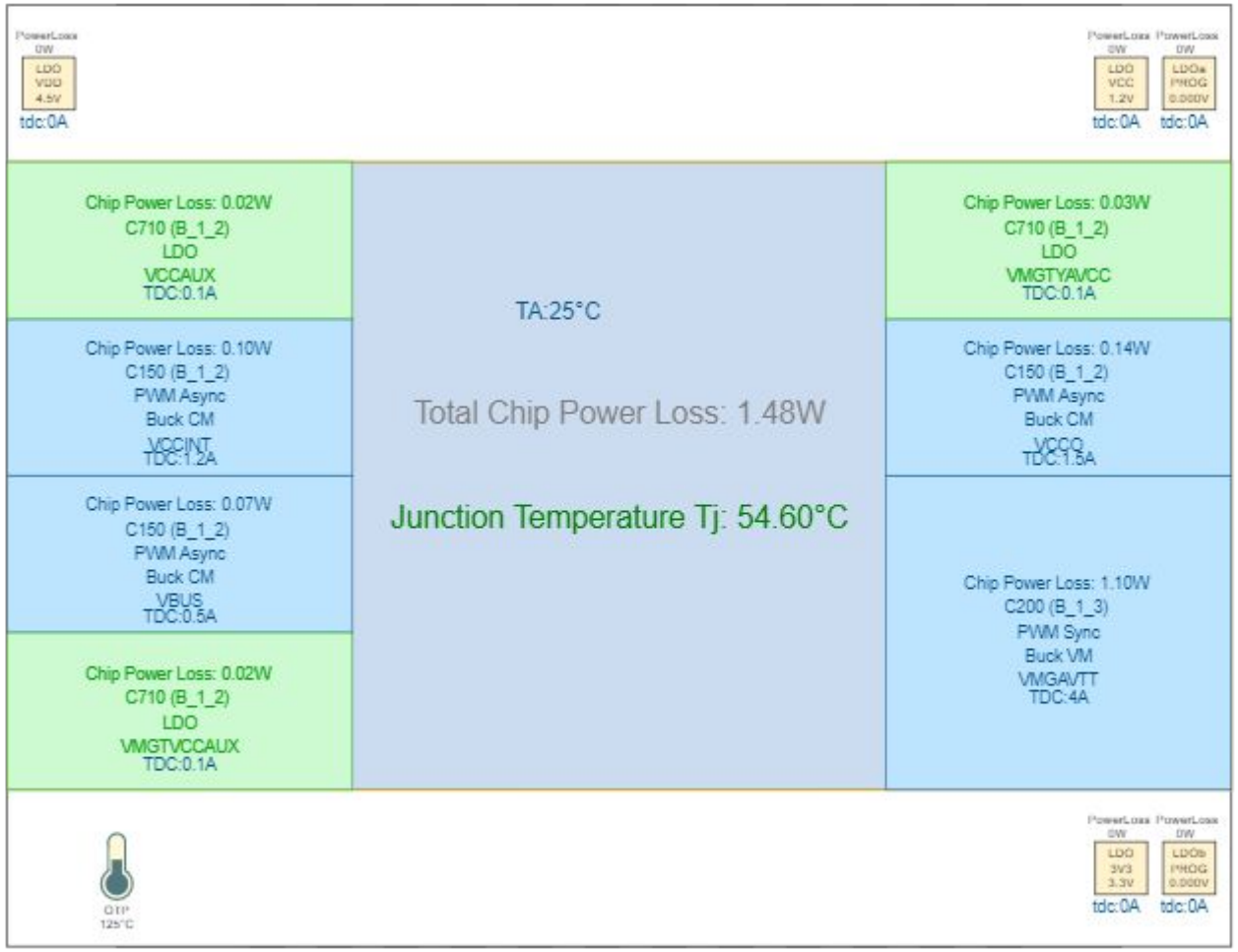
Power Tree Mapping



Mapping (WebAmP View)



Mapping (Thermal View)



AmP8DB6QF65
ARD_X_AUP_A2_IC1
Total Area ≈ 599.41 mm²
Routing Efficiency:
75% Optimized Density Layout

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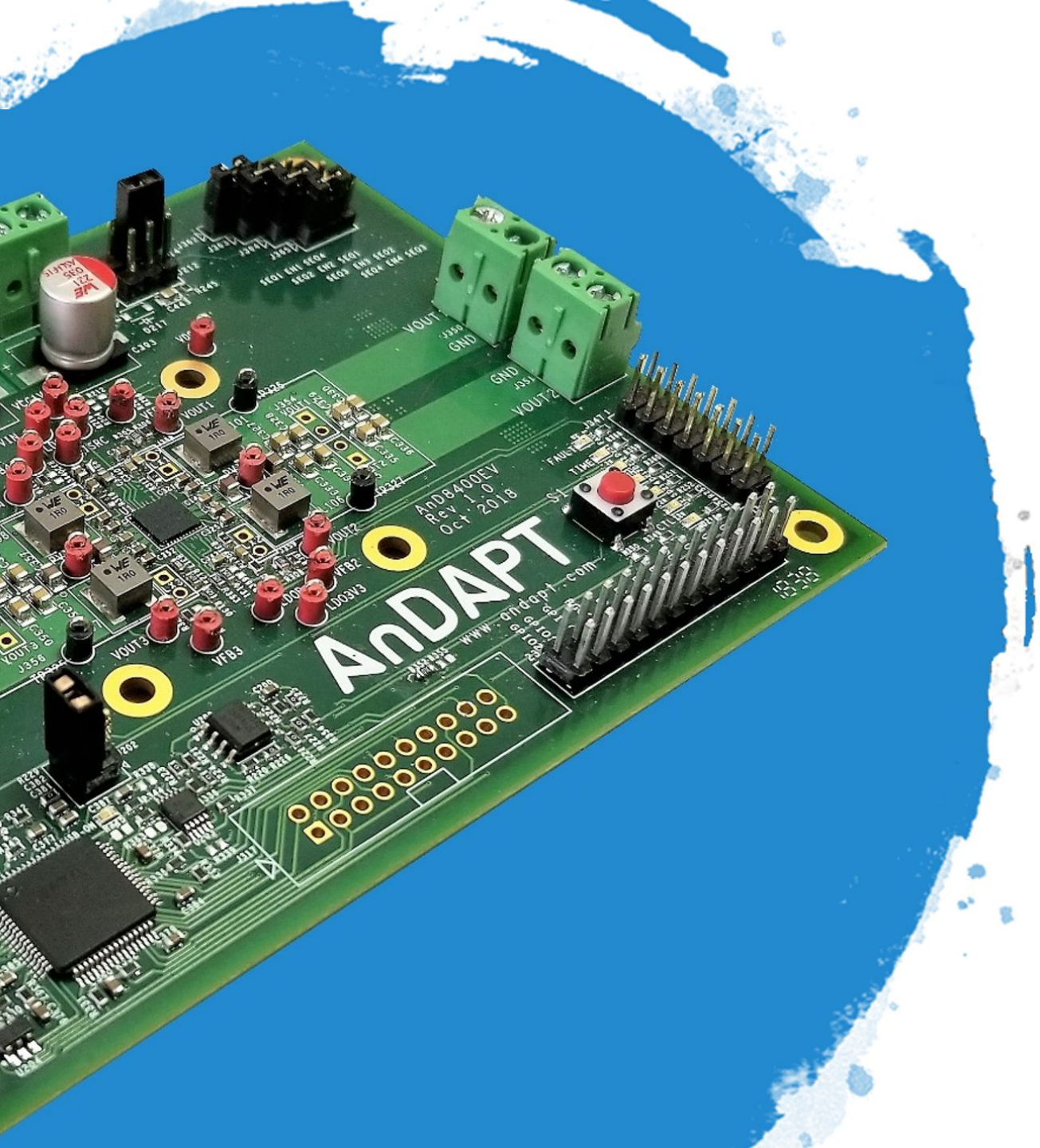

Test Data

Artix UltraScale+ (Medium Power)

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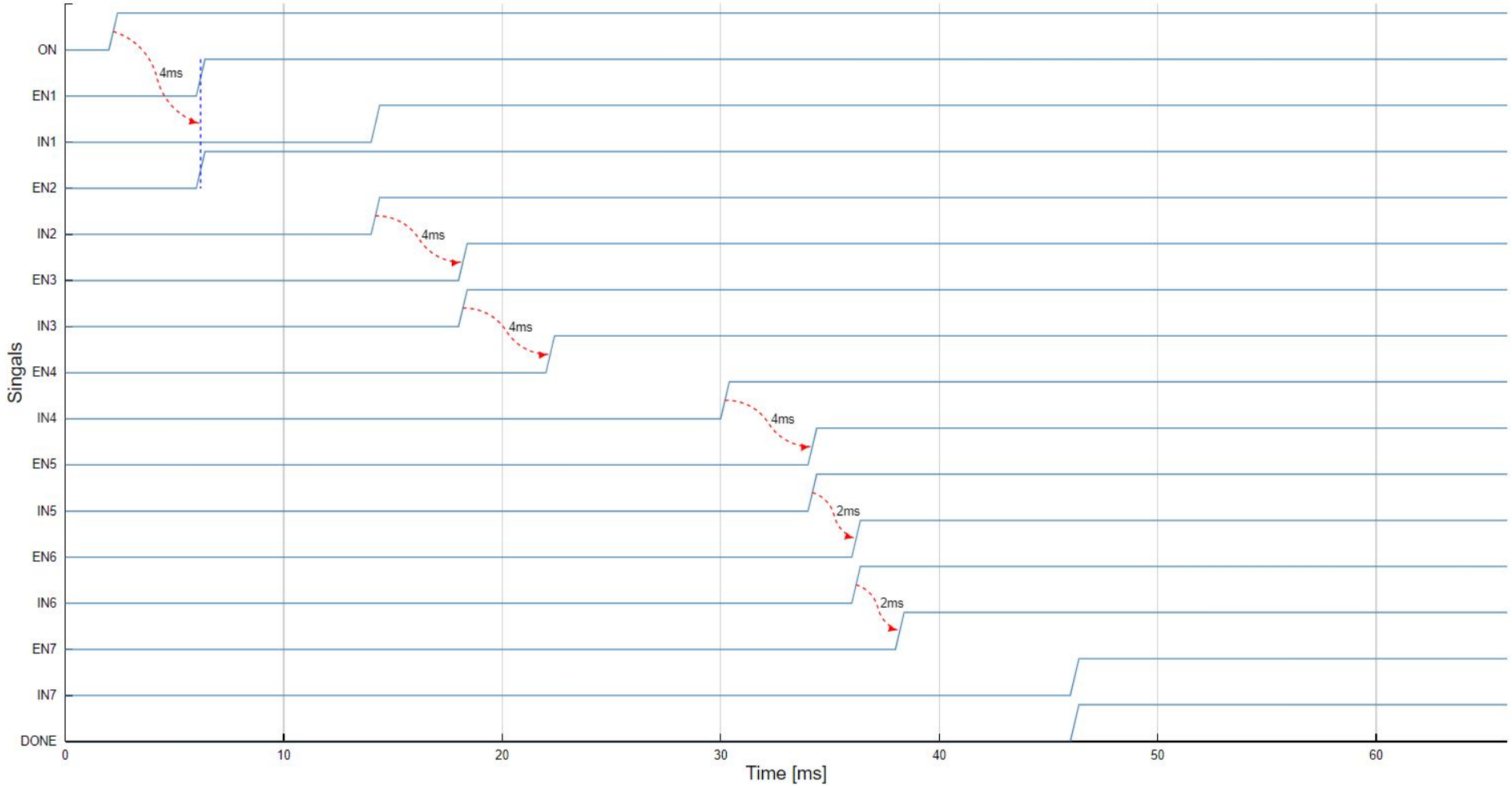
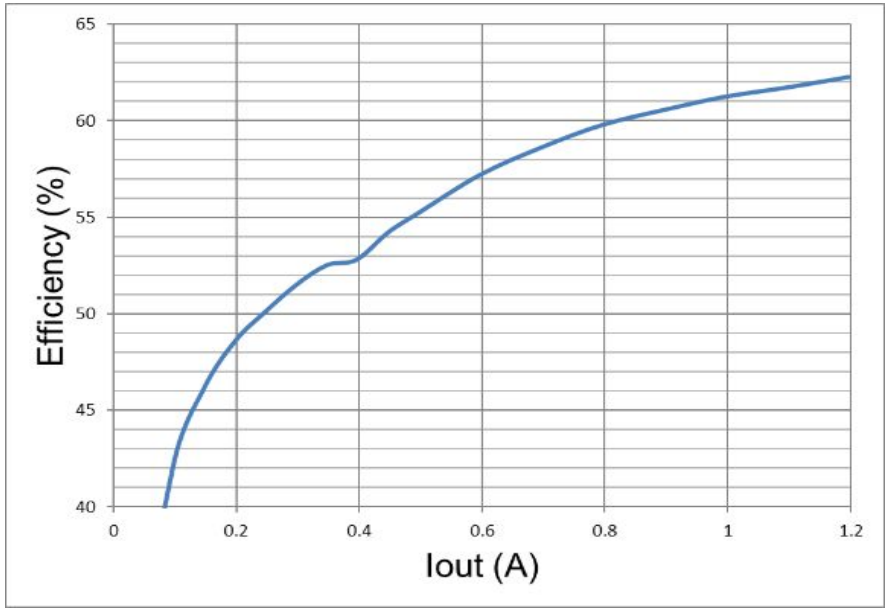
Integrated Sequencer Graphic (Turn ON)

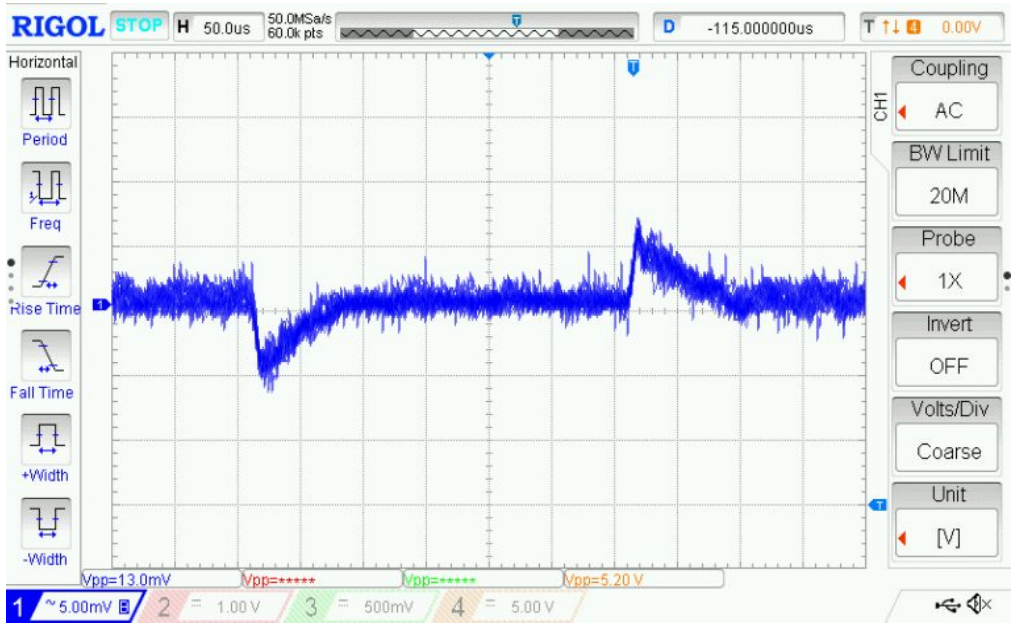


VCCINT
0.72 V / 1.2 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient





Vout = 0.85V
Transient 0.9A to 1.2A@2.5 A/us
Vpp = 13 mV
L = 2.2 uH and C = 94 uF.
f = 571 kHz

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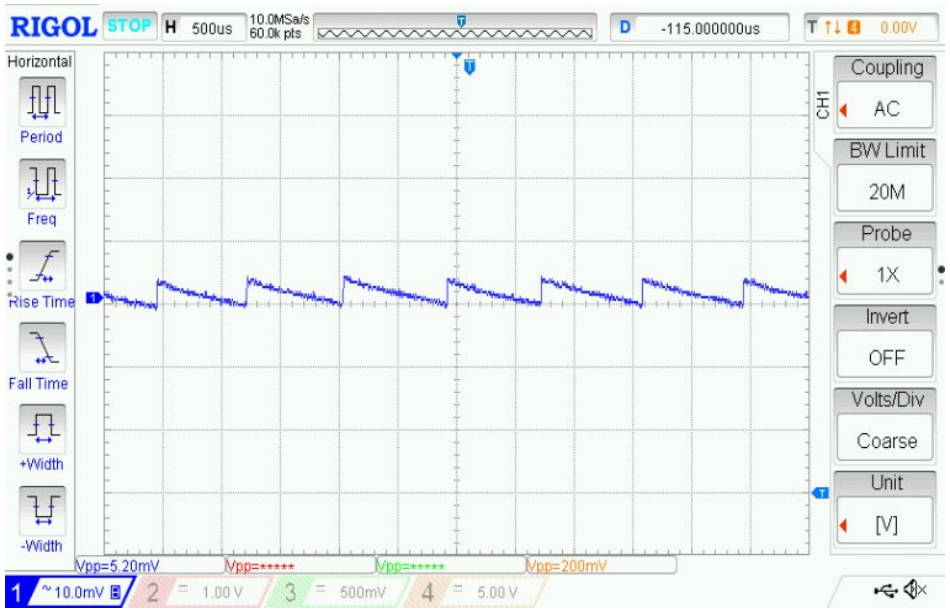
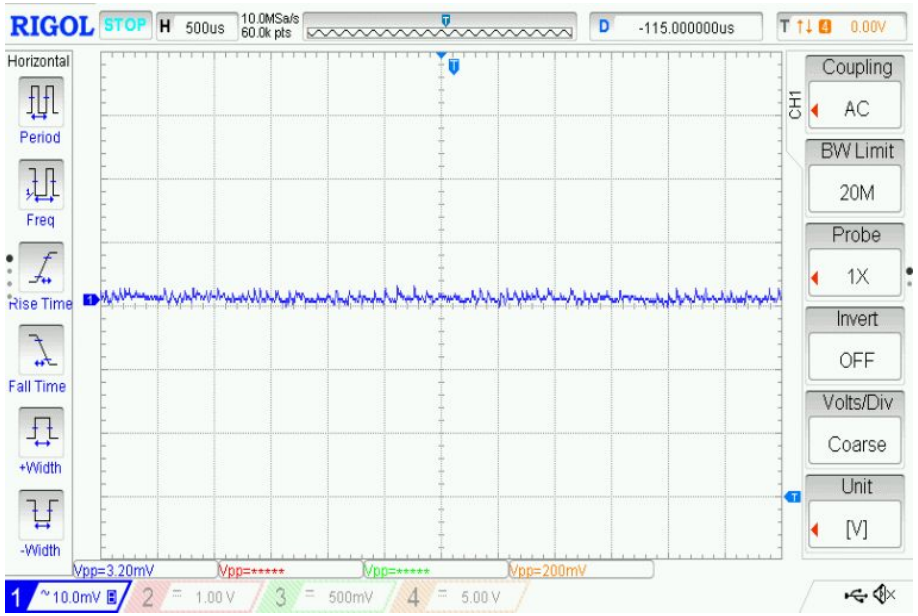
Ripple





No Load
V_{PP} = 5.2 mV

Vout = 0.72 V

1.2A Load
V_{PP} = 3.2 mV

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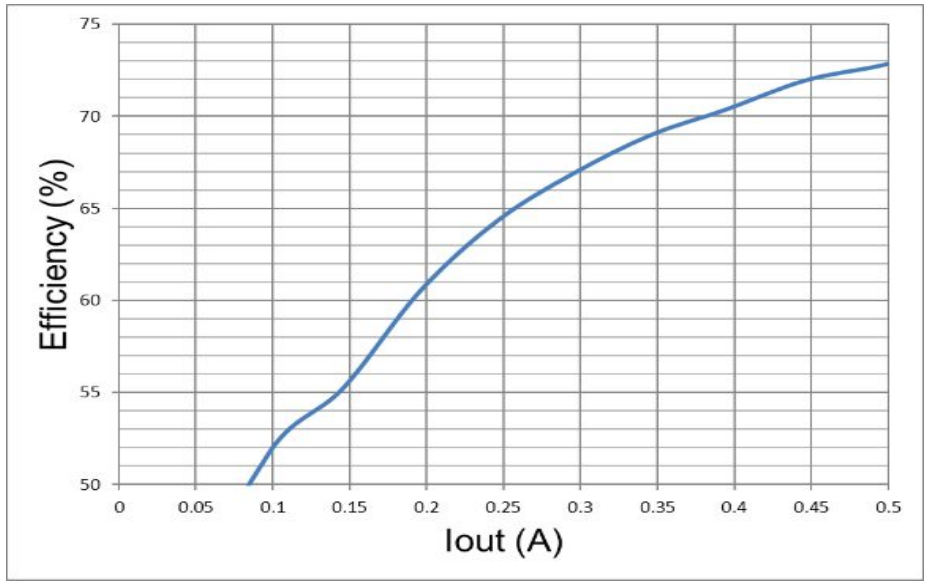
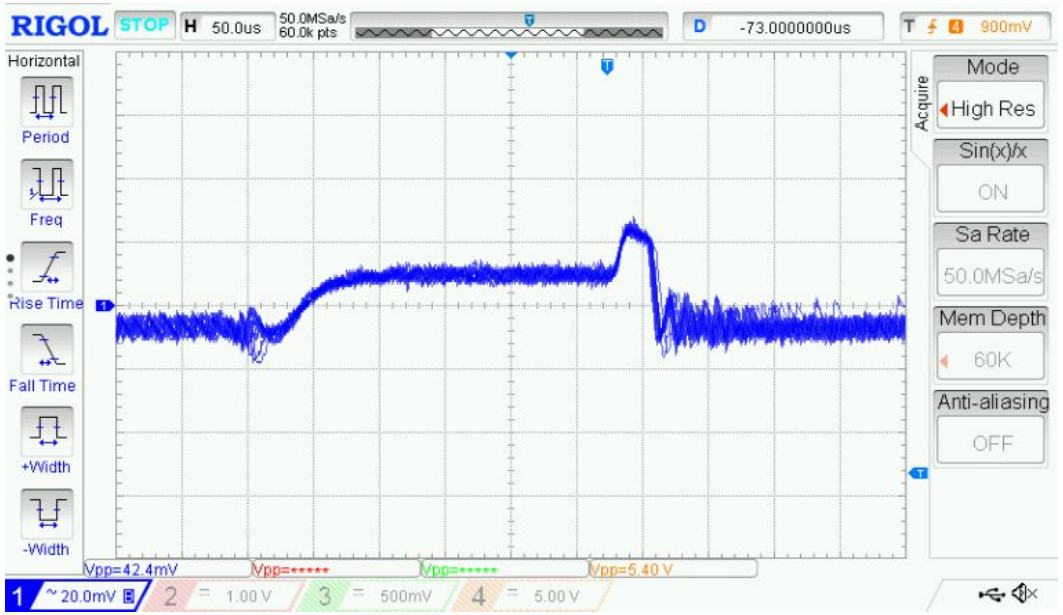
VBUS
2 V / 0.5 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74437334100
- C = 1x47 uF

Efficiency & Transient

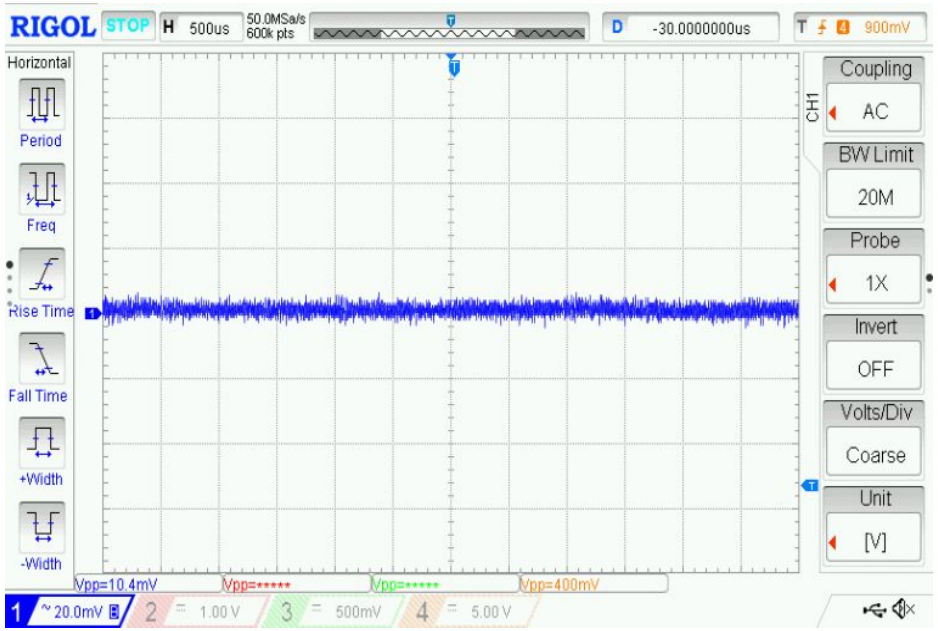




Vout = 2V
Transient 0A to 0.5A@2.5 A/us
Vpp = 42.4 mV
L = 10 uH and C = 47 uF.
f = 571 kHz

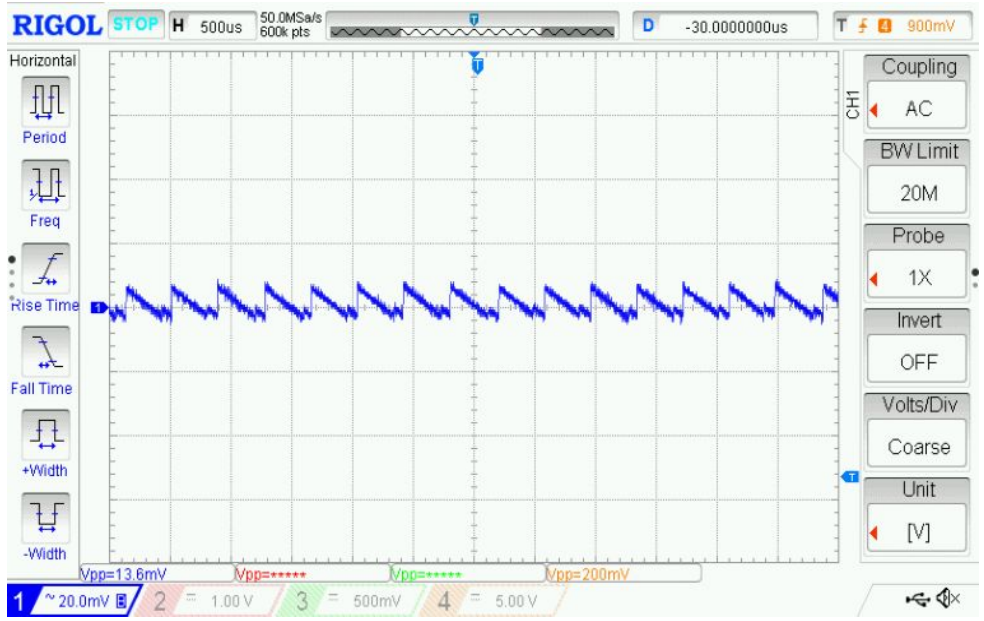
AnDAPT

Ripple



No Load
V_{PP} = 10.4 mV

Vout = 2 V



0.5 A Load
V_{PP} = 13.6 mV

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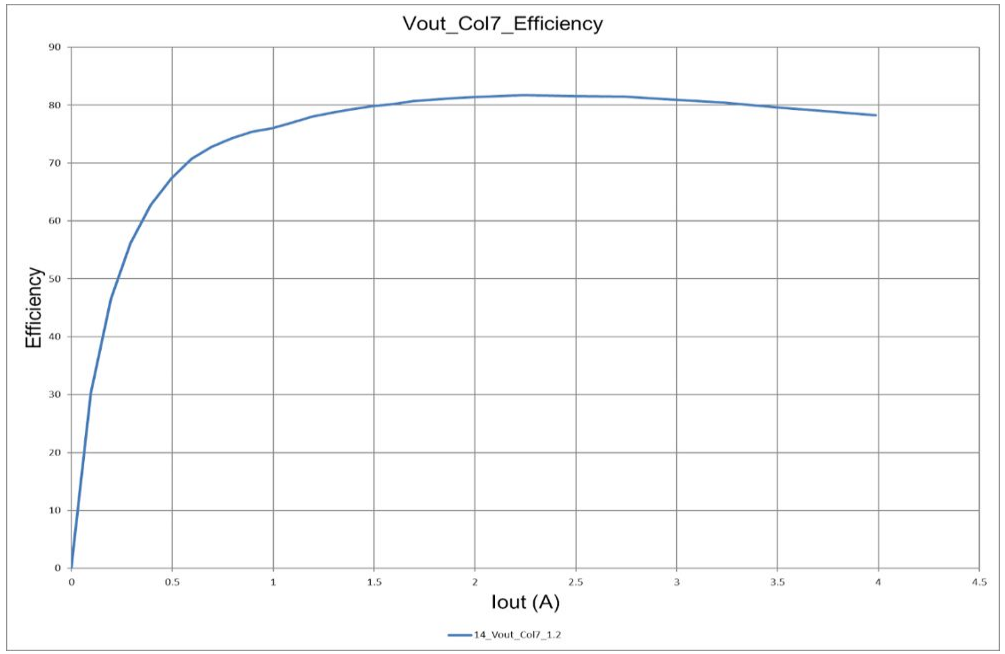
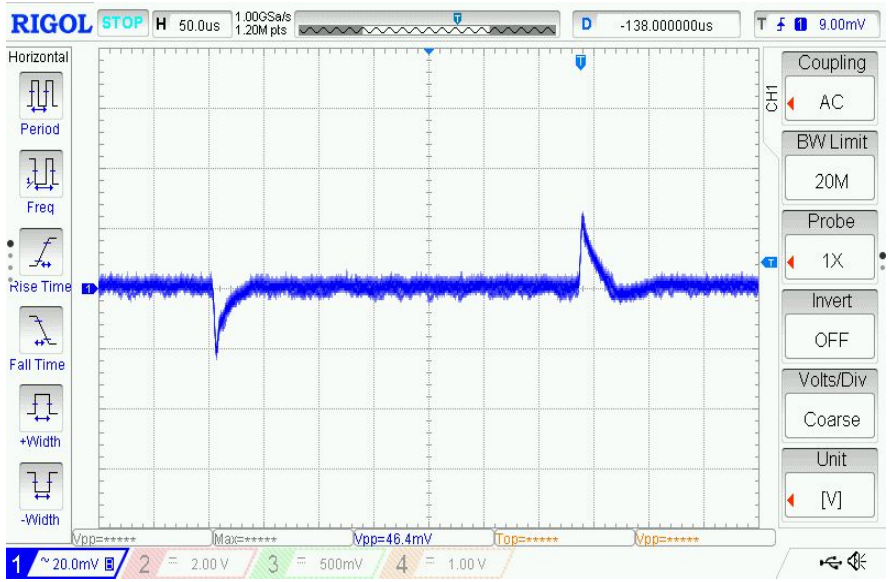
VMGAVTT
1.2 V / 4 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

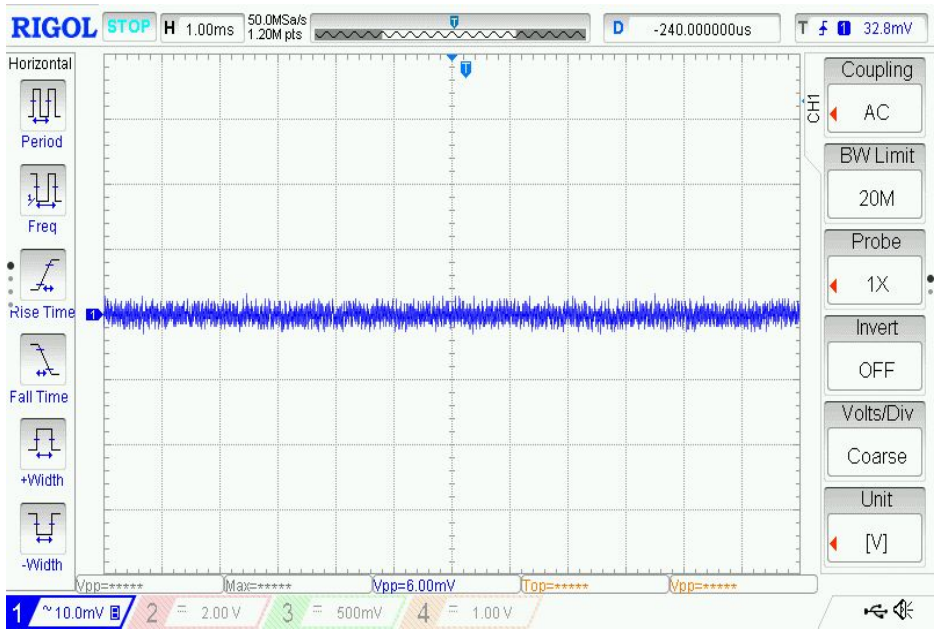
Efficiency & Transient

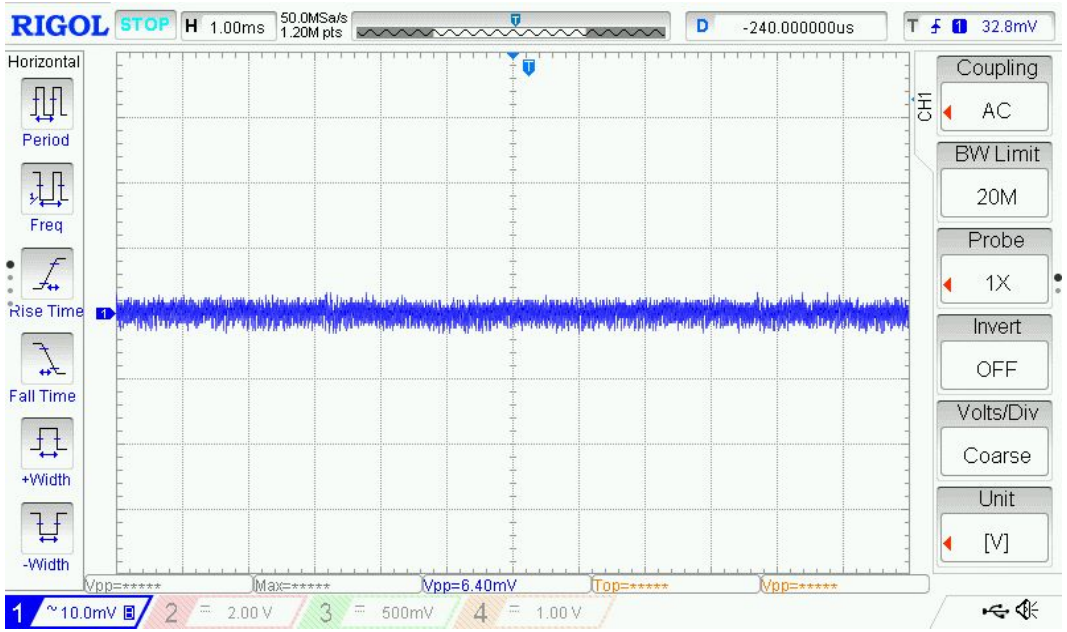




Vout = 1.2V
Transient 0.8A to 4A@10 A/us
Vpp = 46.4 mV
L = 0.56 uH and C = 329 uF.
f = 1 MHz

Ripple





No Load
V_{PP} = 6 mV

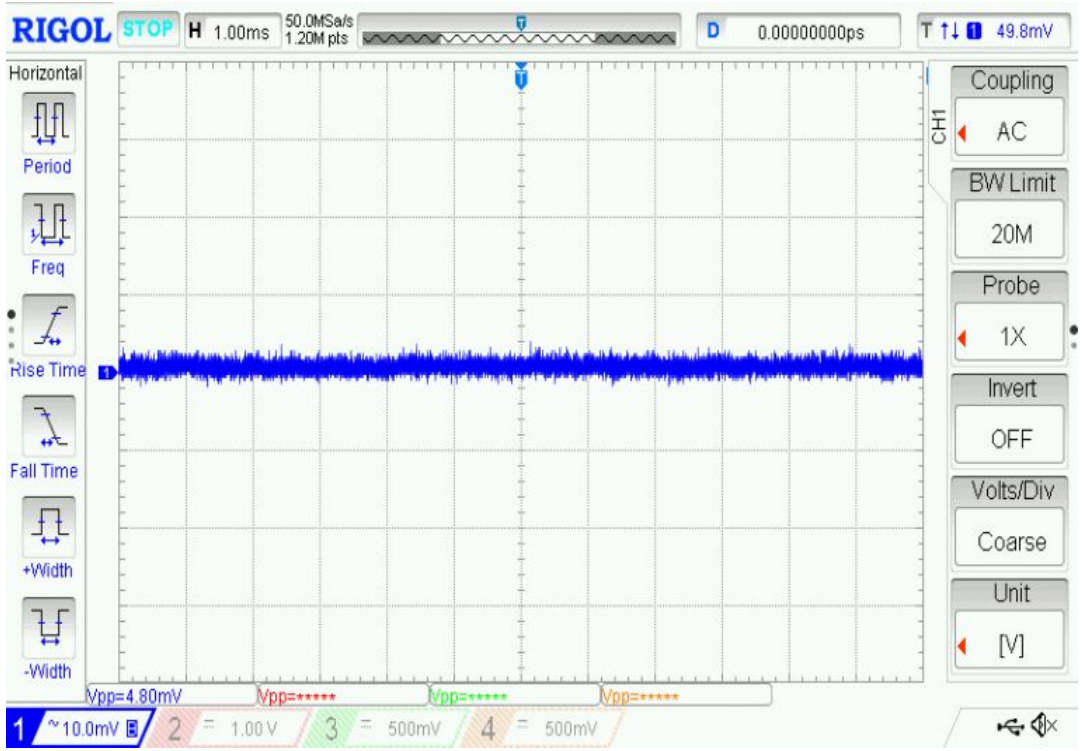
Vout = 1.2 V

4A Load
V_{PP} = 6.4 mV

VMGTVCCAUX
1.8 V / 0.15 A

- C710 LDO

Transient



Vout = 1.8 V
Transient 0.1125 A – 0.15 A @ 2.5 A/µs
V_{PP} = 4.8 mV

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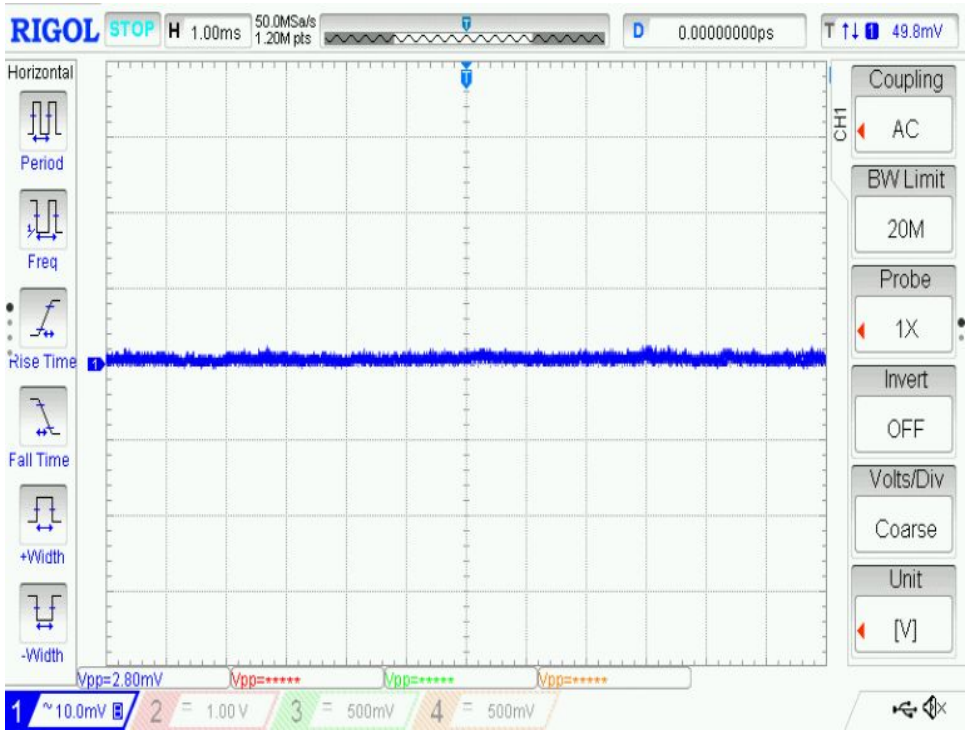
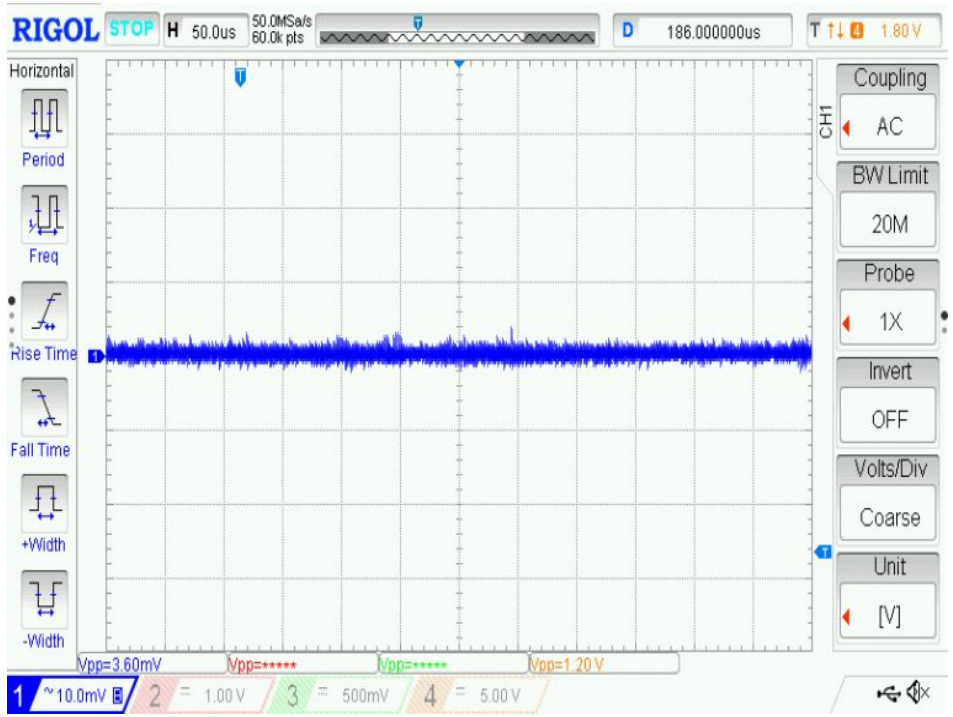
Ripple



No Load
V_{PP} = 2.8 mV

Vout = 1.8 V



0.15 A Load
V_{PP} = 3.6 mV

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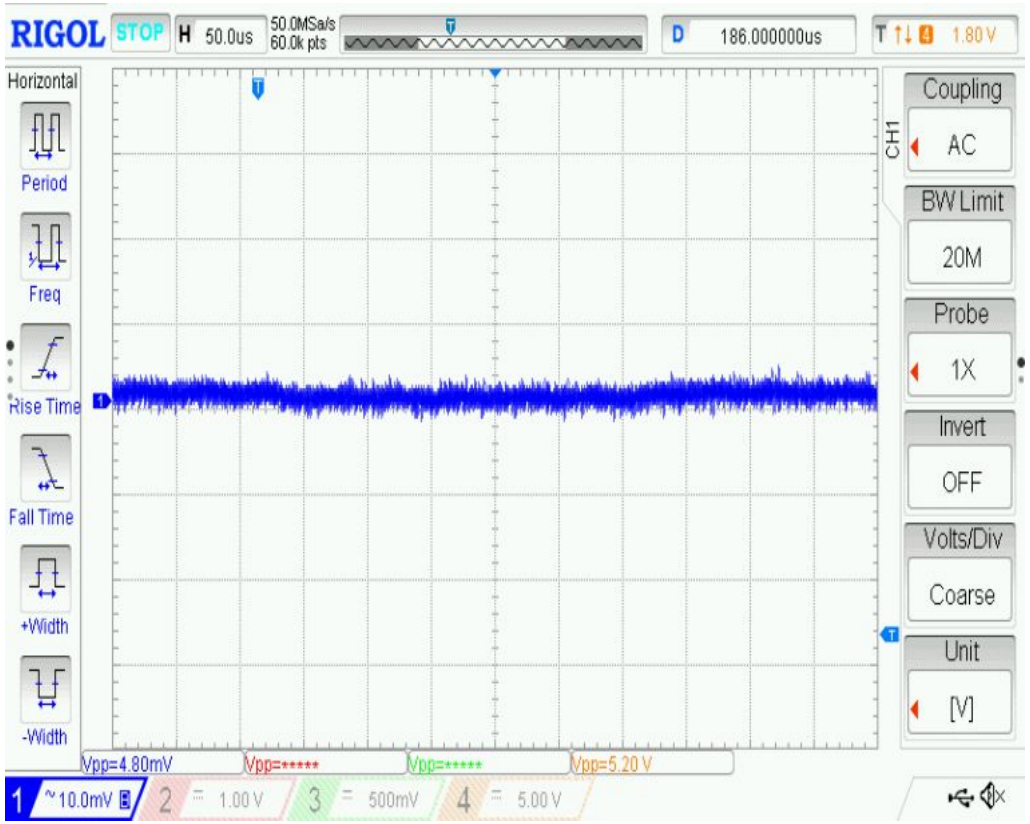
VMGTYAVCC
0.9 V / 0.75 A

- C710 LDO

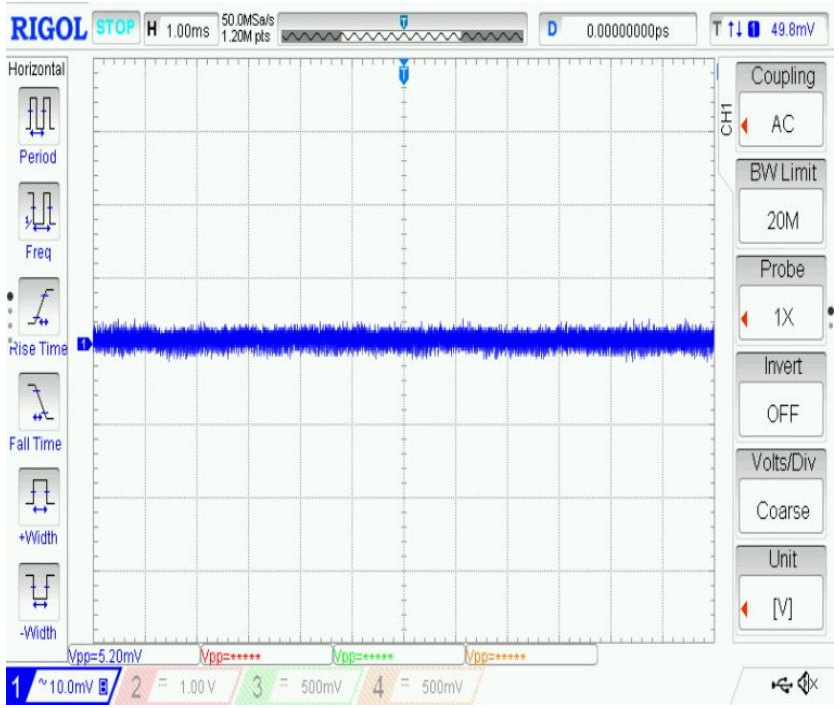
Transient



Vout = 0.9 V
Transient 0.5625 A – 0.75 A @ 2.5 A/µs
V_{PP} = 4.8 mV

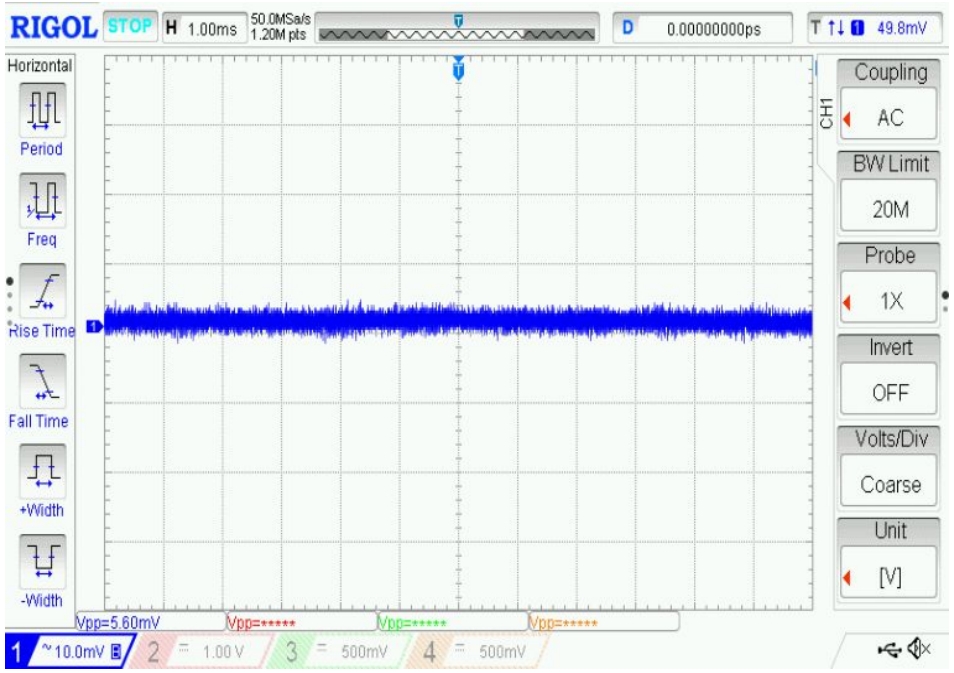
AnDAPT

Ripple



No Load
V_{PP} = 5.20 mV

Vout = 0.9 V

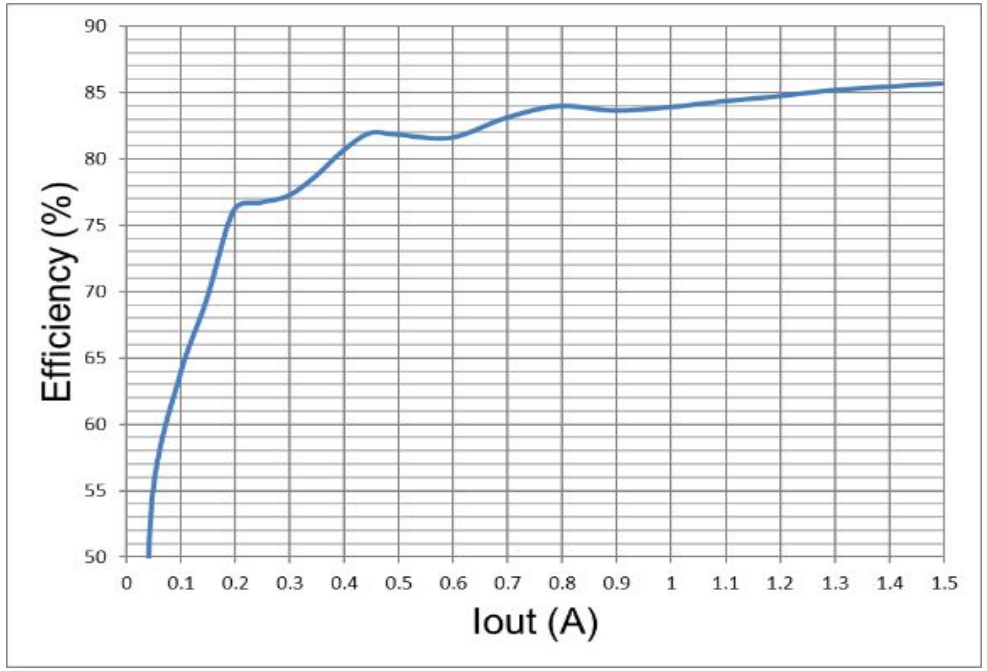


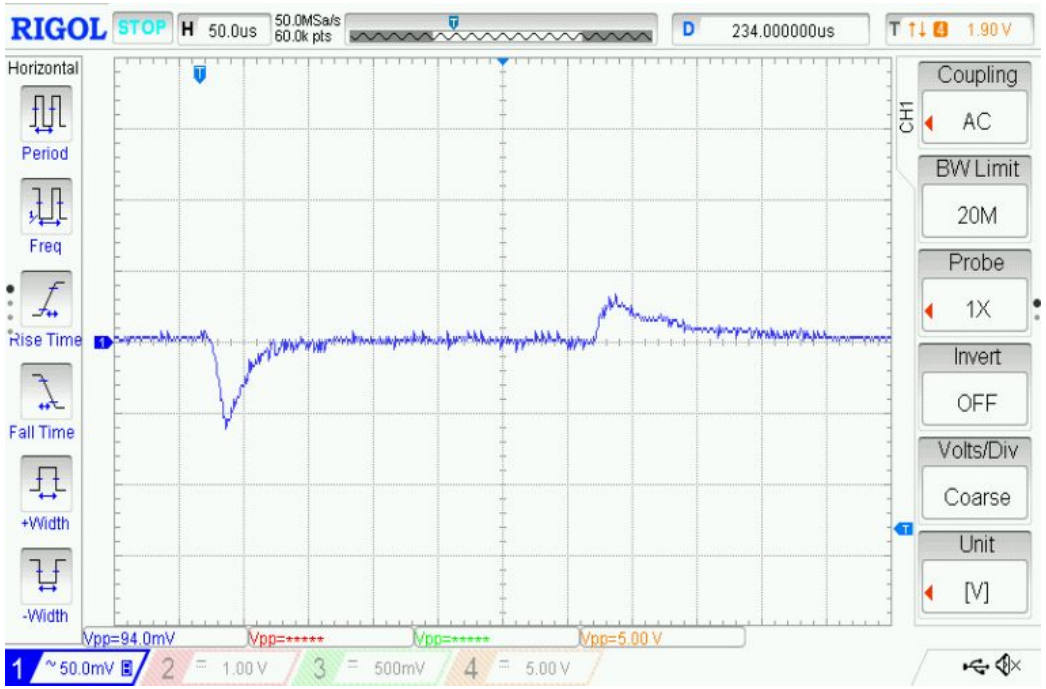
0.75 A Load
V_{PP} = 5.6 mV

VCCO
3.3 V / 1.5 A

- C150 Sync Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient





Vout = 3.3 V
Transient 0.15A – 1.5 A @ 2.5 A/µs
V_{PP} = 94 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

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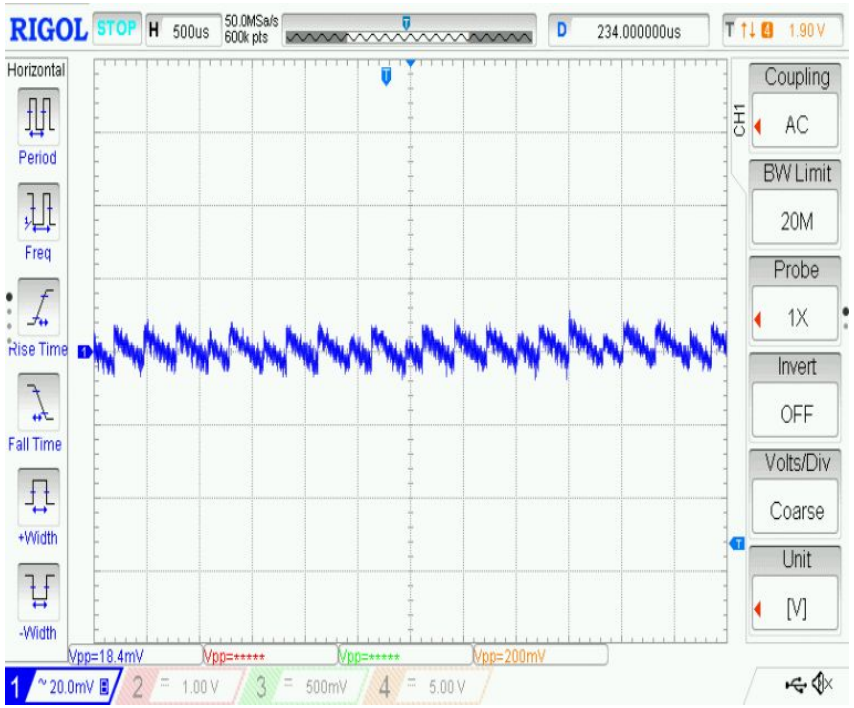
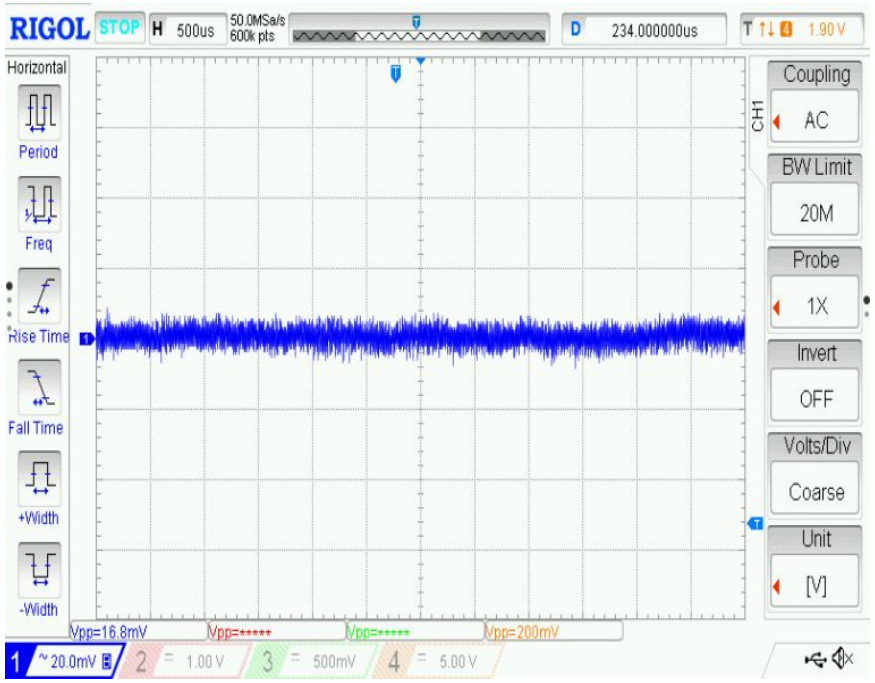
Ripple



No Load
V_{PP} = 18.4 mV

Vout = 3.3 V



1.5 A Load
V_{PP} = 16.8 mV

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End of
Artix UltraScale+ (Minimum Rails) Cost-optimized Portfolio Mappings & Test Data

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Thank You

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