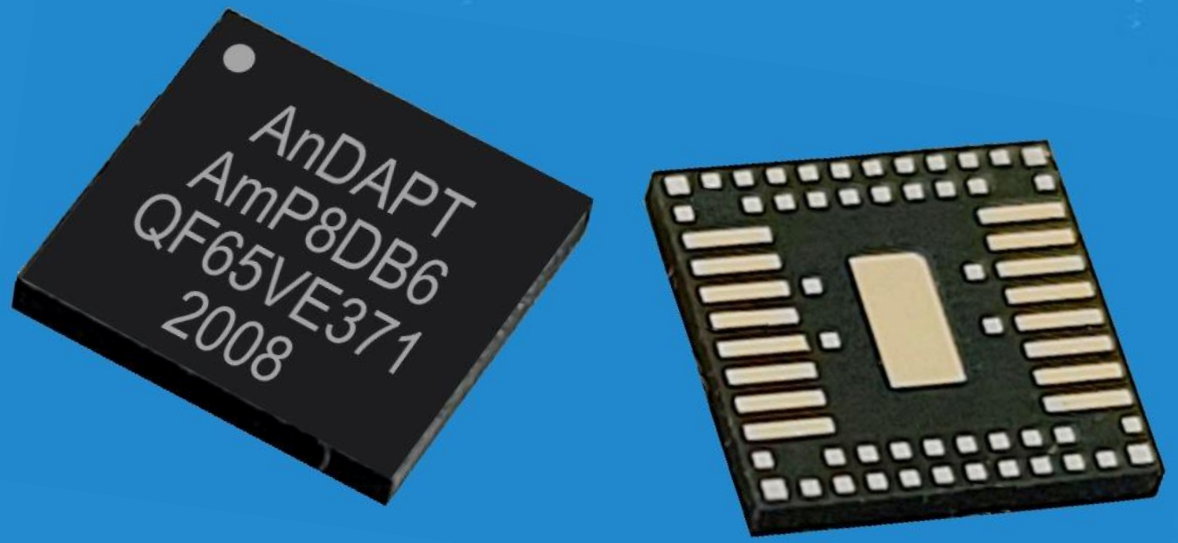

Artix 7 (Medium Low Power)

Mappings & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Artix 7+ family of devices SKUs (Medium Low Power)
- Artix 7+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Artix 7+ family FPGAs

*Xilinx document: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Artix 7 (Medium Low Power) Device SKUs Covered

Supported SKUs
XC7A12T
XC7A15T
XC7A25T
XC7A35T
XC7A50T
XC7A75T

Artix 7 (Medium Low Power)

Can be combined if voltage same

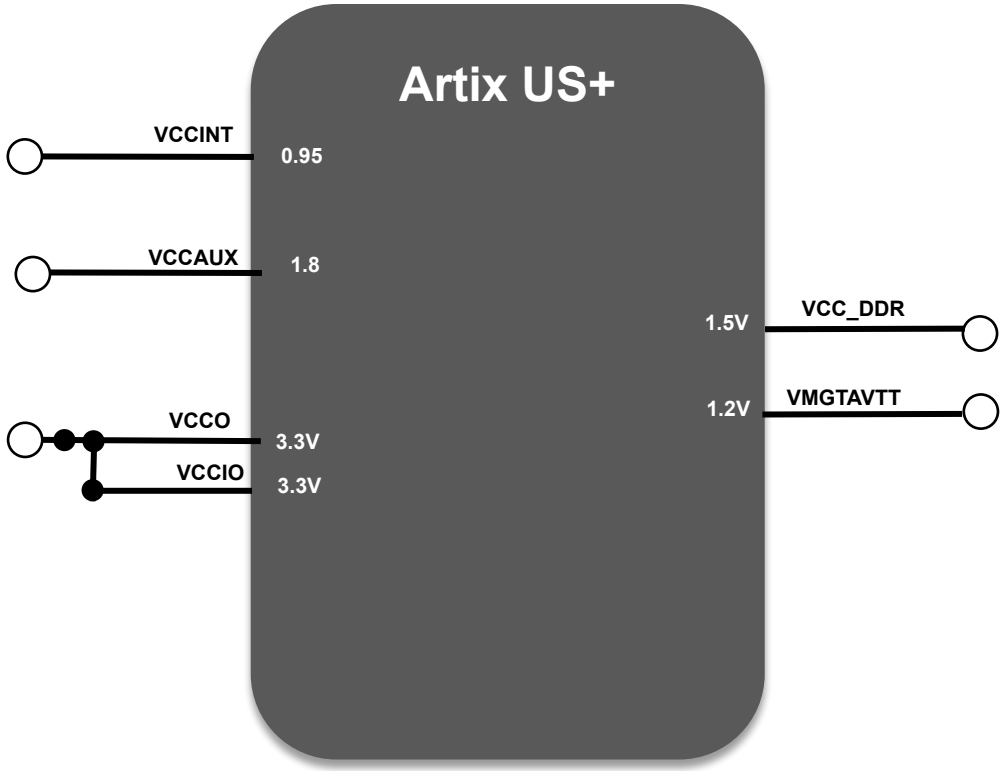

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree: Artix 7 (Medium Low Power)

PVIN = 12V

#	Rail	Seq	Vin (V)	Vout (V)	Iout (A)
1	VCCINT	1	12	0.95/1	5.2
2	VCC_DDR	4	1.8	1.5	2
3	VMGTAVTT	4	12	1.2	1
4	VCCAUX	2	12	1.8	0.31
5	VCCIO	4	12	3.3	0.2
6	VCCO	3	12	3.3	0.03

Power Tree Mapping: Artix 7 (Medium Low Power)

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRAM, MGTAVCC	1	C200	Sync Buck	V_{IN}	12	0.95/1	5.2	ARD_X_AX7_A1_IC1
2	VCC_DDR	4	C150	Sync Buck	V_{IN}	1.8	1.35 to 1.5	<2	ARD_X_AX7_A1_IC1
3	VMGTAVTT	4	C200	Sync Buck	V_{IN}	12	1.2	≤1	ARD_X_AX7_A1_IC1
4	VCCAUX, VCCADC	2	C150	Async Buck	V_{IN}	12	1.8	<0.31	ARD_X_AX7_A1_IC1
6	VCCIO	4	C710	SIM LDO	V_{IN}	12	1.8 or 3.3	<0.2	ARD_X_AX7_A1_IC1
7	VCCO[0.1…]	3	CLDO	Corner LDO	V_{IN}	12	1.2 to 3.3	≤0.03	ARD_X_AX7_A1_IC1

Estimated total area estimated = 602.97 mm^2

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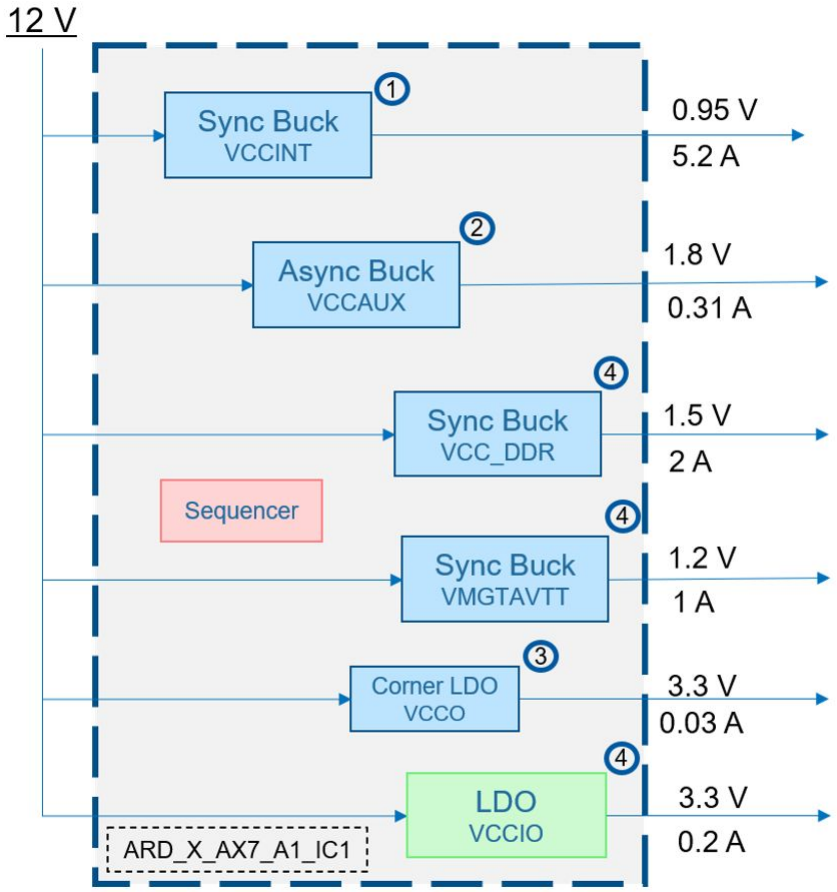
Power Tree Mapping



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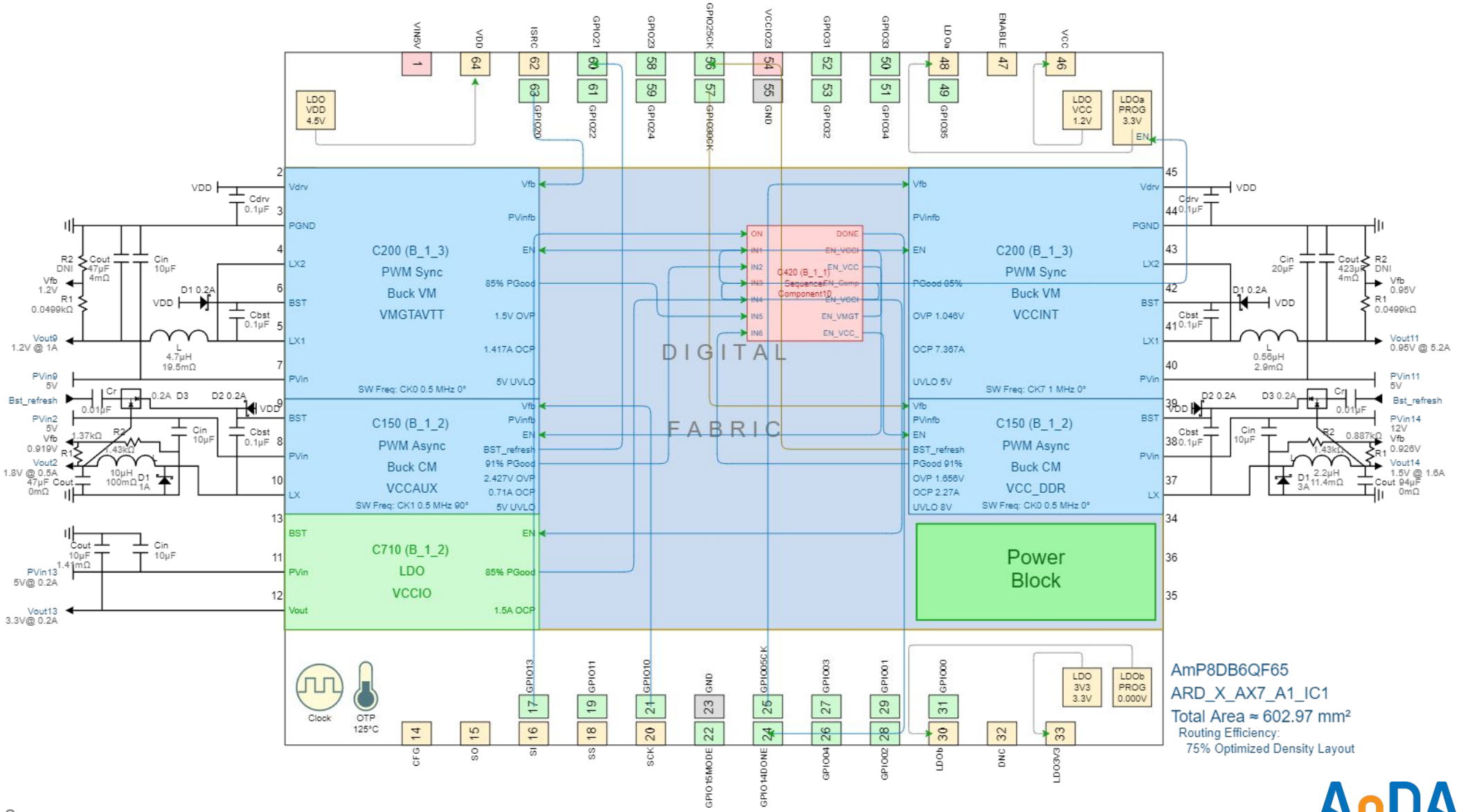
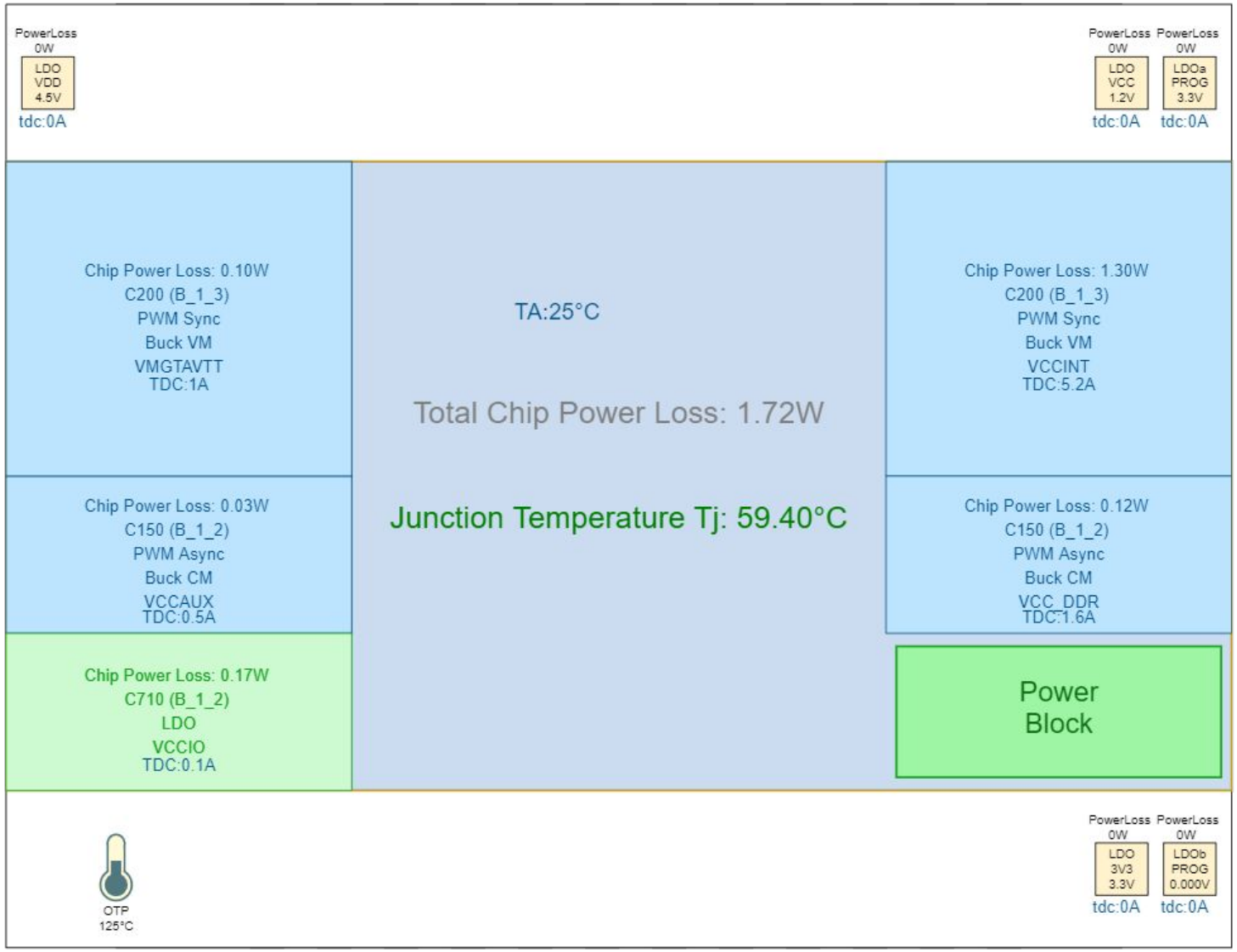
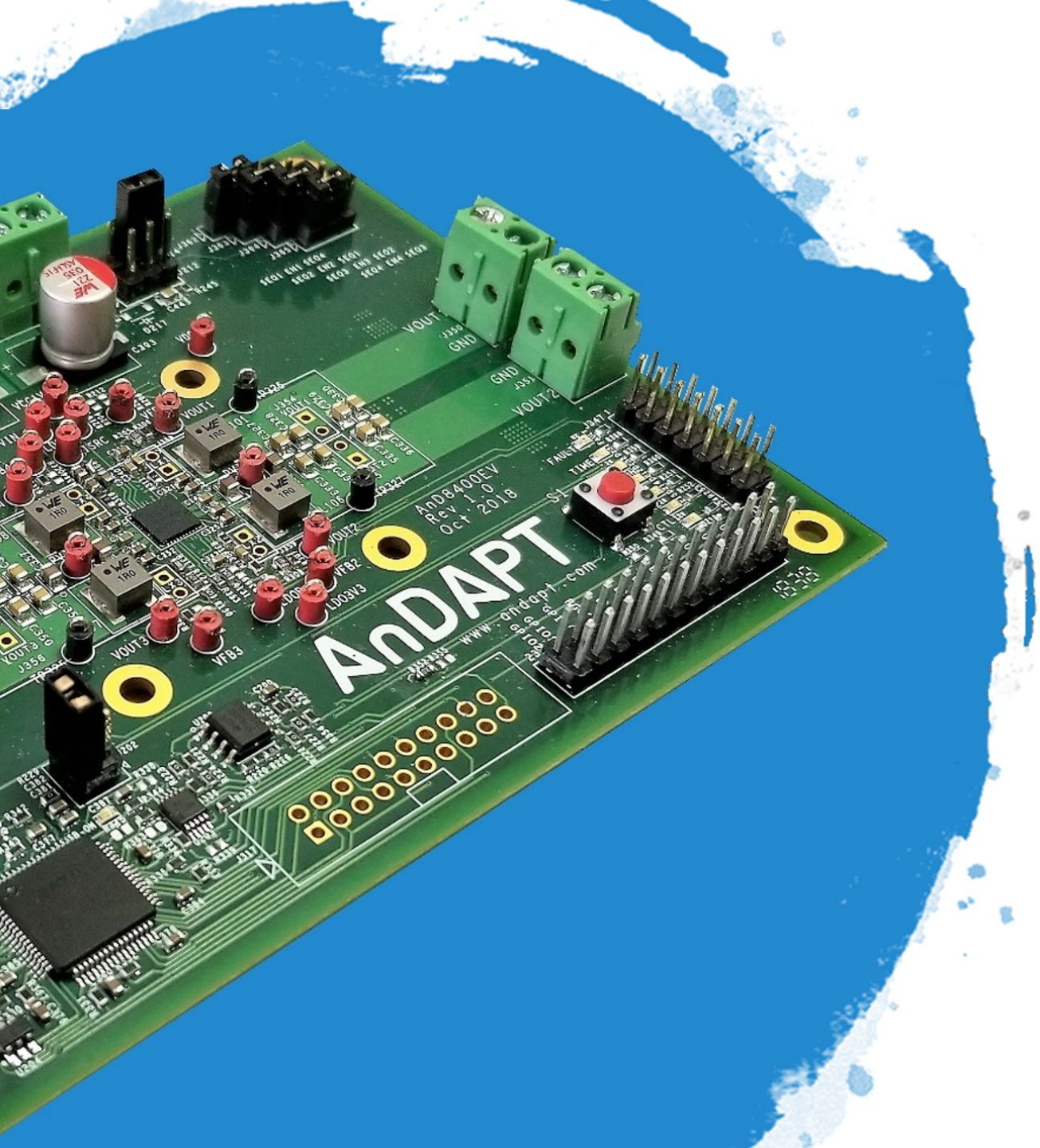
Mapping (WebAmP View)



Mapping (Thermal View)



AmP8DB6QF65
ARD_X_AX7_A1_IC1
Total Area ≈ 602.97 mm²
Routing Efficiency:
75% Optimized Density Layout



Test Data

Artix 7 (Medium Low Power)

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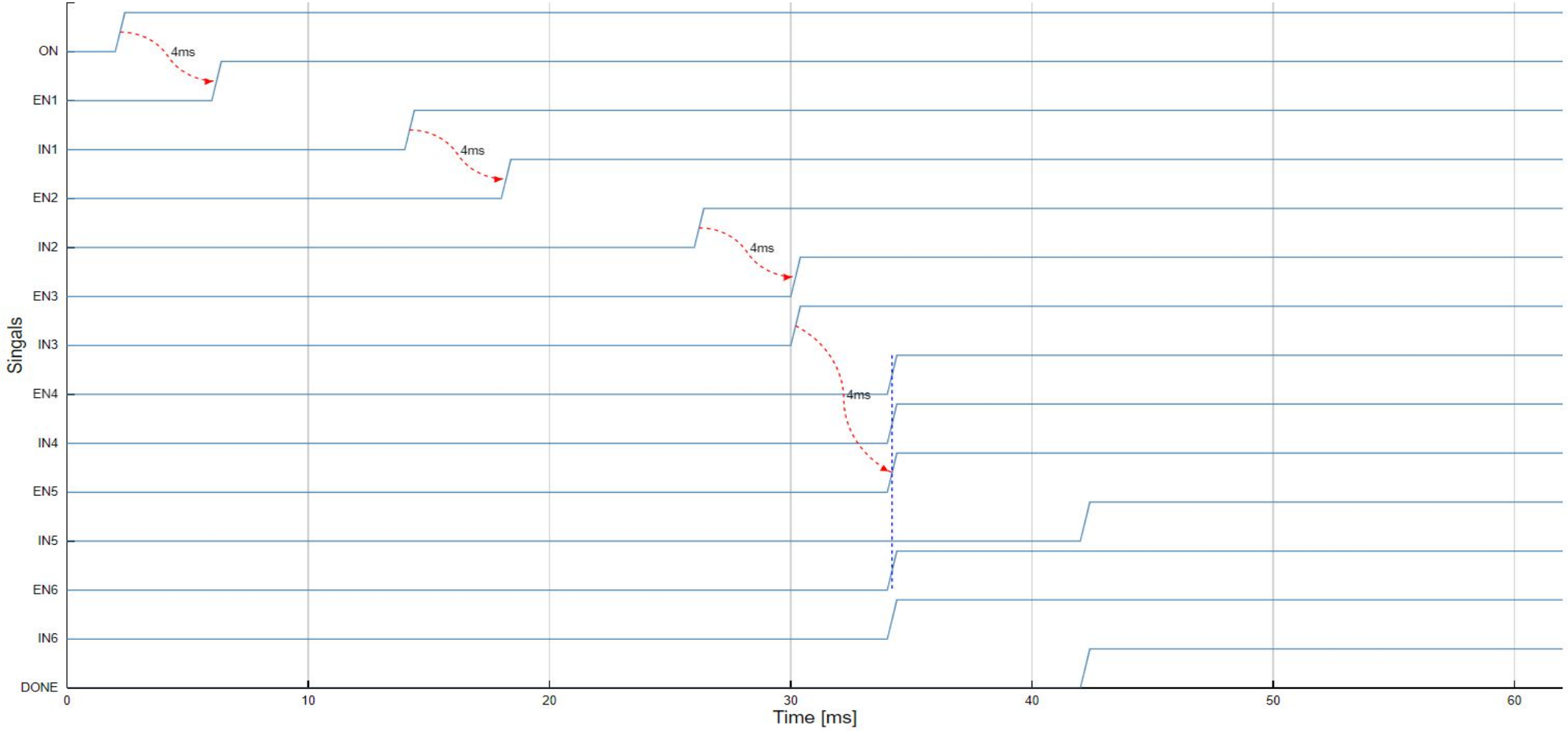
Integrated Sequencer Graphic (Turn ON)



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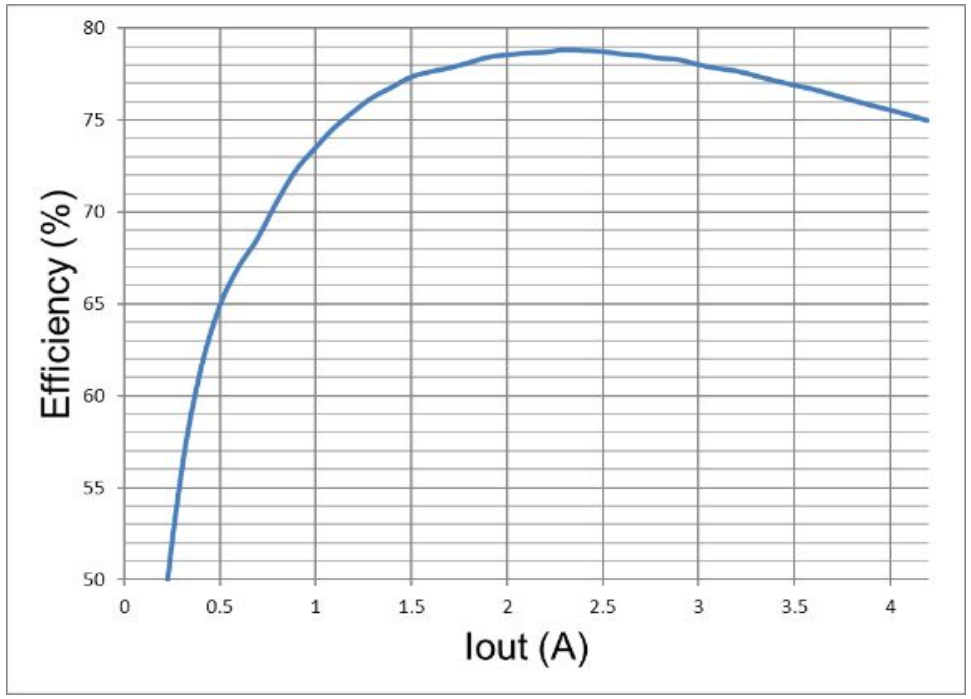
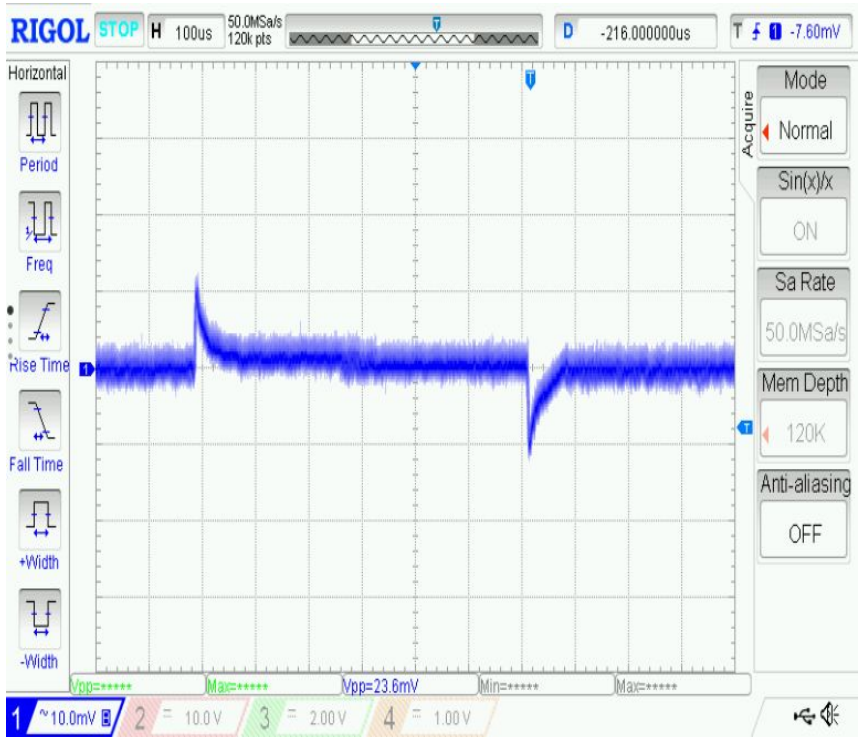
VCCINT
0.95 V / 5.2 A

- C200
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

Efficiency & Transient

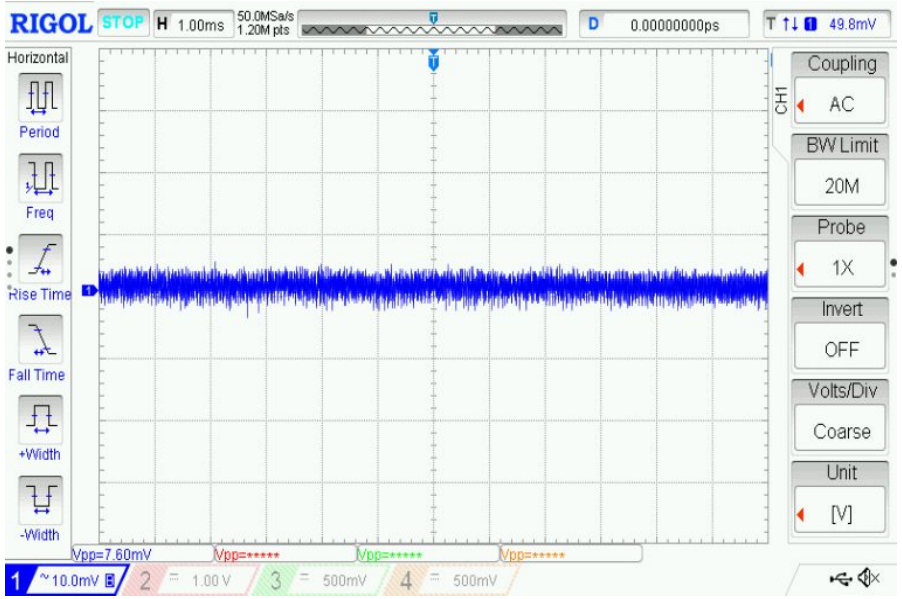




Vout = 0.95V
Transient 3.15A – 4.2A @ 100 A/µs
V_{PP} = 23.6 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

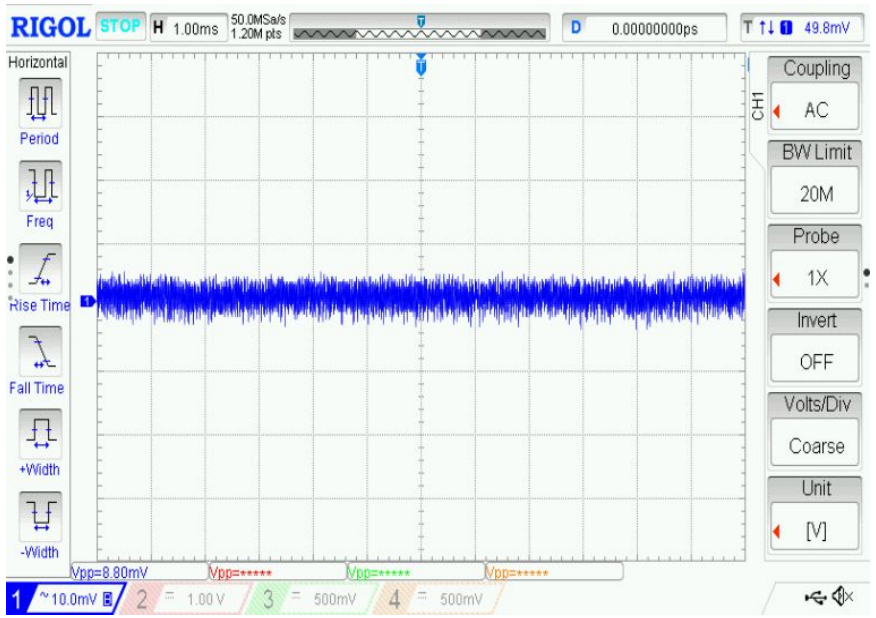
AnDAPT

Ripple



No Load
V_{PP} = 7.6 mV

Vout = 0.95 V



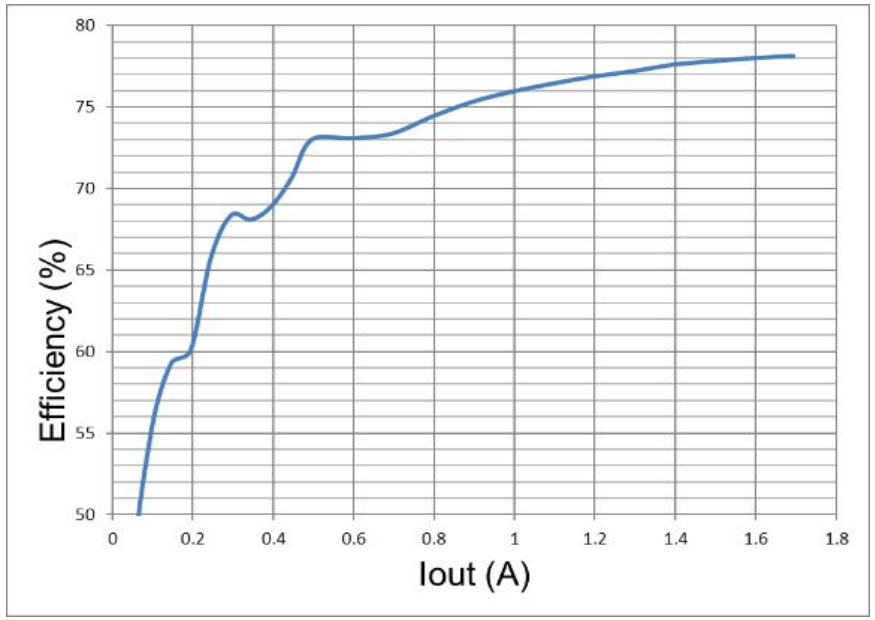
30 A Load
V_{PP} = 8.80 mV

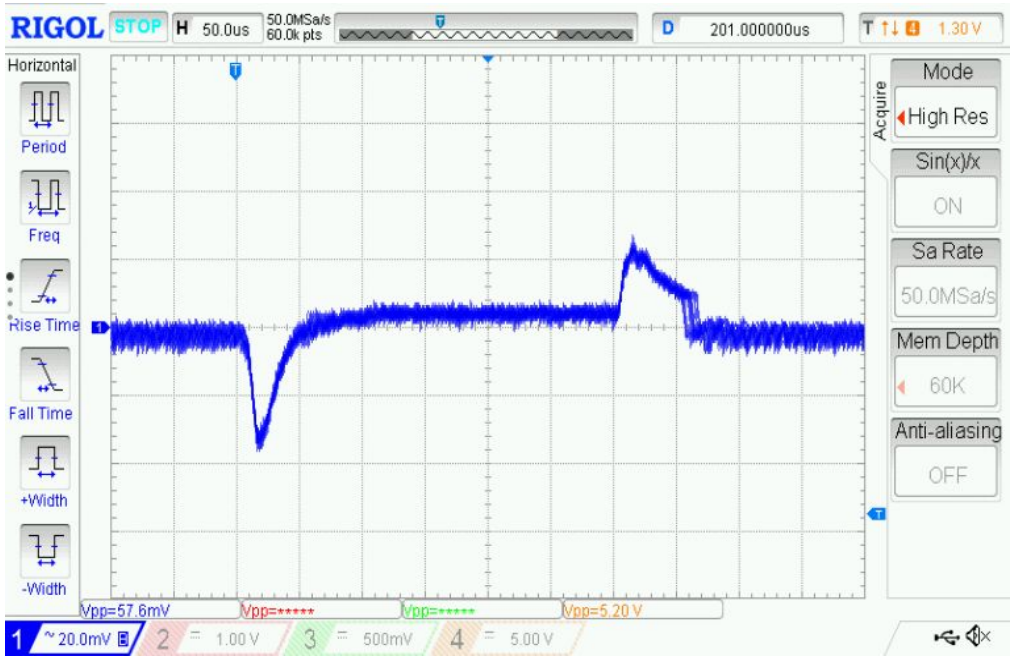
AnDAPT

VCC_DDR
1.5 V / 2 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient

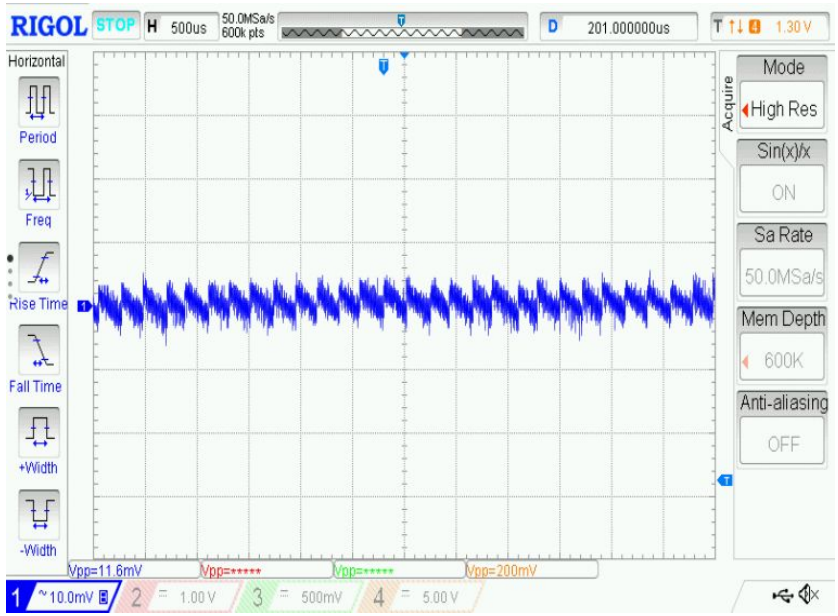




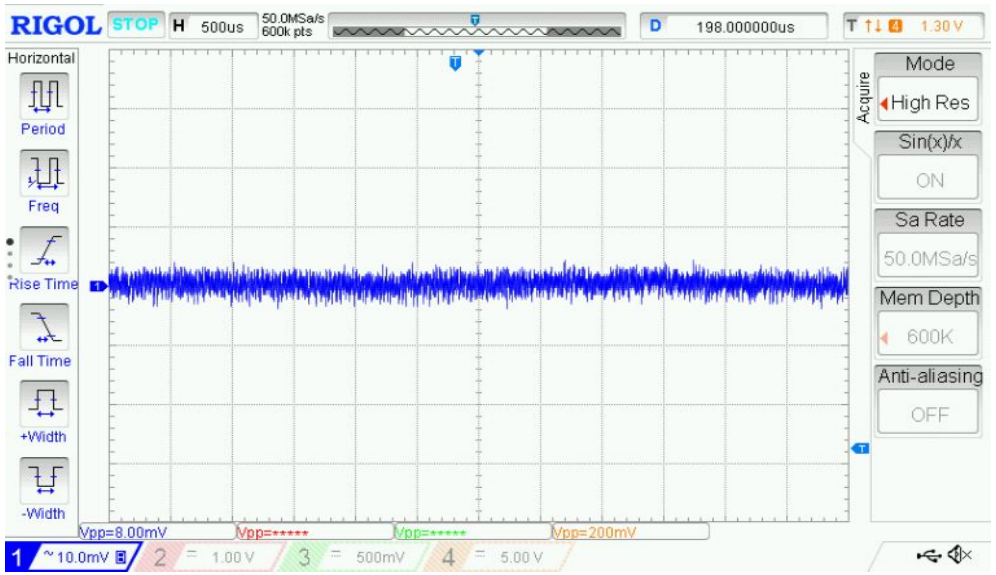
Vout = 1.5V
Transient 0.16A to 1.6A@10 A/us
Vpp = 57.6 mV
L = 2.2 uH and C = 94 uF.
f = 571 kHz

AnDAPT

Ripple



No Load
V_{PP} = 11.6 mV



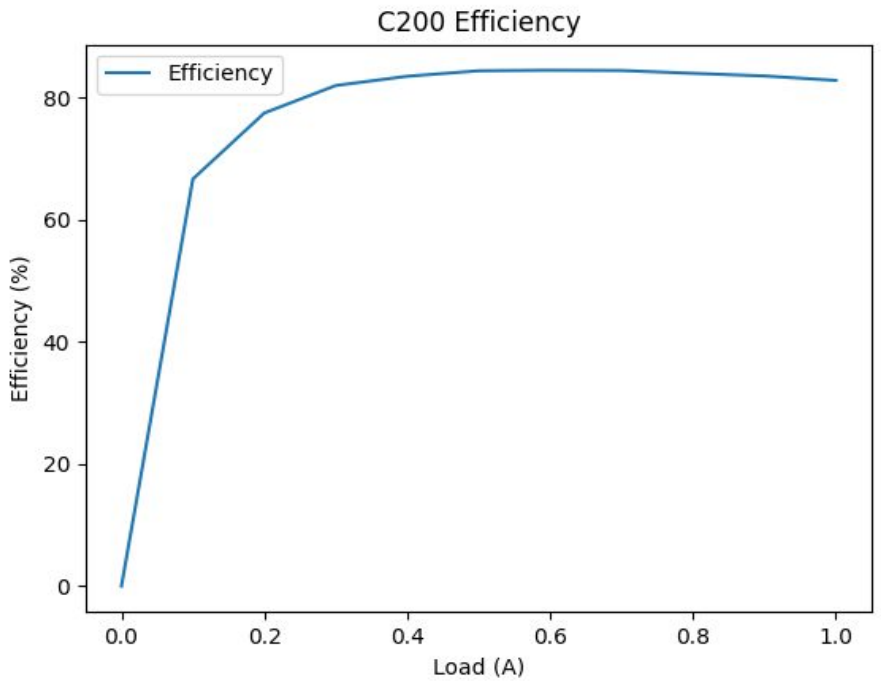
Vout = 1.5 V

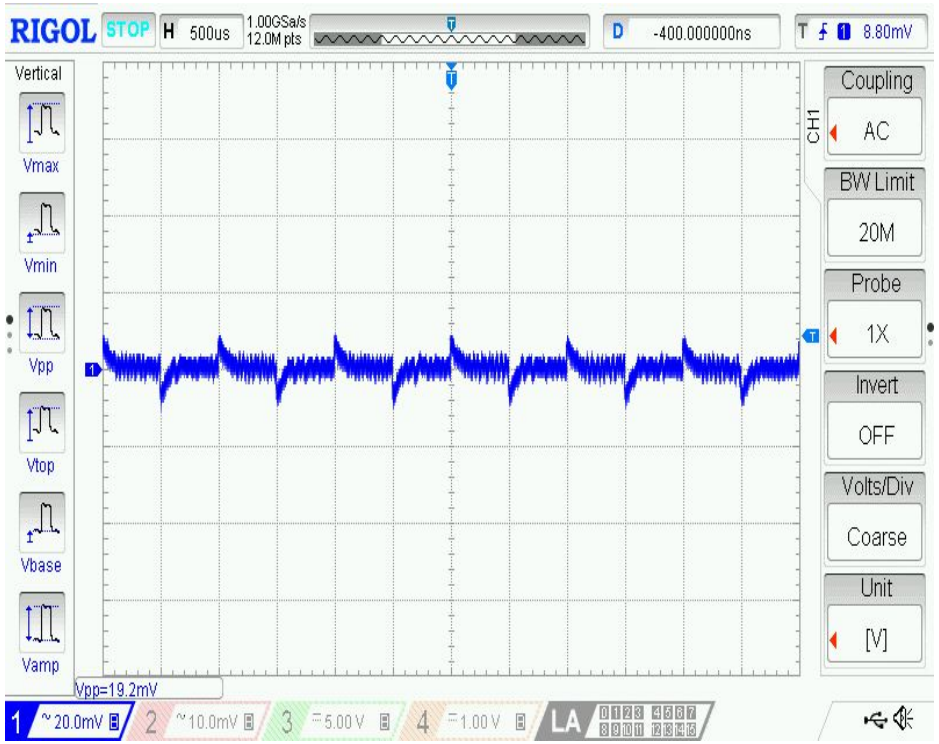
1.5A Load
V_{PP} = 8 mV

VMGTAVTT
1.2 V / 1 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

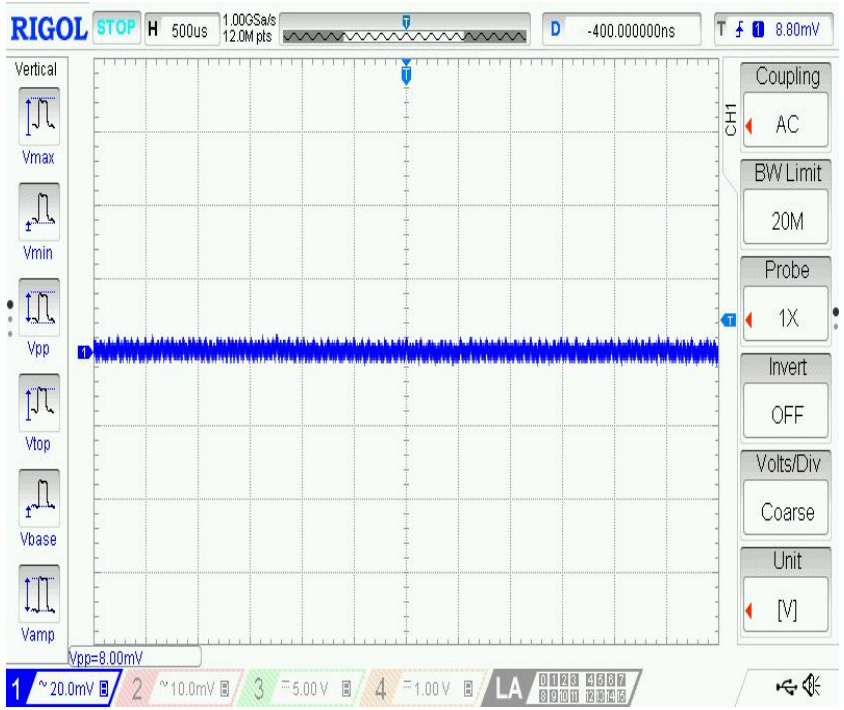
Efficiency & Transient





Vout = 1.2V
Transient 0.75A to 1A@2.5 A/us
Vpp = 19.2 mV
L = 4.7 uH and C = 47 uF.
f = 571 kHz

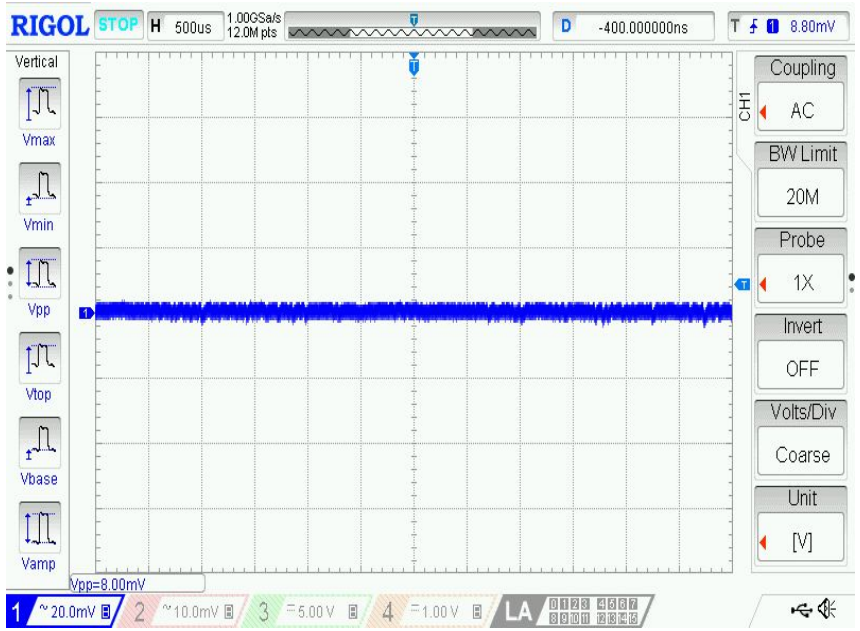
Ripple



No Load

V_{PP} = 8.0 mV

Vout = 1.2 V



1 A Load

V_{PP} = 8 mV

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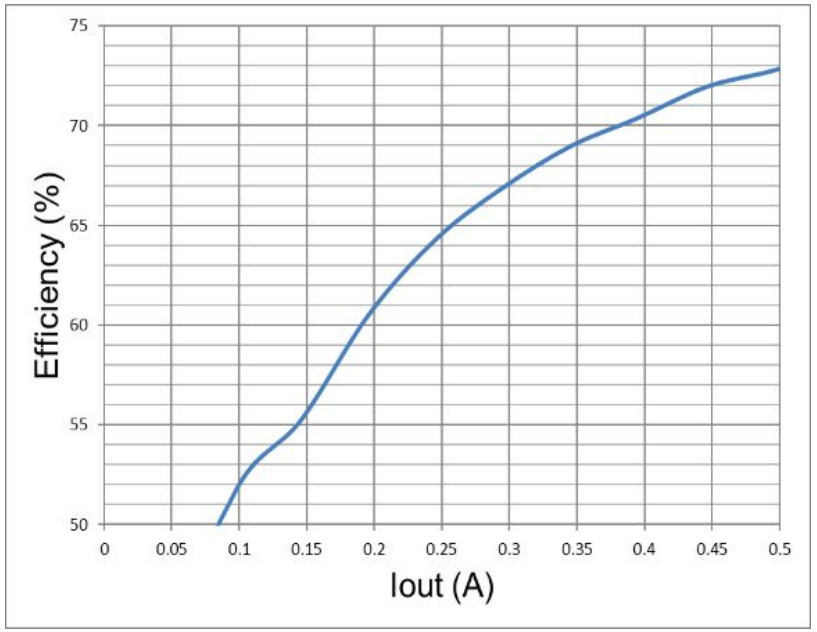
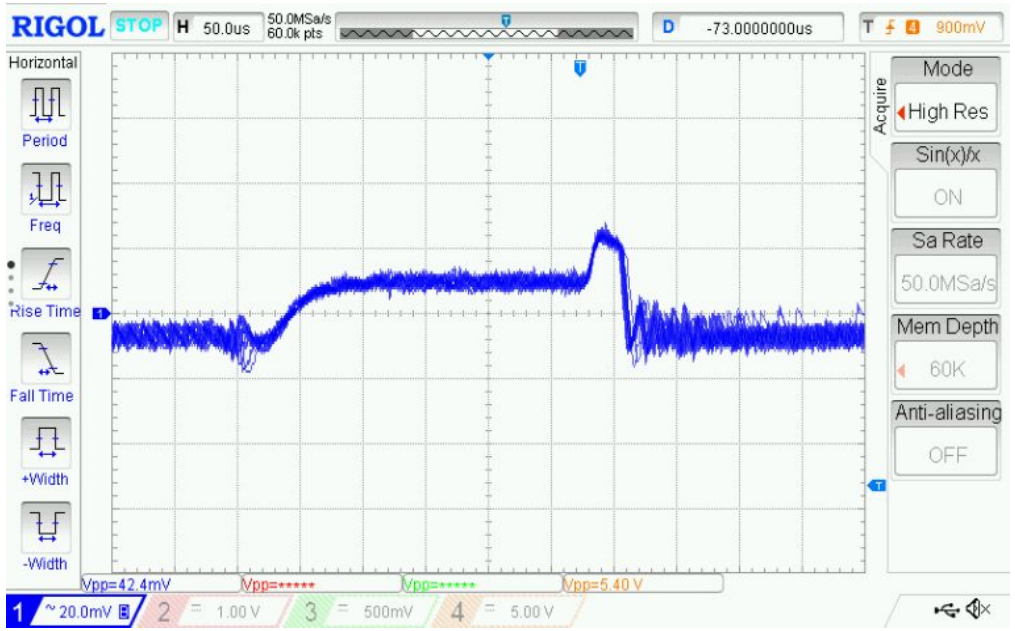
VCCAUX
1.8 V / 0.31A

- C150 Sync Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74437334100
- C = 1x47 uF

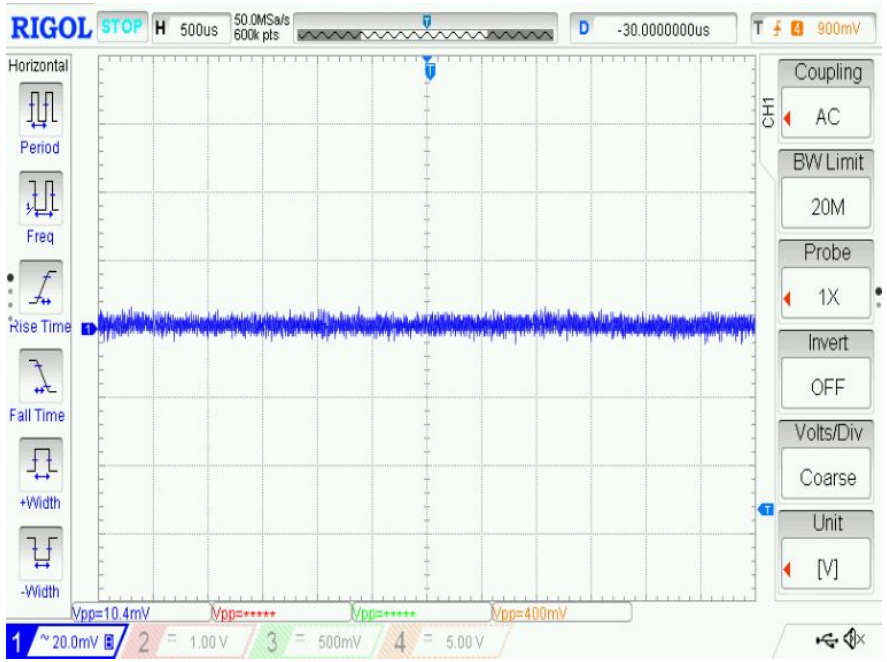
Efficiency & Transient





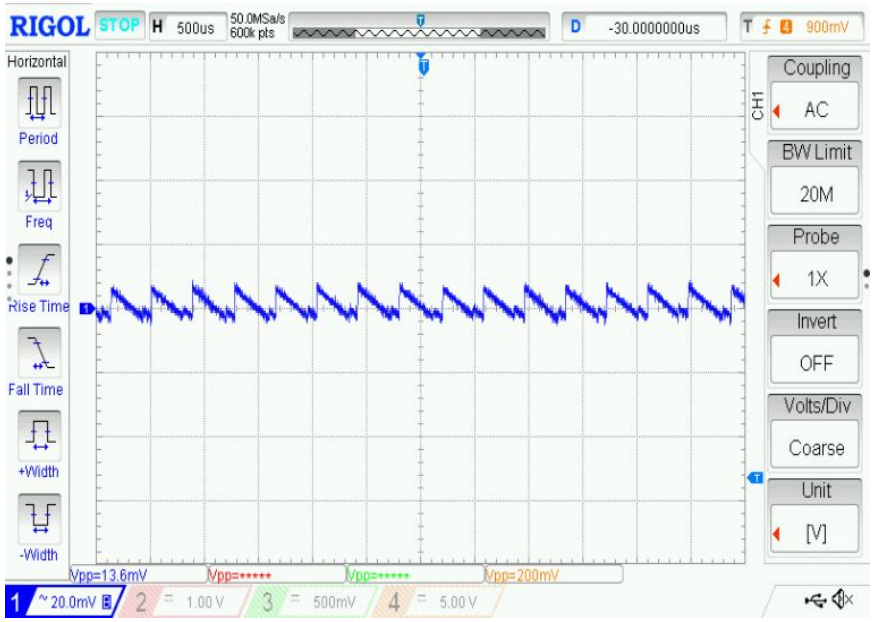
Vout = 1.8V
Transient 0A to 0.5A@2.5 A/us
Vpp = 42.4 mV
L = 10 uH and C = 47 uF.
f = 571 kHz

Ripple



No Load
V_{PP} = 10.4 mV

Vout = 1.8 V



0.5A Load
V_{PP} = 13.6 mV

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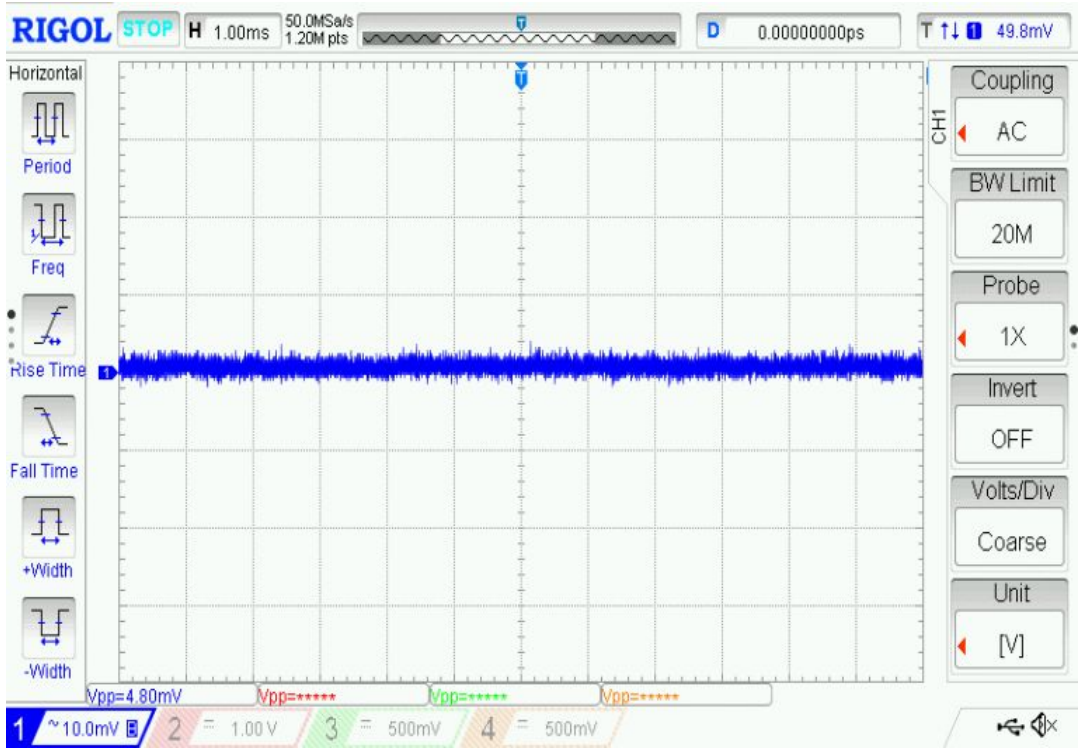
VCCIO
1.8 V / 0.2 A

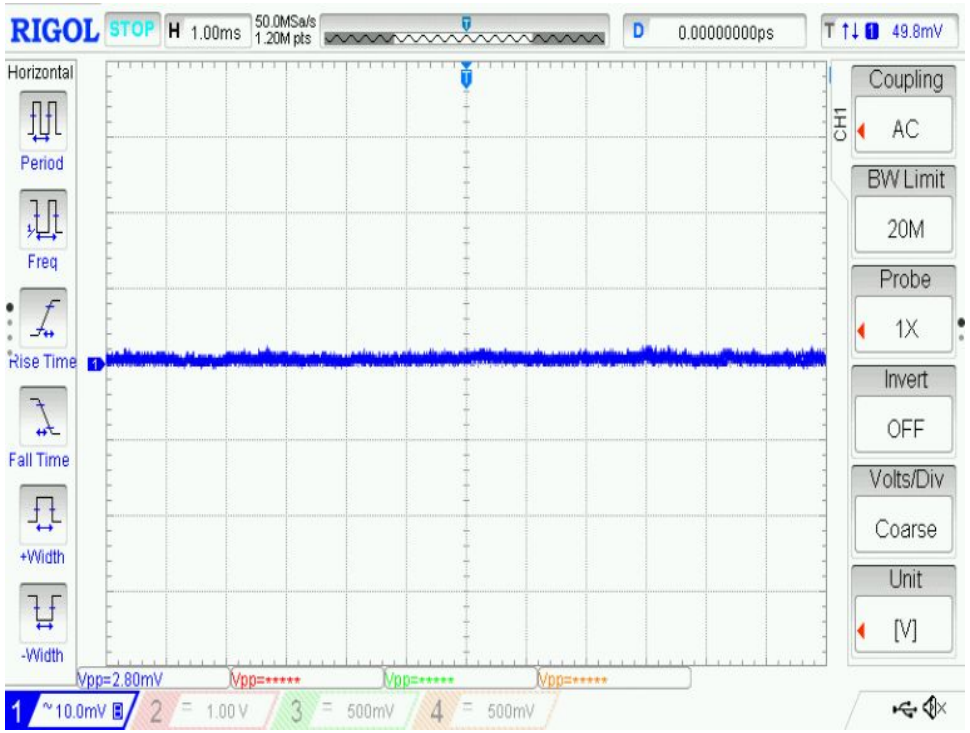
- C710 LDO

Transient



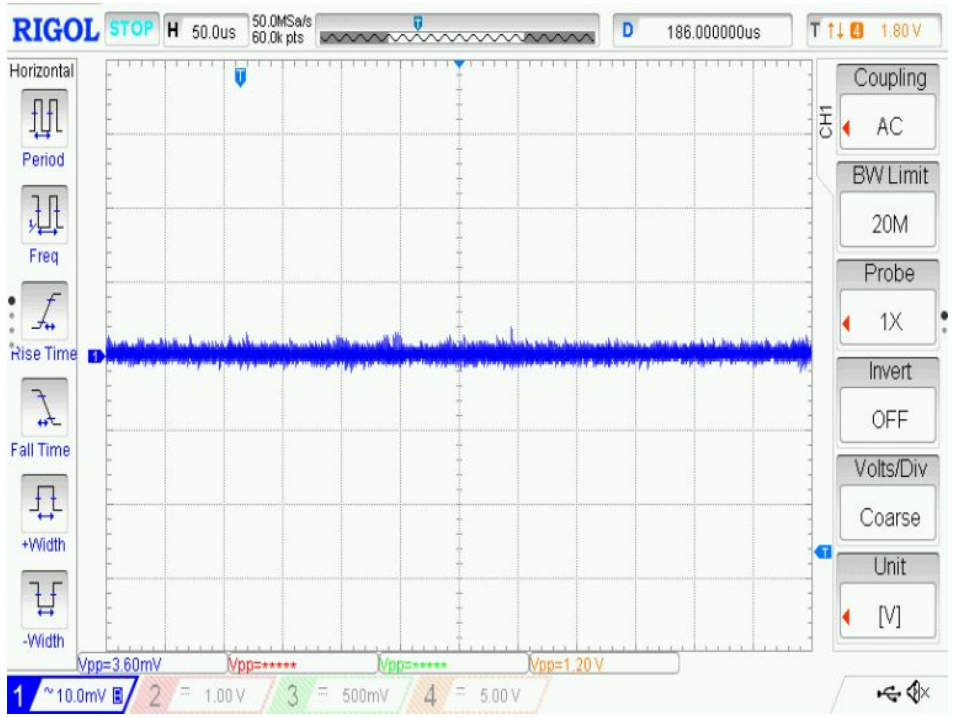
Vout = 1.8 V
Transient 0.1125 A – 0.15 A @ 2.5 A/µs
V_{PP} = 4.8 mV

Ripple



No Load
V_{PP} = 2.8 mV

Vout = 1.8 V



0.15 A Load
V_{PP} = 3.6 mV

VCCO
3.3 V / 0.03 A

- CLDO

End of
Artix UltraScale+ (Minimum Rails) Cost-optimized Portfolio Mappings & Test Data

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Thank You

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