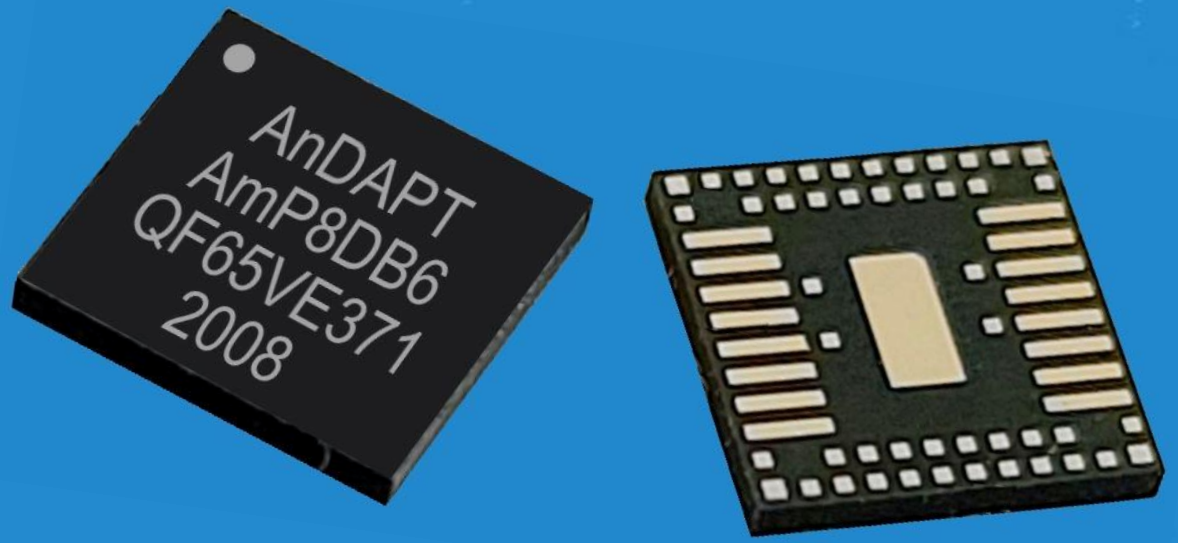


Artix UltraScale+ (High Power)

Mappings & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Artix 7 (High Power) + family of devices SKUs
- Artix 7 (High Power)+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Artix 7 (High Power)+ family FPGAs

*Xilinx document: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Artix 7 (High Power) Device SKUs Covered

Supported SKUs
XC7A100T
XC7A200T

Artix 7 (High Power)

Can be combined if voltage same

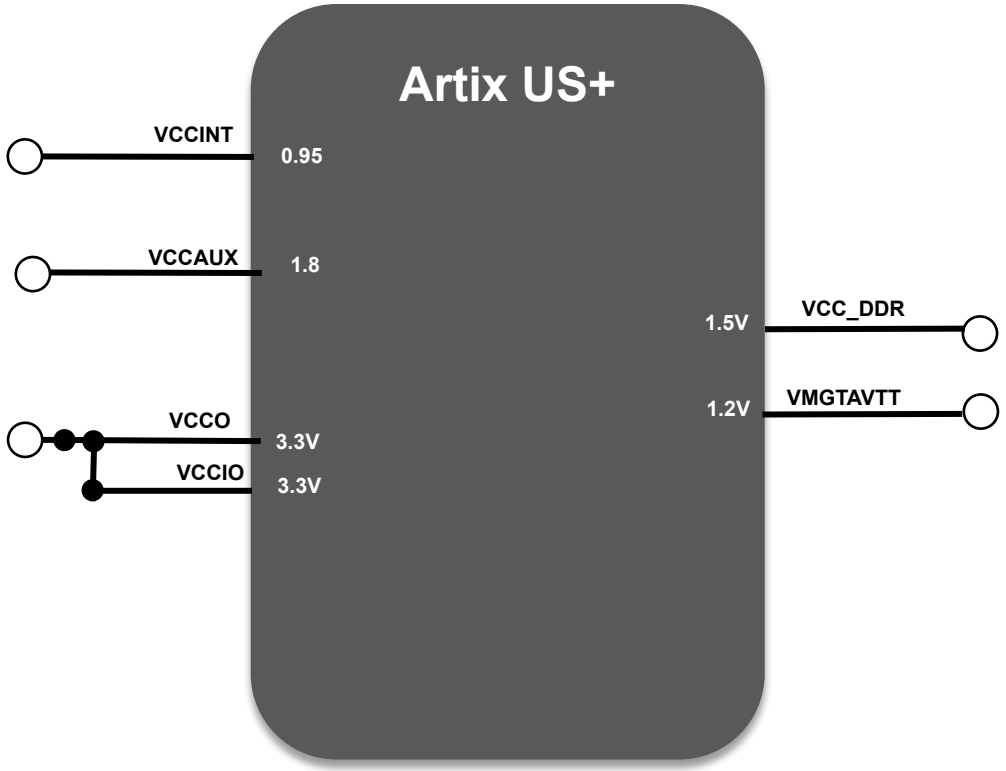


Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree: Artix 7 (High Power)

PVIN = 12V/18V

#	Rail	Seq	Vin (V)	Vout (V)	Iout (A)
1	VCCINT	1	12	0.95/1	8.7
2	VCC_DDR	4	1.8	1.35 to 1.5	2
3	VMGTAVTT	4	12	1.2	1
4	VCCAUX	2	12	1.8	0.35
5	VCC_IO	4	12	3.3	0.2
6	VCCO	3	12	3.3	0.05

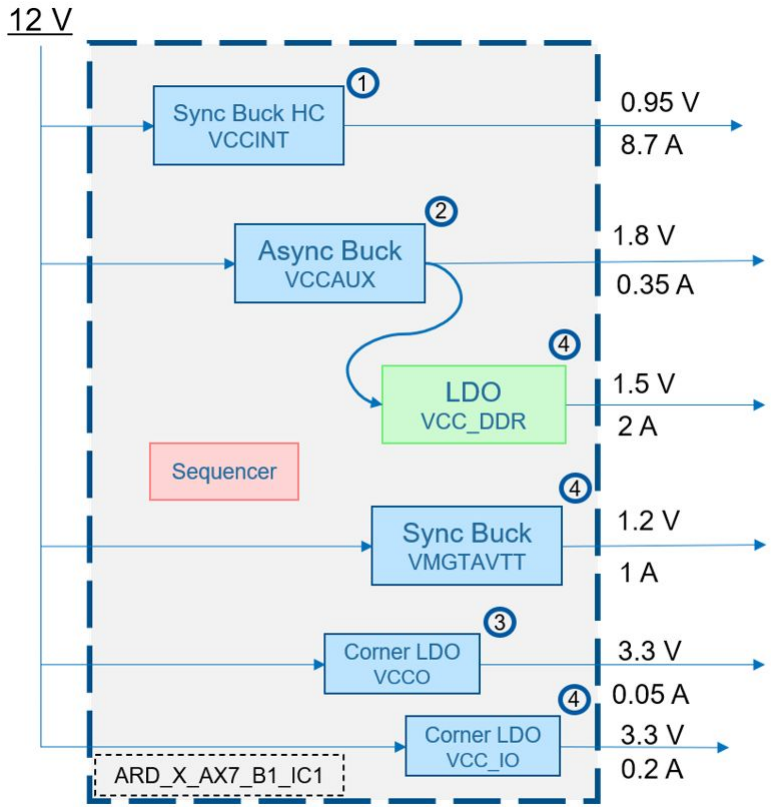
Power Tree Mapping: Artix 7 (High Power)

PVIN = 12V

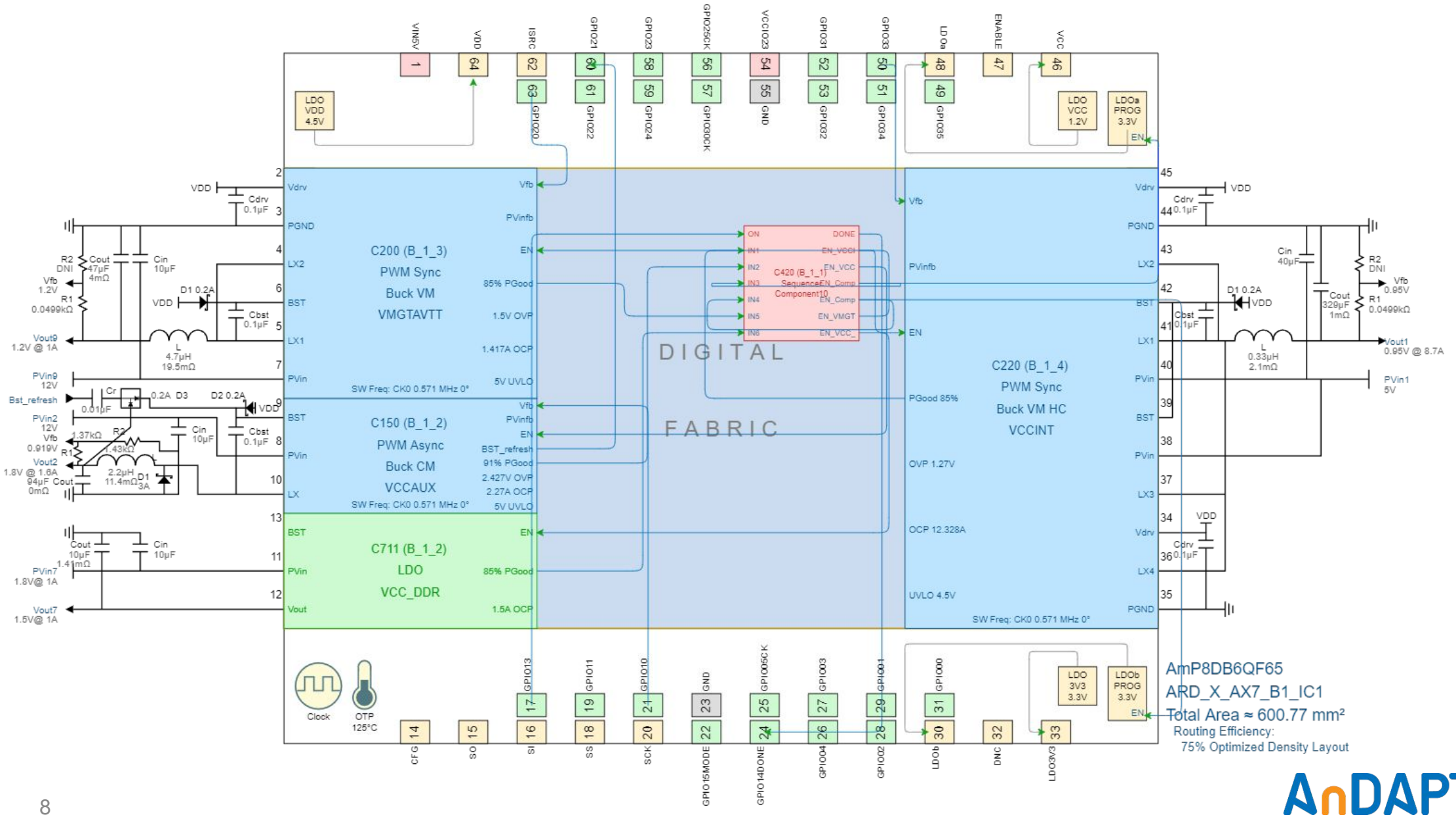
#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRAM, MGTAVCC	1	C220	Sync Buck HC	V_{IN}	12	0.95/1	8.7	ARD_X_AX7_B1_IC1
2	VCC_DDR	4	C710	SIM LDO	VCCAUX	1.8	1.35 to 1.5	<2	ARD_X_AX7_B1_IC1
3	VMGTAVTT	4	C200	Sync Buck	V_{IN}	12	1.2	≤1	ARD_X_AX7_B1_IC1
4	VCCAUX, VCCADC	2	C150	Async Buck	V_{IN}	12	1.8	<(0.35 + 2)	ARD_X_AX7_B1_IC1
6	VCC_IO	4	CLDO	Corner LDO	V_{IN}	12	1.8 or 3.3	<0.2	ARD_X_AX7_B1_IC1
7	VCCO[0.1…]	3	CLDO	Corner LDO	V_{IN}	12	1.2 to 3.3	≤0.05	ARD_X_AX7_B1_IC1

Estimated total area estimated = 600.77 mm^2

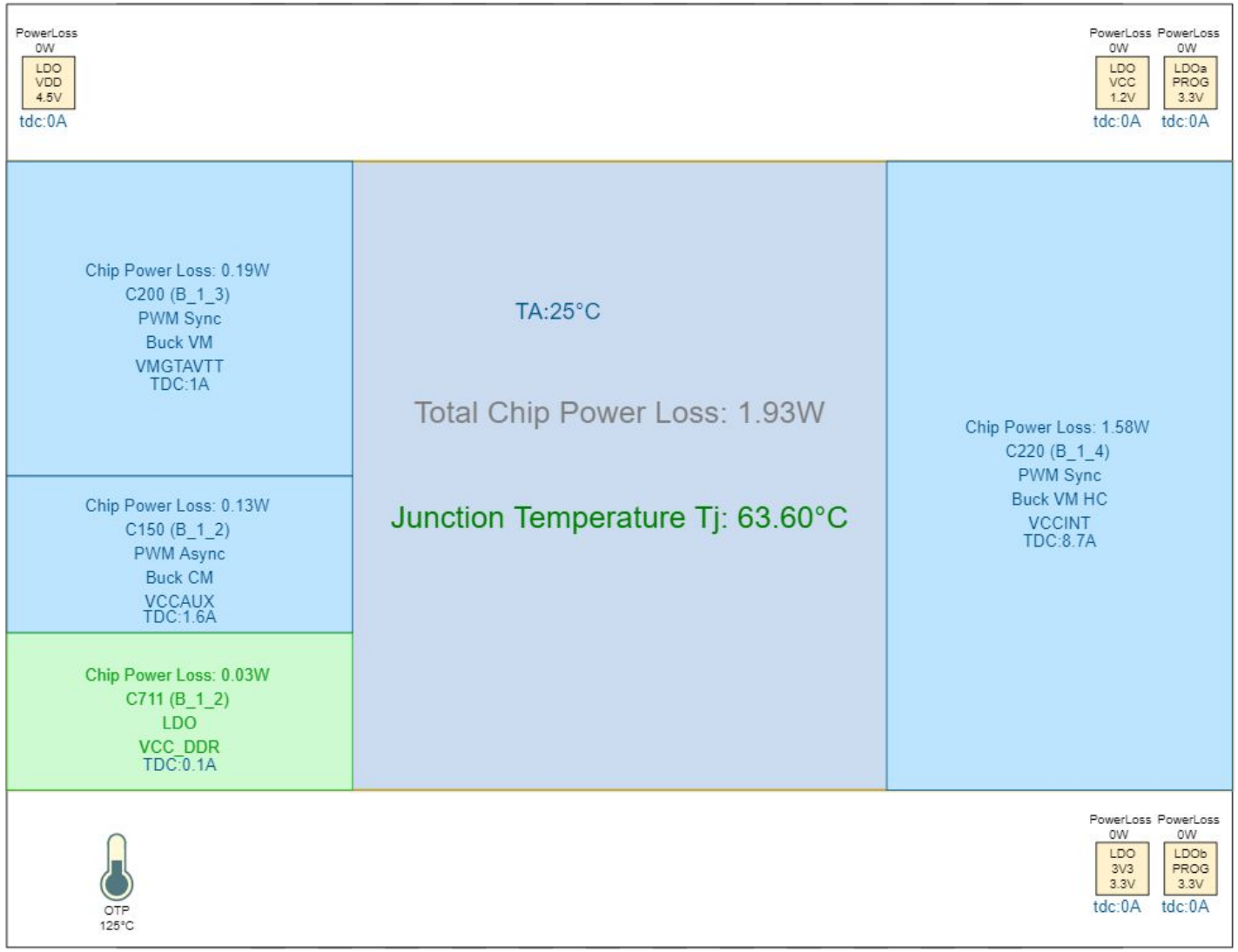
Power Tree Mapping



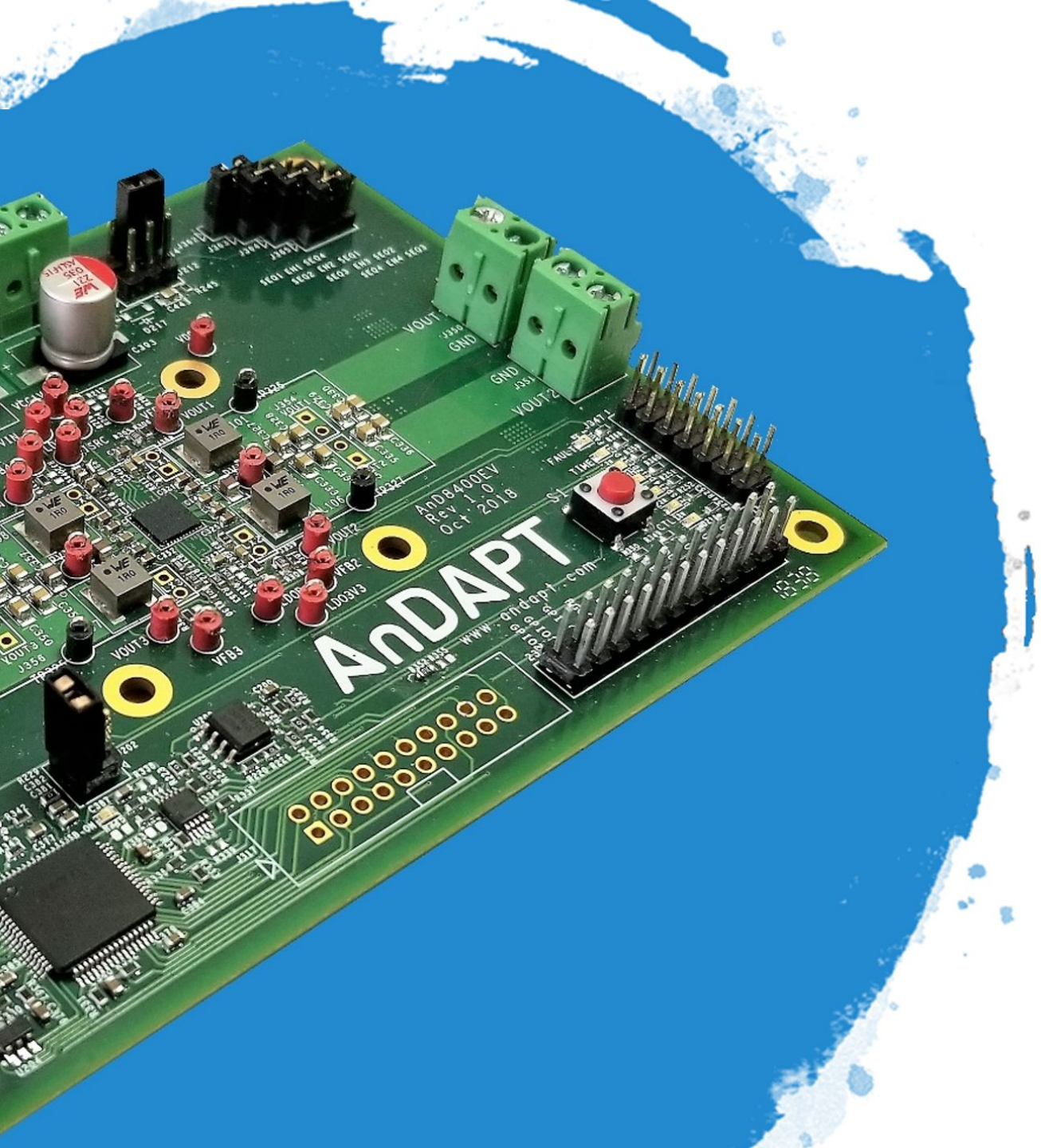
Mapping (WebAmP View)



Mapping (Thermal View)



AmP8DB6QF65
ARD_X_AX7_B1_IC1
Total Area ≈ 600.77 mm²
Routing Efficiency:
75% Optimized Density Layout



Test Data

Artix 7 (High Power)

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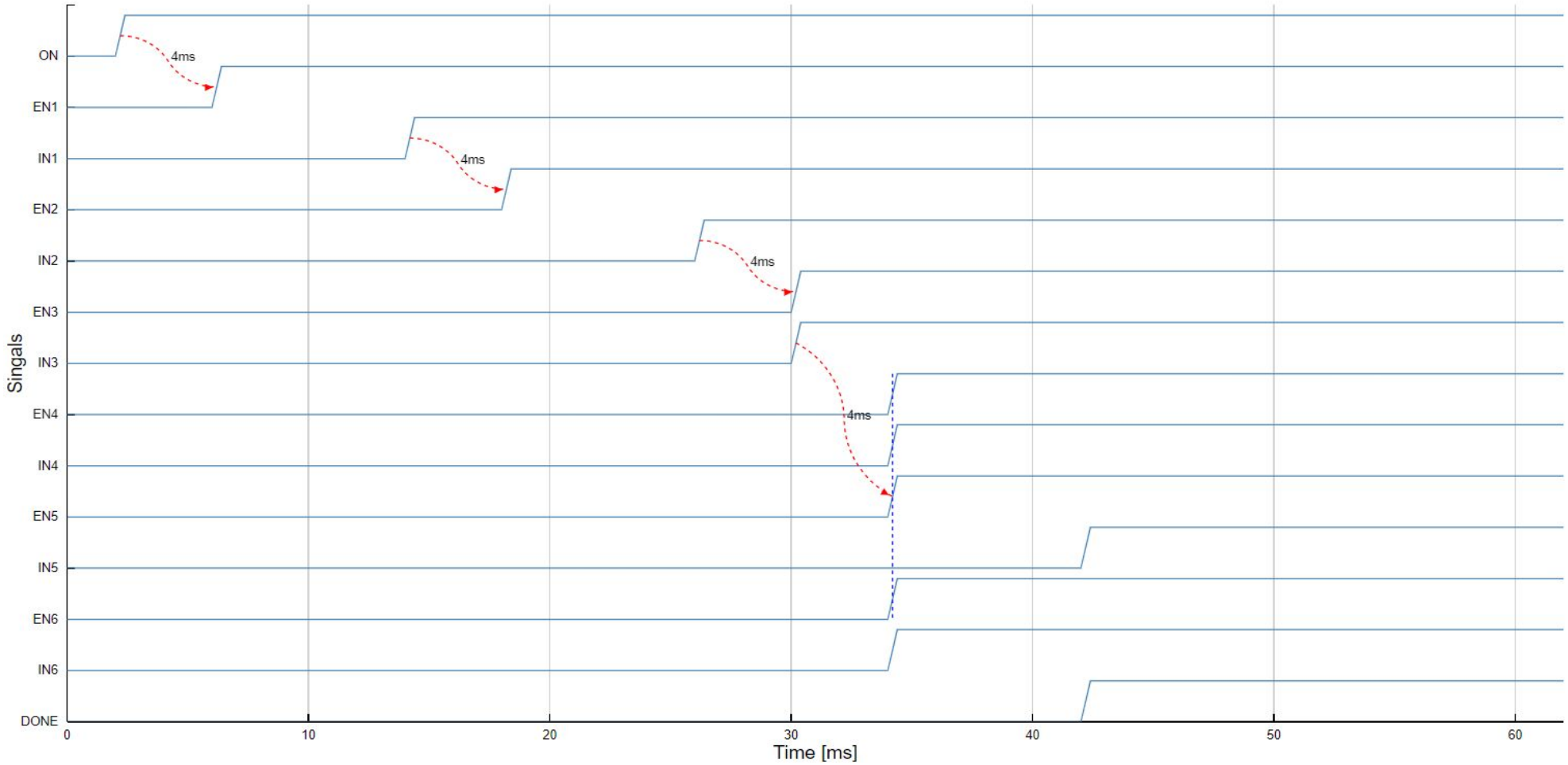
Integrated Sequencer Graphic (Turn ON)



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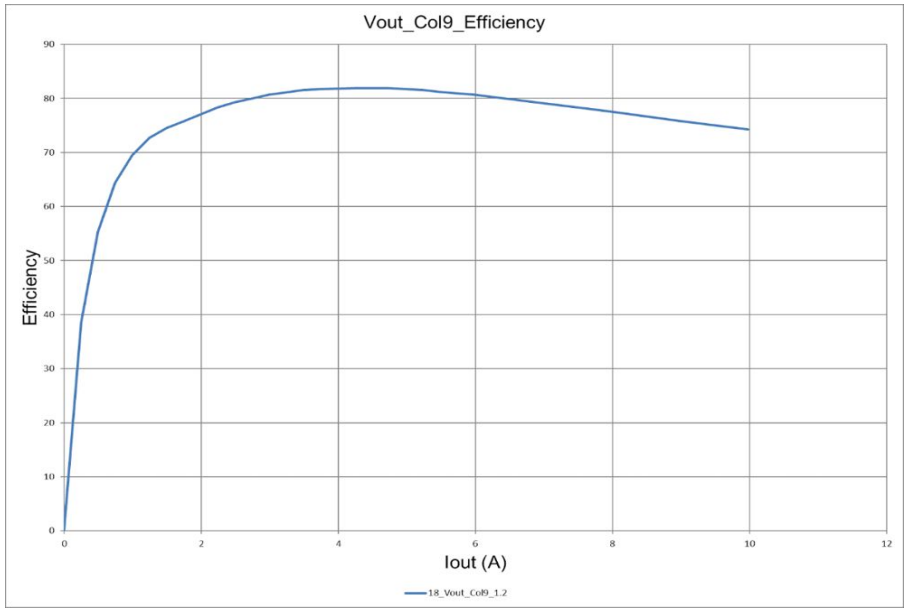
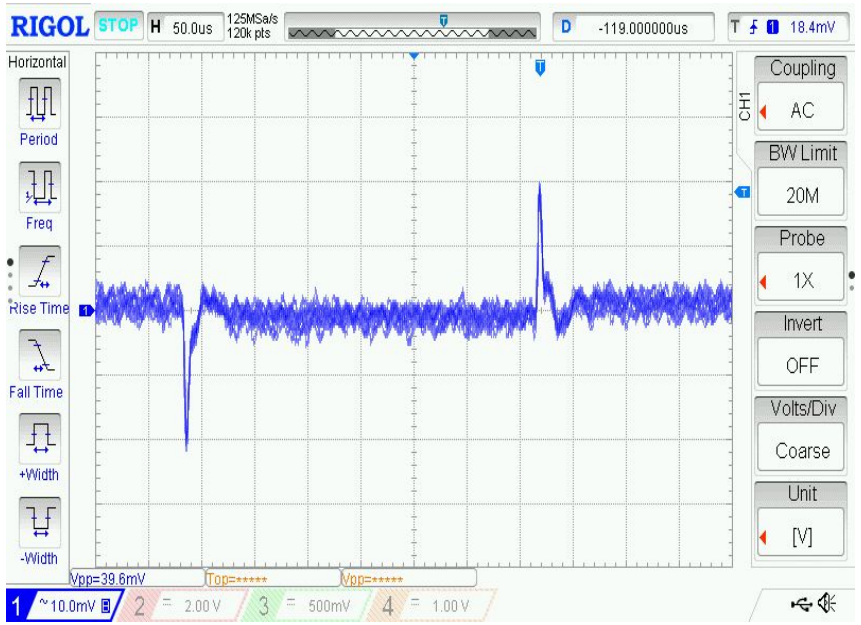
VCCINT
1 V / 8.7 A

- C220 Sync Buck HC
- Fsw = 571 kHz
- L = 0.33 µH, P/N Wurth 744308033
- C = 329 uF

Efficiency & Transient





Vout = 1 V
Transient 7.5 A – 10 A @ 10 A/µs
V_{PP} = 39.6 mV
Fsw = 571 kHz
Lout = 0.33 µH, Cout = 329 µF

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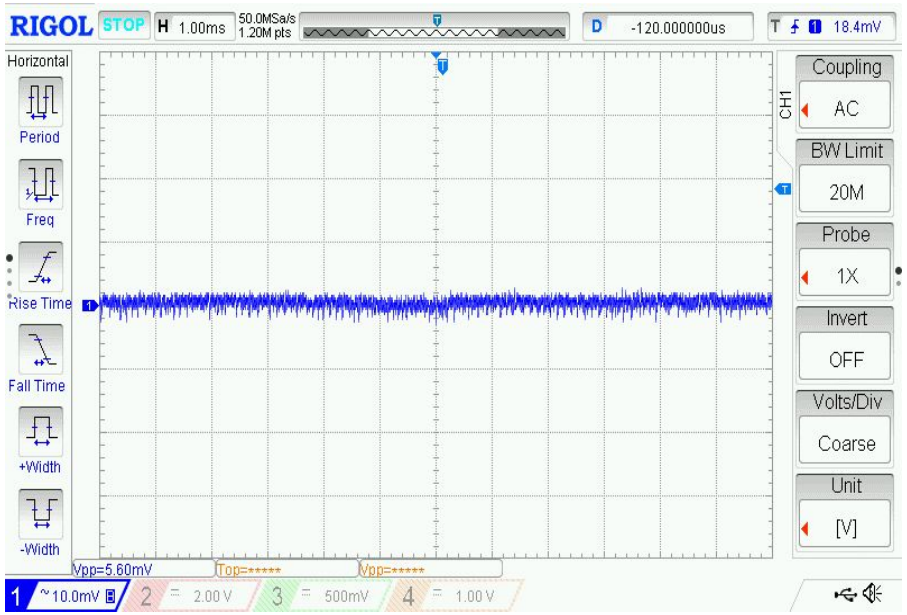
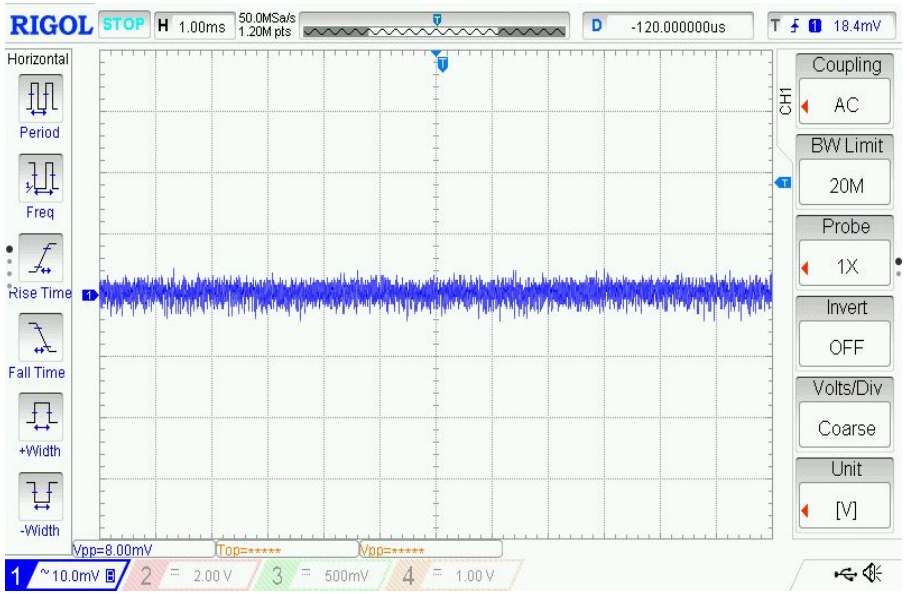
Ripple



No Load
V_{PP} = 5.60 mV

Vout = 1 V

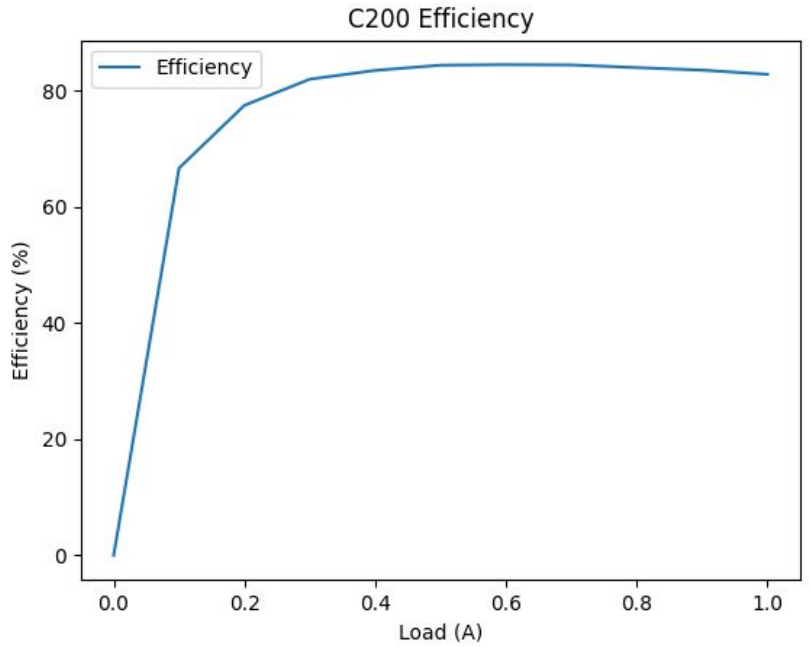


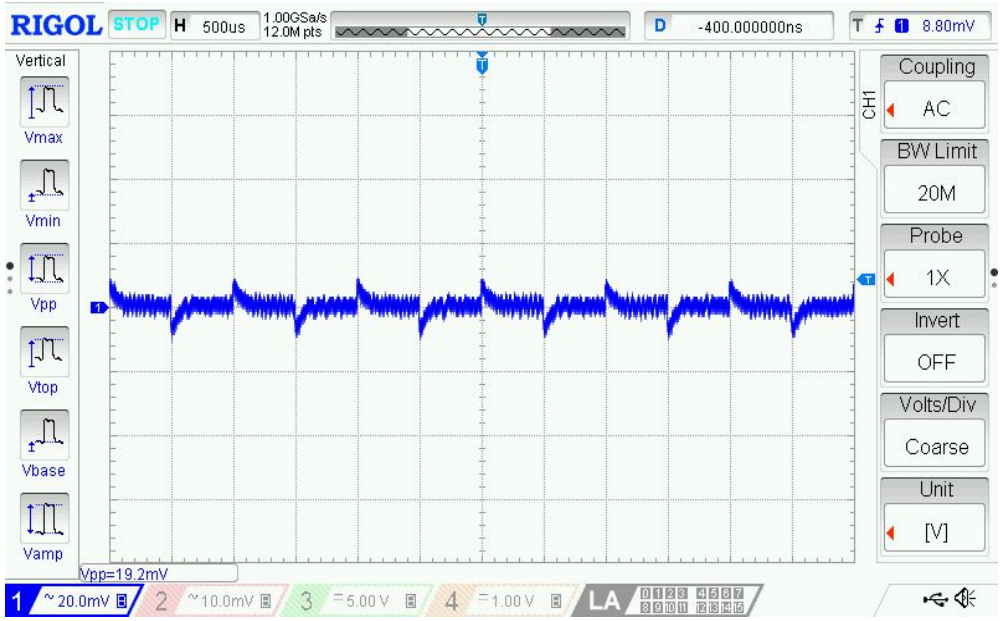
10A Load
V_{PP} = 8 mV

VMGTAVTT
1.2 V / 1A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

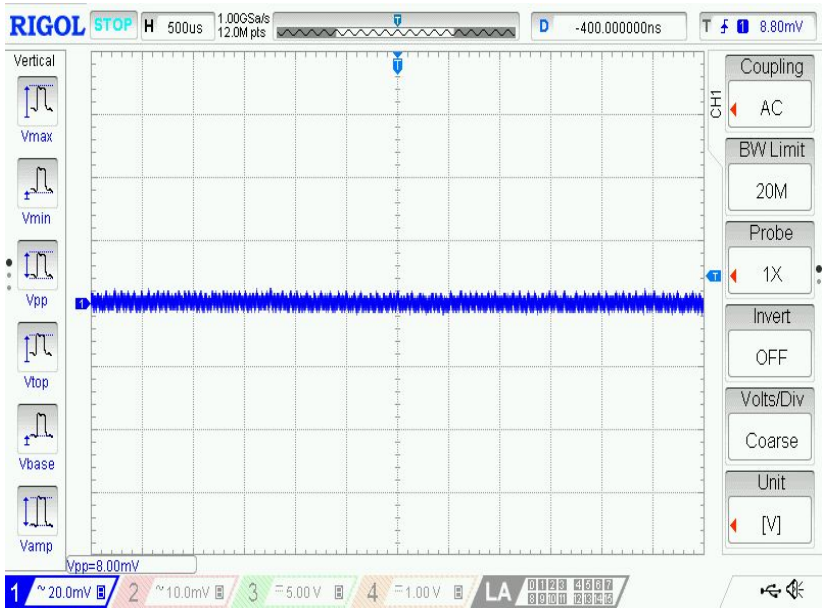
Efficiency & Transient





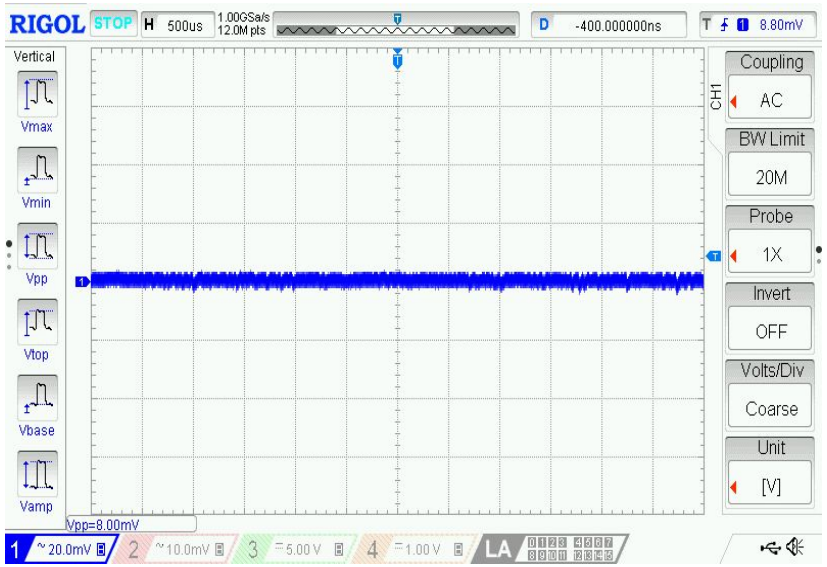
Vout = 1.2 V
Transient 0.75 A – 1 A @ 2.5 A/µs
V_{PP} = 19.2 mV
Fsw = 571 kHz
Lout = 4.7 µH, Cout = 1 x 47 µF

Ripple



No Load
V_{PP} = 8 mV

Vout = 1.2 V

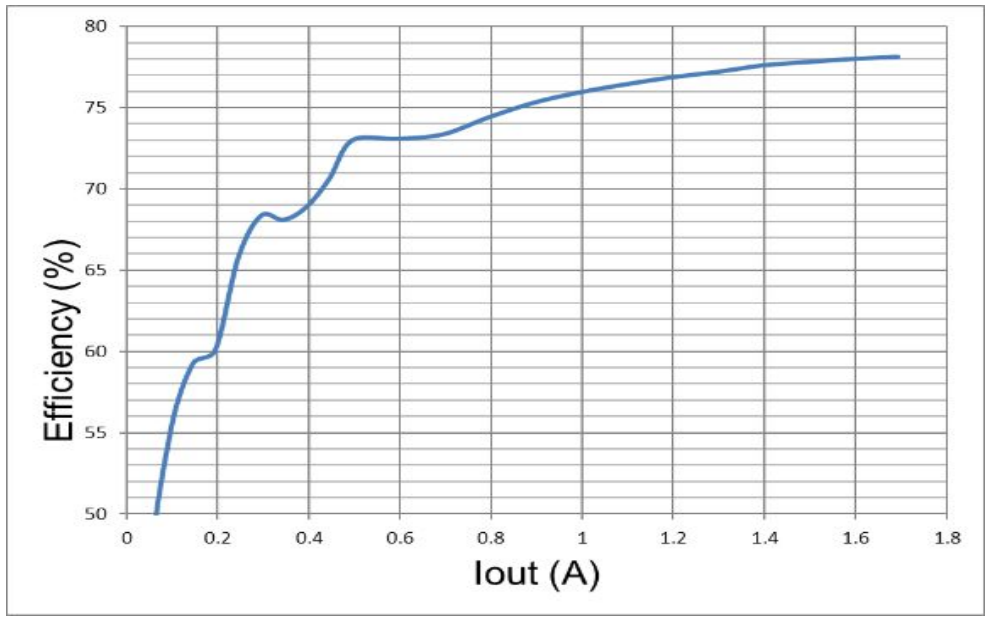


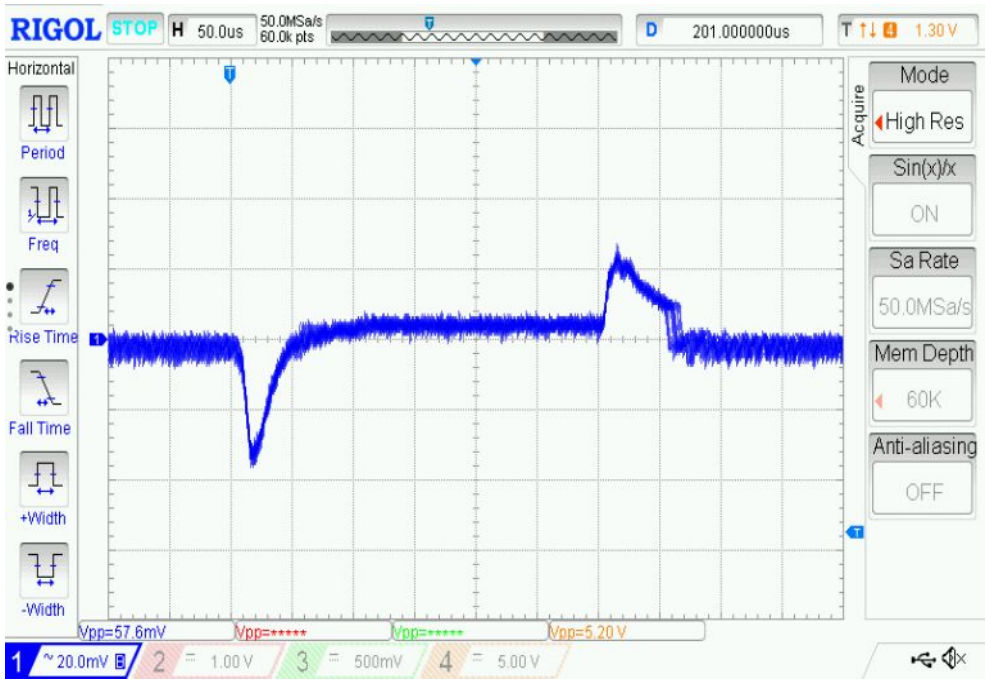
1.6 A Load
V_{PP} = 8 mV

VCCAUX
1.8 V / 0.35 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient





Vout = 1.8 V
Transient 0.16A – 1.6 A @10 A/µs
V_{PP} = 57.6 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

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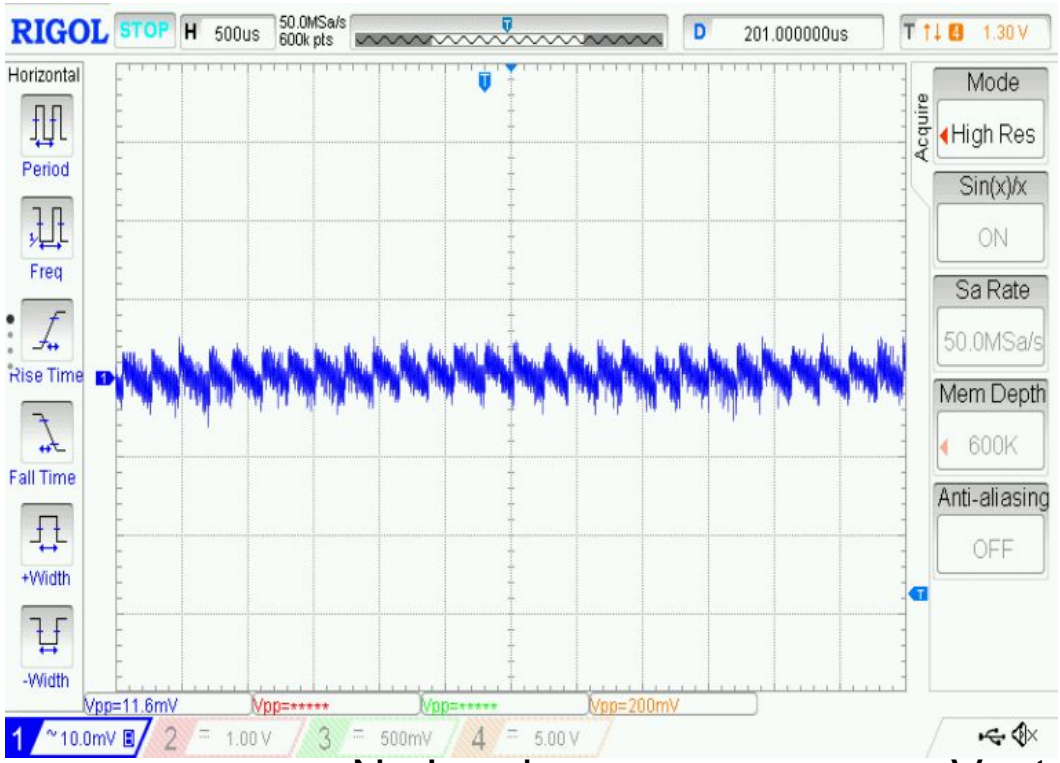
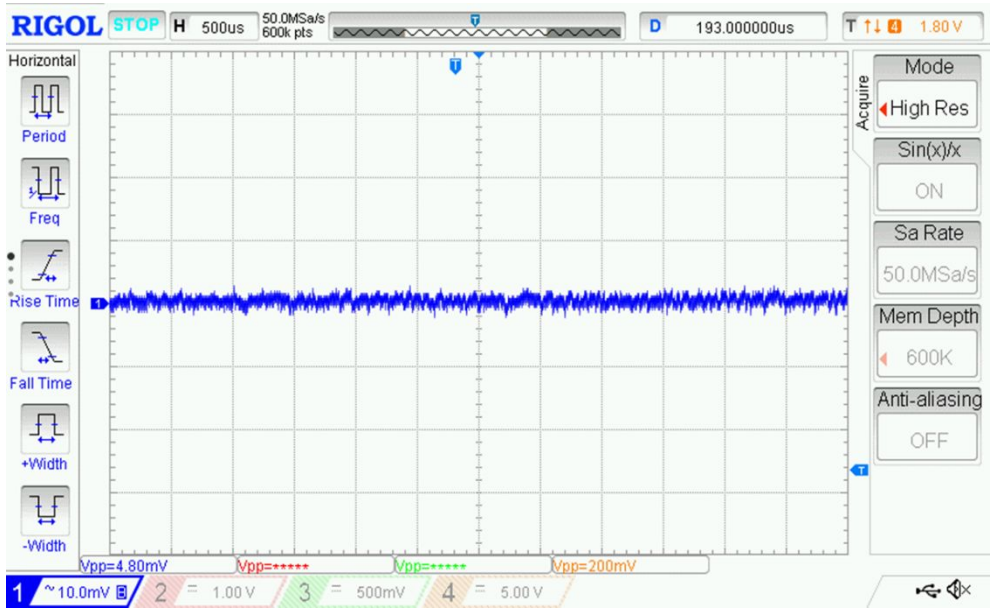
Ripple



No Load
V_{PP} = 11.6 mV

Vout = 1.8 V



1.6A Load
V_{PP} = 4.8 mV

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VCC_IO
3.3 V / 0.2 A

- CLDO

VCCO
3.3 V / 0.05 A

- CCLDO

End of
Artix UltraScale+ (Minimum Rails) Cost-optimized Portfolio Mappings & Test Data

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Thank You

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