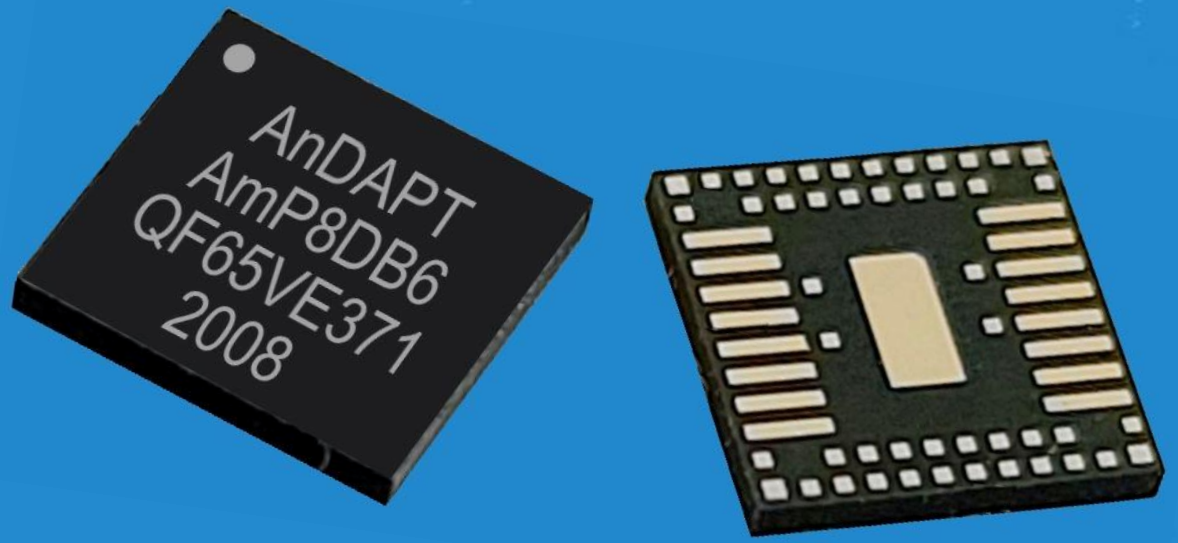

Kintex UltraScale+ (Min Rails)

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Kintex UltraScale+ (US+) family of devices SKU list (Minimum Rails) in cost-optimized portfolio
- Kintex US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Kintex US+ family FPGAs

Kintex UltraScale+ Device SKUs Covered- Minimum Rails

Supported SKUs
XCKU3P
XCKU5P
XCKU9P
XCKU11P
XCKU13P
XCKU15P

Kintex UltraScale+ (Min Rails)

Can be combined if voltage same

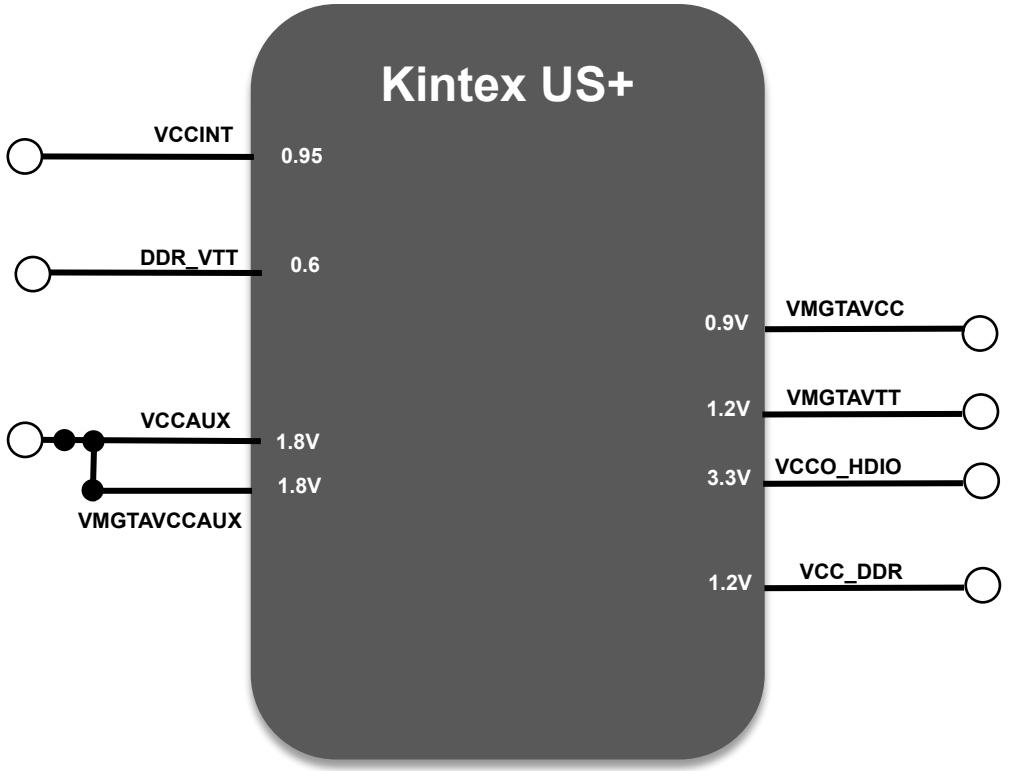

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree Mapping: Kintex UltraScale+ (Min Rails)

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCINT (VCCINT, VCCINT_IO, VCCBRAM)	1	C860	1-ph DrMOS Ctrl	PVIN	12	0.85	30	ARD_X_KUP_A_IC1
2	VCCAUX (VCCAUX, VCCAUX_IO, VCCADC)	2	C200	Sync Buck	PVIN	12	1.8	2	
3	VMGTAVTT	3	C200	Sync Buck	PVIN	12	1.2	4	
4	VMGTAVCCAUX	4	C200	Sync Buck	PVIN	12	1.8	0.1	
5	VMGTAVCC	5	C200	Sync Buck	PVIN	12	0.9	4	ARD_X_KUP_A_IC2
6	VCCO_HDIO (VCCO_HDIO, VCCO_HPIO)	6	C200	Sync Buck	PVIN	12	3.3	6	
7	VCC_DDR	7	C200	Sync Buck	PVIN	12	1.2	4	
8	DDR_VTT	8	C210	VTT Terminator	VCC_DDR	1.2	0.6	2	

Estimated total area = 782.64 mm^2 (IC1) + 557.63 mm^2 (IC2) = 1340.27

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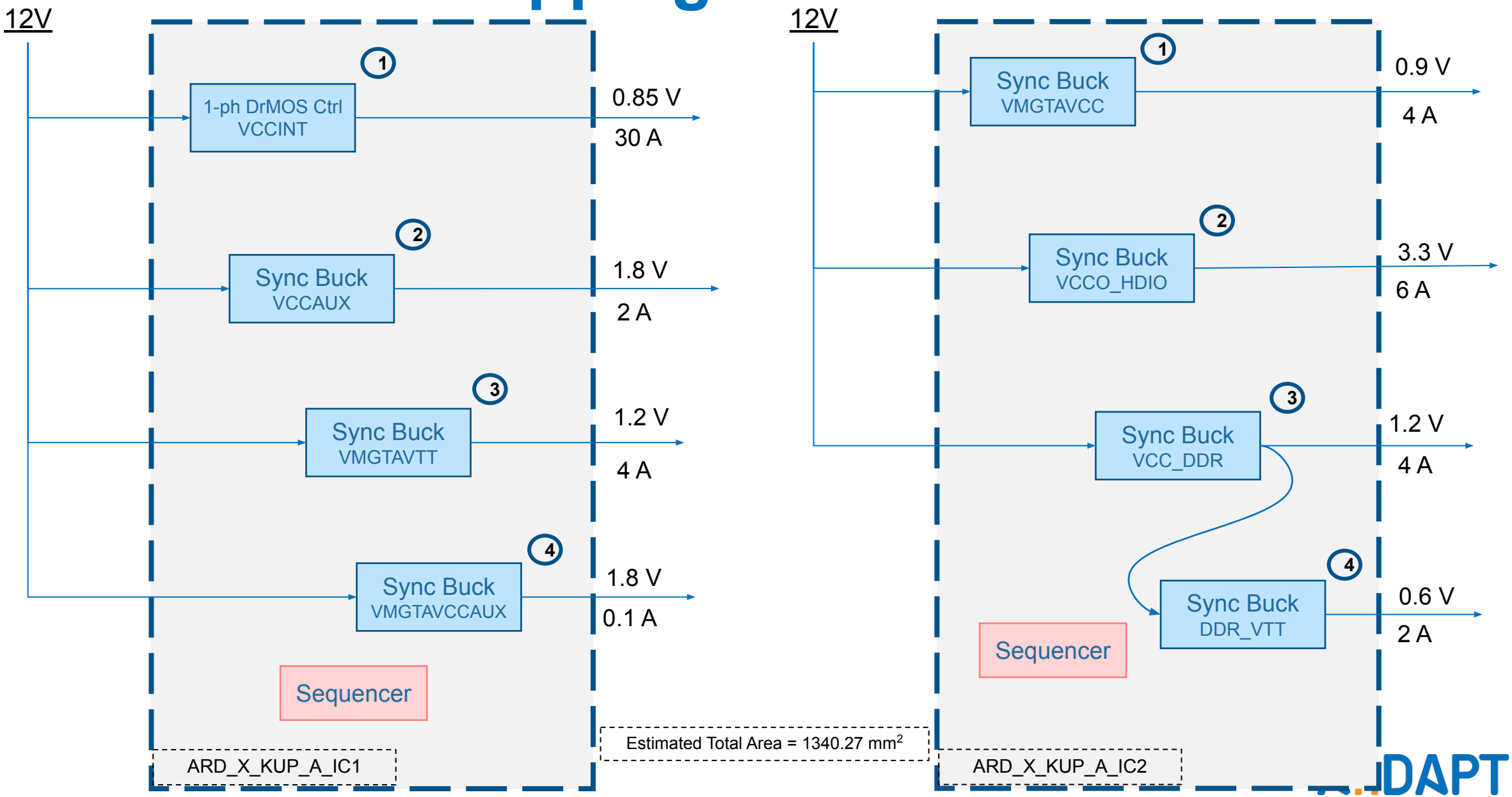
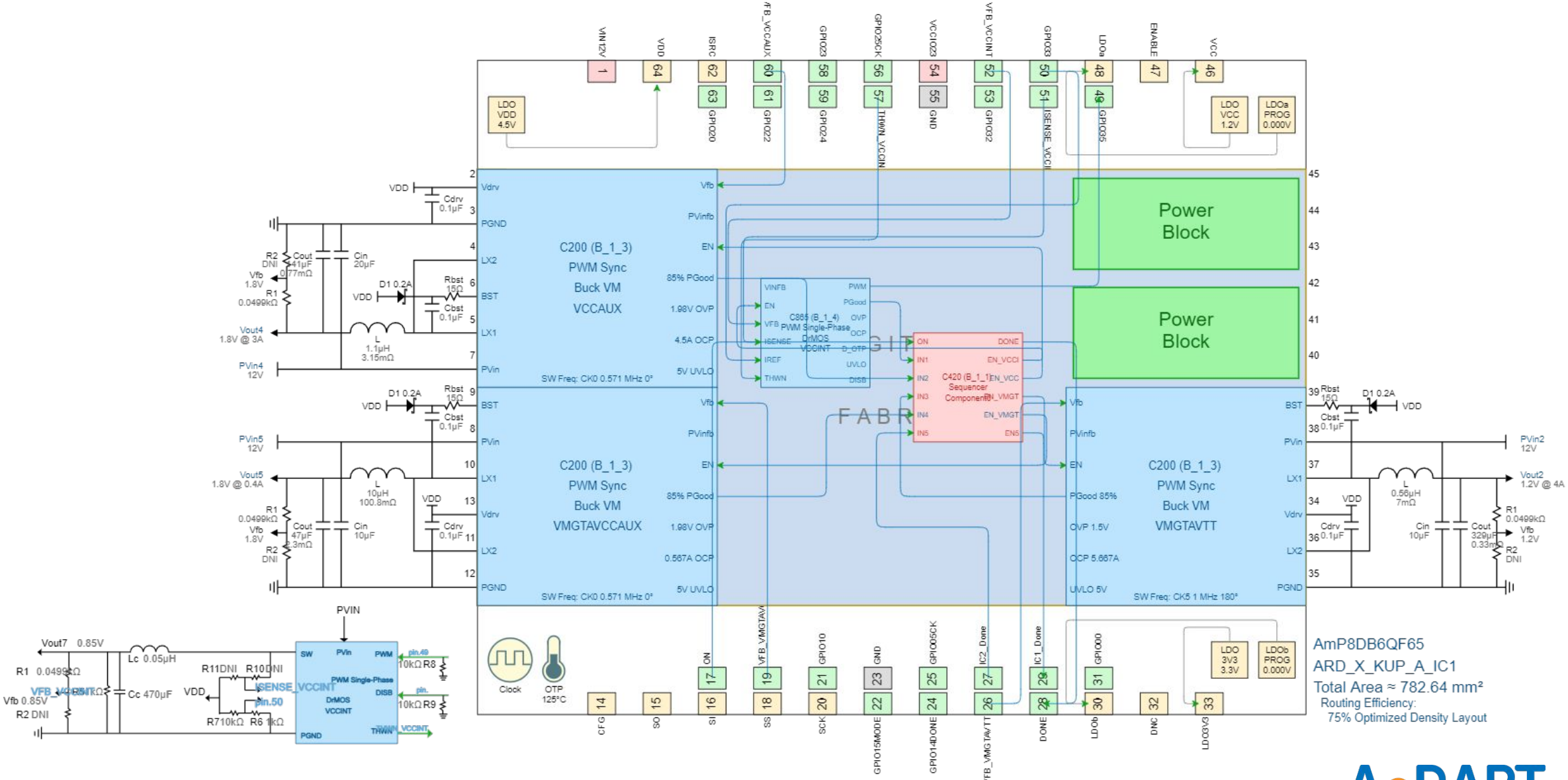
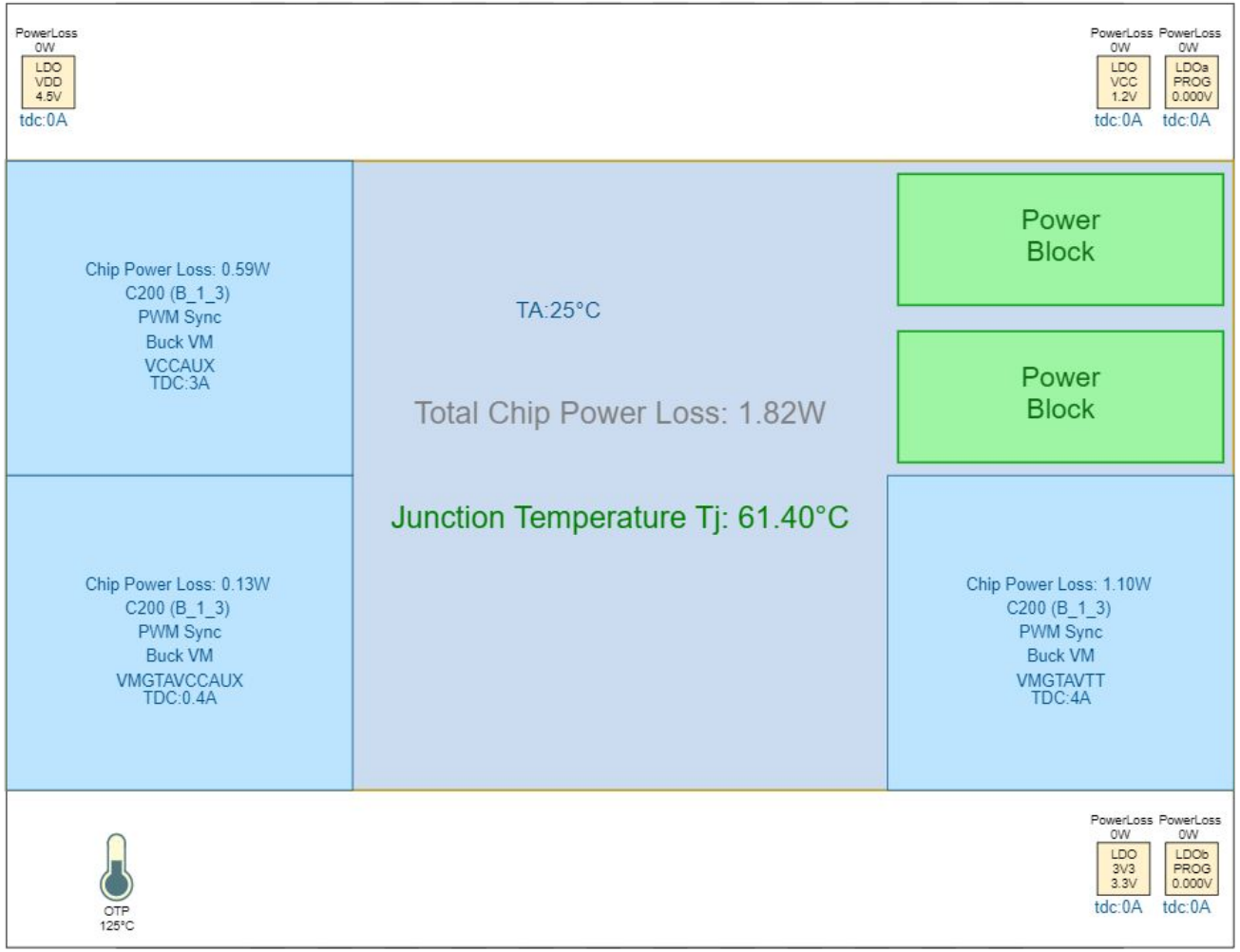
Power Tree Mapping



Mapping (WebAmP View) –IC1



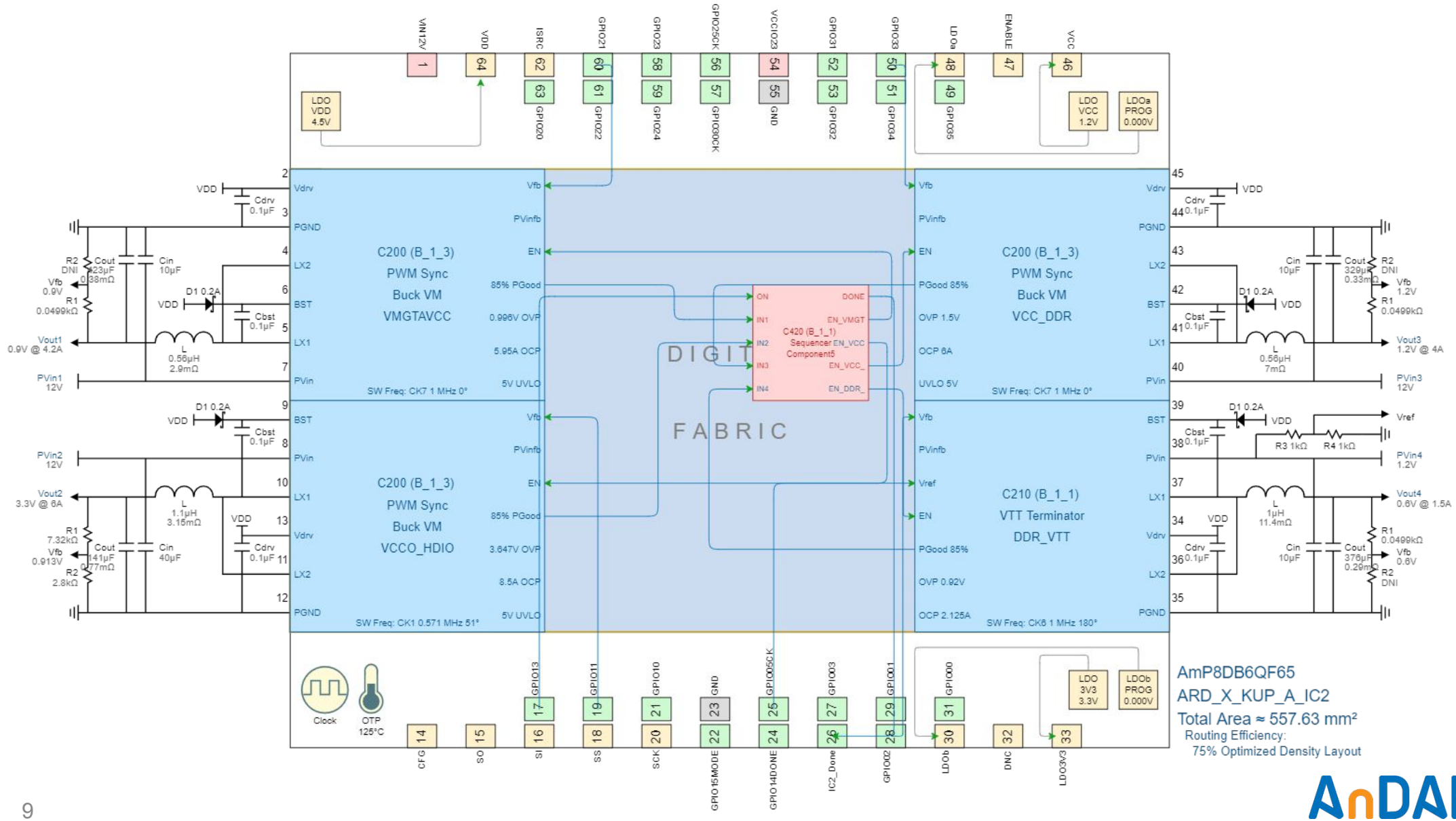
Mapping (Thermal View) –IC1



AmP8DB6QF65
ARD_X_KUP_A_IC1
Total Area ≈ 782.64 mm²
Routing Efficiency:
75% Optimized Density Layout

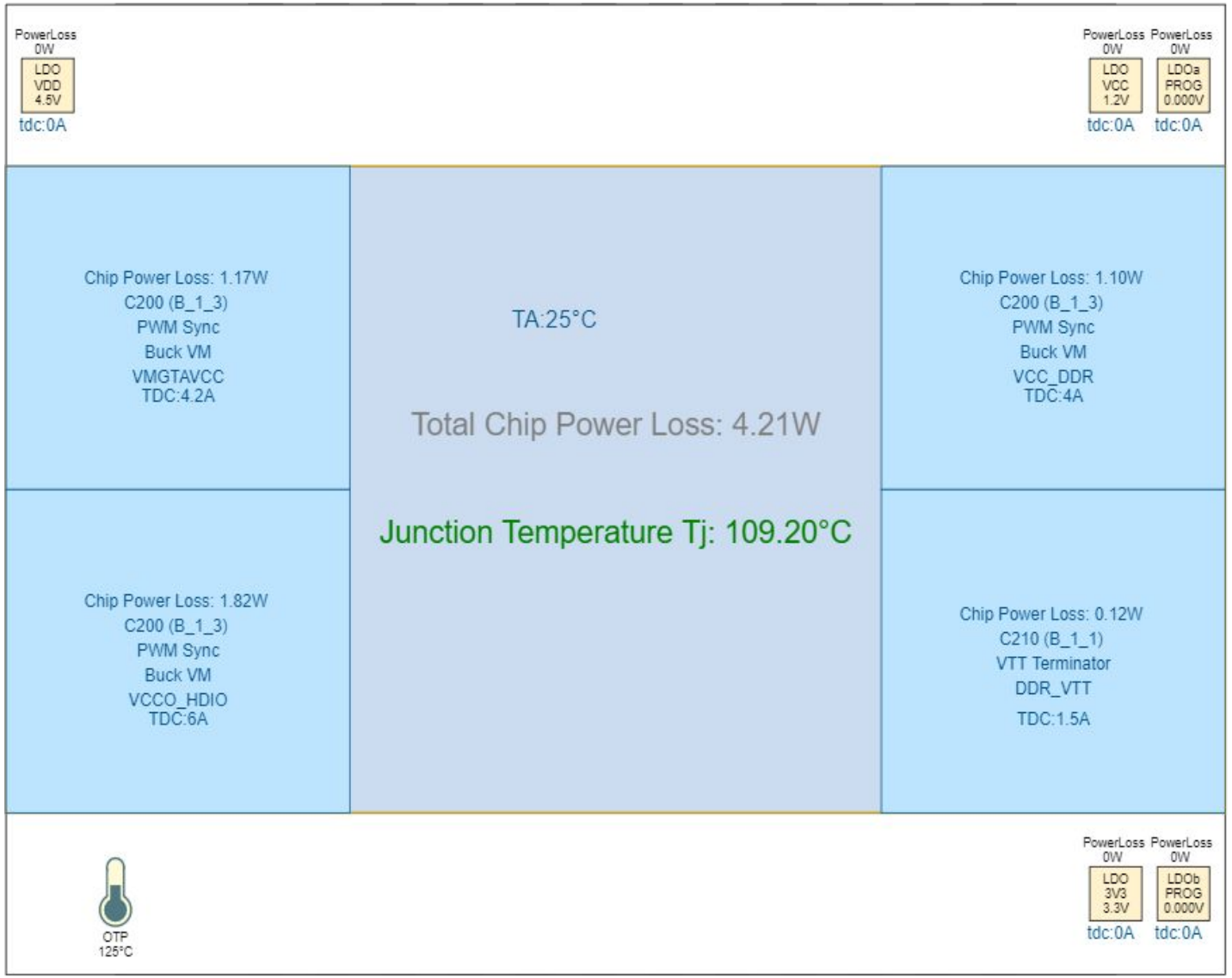
AnDAPT

Mapping (WebAmP View) –IC2

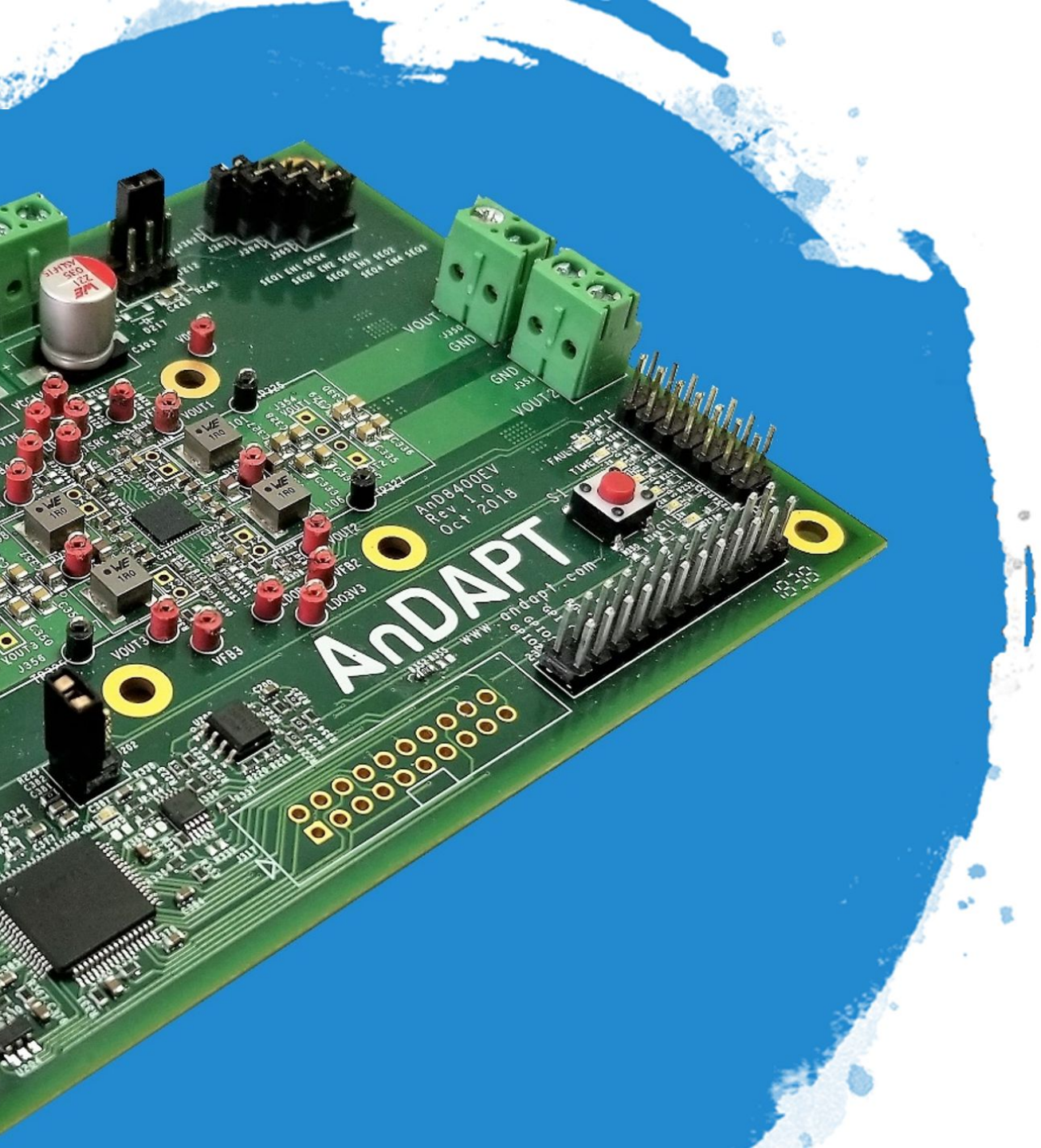


AmP8DB6QF65
ARD_X_KUP_A_IC2
Total Area ≈ 557.63 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (Thermal View) –IC2



AmP8DB6QF65
ARD_X_KUP_A_IC2
Total Area ≈ 557.63 mm²
Routing Efficiency:
75% Optimized Density Layout

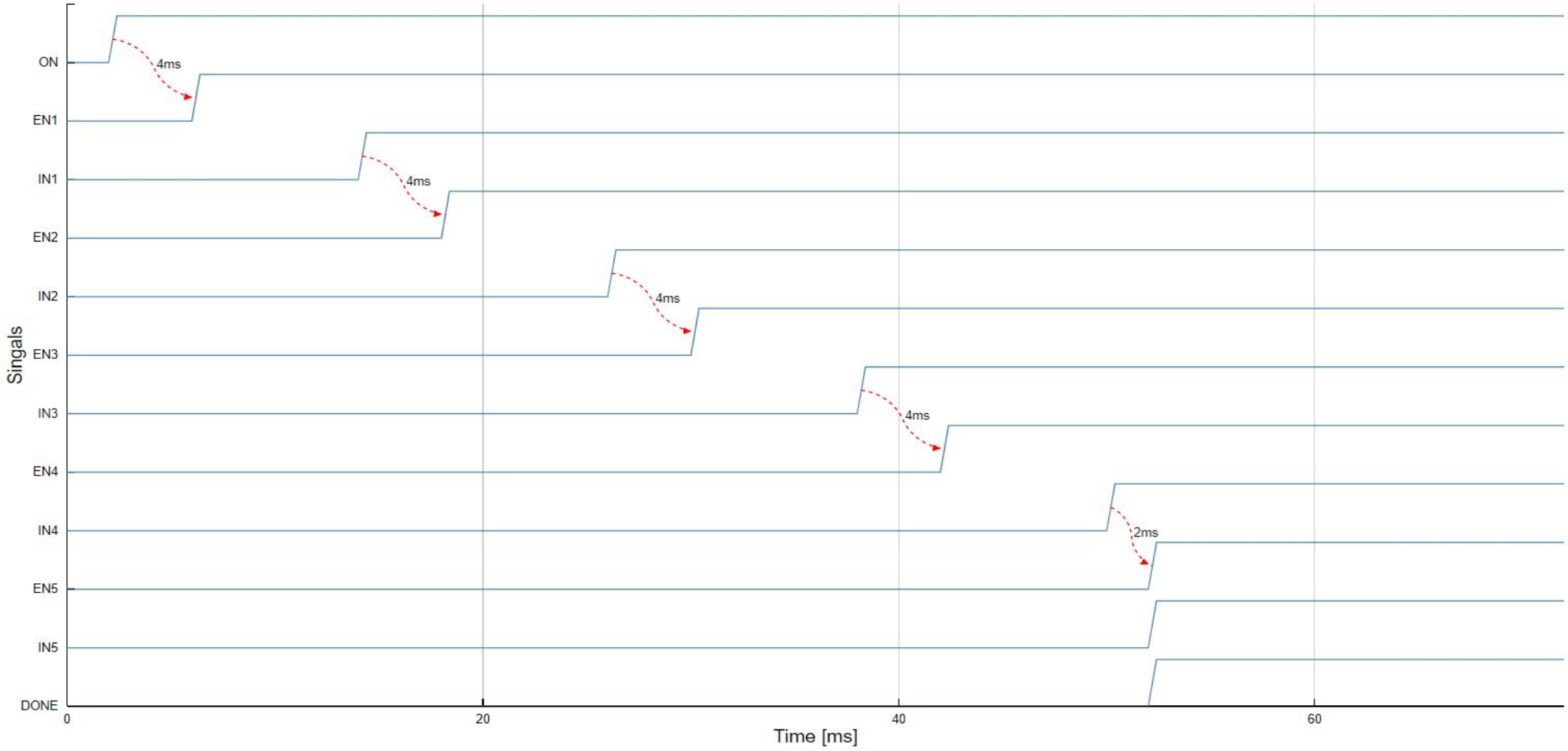


Test Data

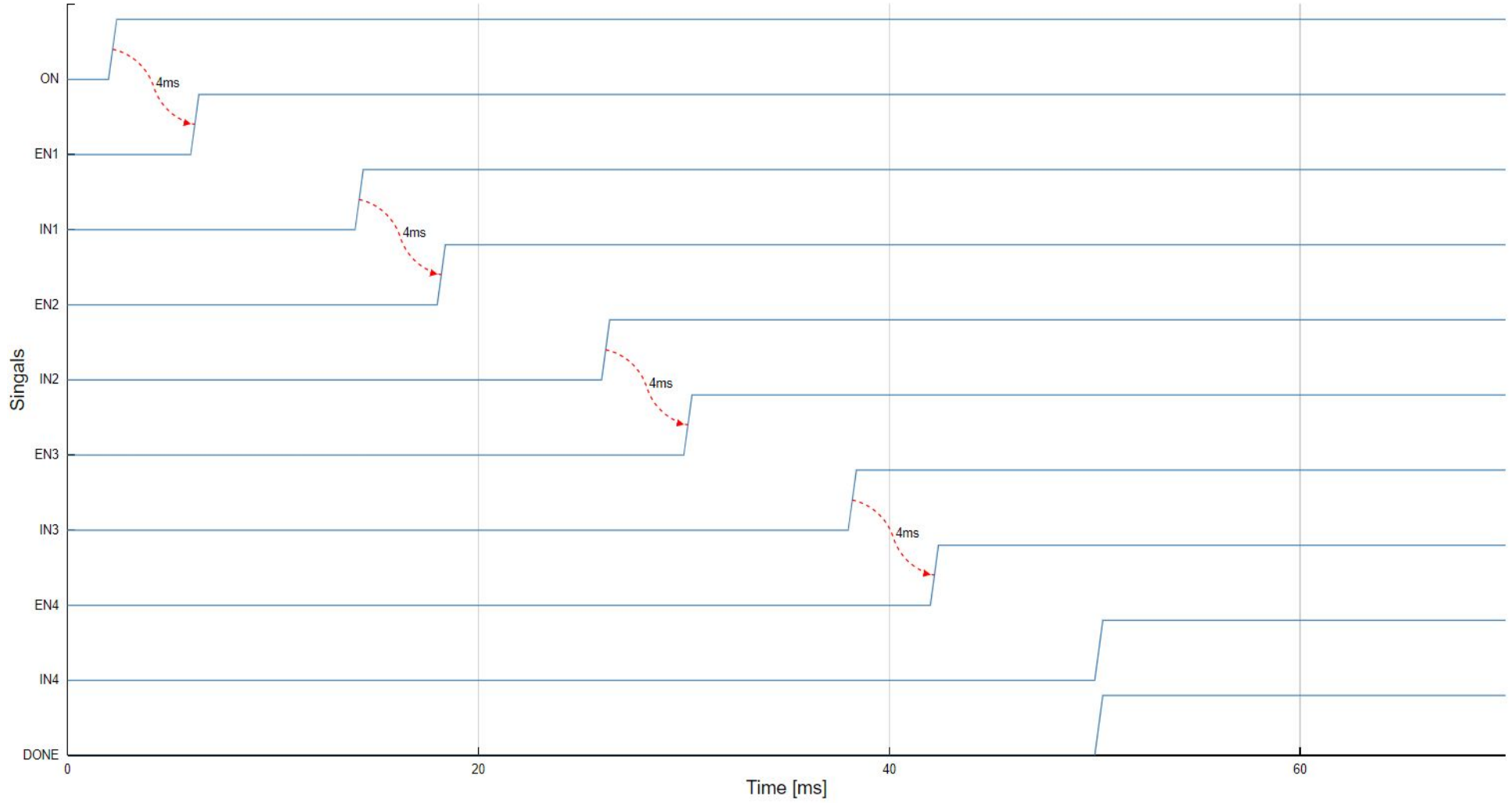
Kintex UltraScale+ (Minimum Rails)

AnDAPT

Integrated Sequencer Graphic ARD_X_KXU_A_IC1 (Turn ON)



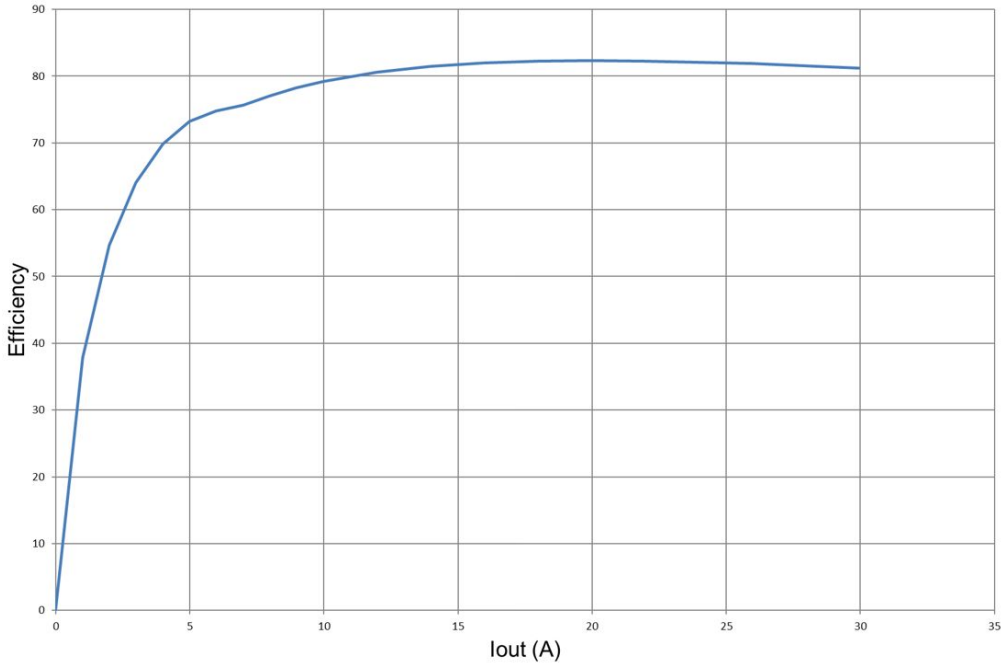
Integrated Sequencer Graphic ARD_X_KXU_A_IC2 (Turn ON)

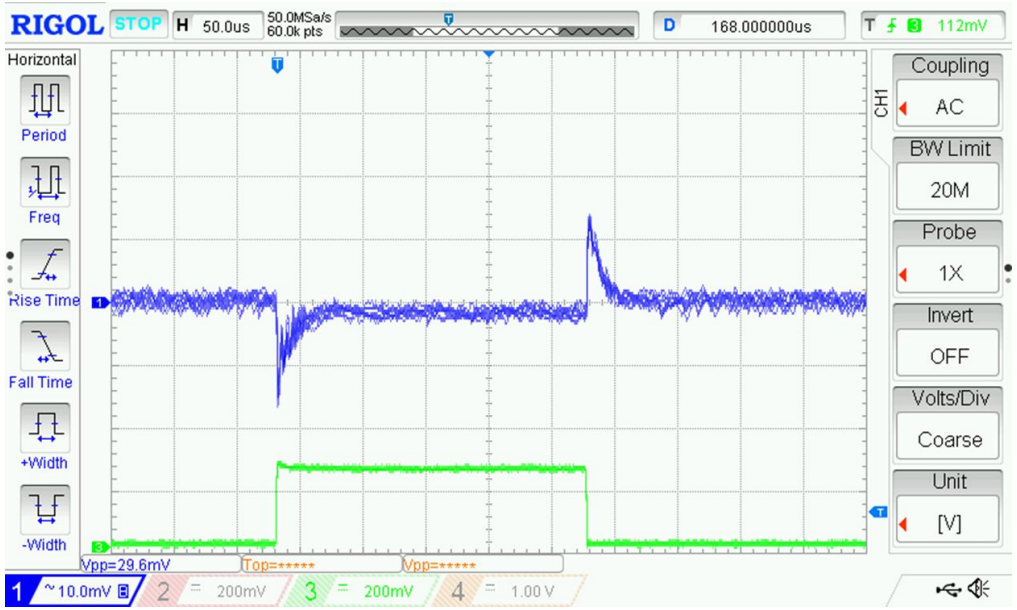


VCCINT, VCCINT_IO, VCCBRAM 0.85 V / 30 A

- C865 DrMOS Ctrl
- Fsw = 1 MHz
- L = 0.05 µH, P/N Wurth 994-SLC7530S-500MLC
- C = 10x47 uF + 2x220 uF

Efficiency & Transient





Vout = 0.85 V
Transient 22.5A – 30A @ 100 A/µs
V_{PP} = 29.6 mV
Fsw = 1 MHz
Lout = 0.05 µH, Cout = 10x47 µF + 2x220 uF

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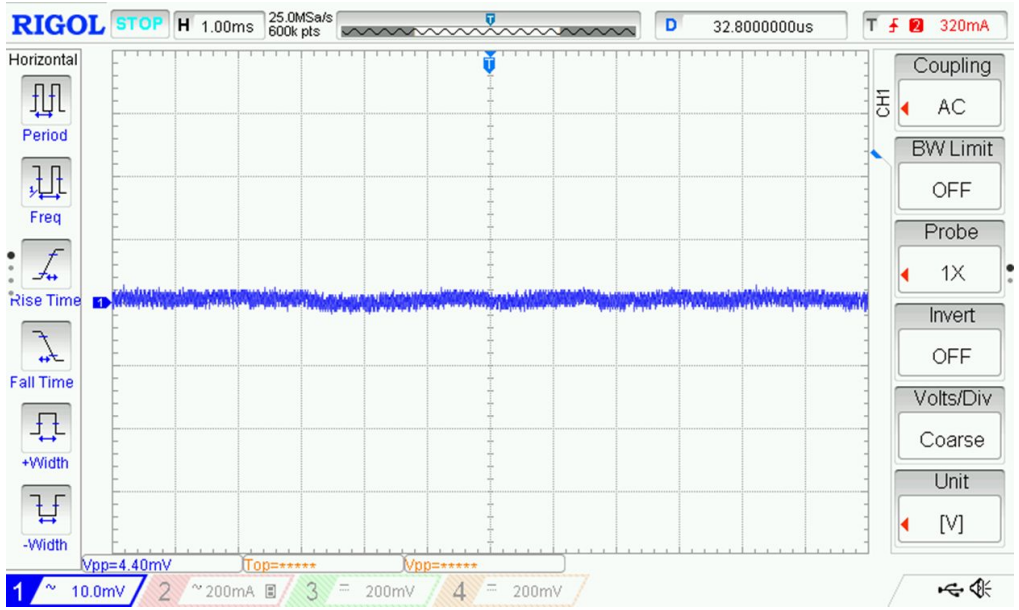
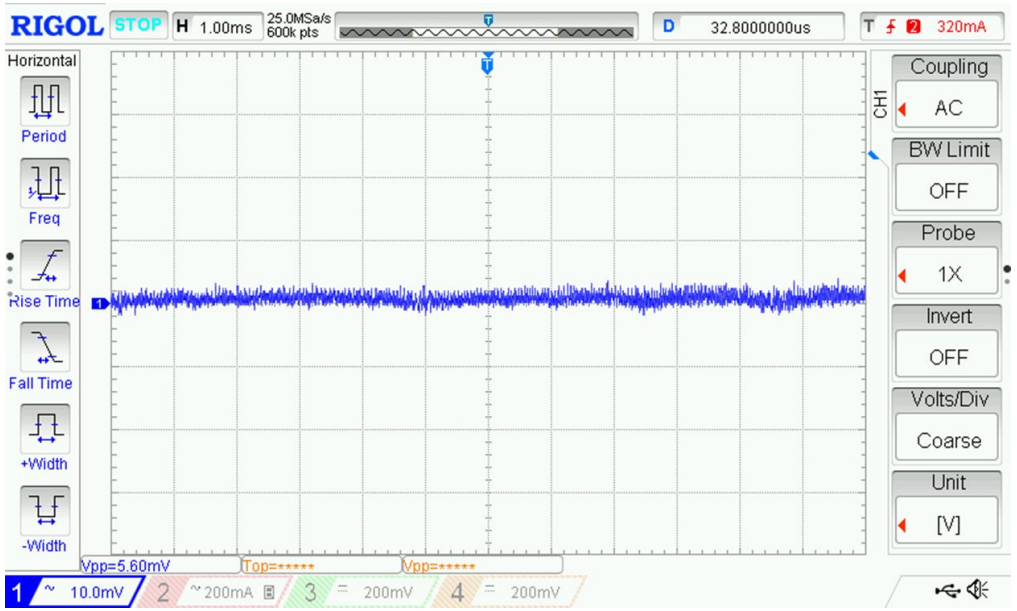
Ripple



No Load
V_{PP} = 4.4 mV

Vout = 0.85 V



30 A Load
V_{PP} = 5.6 mV

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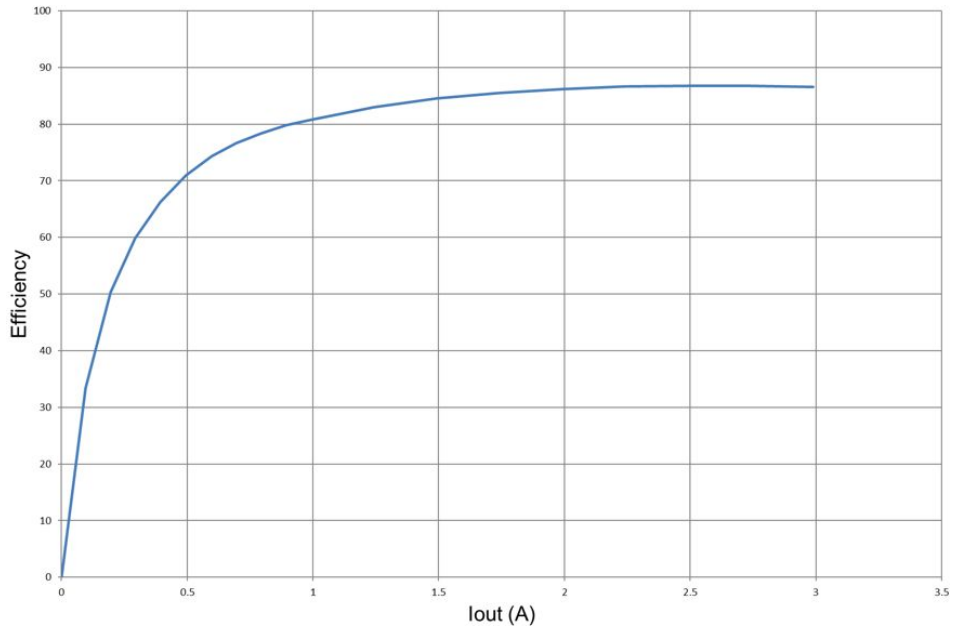
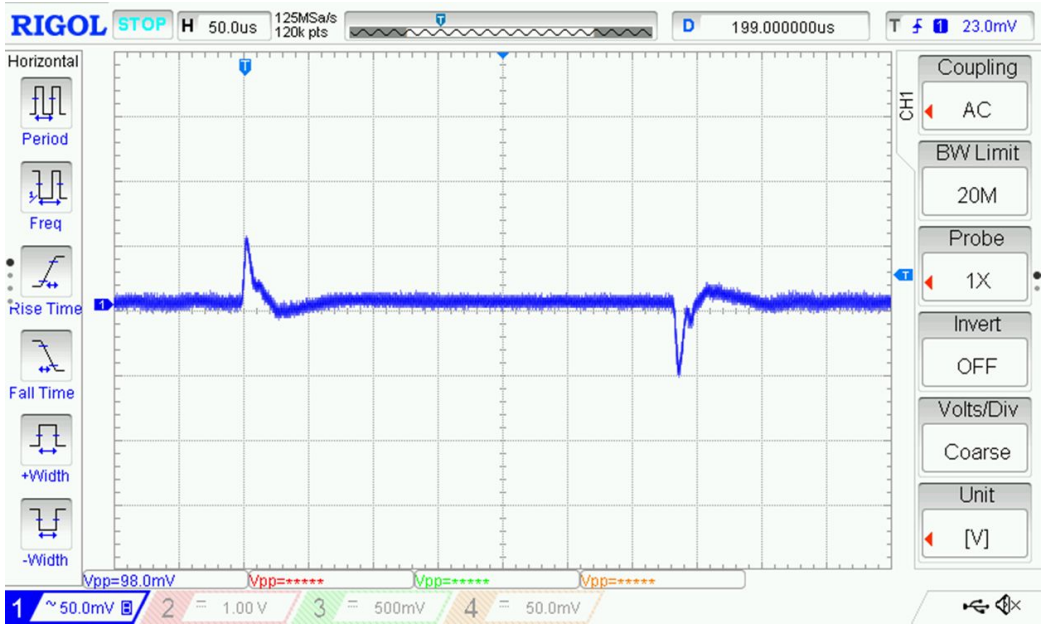
VCCAUX, VCCAUX_IO, VCCADC 1.8 V / 2 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

Efficiency & Transient

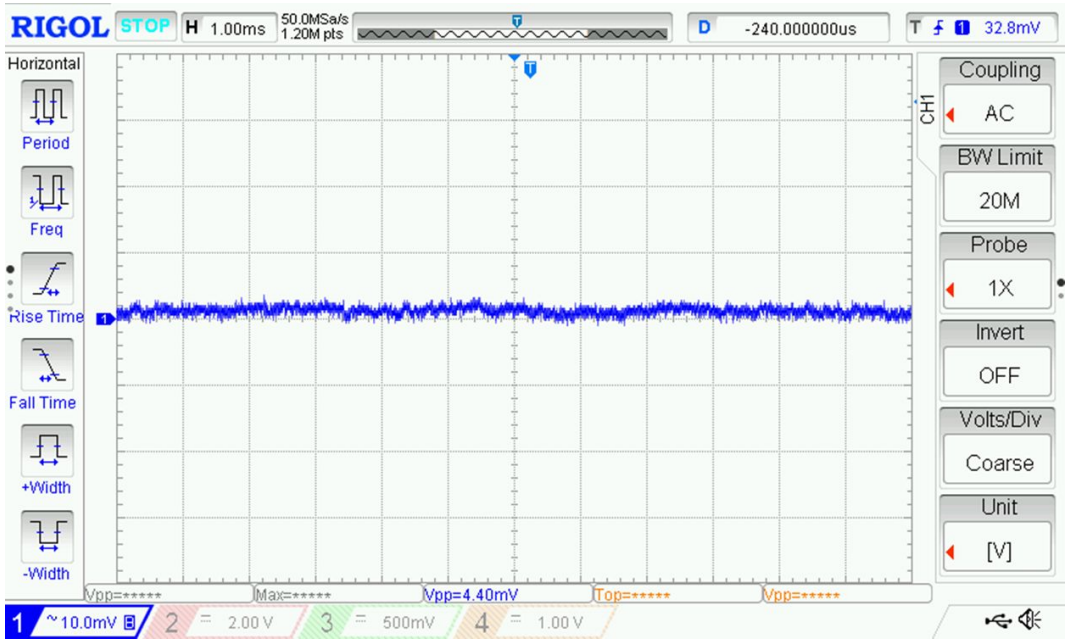




Vout = 1.8 V
Transient 0.3 A – 3A @ 10 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

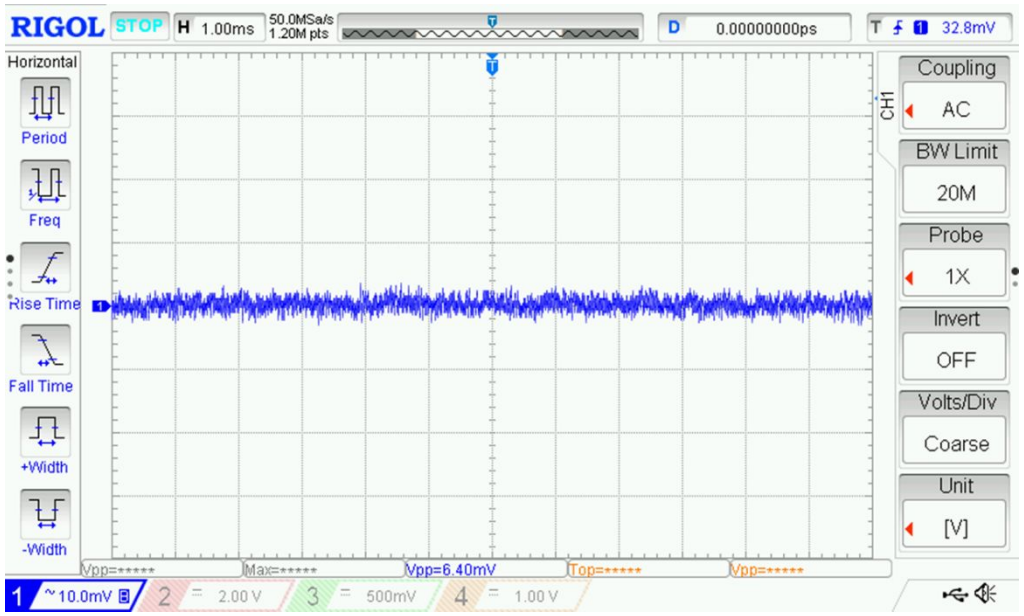
AnDAPT

Ripple



No Load
V_{PP} = 4.4 mV

Vout = 1.8 V

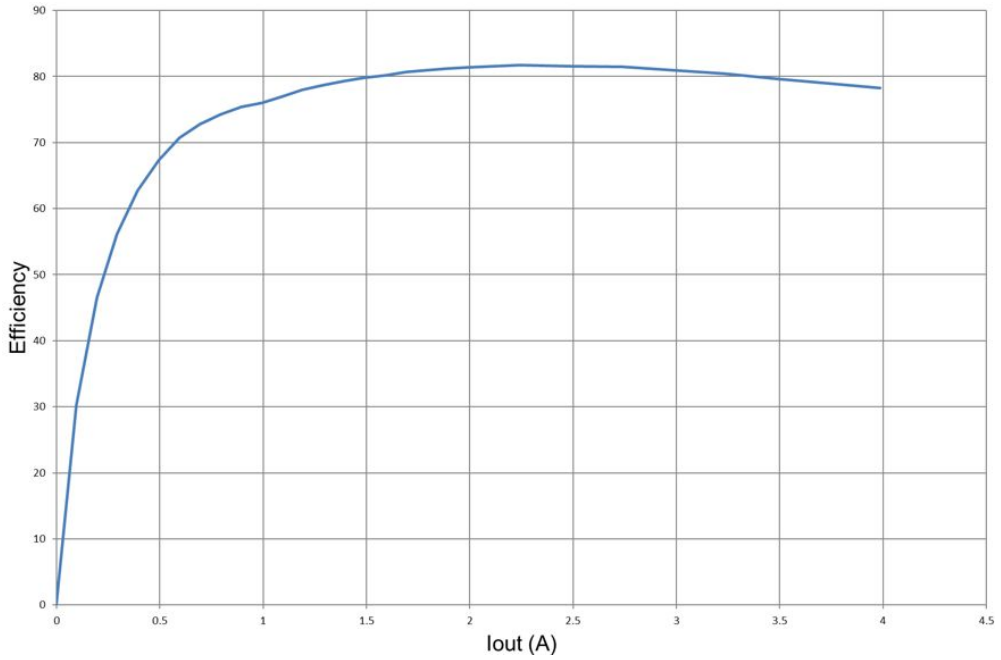


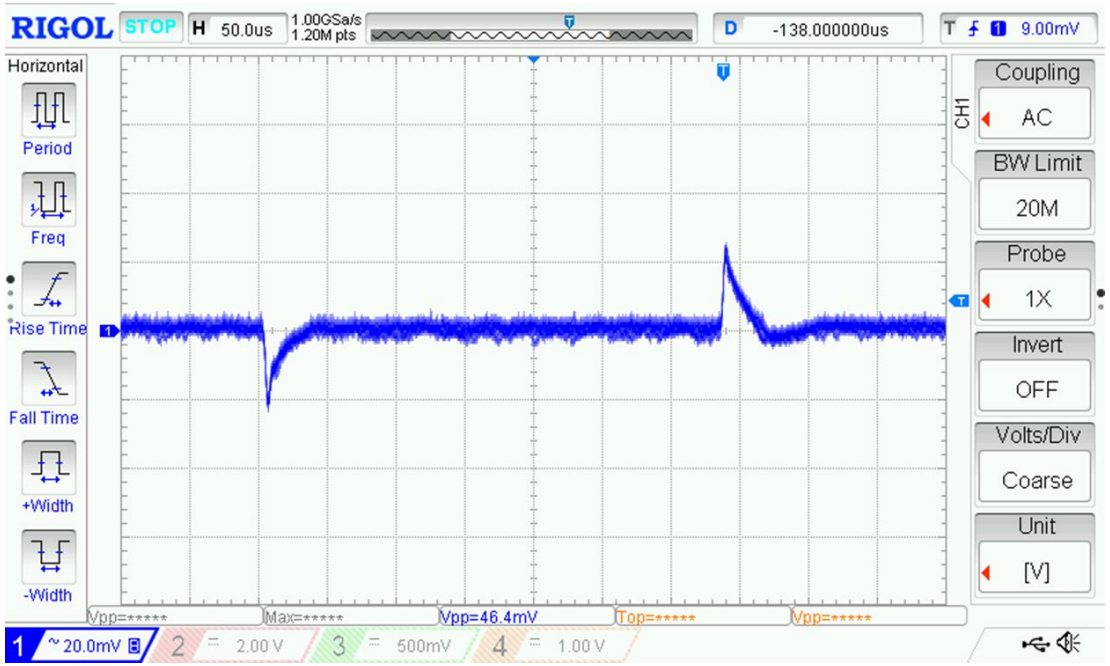
3 A Load
V_{PP} = 6.4 mV

VMGTAVTT
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

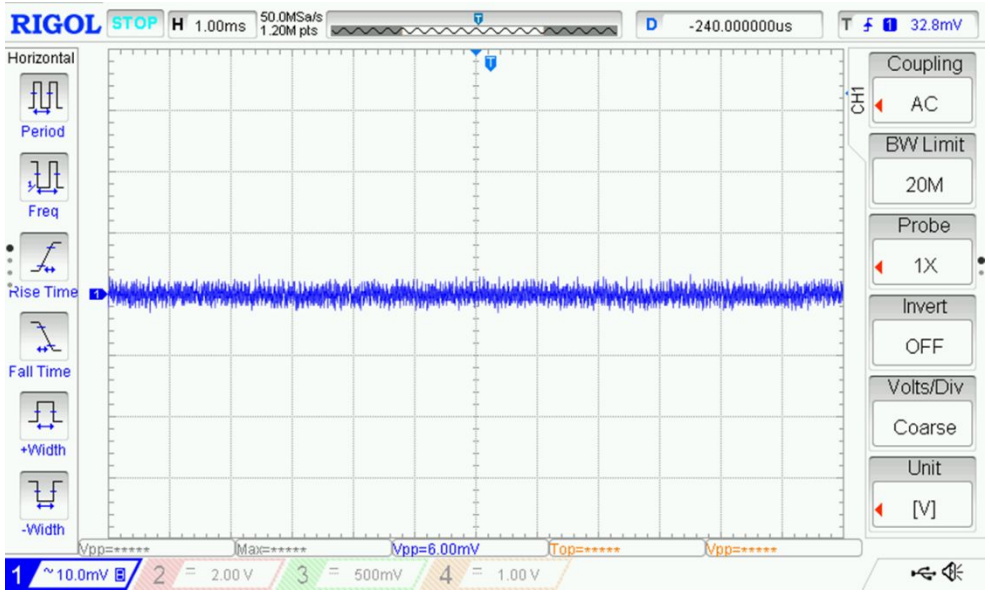
Efficiency & Transient





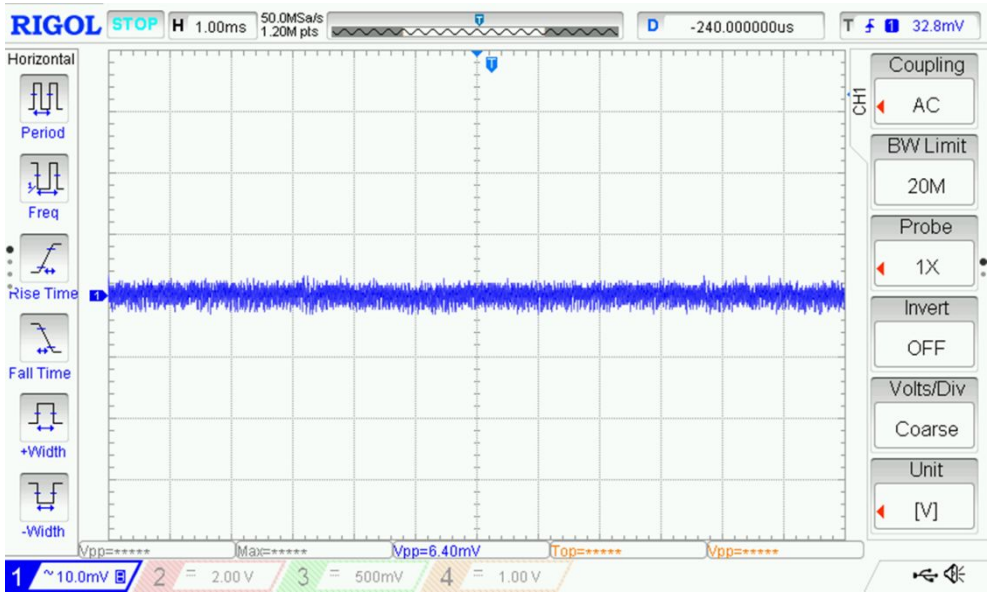
Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



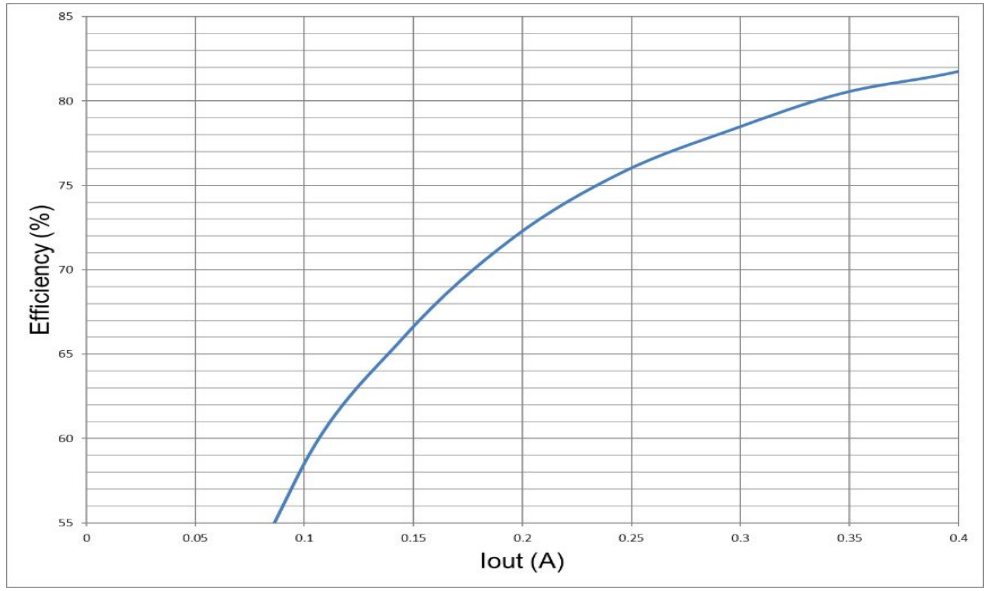
0.035 A Load
V_{PP} = 6.4 mV

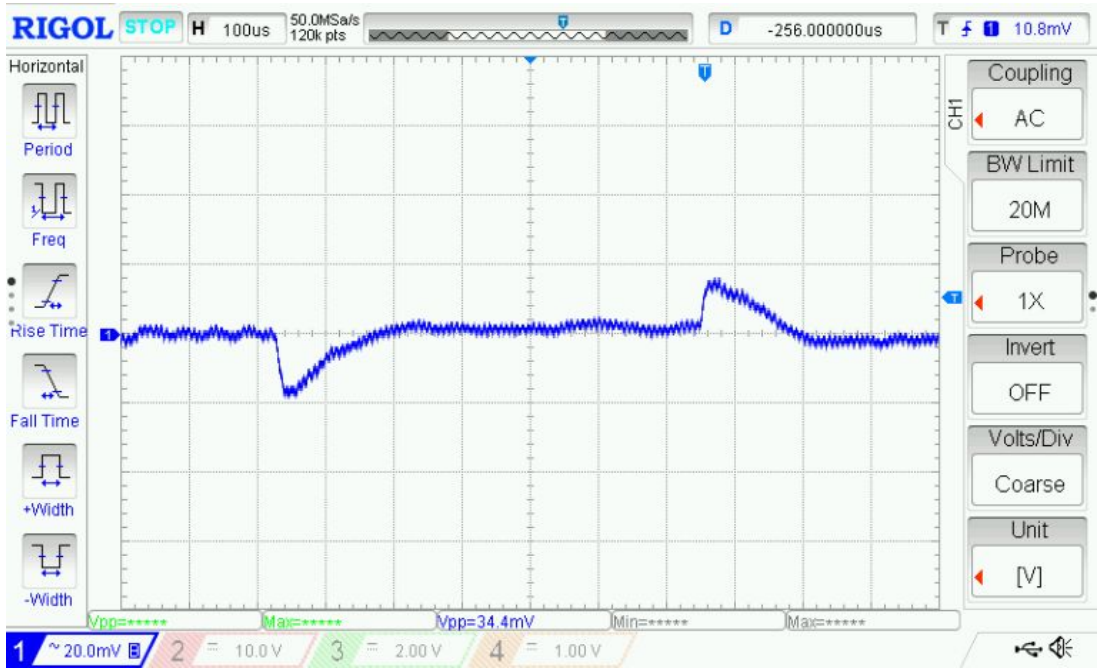
AnDAPT

VMGTAVCCAUX
1.8 V / 0.1 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74438357100
- C = 1x47 uF

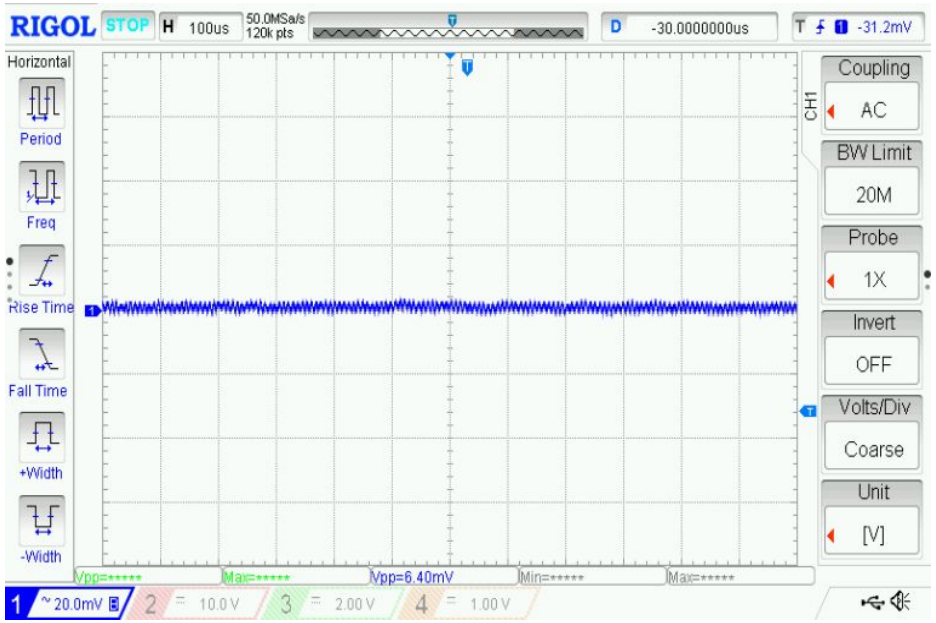
Efficiency & Transient



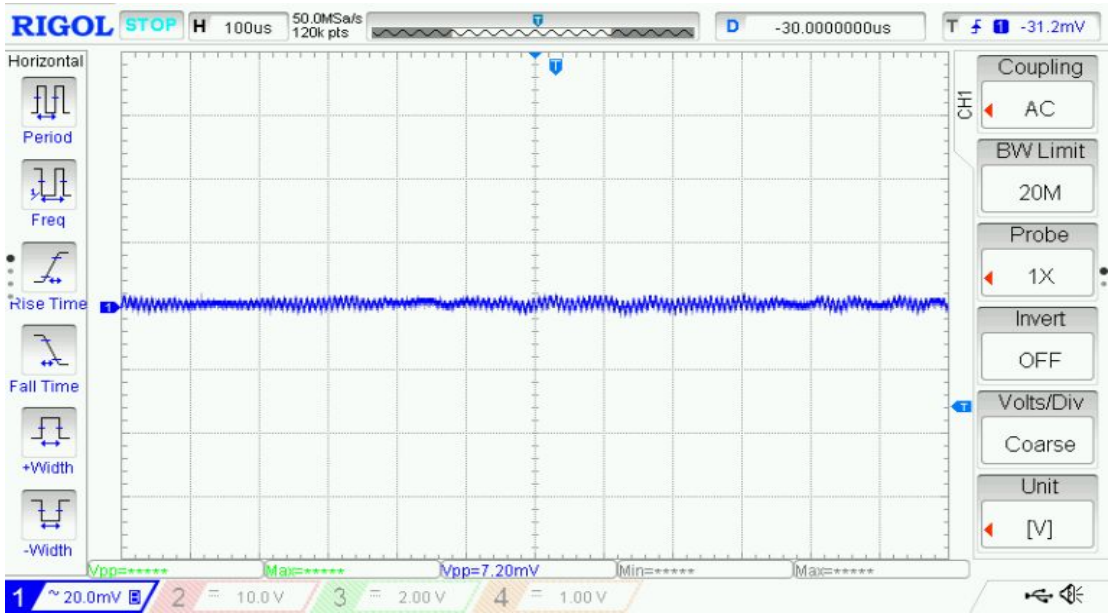


Vout = 1.8 V
Transient 0.12 A – 0.4 A @ 2.5 A/µs
V_{PP} = 34.4 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1 x 47 µF

Ripple



No Load
V_{PP} = 6.4 mV



Vout = 1.8 V

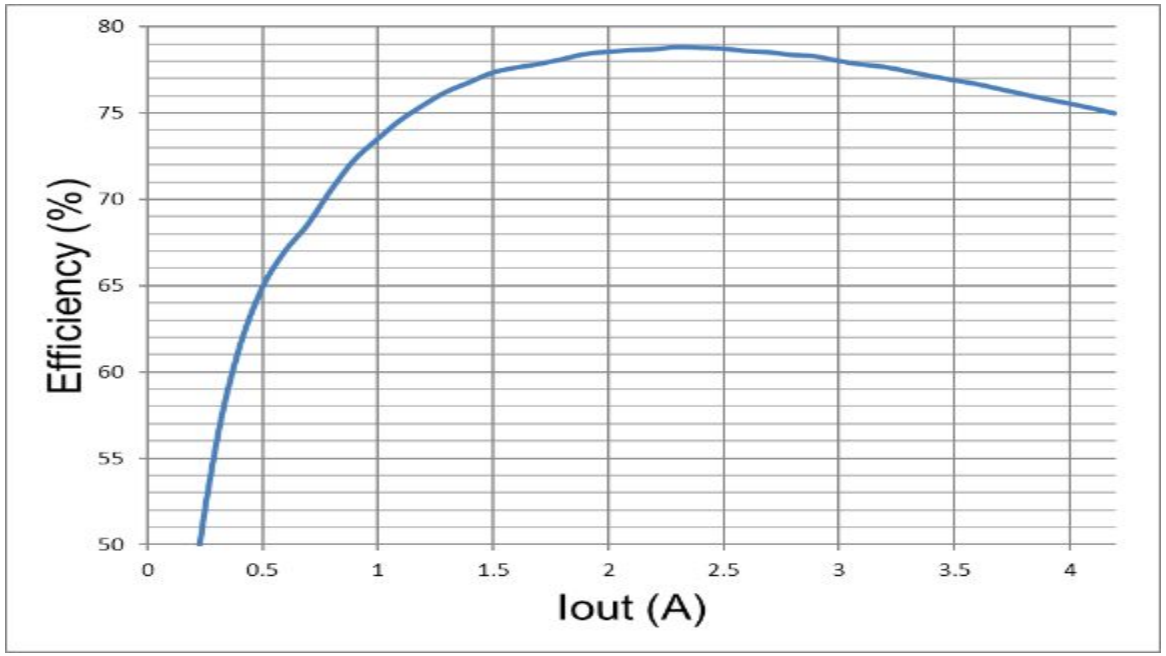
0.4 A Load
V_{PP} = 7.2 mV

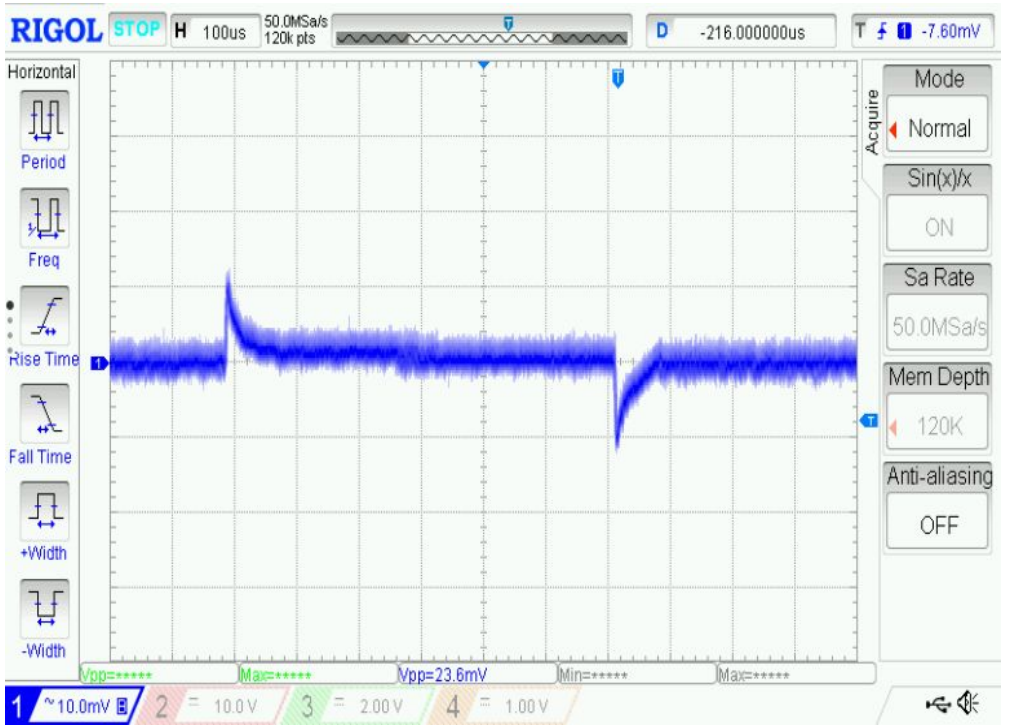
AnDAPT

VMGTAVCC
0.9 V / 4 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

Efficiency & Transient

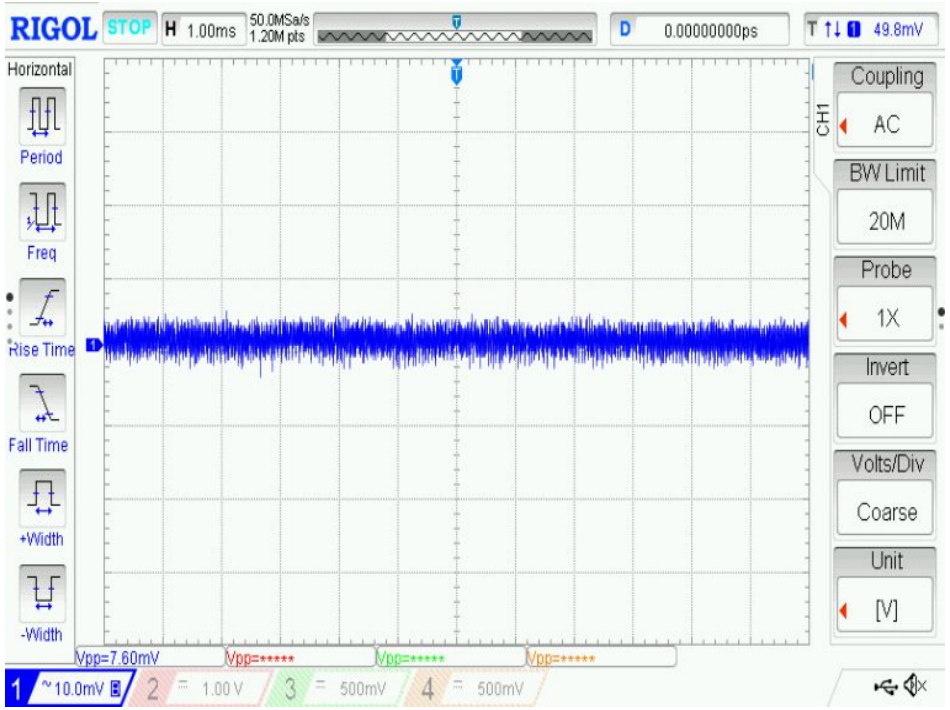




Vout = 0.9V
Transient 4.5 A – 6 A @ 10 A/µs
V_{PP} = 23.6 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

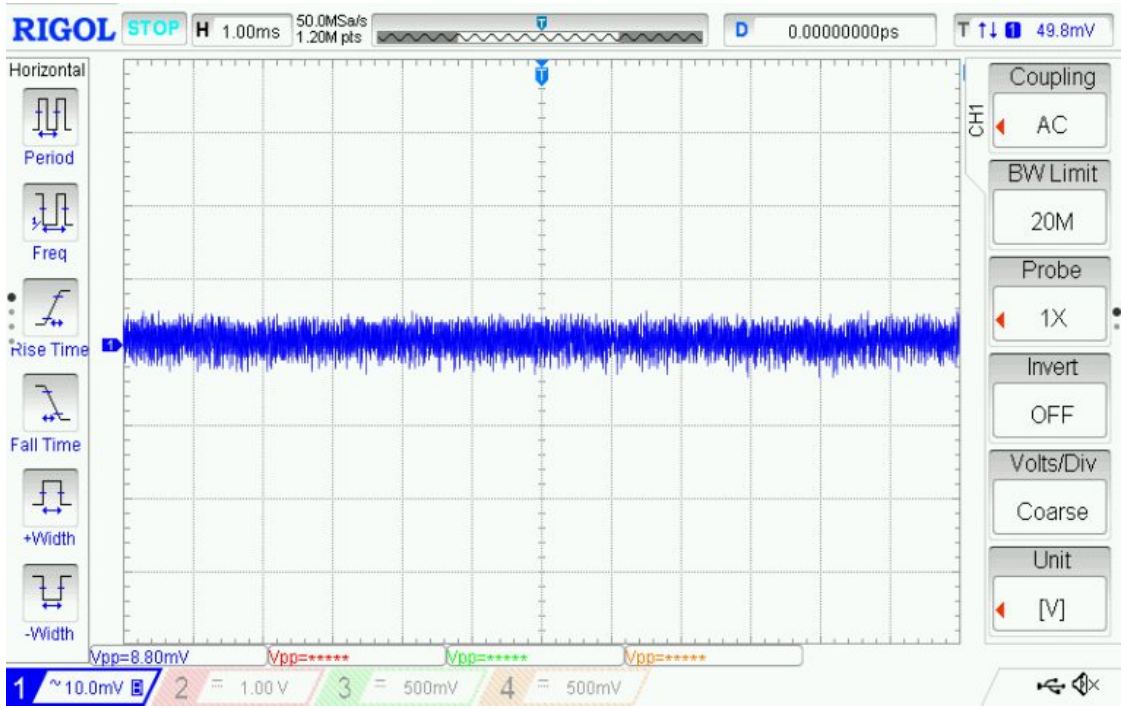
AnDAPT

Ripple



No Load
V_{PP} = 7.6 mV

Vout = 0.9 V



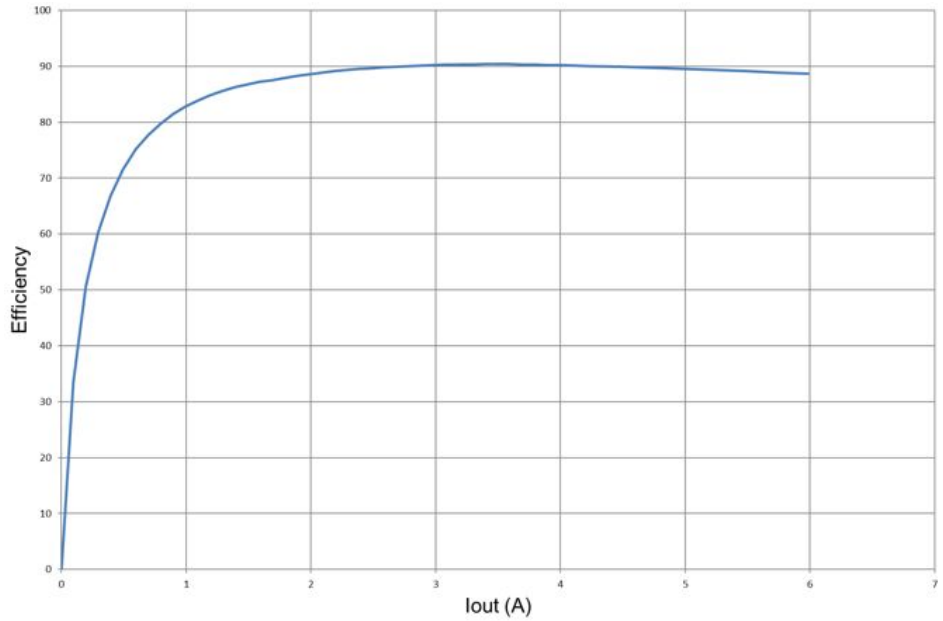
4.2 A Load
V_{PP} = 8.80 mV

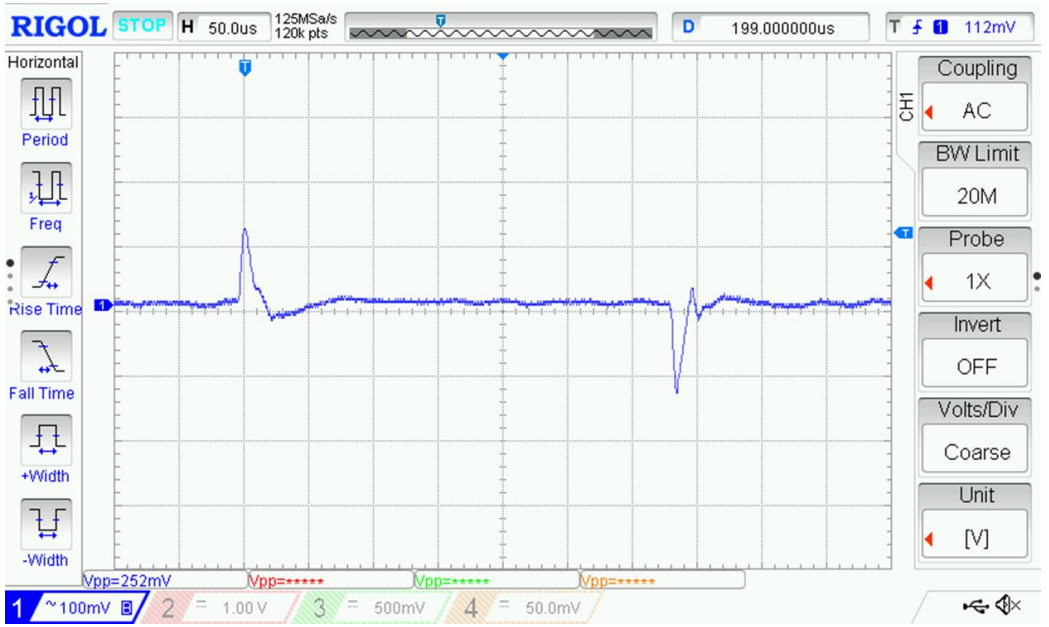
AnDAPT

VCCO_HDIO, VCCO_HPIO 3.3 V / 6 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

Efficiency & Transient

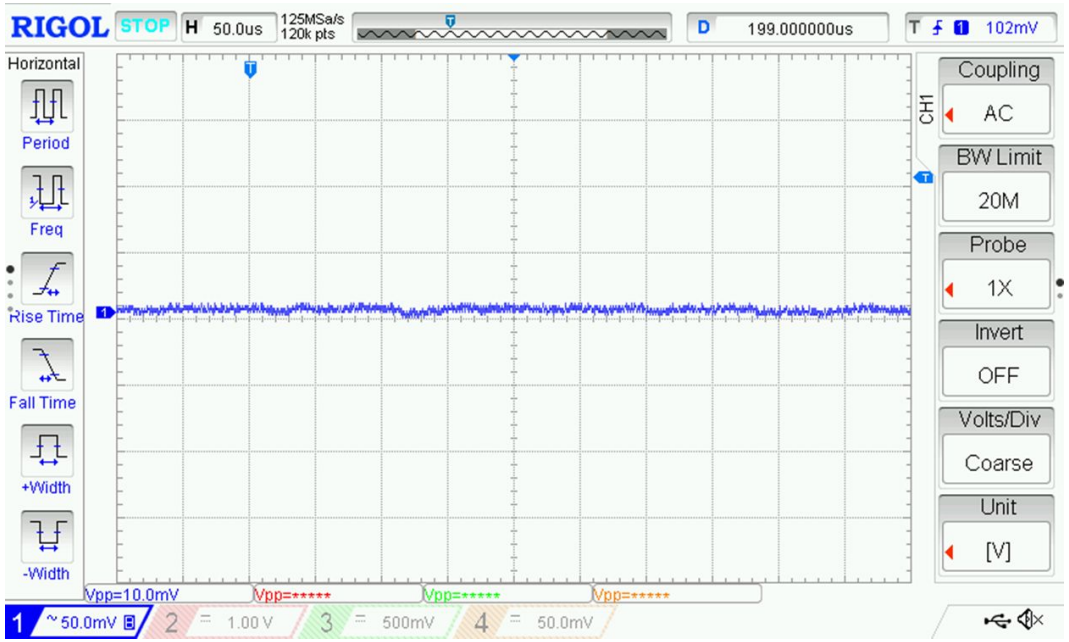




Vout = 3.3 V
Transient 0.6 A – 6 A @ 10 A/µs
V_{PP} = 252 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

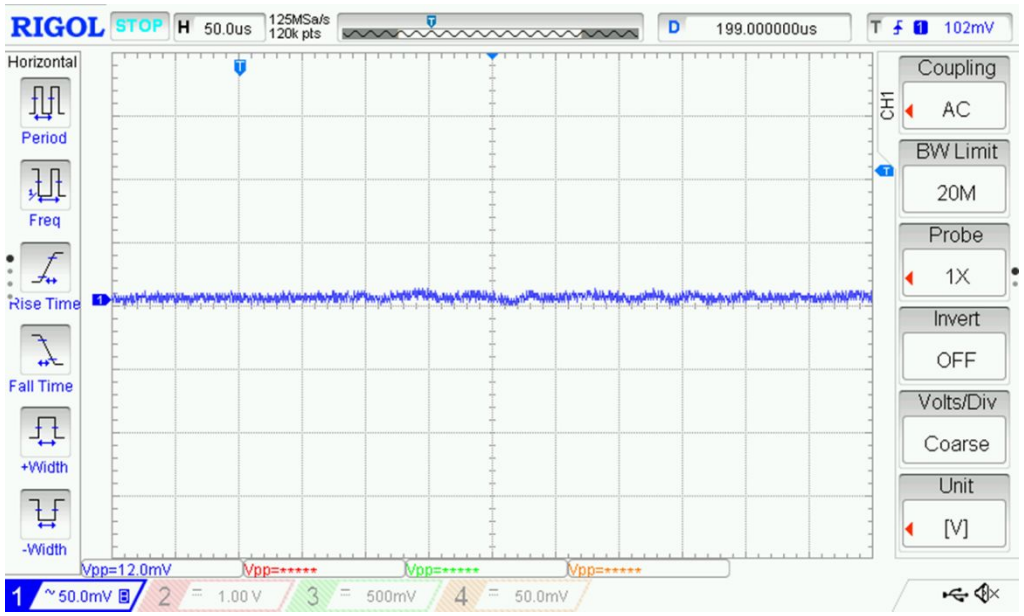
AnDAPT

Ripple



No Load
V_{PP} = 10 mV

Vout = 1.8 V



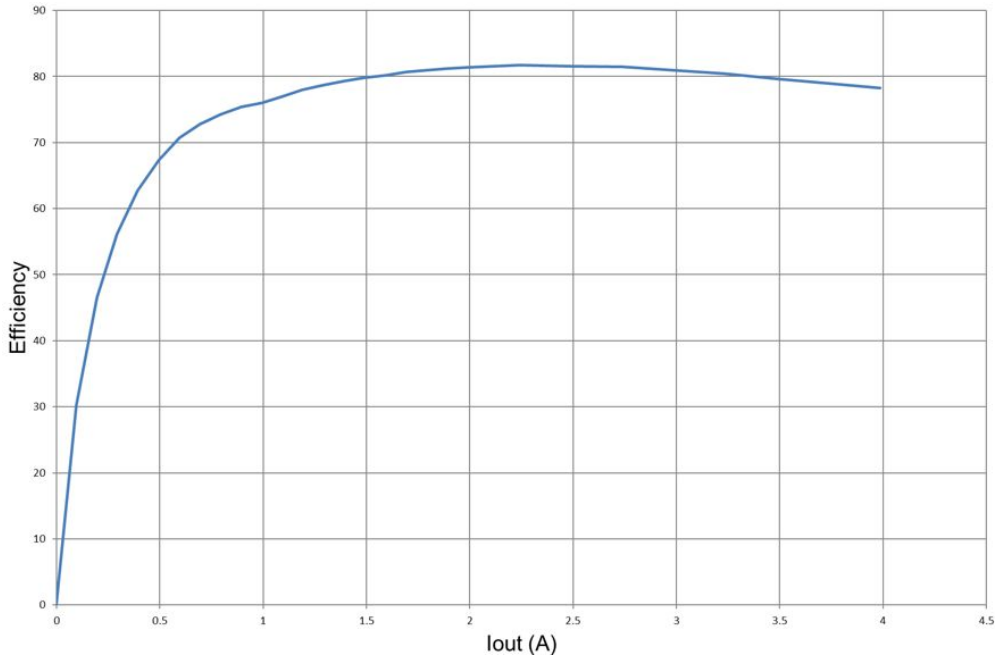
3 A Load
V_{PP} = 12 mV

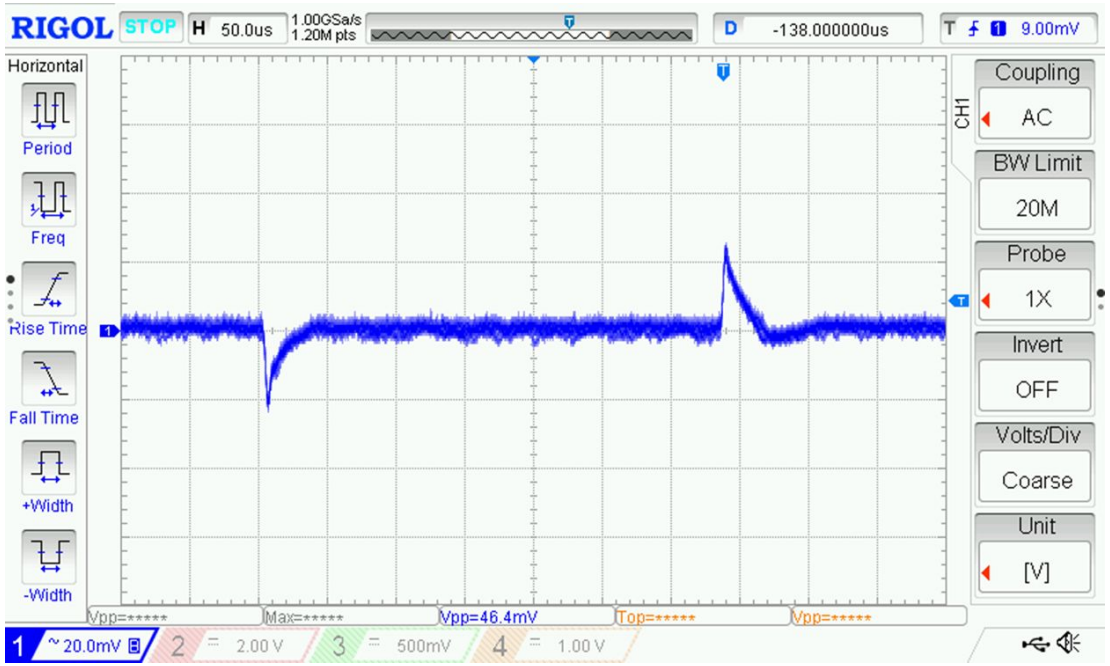
AnDAPT

VCC_DDR
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

Efficiency & Transient

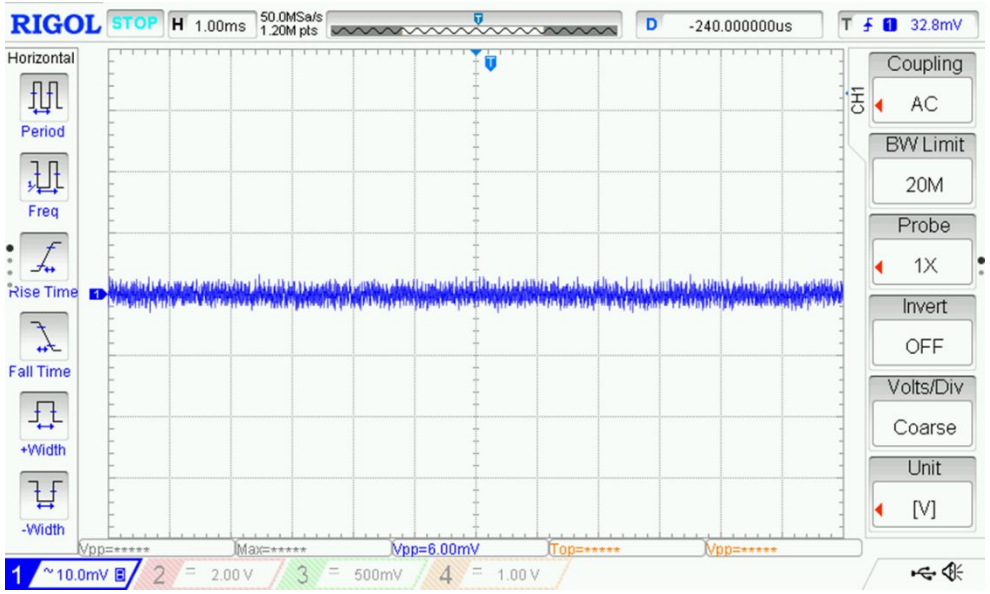




Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

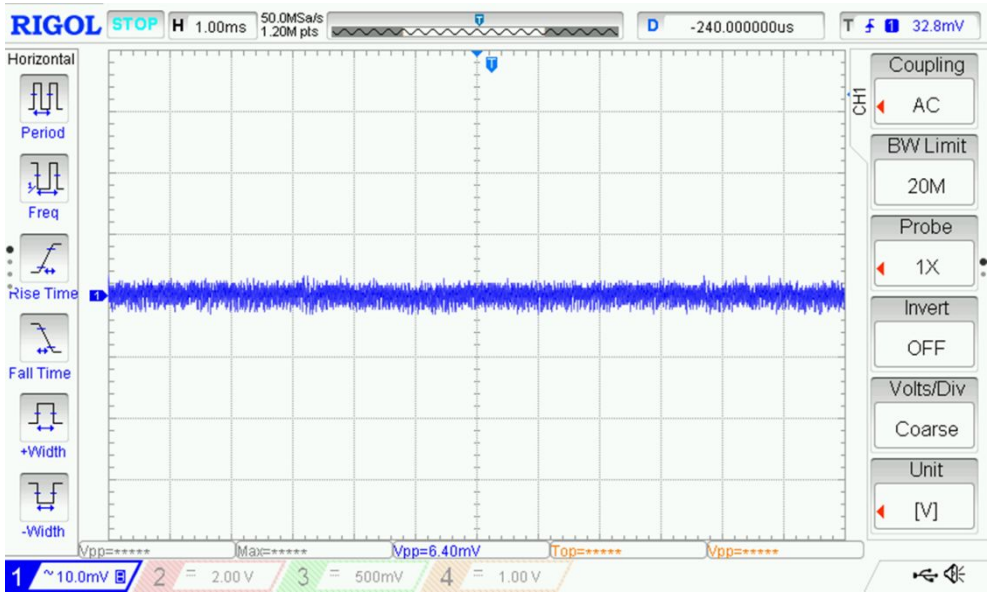
AnDAPT

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



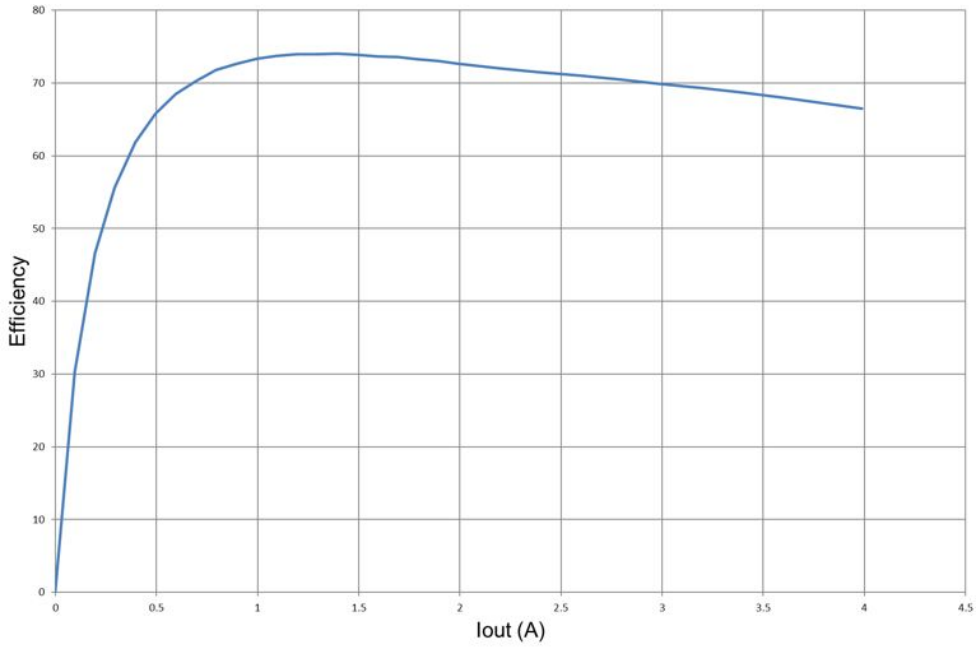
0.035 A Load
V_{PP} = 6.4 mV

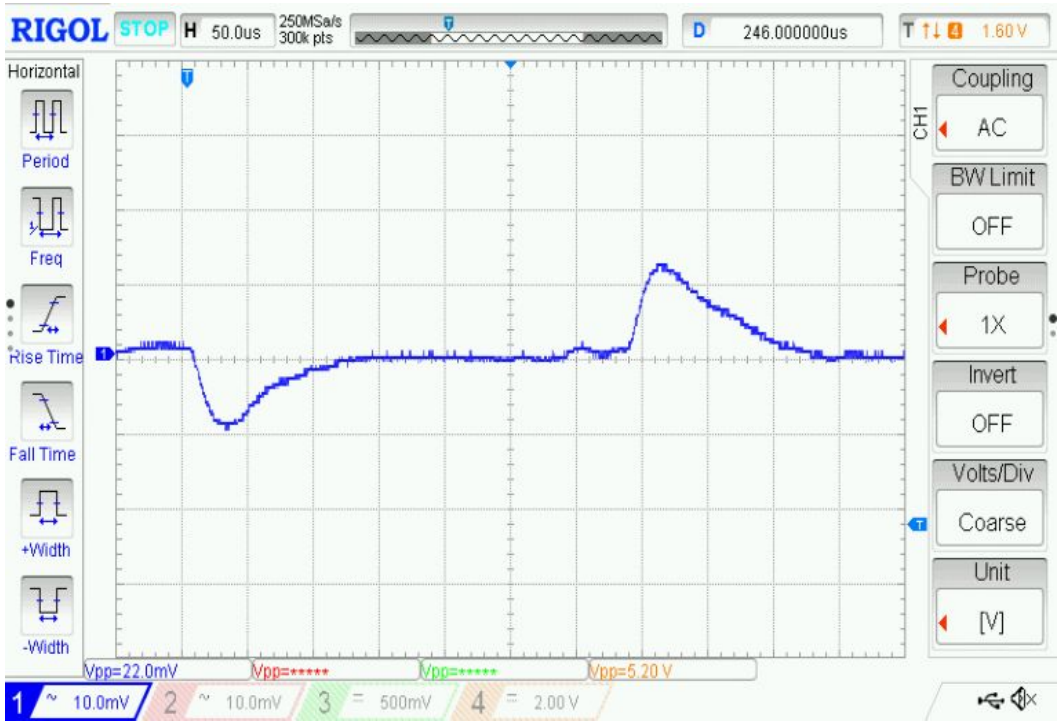
AnDAPT

DDR_VTT
0.6 V / 2 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 1 µH, P/N Wurth 74438366010
- C = 8x47 uF

Efficiency & Transient

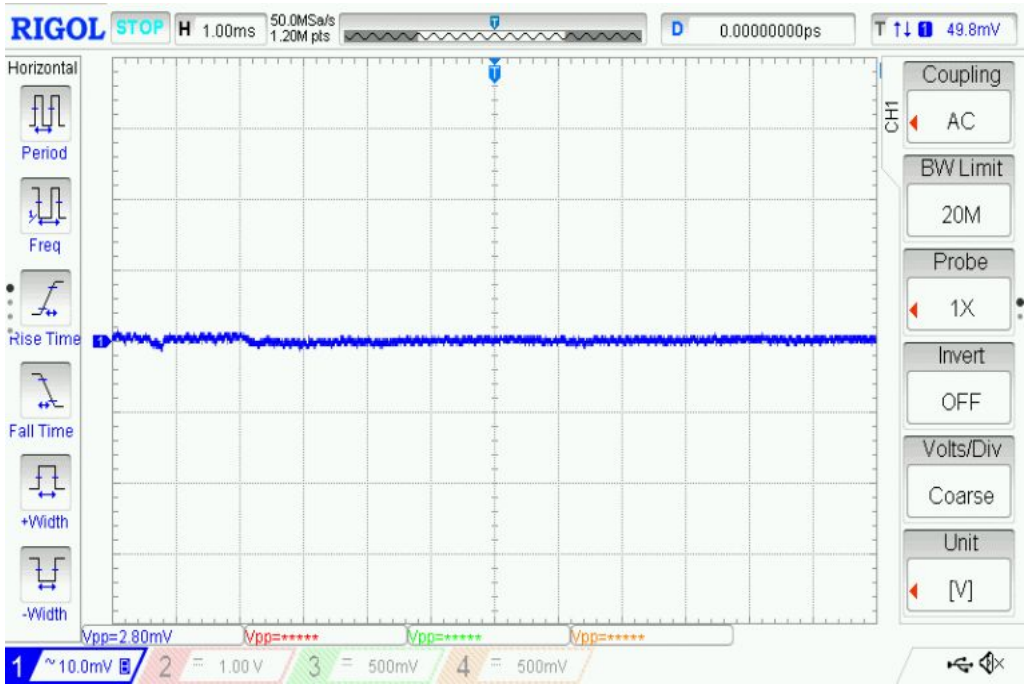




Vout = 0.6 V
Transient 1.125A – 1.5 A @ 2.5 A/µs
V_{PP} = 22 mV
Fsw = 1 MHz
Lout = 1 µH, Cout = 8 x 47 µF

AnDAPT

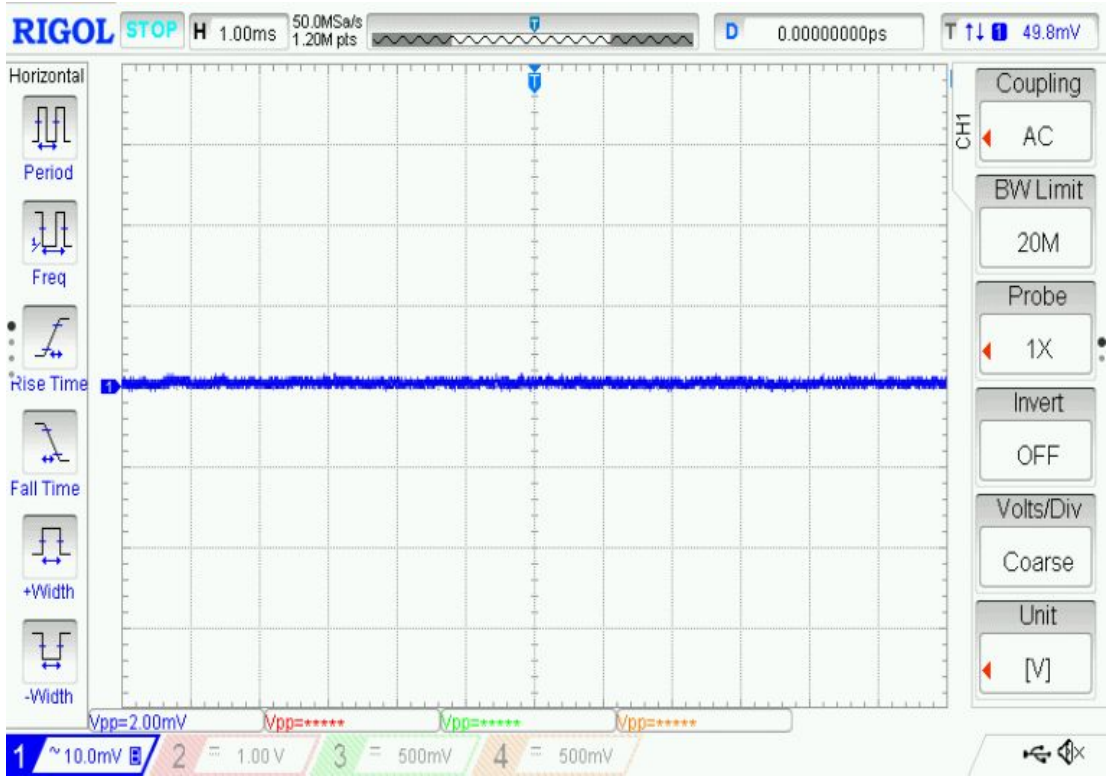
Ripple



No Load

V_{PP} = 2.8 mV

Vout = 0.6 V



4 A Load

V_{PP} = 2 mV

AnDAPT

Thank You

AnDAPT