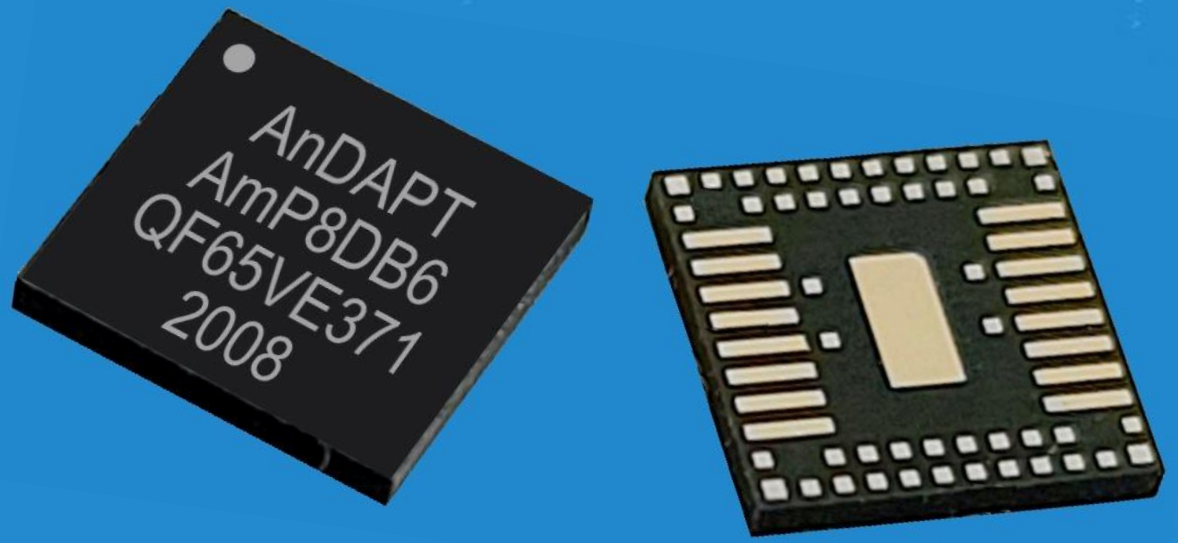


Kintex UltraScale

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

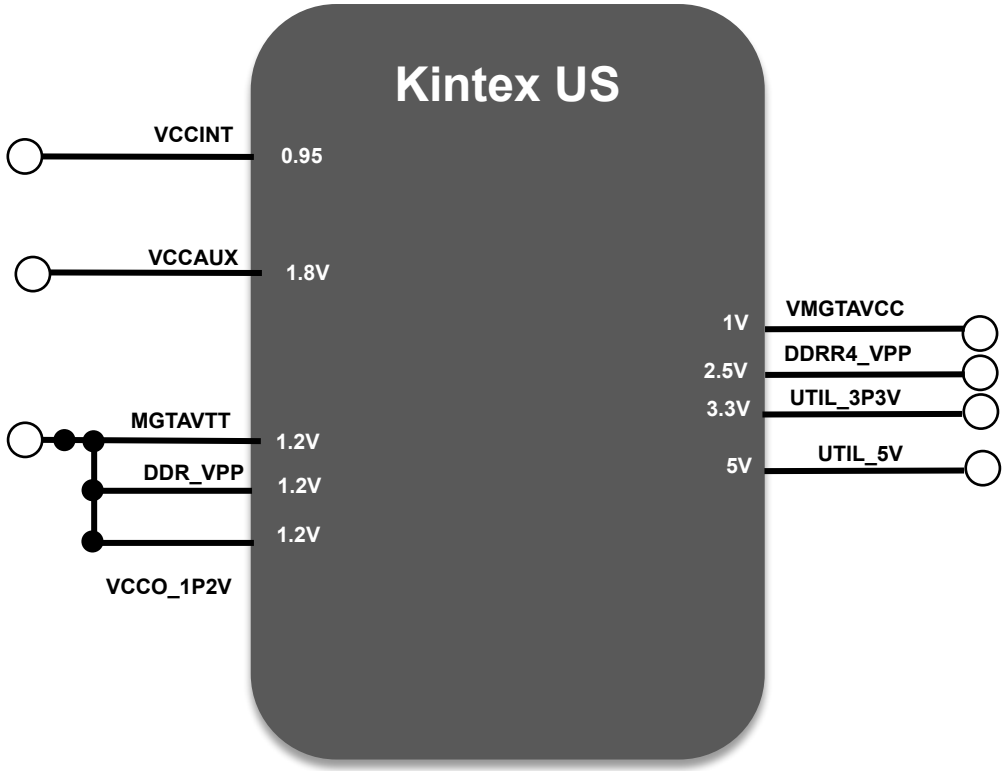
- Xilinx Kintex UltraScale + family of devices SKUs
- Kintex UltraScale + power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Kintex UltraScale + family FPGAs

Kintex UltraScale Device SKUs Covered- Minimum Rails

Supported SKUs
XCKU025
XCKU035
XCKU040
XCKU060
XCKU085
XCKU095
XCKU115

Kintex UltraScale

Can be combined
if voltage same



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Power Tree: Kintex UltraScale

PVIN = 12V/1.2V

#	Rail	Seq	Vin (V)	Vout (V)	Iout (A)
1	VCCINT	1	12	0.95	30
2	VCCAUX	3	12	1.8	4
3	VMGTAVCC	1	12	1	2
4	VMGTAVTT	2	12	1.2	4
5	VCCO_1P2V	4	1.2	1.2	2
6	DDR_VPP	5	12	1.2	2
7	DDR4_VPP	6	12	2.5	0.25
8	UTIL_3P3V	7	12	3.3	1
9	UTIL_5V	8	12	5	1

Power Tree Mapping: Kintex UltraScale

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC	Comment
1	VCCINT, BRAM, VCCINT_IO	1	C860	DrMOS Ctrl	PVIN	12	0.95	30	ARD_X_KXU_A_IC1	
2	VCCAUX, VCCAUXIO, MGTVCCAUX, VCCO_1P8V	3	C200	Sync Buck	PVIN	12	1.8	4	ARD_X_KXU_A_IC1	
3	MGTAVCC	1	C200	Sync Buck	PVIN	12	1	2	ARD_X_KXU_A_IC1	
4	MGTAVTT	2	C200	Sync Buck	PVIN	12	1.2	2 + 2	ARD_X_KXU_A_IC1	
5	VCCO_1P2V	4	C750	Load Switch	MGTAVTT	1.2	1.2	2	ARD_X_KXU_A_IC1	
6	DDR_VPP, DDR_VTT	5	C200	Sync Buck	PVIN	12	1.2	2	ARD_X_KXU_A_IC2	Optional
7	DDR4_VPP	6	C200	Sync Buck	PVIN	12	2.5	0.25	ARD_X_KXU_A_IC2	
8	UTIL_3P3V	7	C200	Sync Buck	PVIN	12	3.3	1	ARD_X_KXU_A_IC2	
9	UTIL_5V	8	C150	Async Buck	PVIN	12	5	1	ARD_X_KXU_A_IC2	

Estimated total area estimated* = 711.97 mm^2 (IC1) + 451.8 mm^2 * (IC2) = 1163.77 mm^2

*With 75% Layout optimization density

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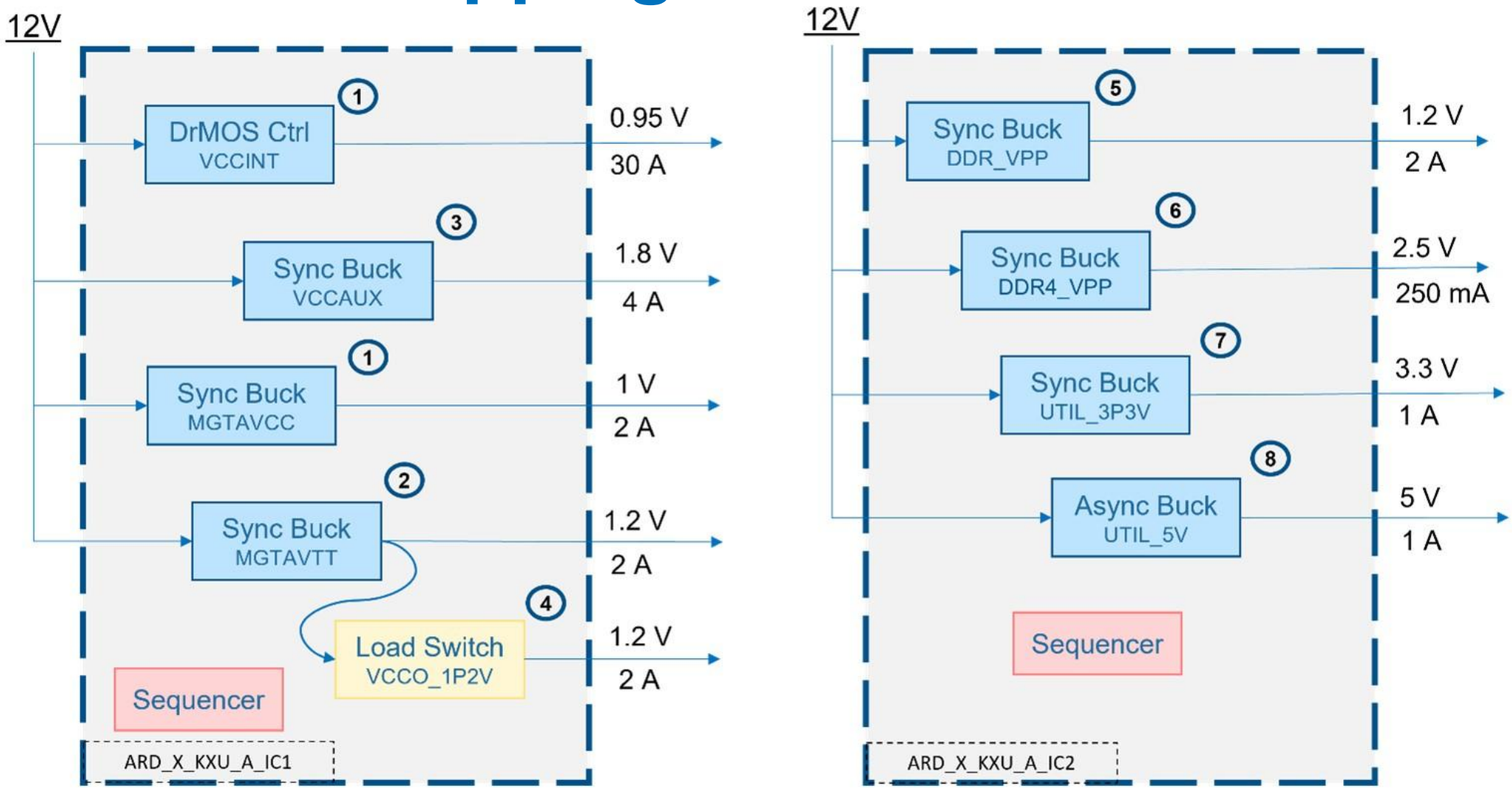
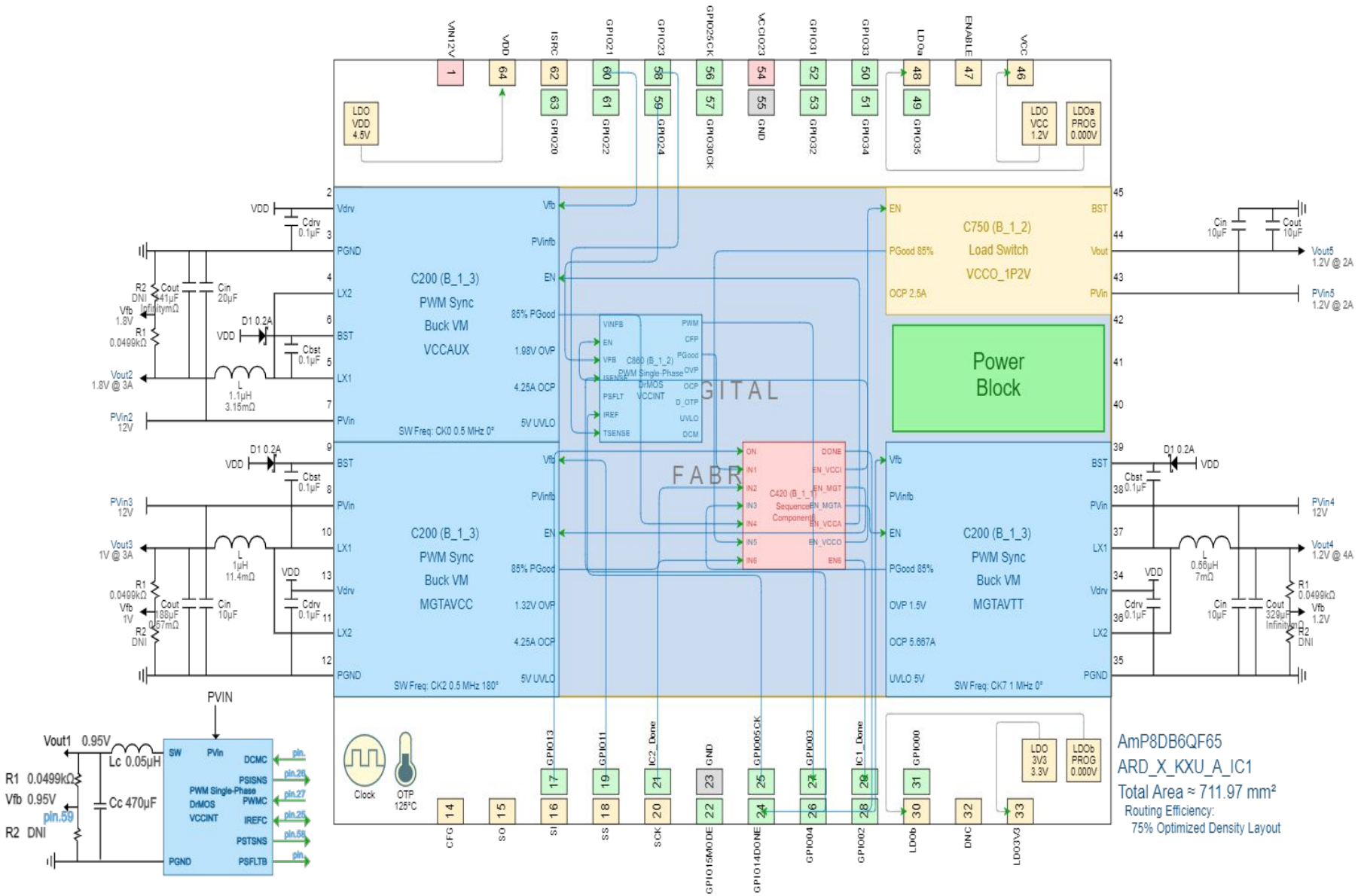
Power Tree Mapping



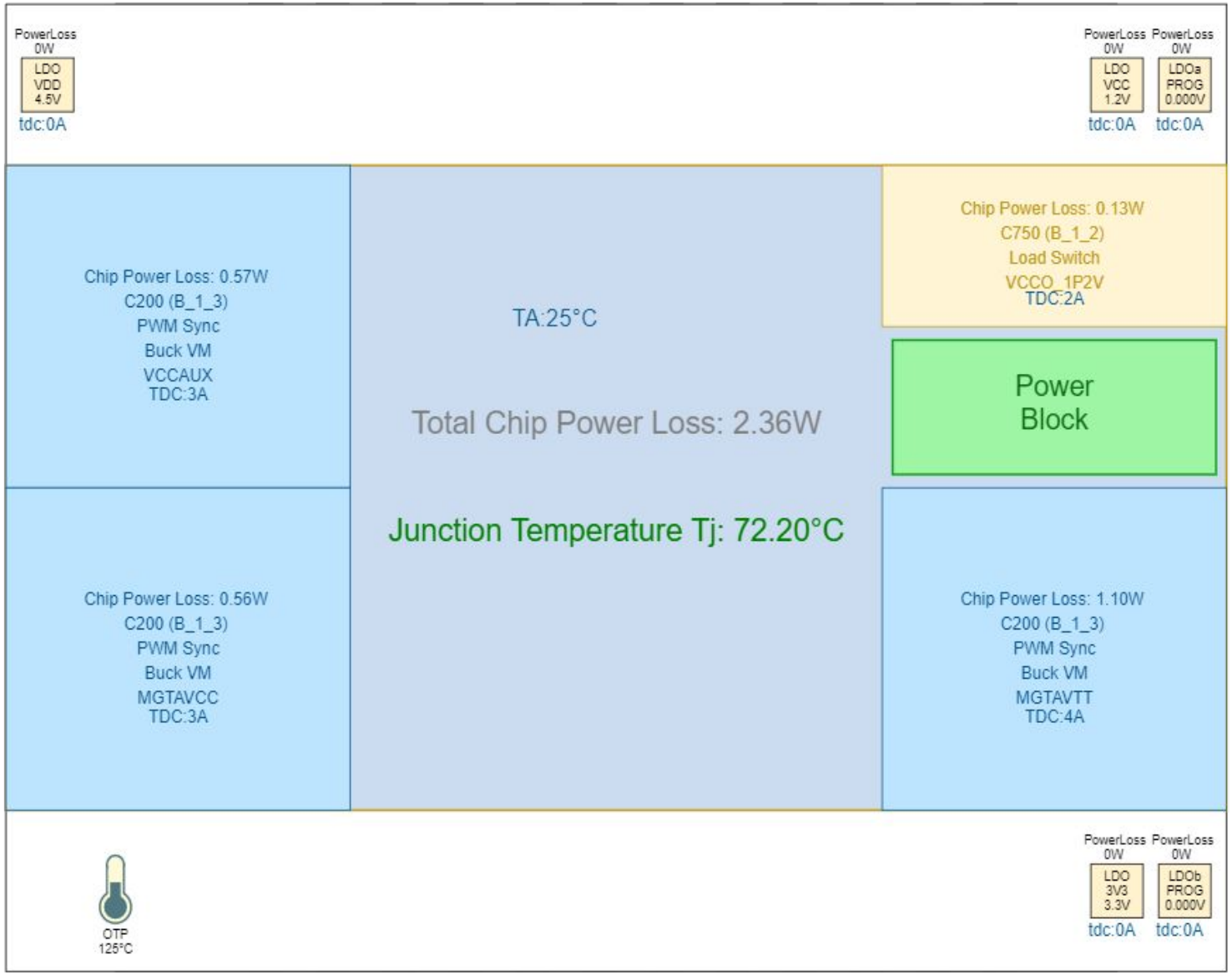
Estimated Total Area = 1163.77 mm^2

AnDAPT

Mapping (WebAmP View) IC1



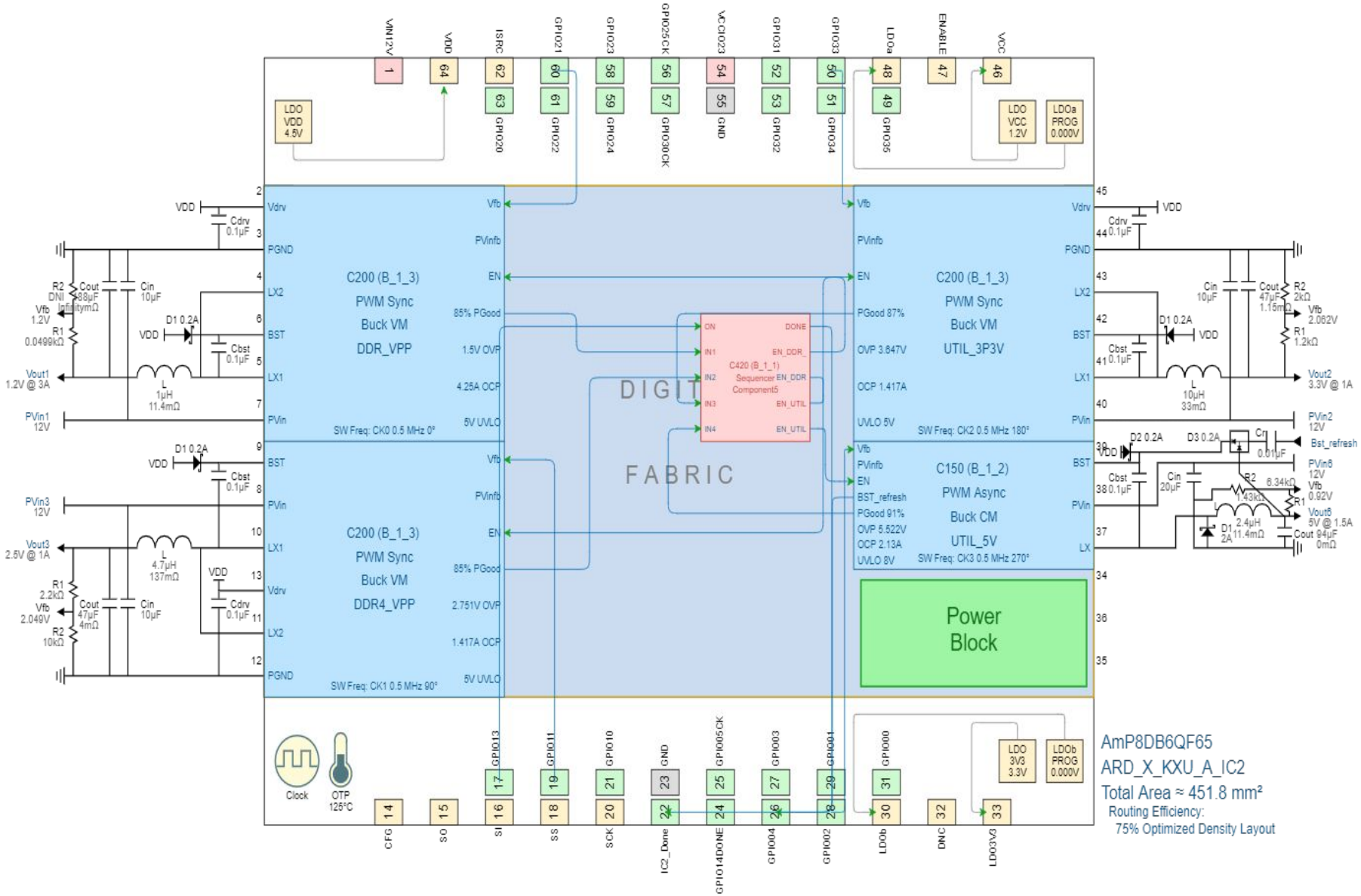
Mapping (Thermal View) IC1



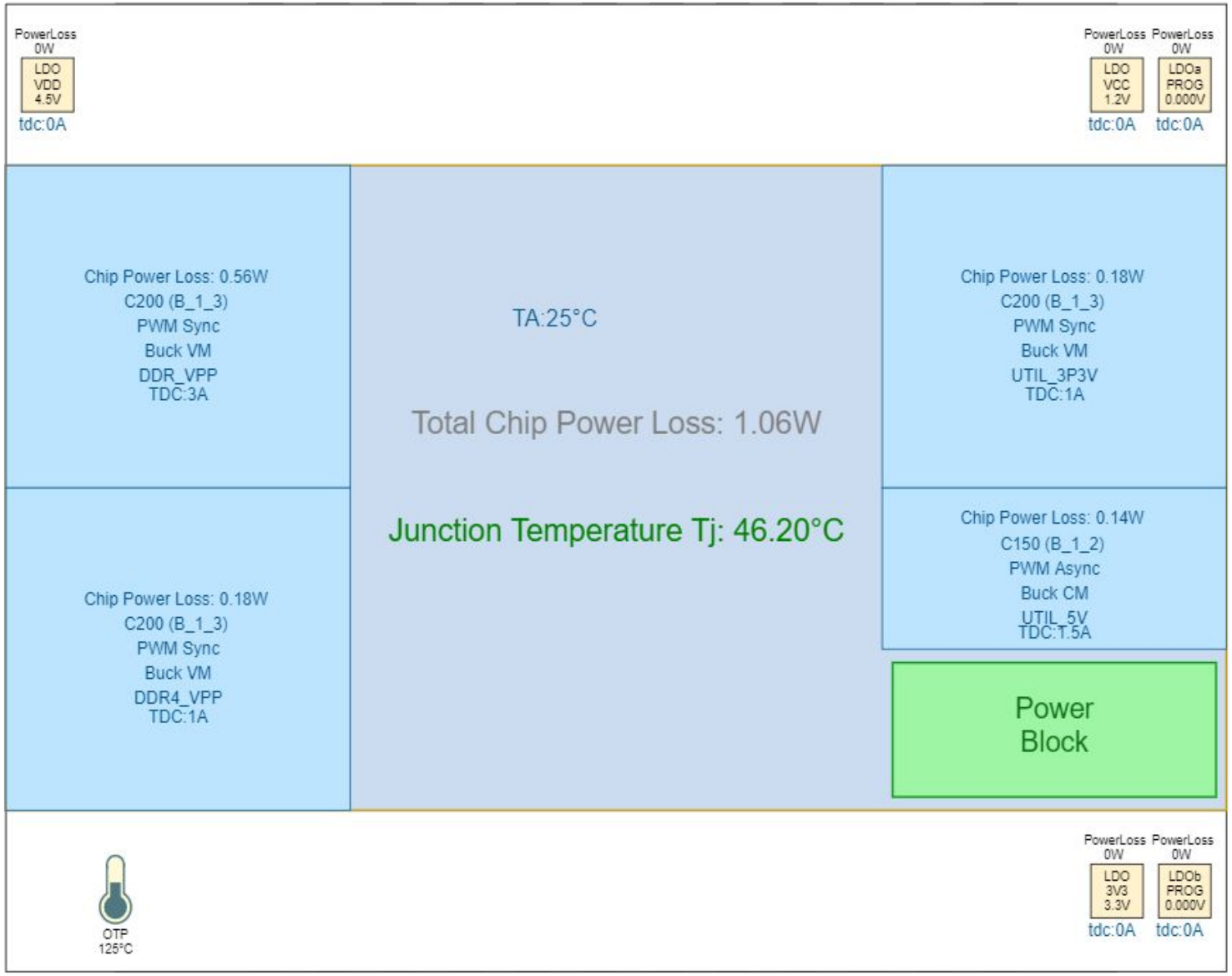
AmP8DB6QF65
ARD_X_KXU_A_IC1
Total Area ≈ 711.97 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT

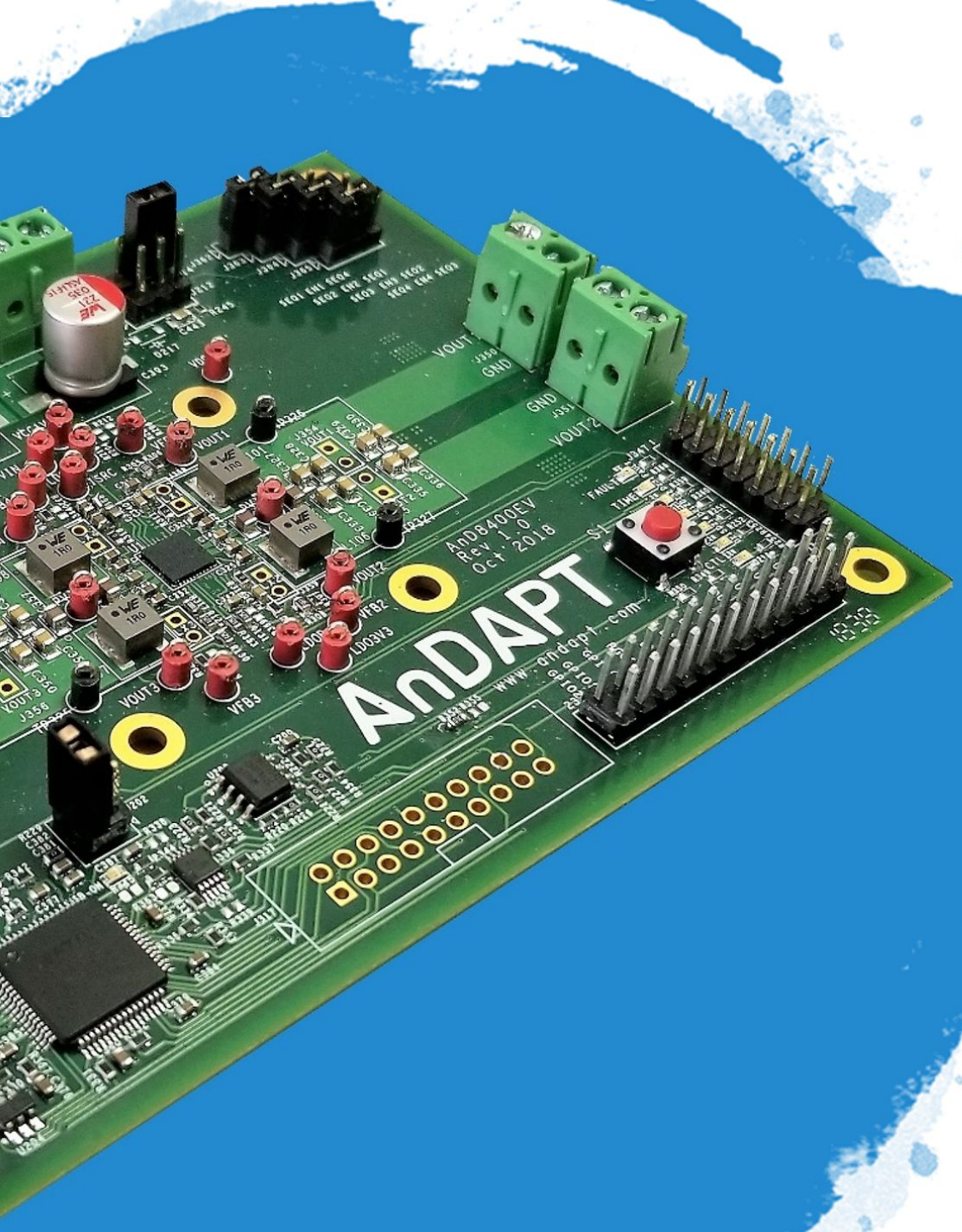
Mapping (WebAmP View) IC2



Mapping (Thermal View) IC2



AmP8DB6QF65
ARD_X_KXU_A_IC2
Total Area ≈ 451.8 mm²
Routing Efficiency:
75% Optimized Density Layout

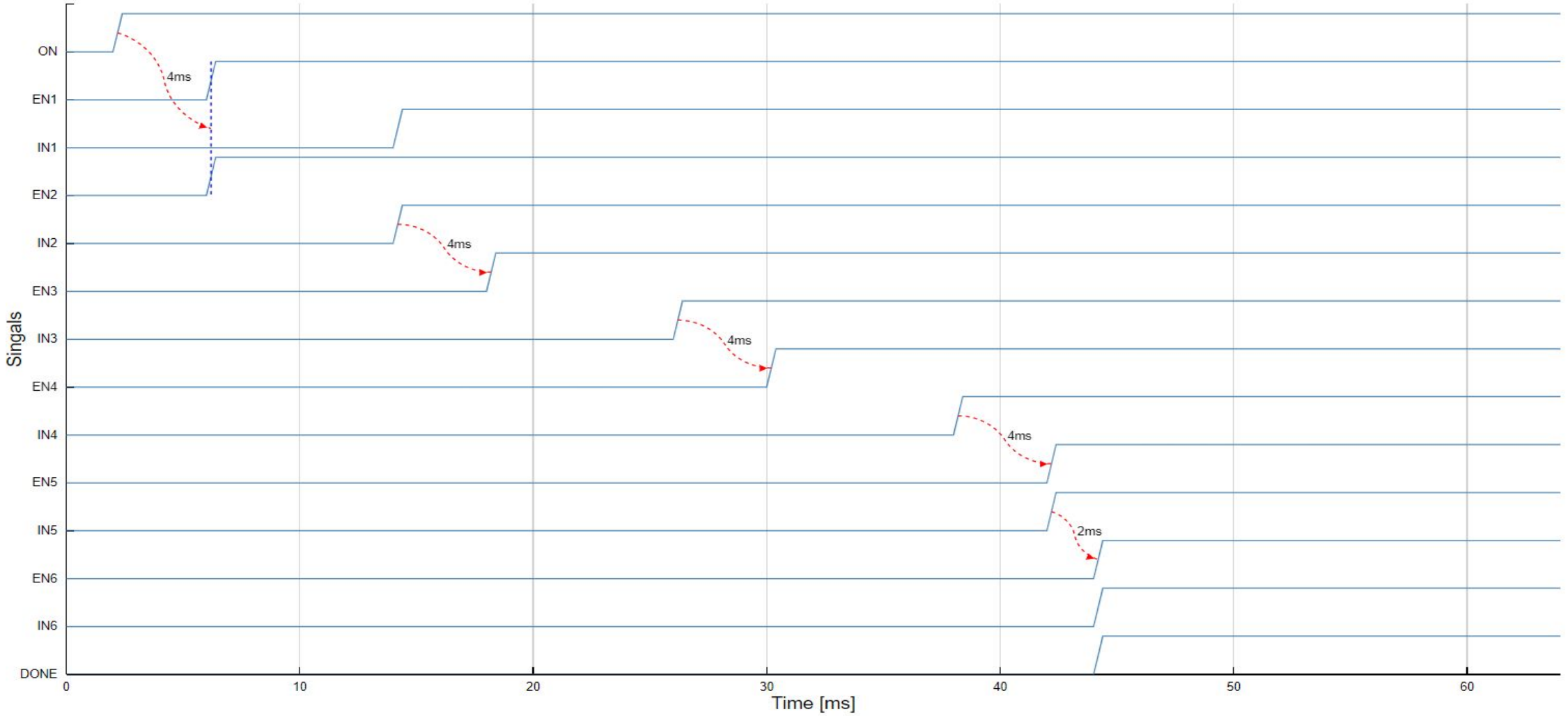


Test Data

Kintex UltraScale

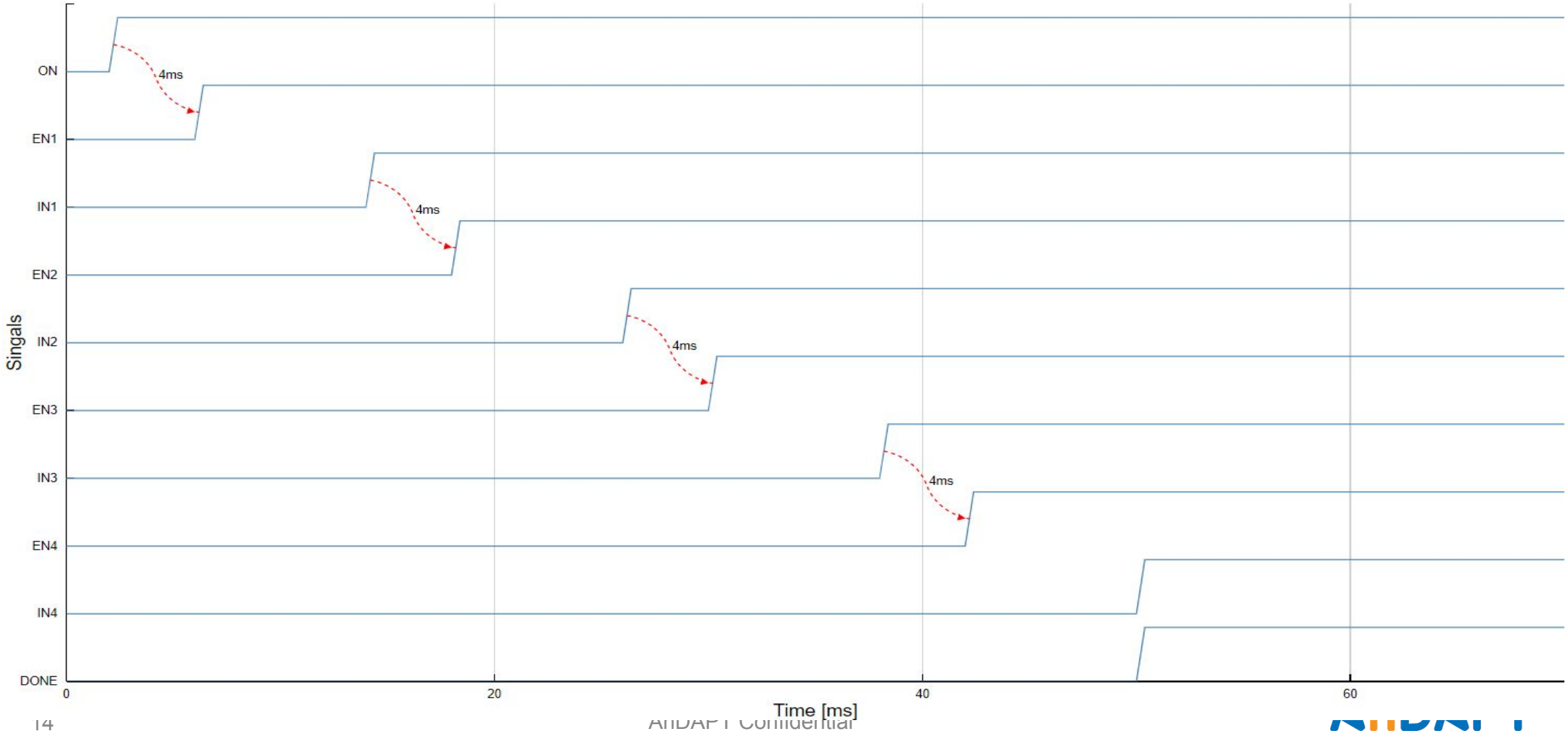
AnDAPT

Integrated Sequencer Graphic IC1 (Turn ON)



AnDAPT

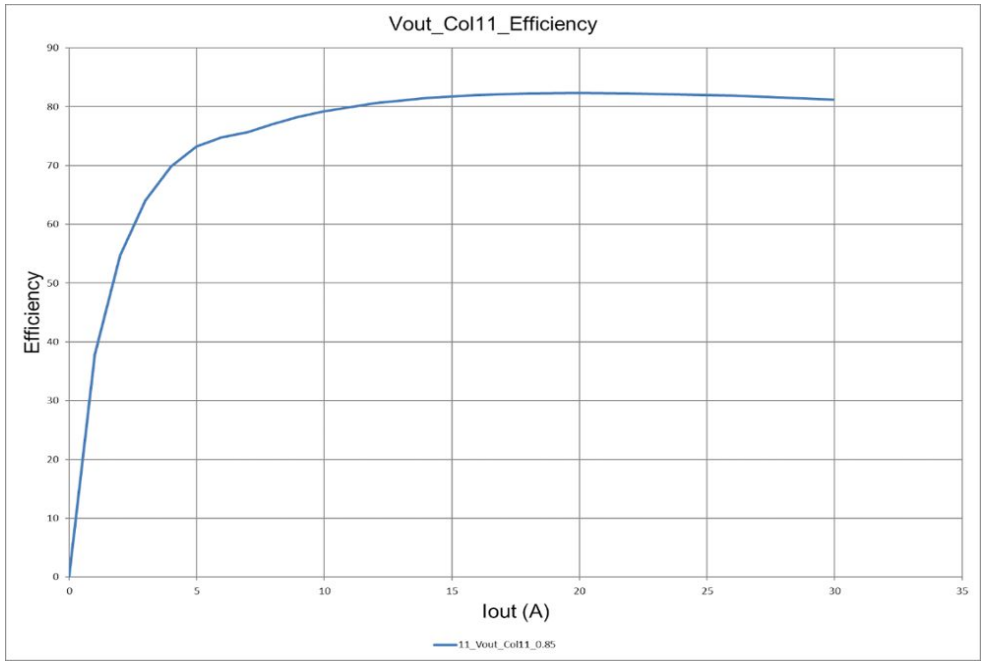
Integrated Sequencer Graphic IC2 (Turn ON)

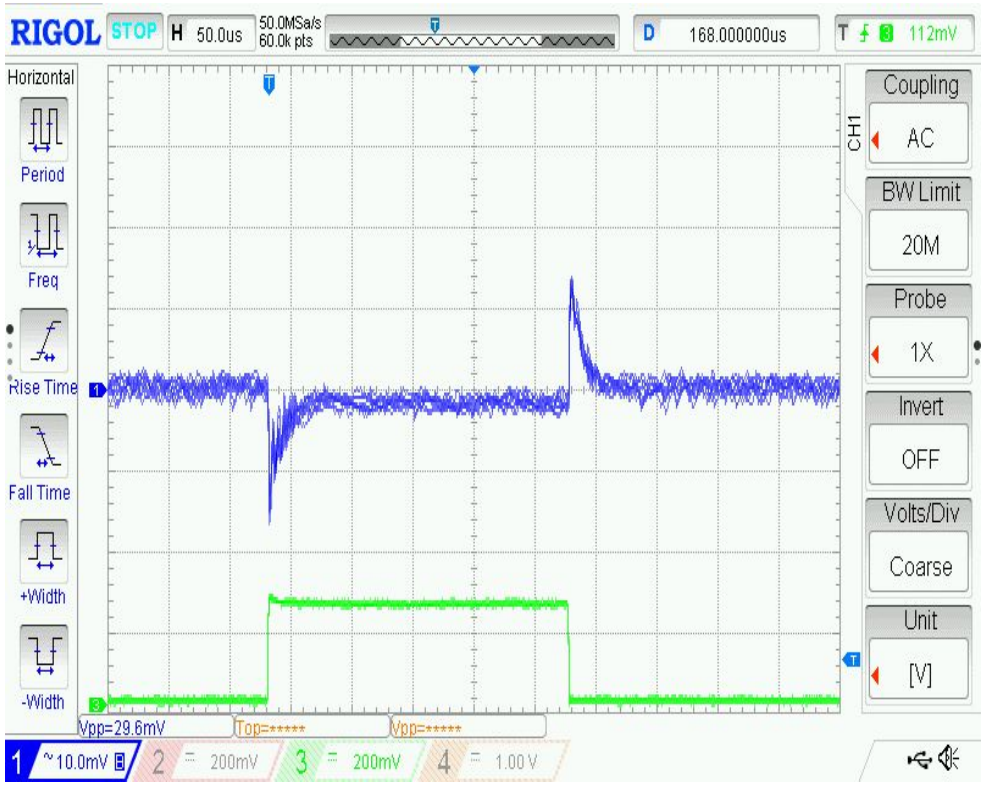


VCCINT
0.95 V / 30 A

- C860
- Fsw = 1 MHz
- L = 0.05 µH, P/N Wurth 744304010
- C = 10x47 uF +2 x 220 uF

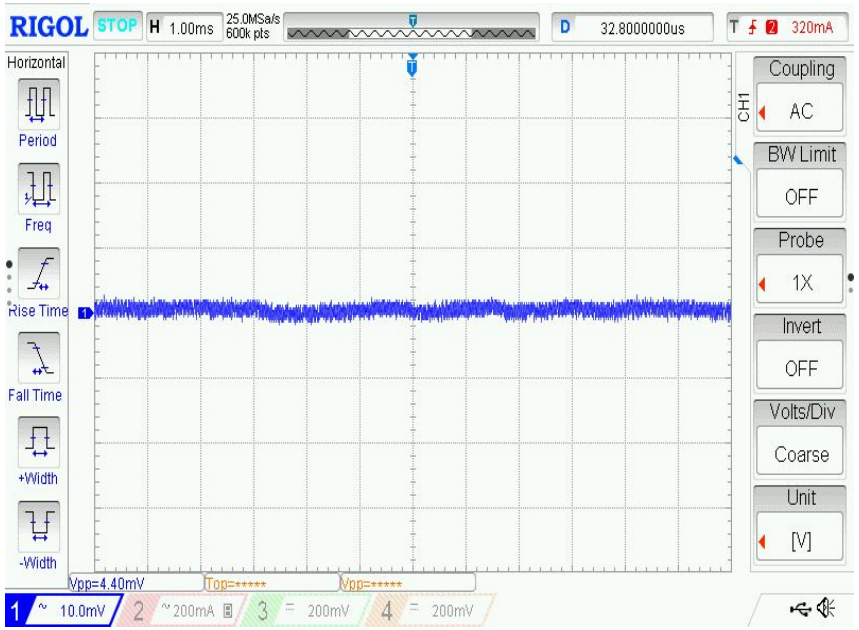
Efficiency & Transient





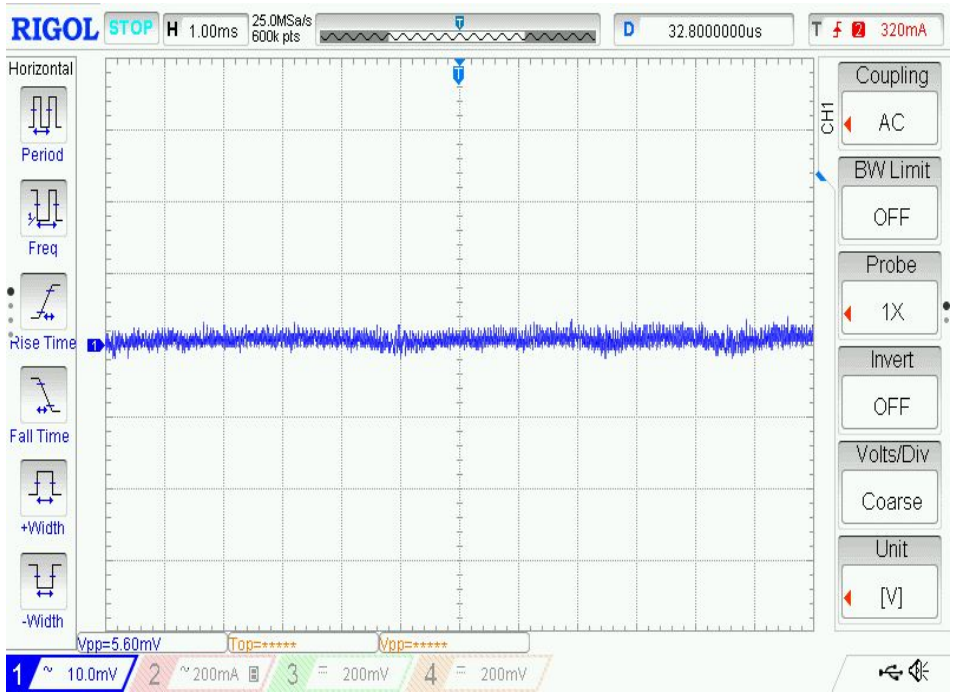
Vout = 0.85V
Transient 22.5A – 30A @ 100 A/µs
V_{PP} = 29.6 mV
Fsw = 1 MHz
Lout = 0.05 µH, 10x47 uF +2 x 220 uF

Ripple



No Load
V_{PP} = 4.40 mV

Vout = 0.85 V



30 A Load
V_{PP} = 5.60 mV

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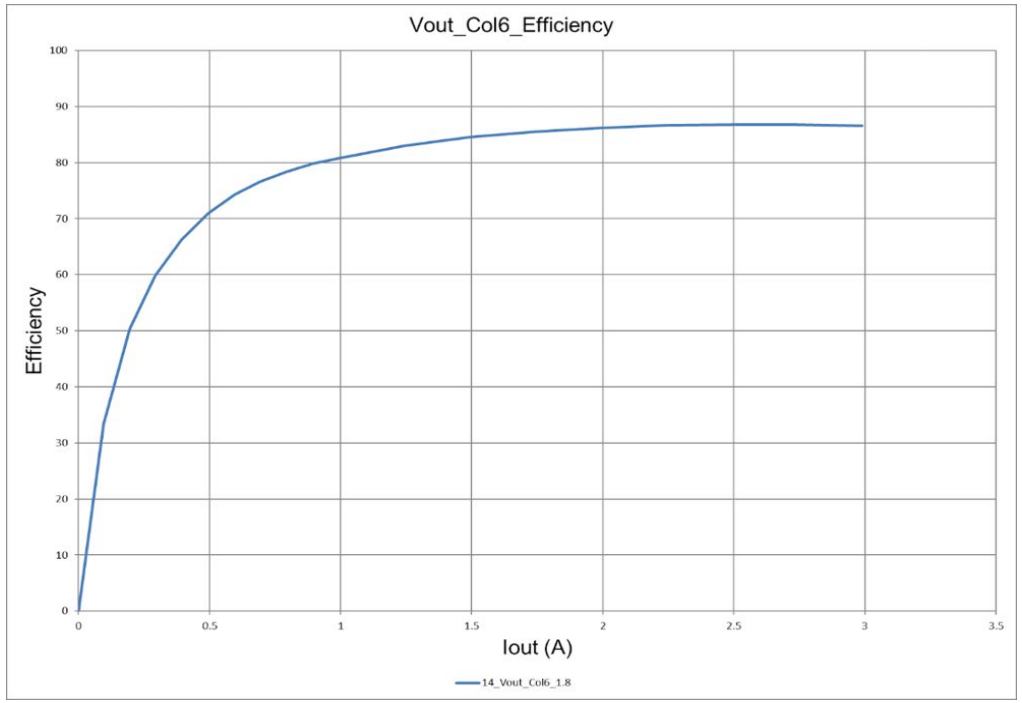
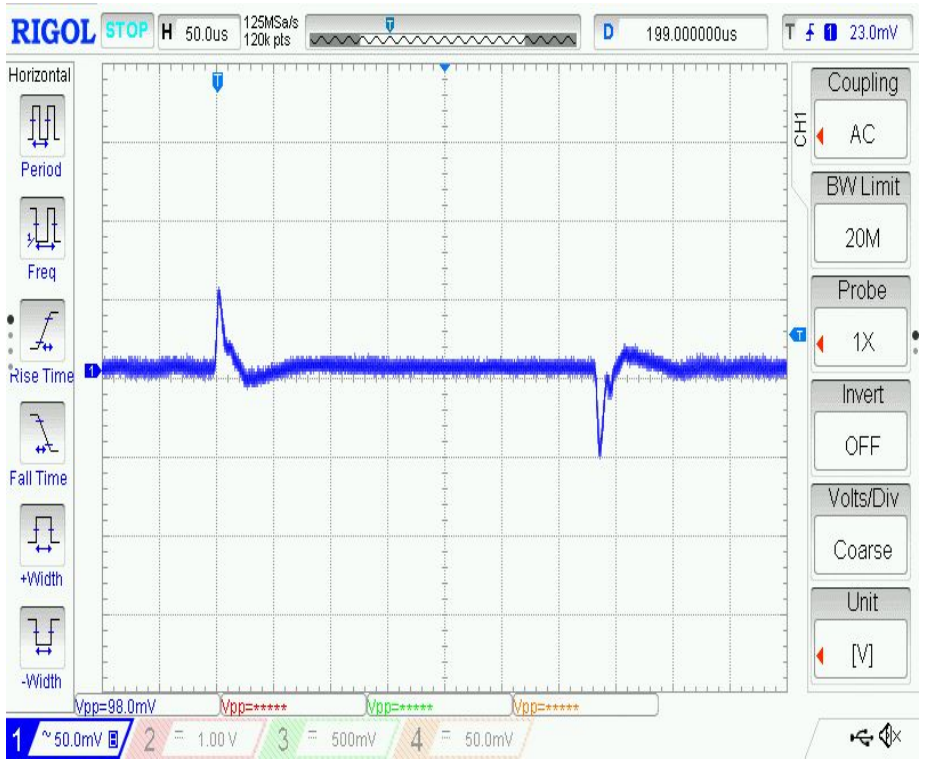
VCCAUX
1.8 V / 4 A

- C200 Sync Buck
- Fsw = 0.571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

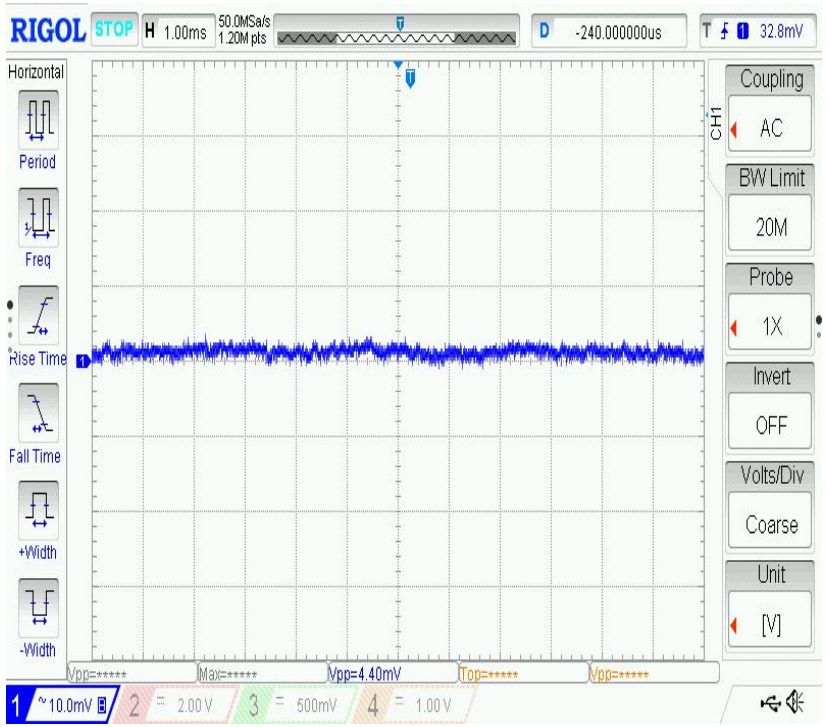
Efficiency & Transient





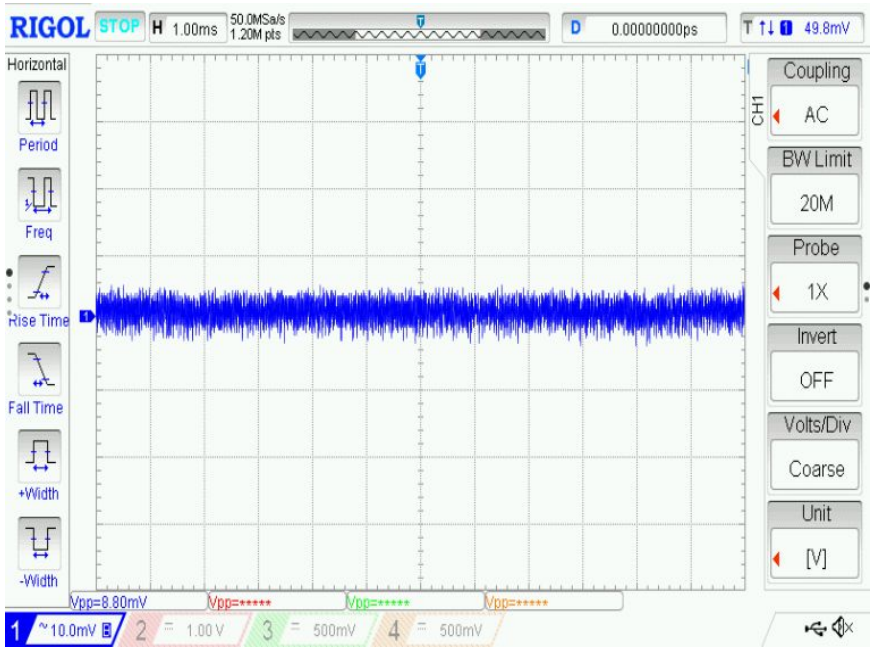
Vout = 1.8 V
Transient 0.3 A – 3 A @ 10 A/µs
V_{PP} = 98 mV
Fsw = 571 kHz
Lout = 1.1 µH, Cout = 3 x 47 µF

Ripple



No Load
V_{PP} = 4.4 mV

Vout = 1.8 V

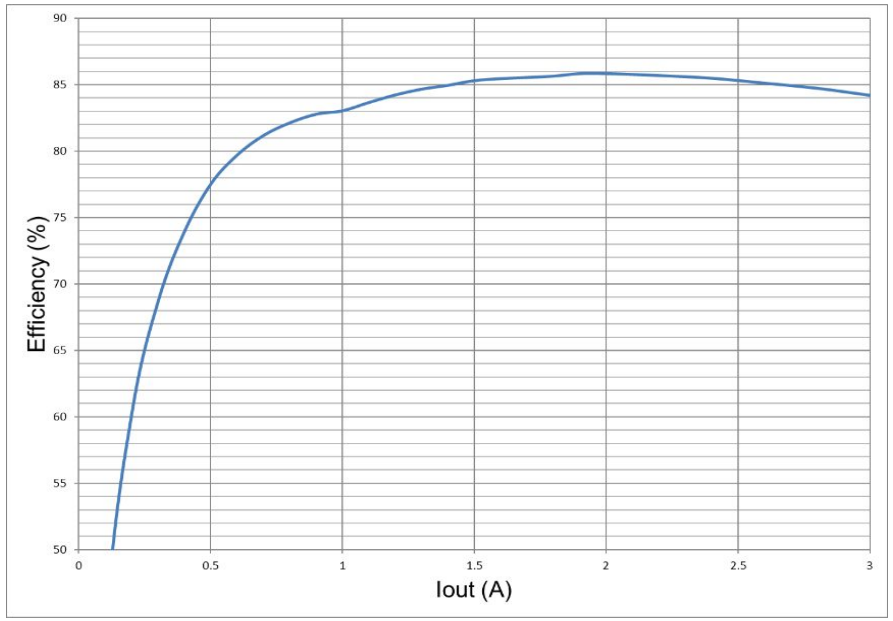


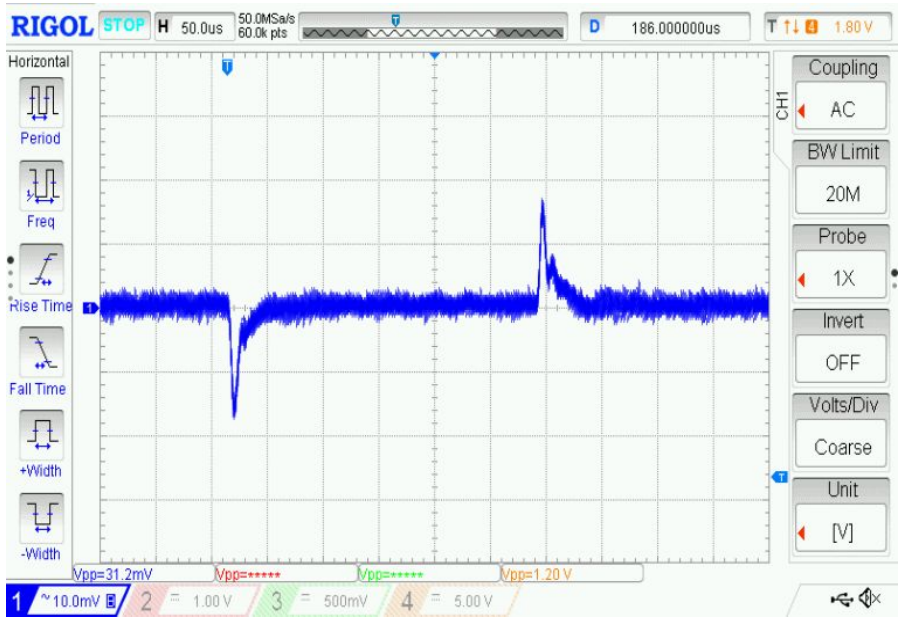
3 A Load
V_{PP} = 8.80 mV

MGTAVCC
1 V / 2 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1 µH, P/N Wurth 74438366010
- C = 4x47 uF

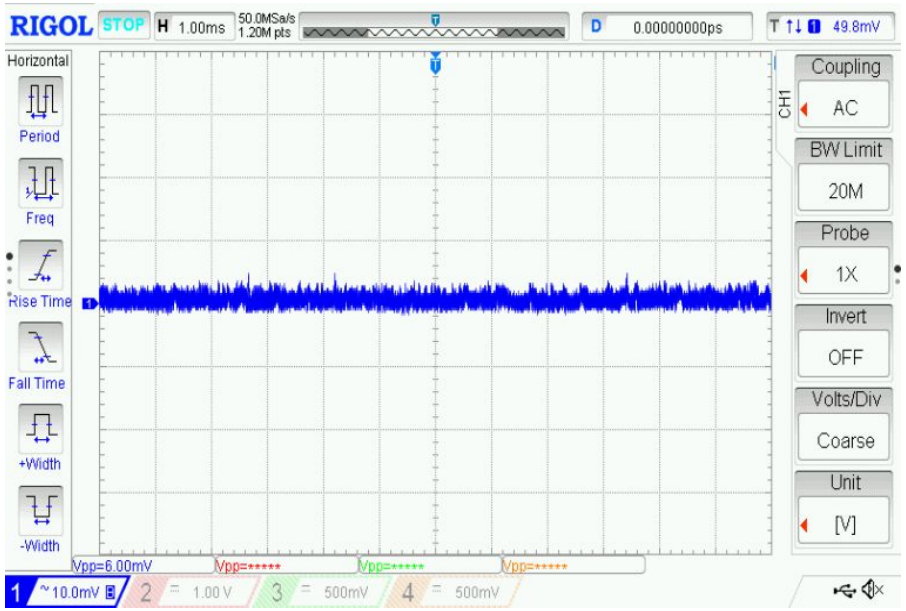
Efficiency & Transient





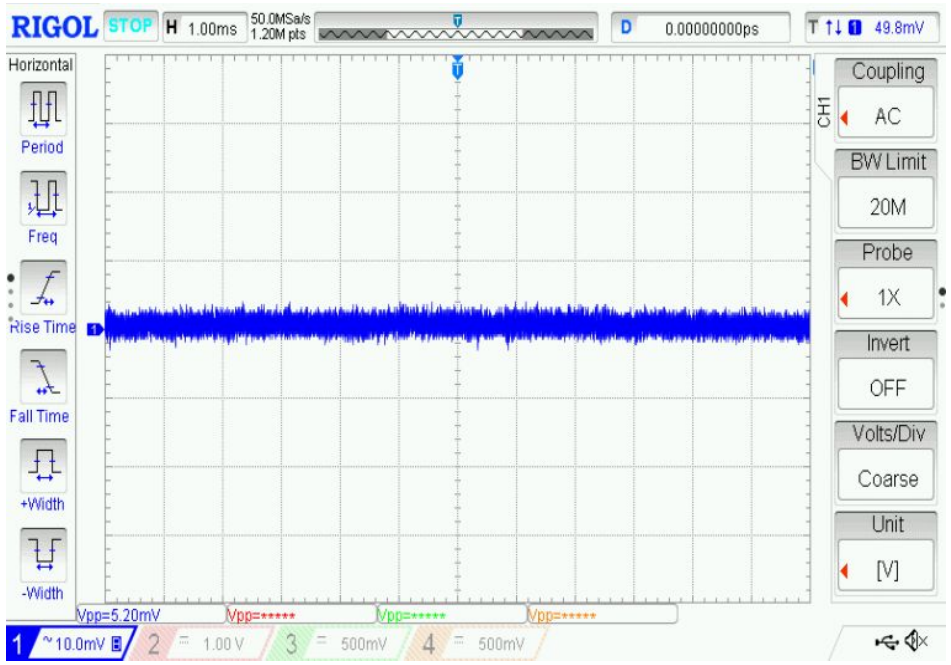
Vout = 1 V
Transient 2.25 A – 3 A @ 60 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

Ripple



No Load
V_{PP} = 6 mV

Vout = 1 V



3 A Load
V_{PP} = 5.2 mV

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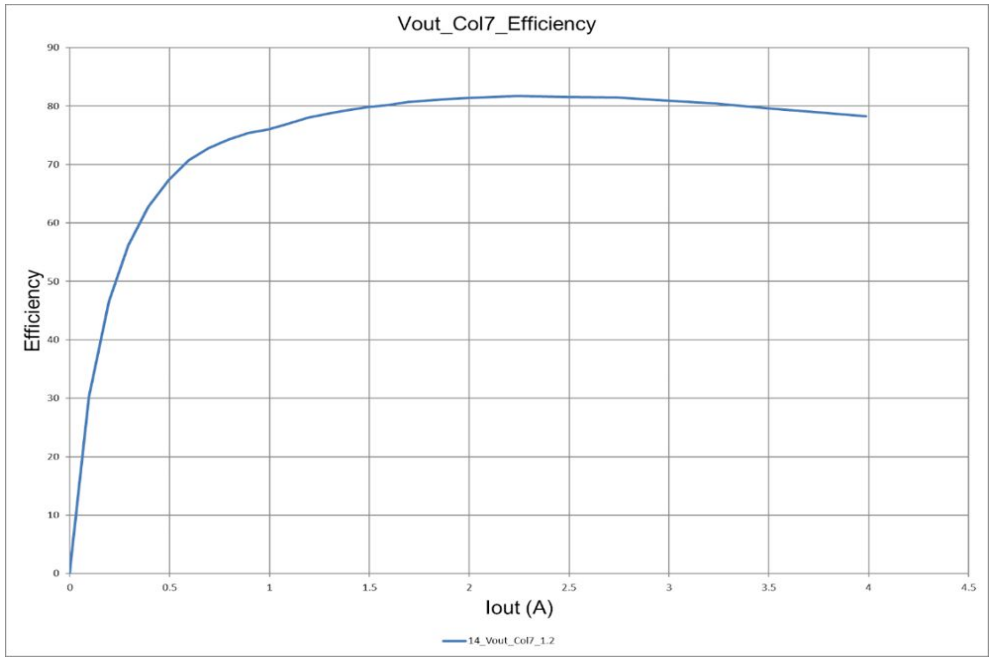
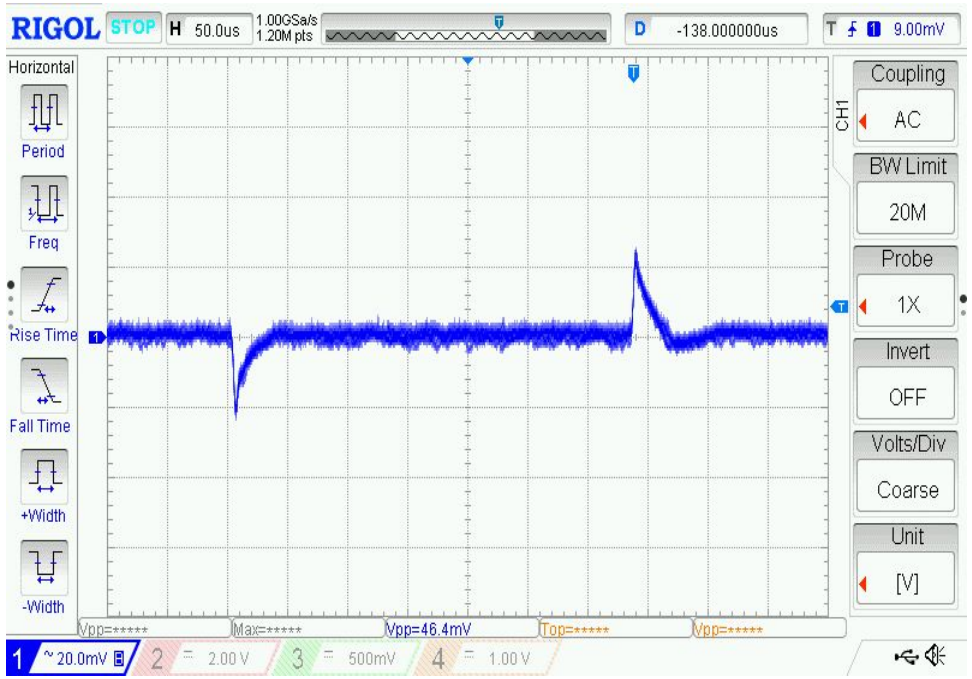
MGTAVTT
1.2 V / 4 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

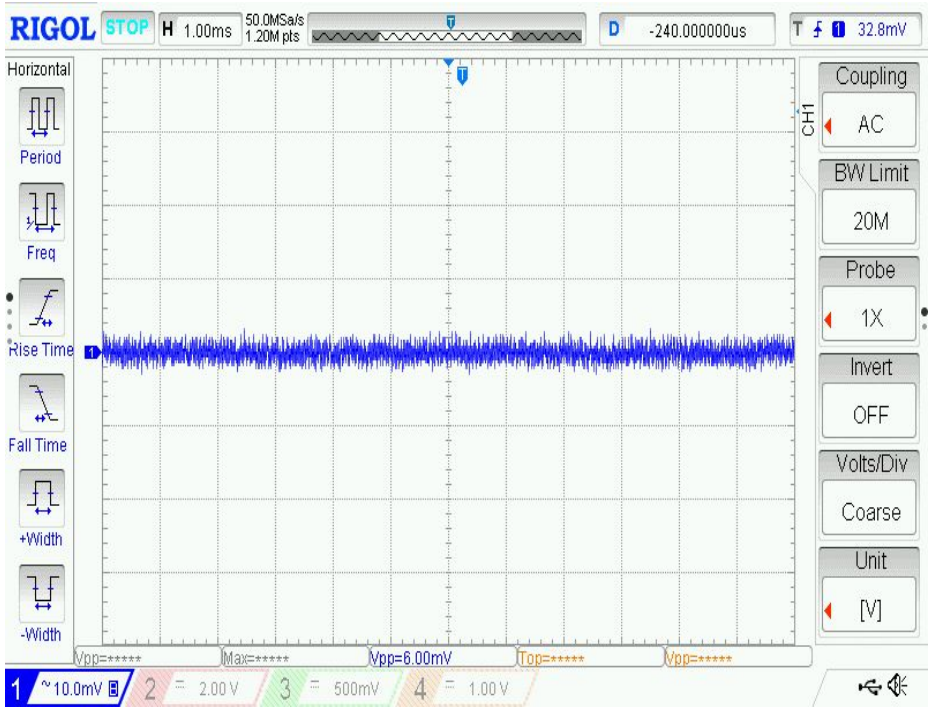
Efficiency & Transient





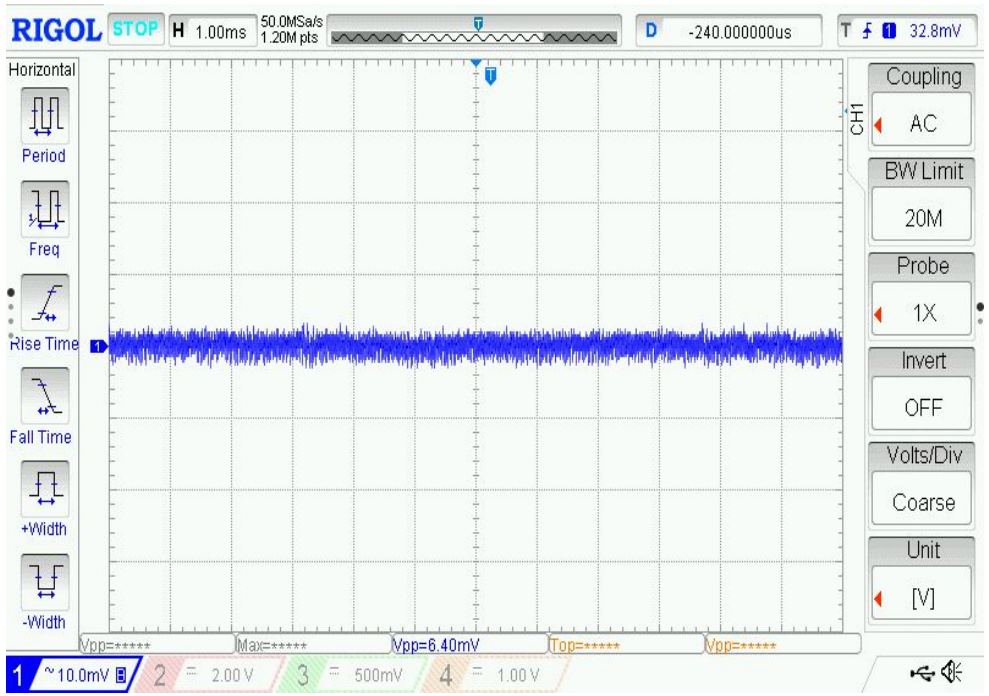
Vout = 1.2 V
Transient 0.8 A – 4A @10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



4 A Load
V_{PP} = 6.40 mV

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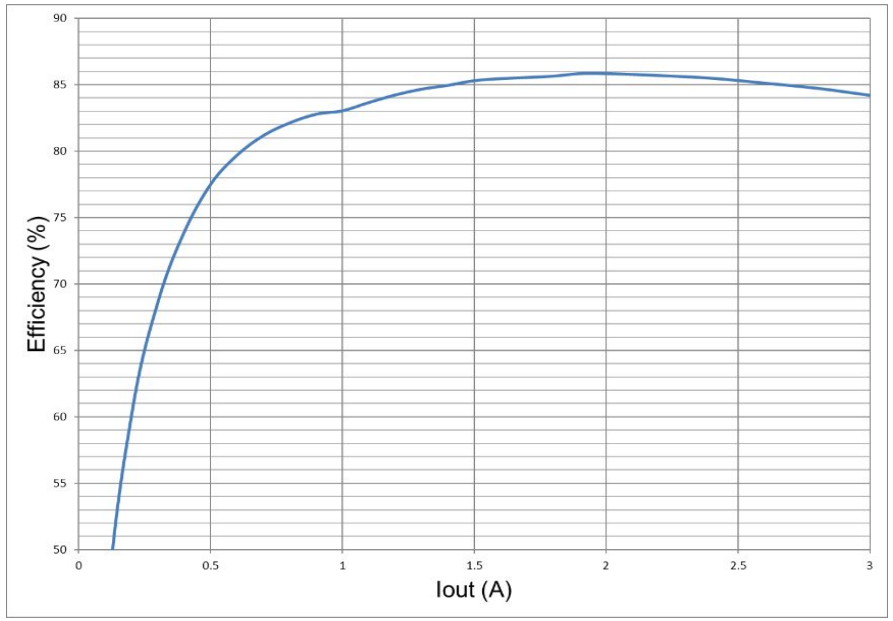
VCCO_1P2V
1.2 V / 2 A

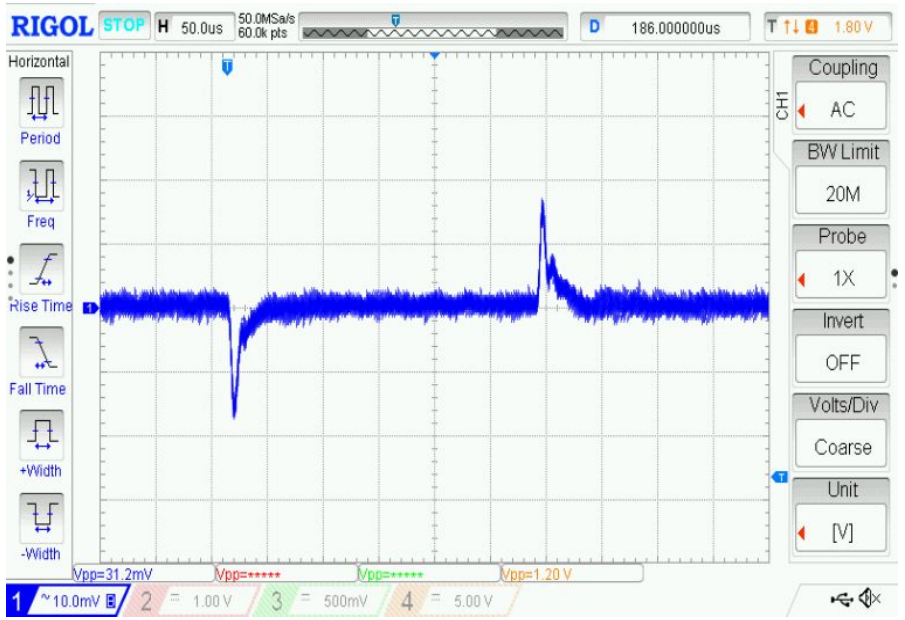
- C750 Load Switch

DDR_VPP
1.2 V / 2 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1 µH, P/N Wurth 74438366010
- C = 4x47 uF

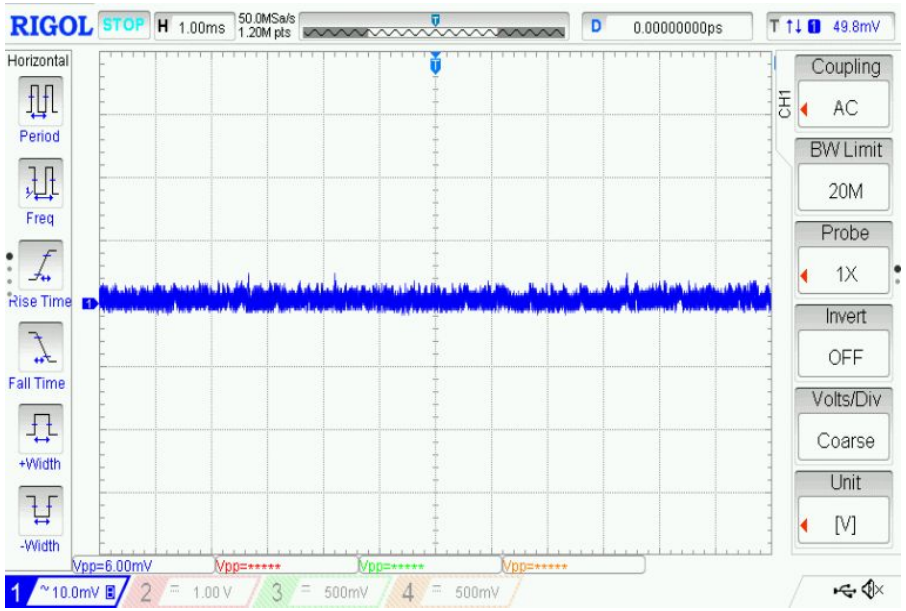
Efficiency & Transient





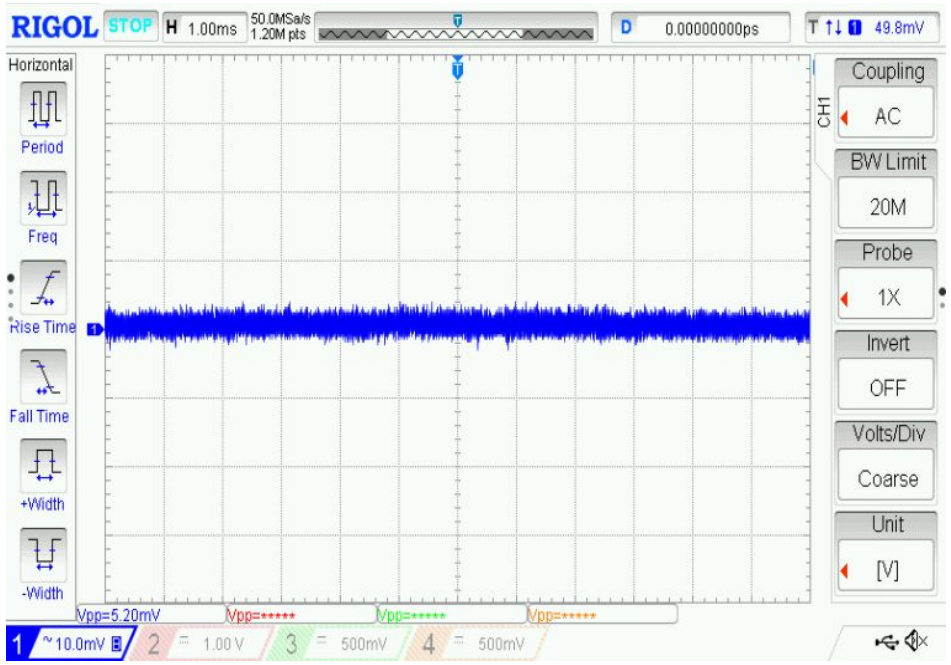
Vout = 1.2 V
Transient 2.25 A – 3 A @ 60 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



3 A Load
V_{PP} = 5.2 mV

AnDAPT

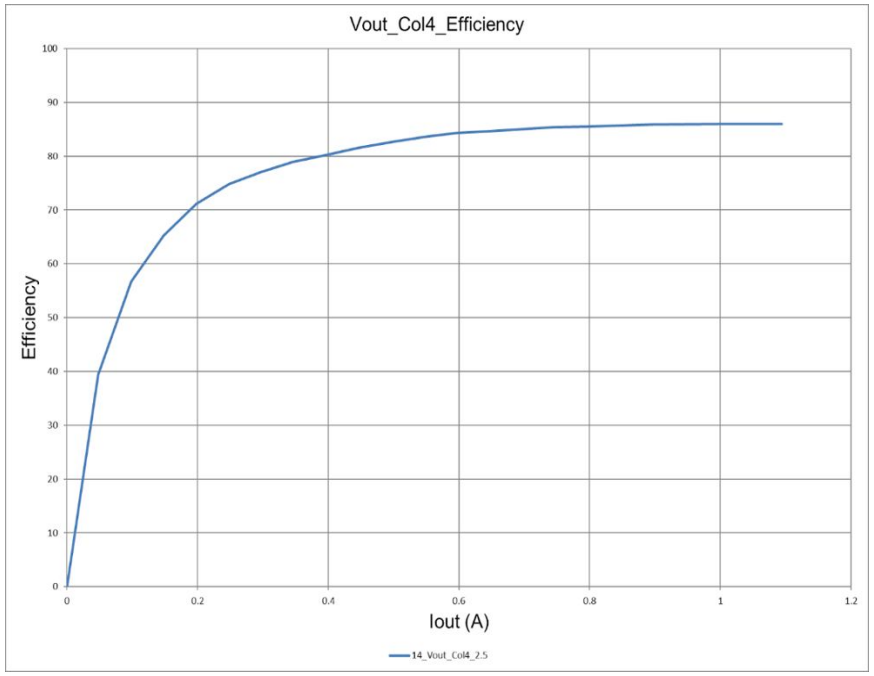
VCCO_1P2V
1.2 V / 2 A

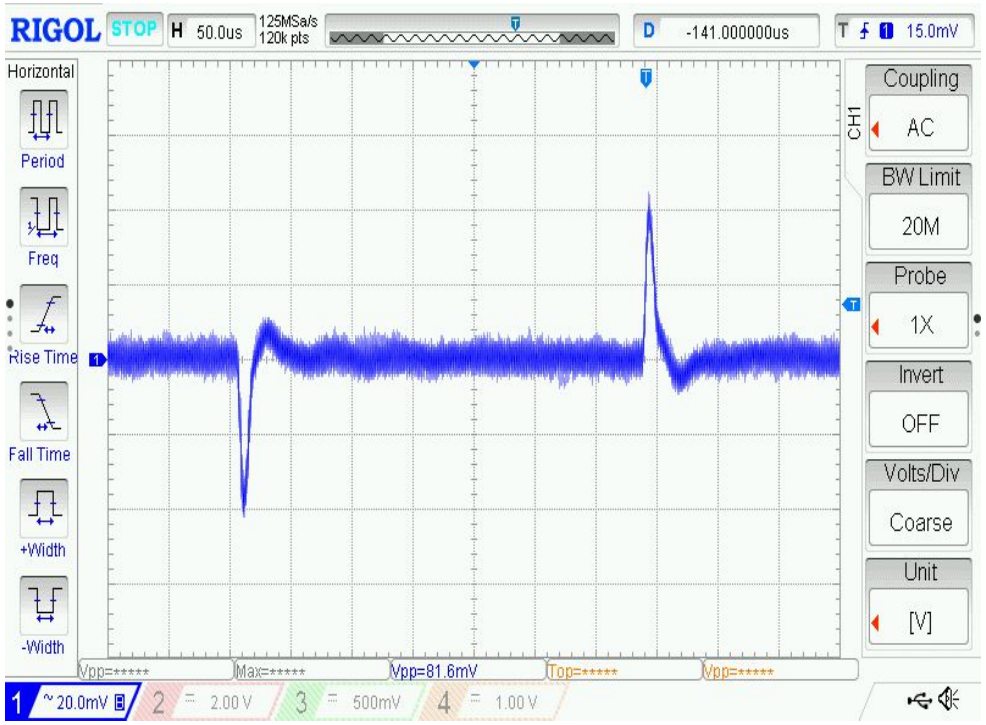
- C750 Load Switch

DDR4_VPP
2.5 V / 0.25 A

- C200 Synch Buck
- Fsw = 571 kHz
- L = 4.7 µH, P/N Wurth 74438336047
- C = 47 uF

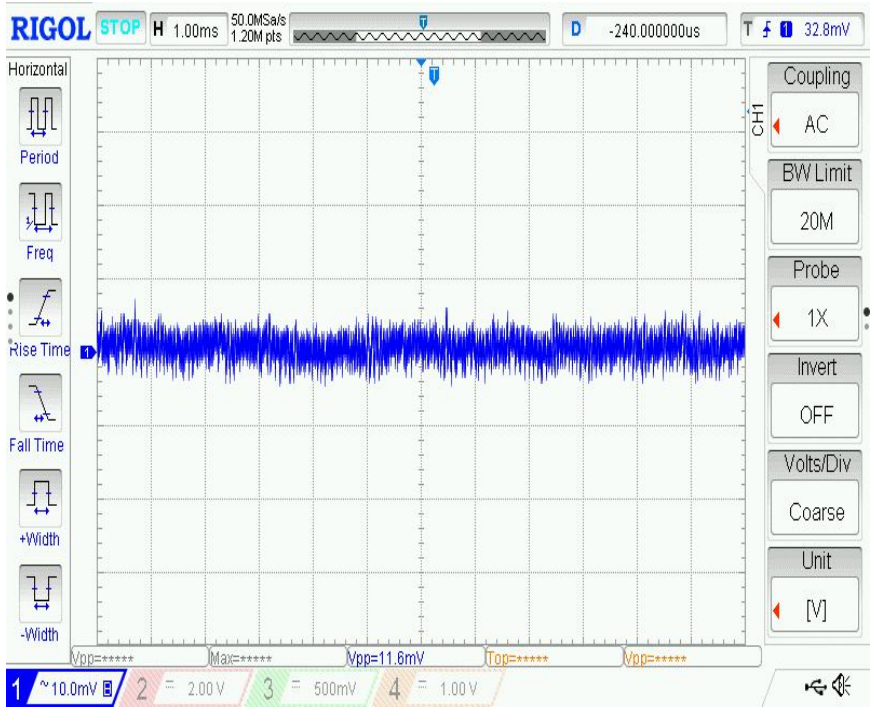
Efficiency & Transient





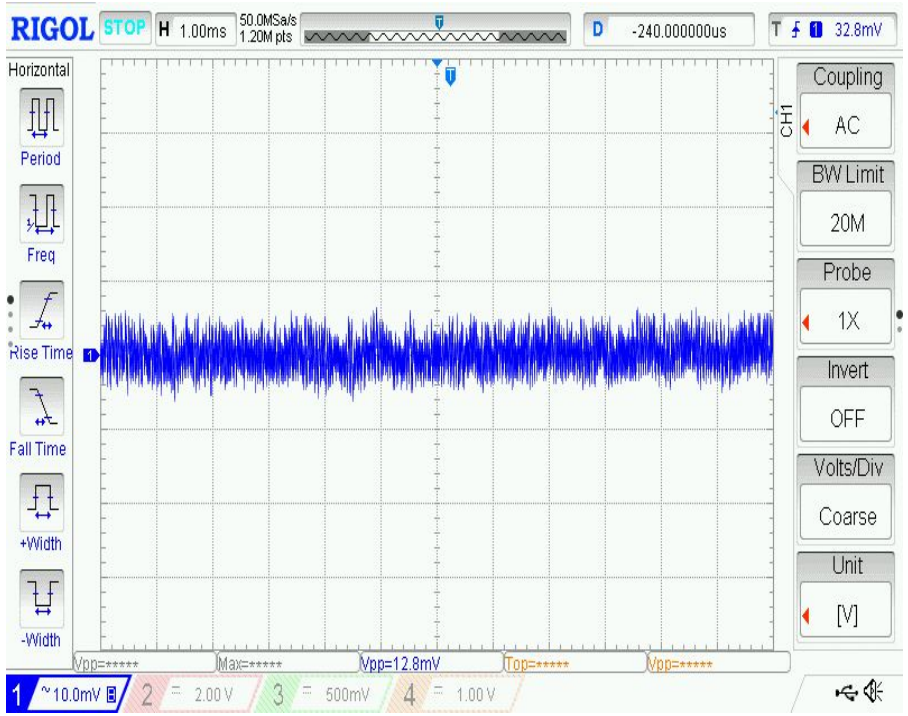
Vout = 2.5 V
Transient 0.2 A – 1A @ 10 A/µs
V_{PP} = 81.6 mV
Fsw = 571 kHz
Lout = 4.7 µH, Cout = 47 µF

Ripple



No Load
V_{PP} = 11.6 mV

Vout = 2.5 V

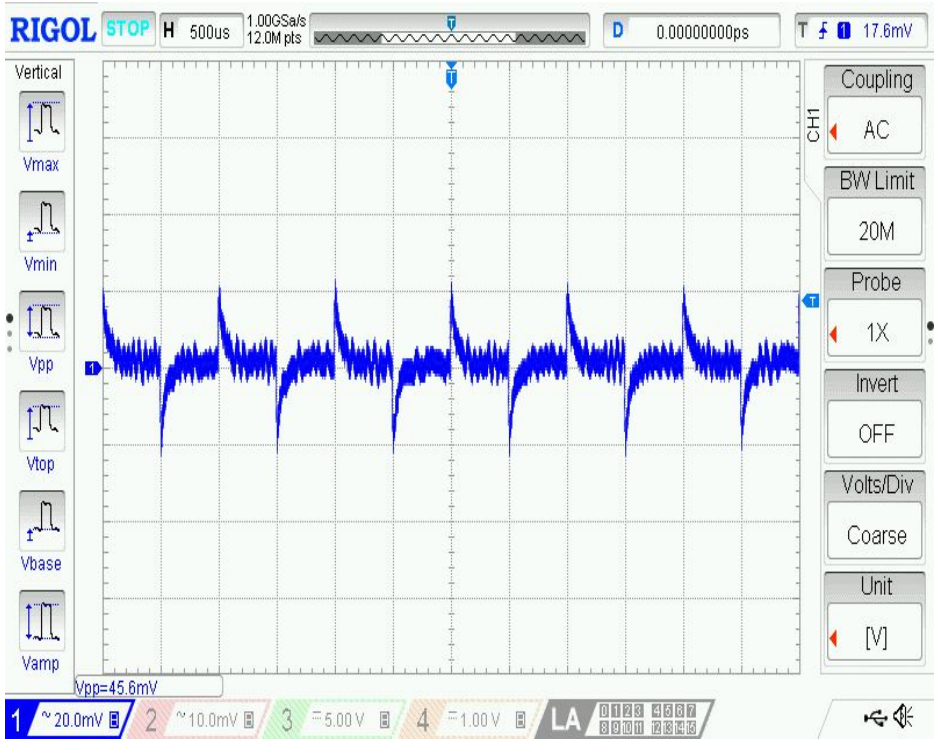


1 A Load
V_{PP} = 12.8 mV

UTIL_3P3V
3.3 V / 1 A

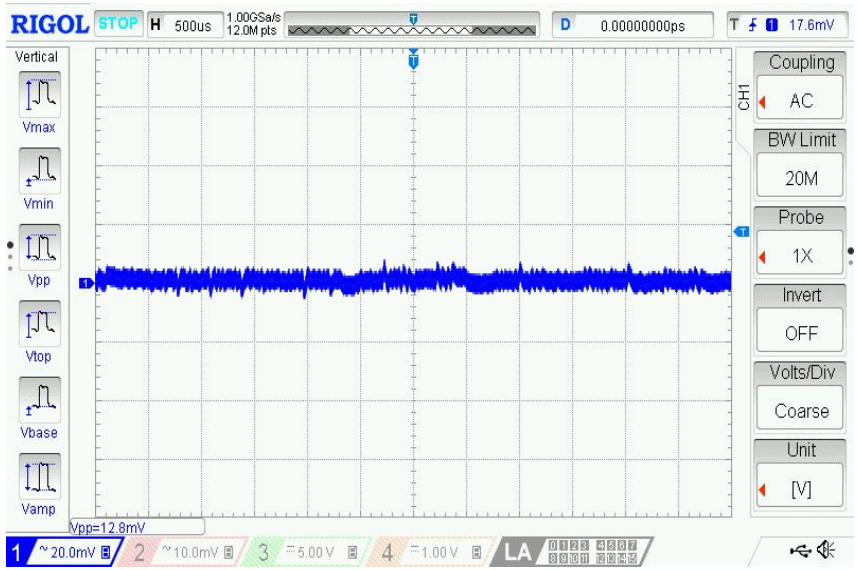
- C200 Synch Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 744314101
- C = 1x47 uF

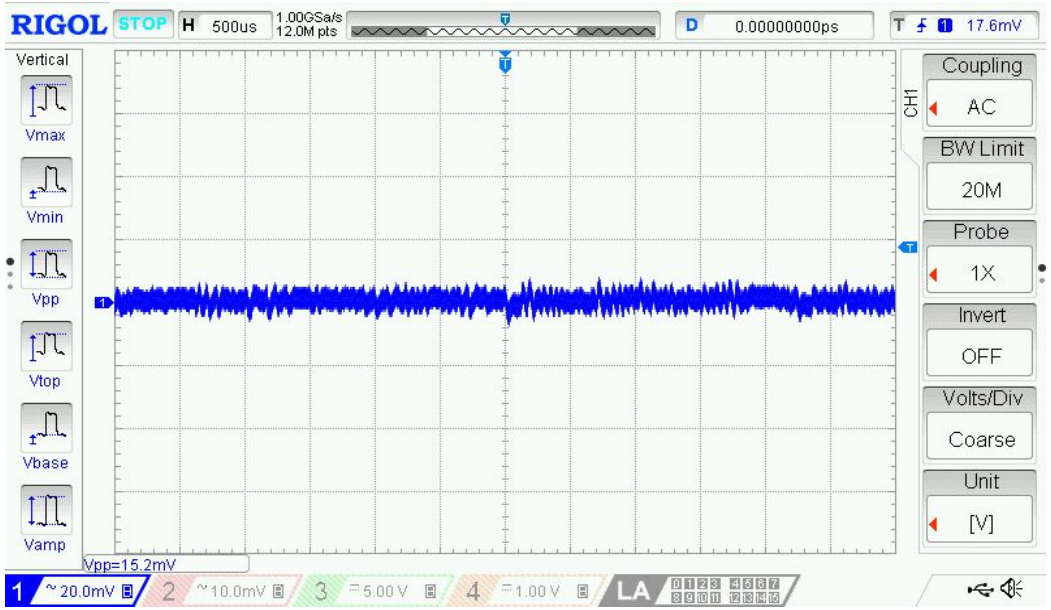
Efficiency & Transient



Vout = 3.3 V
Transient 0.75 A – 1A @ 2.5 A/µs
V_{PP} = 45.6 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1 x 47 µF

Ripple





No Load
V_{PP} = 12.8 mV

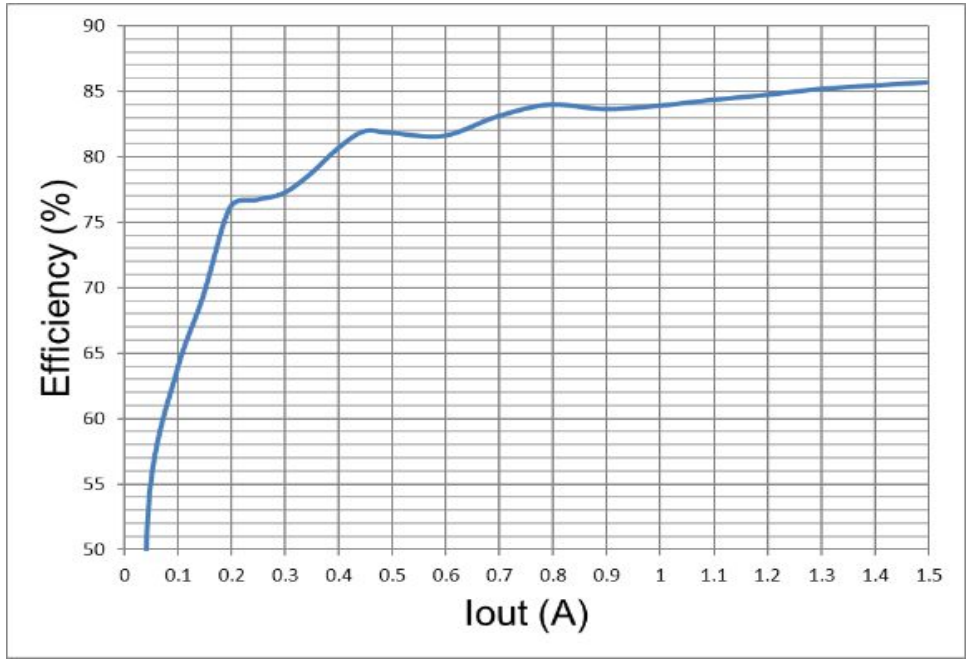
Vout = 3.3 V

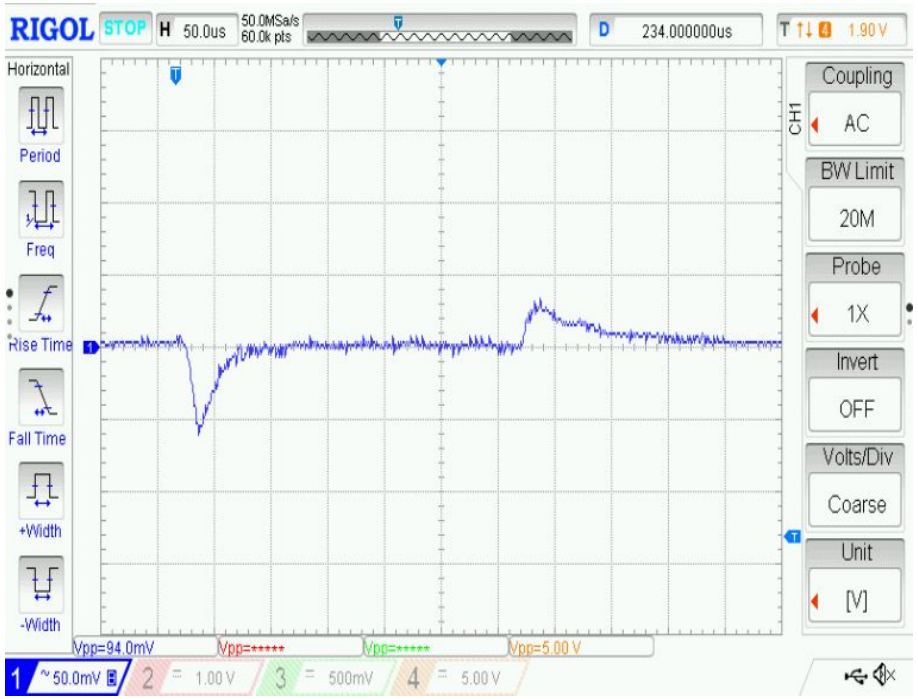
1 A Load
V_{PP} = 15.2 mV

UTIL_5V
5 V / 1 A

- C150 Asynch Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient

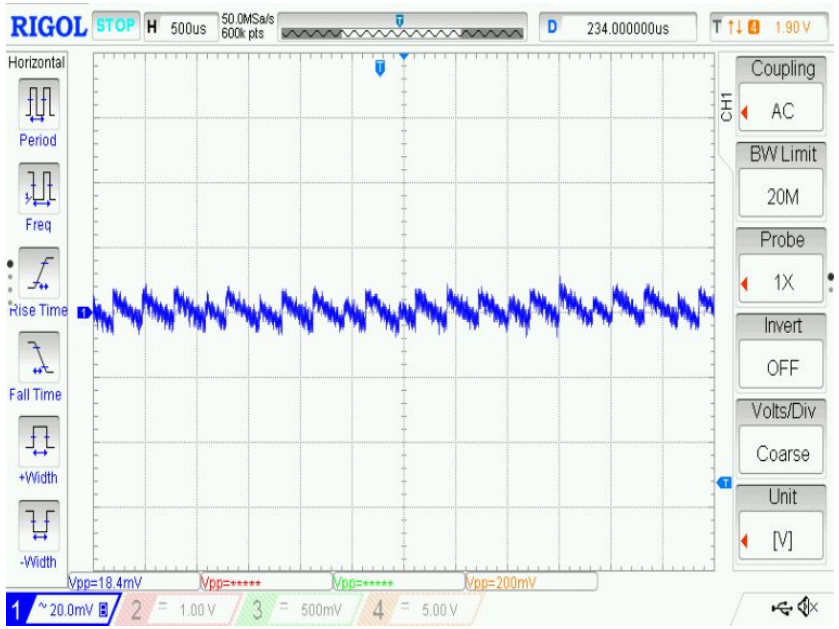




Vout = 3.3 V
Transient 0.15 A – 1.5A @ 2.5 A/µs
V_{PP} = 94 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

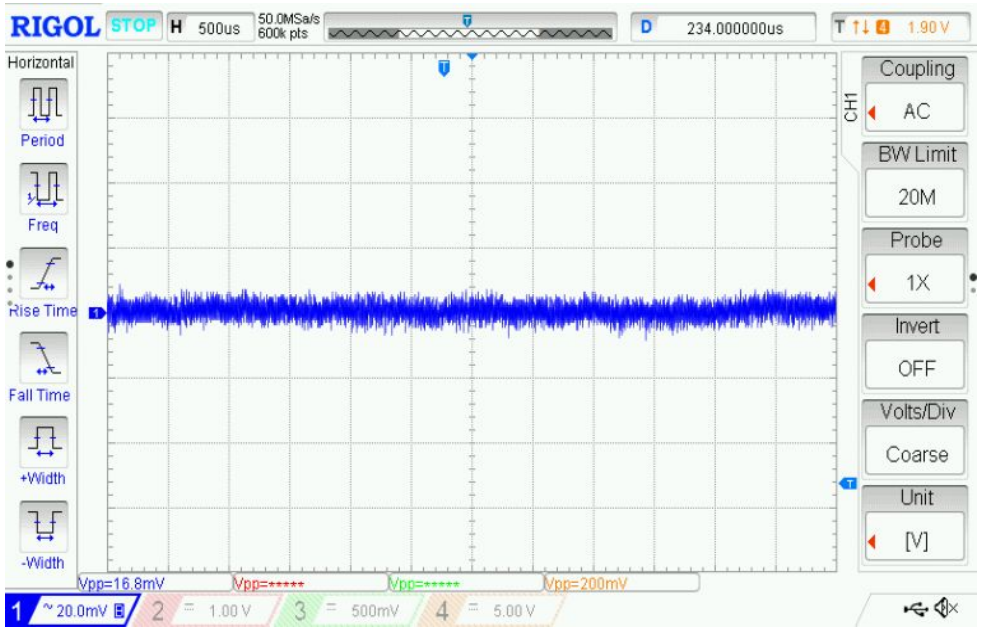
AnDAPT

Ripple



No Load
V_{PP} = 18.4 mV

Vout = 3.3 V



1.5 A Load
V_{PP} = 16.8 mV

AnDAPT

Thank You

AnDAPT