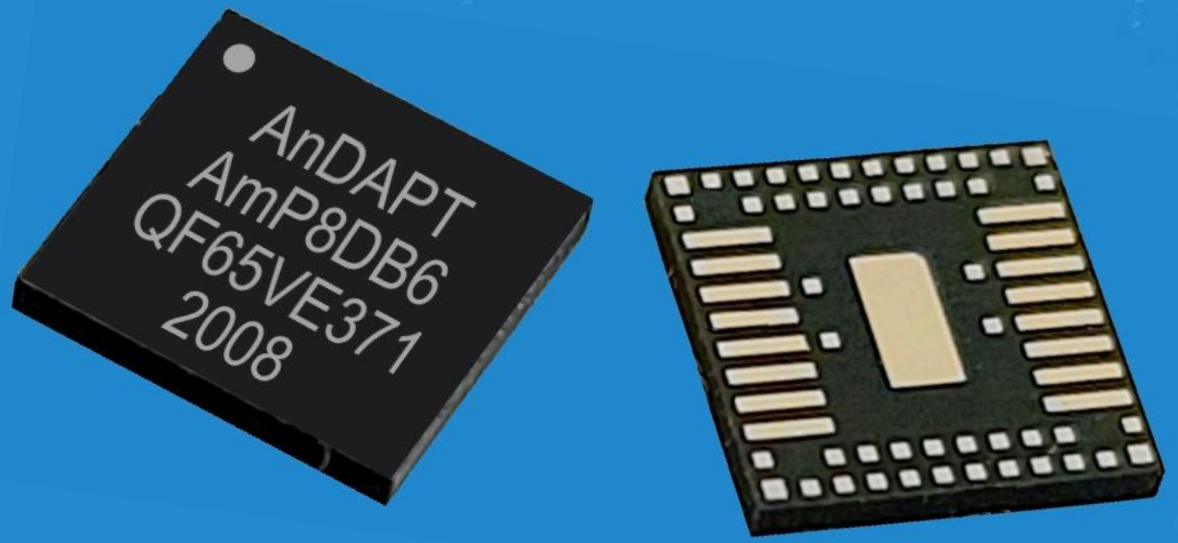


Xilinx Versal AI Core (Mid/High Voltage, Minimum Rails) Power Solution

Power Mapping

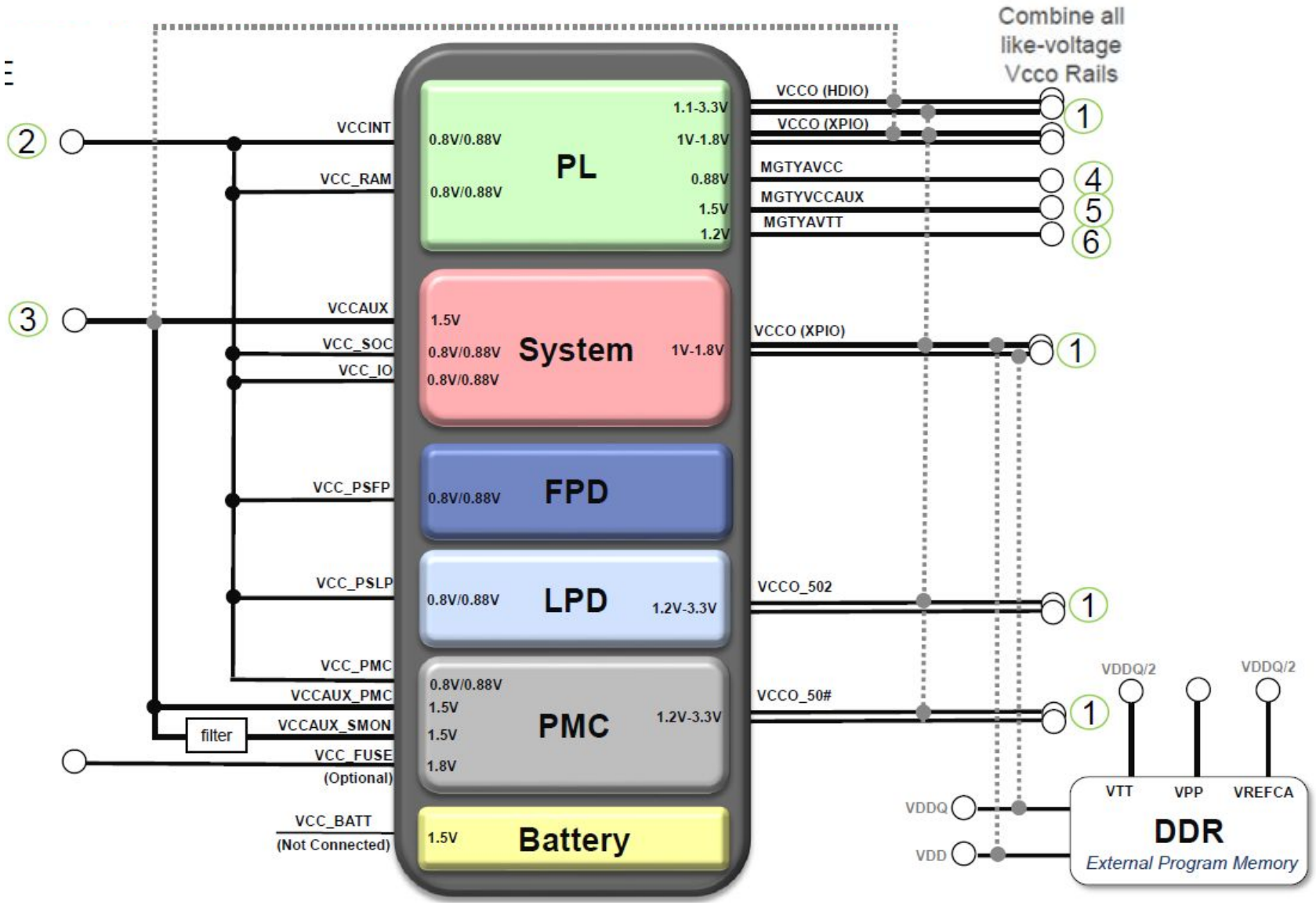
AnDAPT Marketing Team

AnDAPT

Versal AI Core Power Mapping Highlights

- Power tree mappings completed per data received from Xilinx Power Management team
- Both Typical and Upper use-cases are served by the same design
- Data gathered and bench tested by applications team at AnDAPT
  - Data meets or exceeds Xilinx power and timing specifications
- Total 9 power rails covered by 2x AmP ICs including memory and termination rails
- VCCINT (core rail) draws current from 132 A to 165 A and thus will be served using an external IC enabled/disabled by AmP IC
- Total solution area (excluding external core rail) is 1092.92 mm^2
- Presentation contains thermal views of both ICs

Xilinx Versal AI Core Power Tree



Versal AI Core Power Rails: Mid/High Voltage, Minimum Rails (Typical & Upper)

Sequence	Rail Name		AI Core	
		Voltage (V)	Typical (A)	Upper (A)
Rail 1	VCCINT/VCCINT_IO/VCCRAM, VCC_SOC, VCC_PSLP, VCC_PSFP, VCC_PMC	0.8V/0.88V	132.01	165.01
Rail 2	VCCAUX, VCCAUX_PMC, VCCAUX_SMON	1.5V	3.12	3.9
Rail 3	MGTAVCC	0.88V	2.47	3.08
Rail 4	MGTAVAUX	1.5V	0.23	0.29
Rail 5	MGTAVTT	1.2V	3.85	4.81
Rail 6	VCCO_PMIO[0…]	1.1V-3.3V, 1V-1.8V, 1.2V-3.3V	3.39	4.24
Current Total (A)			**138.52**	**173.15**

Power Tree Mapping: Versal AI Core (Mid/High Voltage, Minimum Rails)

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCO_XPIO (VCCO_XPIO, VCCO_HDIO)	1	Sync Buck	C200	PVIN	12	1.5	6	ARD_X_VRACRB_IC1
2	VCCO_502 (VCCO_502, VCCO_50X)	1	Sync Buck	C200	PVIN	12	1.5	4.3	
3	VCCINT (VCCINT, VCC_RAM, VCC_SOC, VCC_IO, VCC_PSFP, VCC_PSLP, VCC_PMC)	2	Ext IC	-	PVIN	12	0.8/0.88	165	
4	VCCAUX (VCCAUX, VCCAUX_PMC, VCCAUX_SMON)	3	Sync Buck	C200	PVIN	12	1.5	3.9 + 0.3	
5	MGTYAVCC	4	Sync Buck	C200	PVIN	12	0.88	3.1	
6	MGTYVCCAUX	5	LDO	C710	VCCAUX	1.5	0.88	0.3	ARD_X_VRACRB_IC2
7	MGTYAVTT	6	Sync Buck	C200	PVIN	12	1.2	4.9	
8	VDDQ	7	Sync Buck	C200	PVIN	12	1.2	3 + 2	
9	VTT	8	VTT Terminator	C210	VDDQ	1.2	0.6	2	

PVIN = 12V

Total estimated solution area = 1092.92 mm^2

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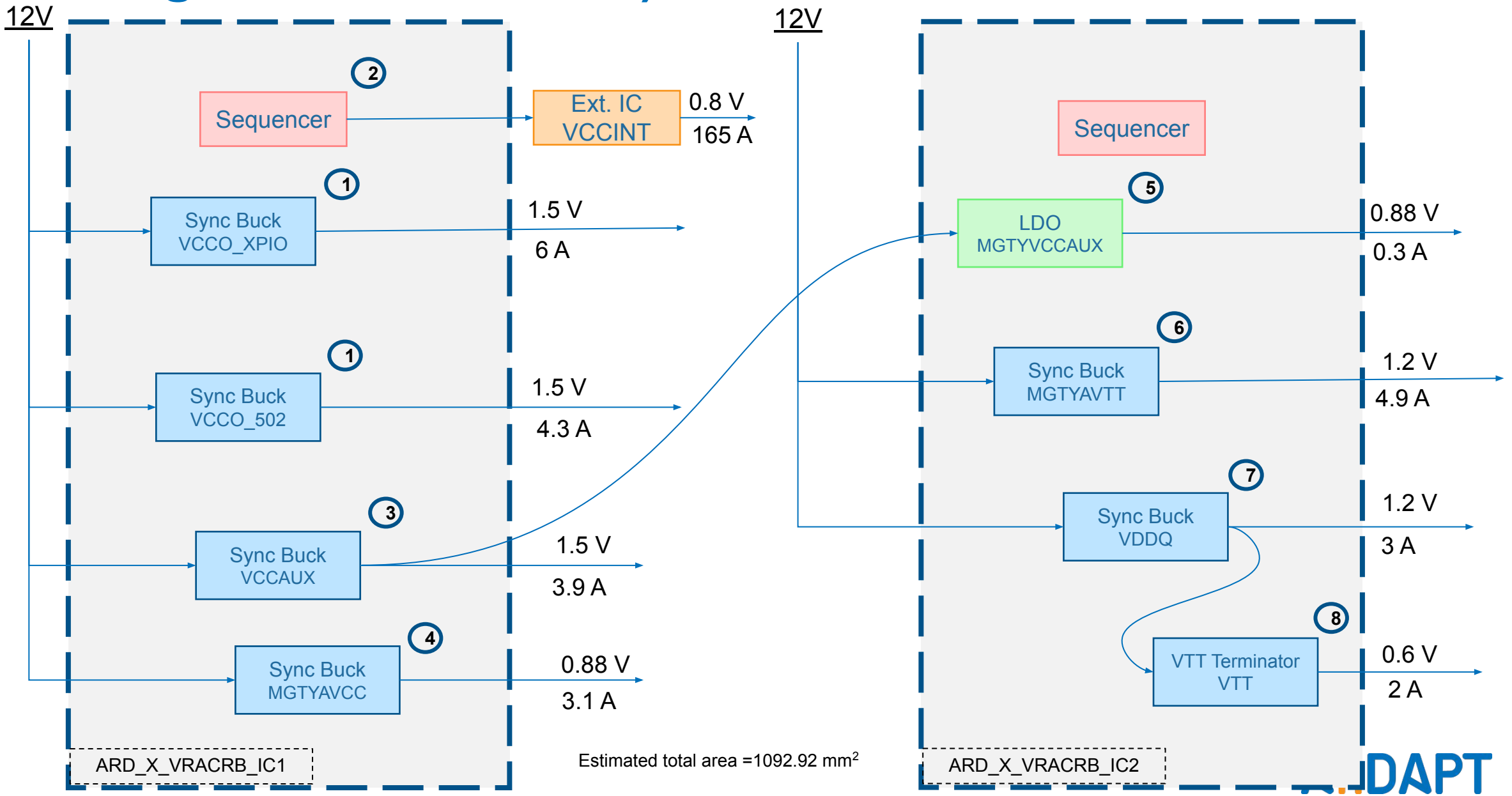
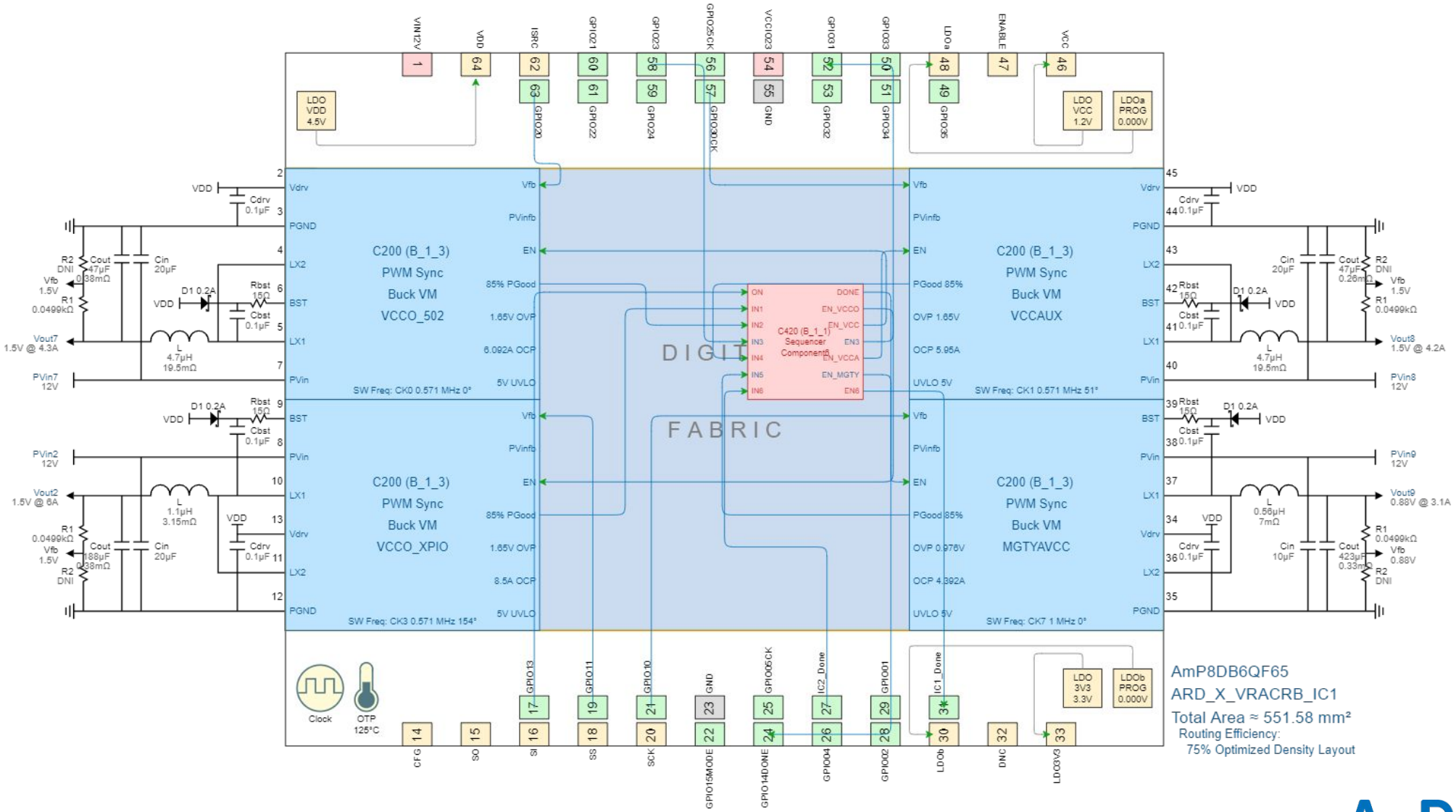
Power Tree Mapping: Versal AI Core (Mid/High Voltage, Minimum Rails)

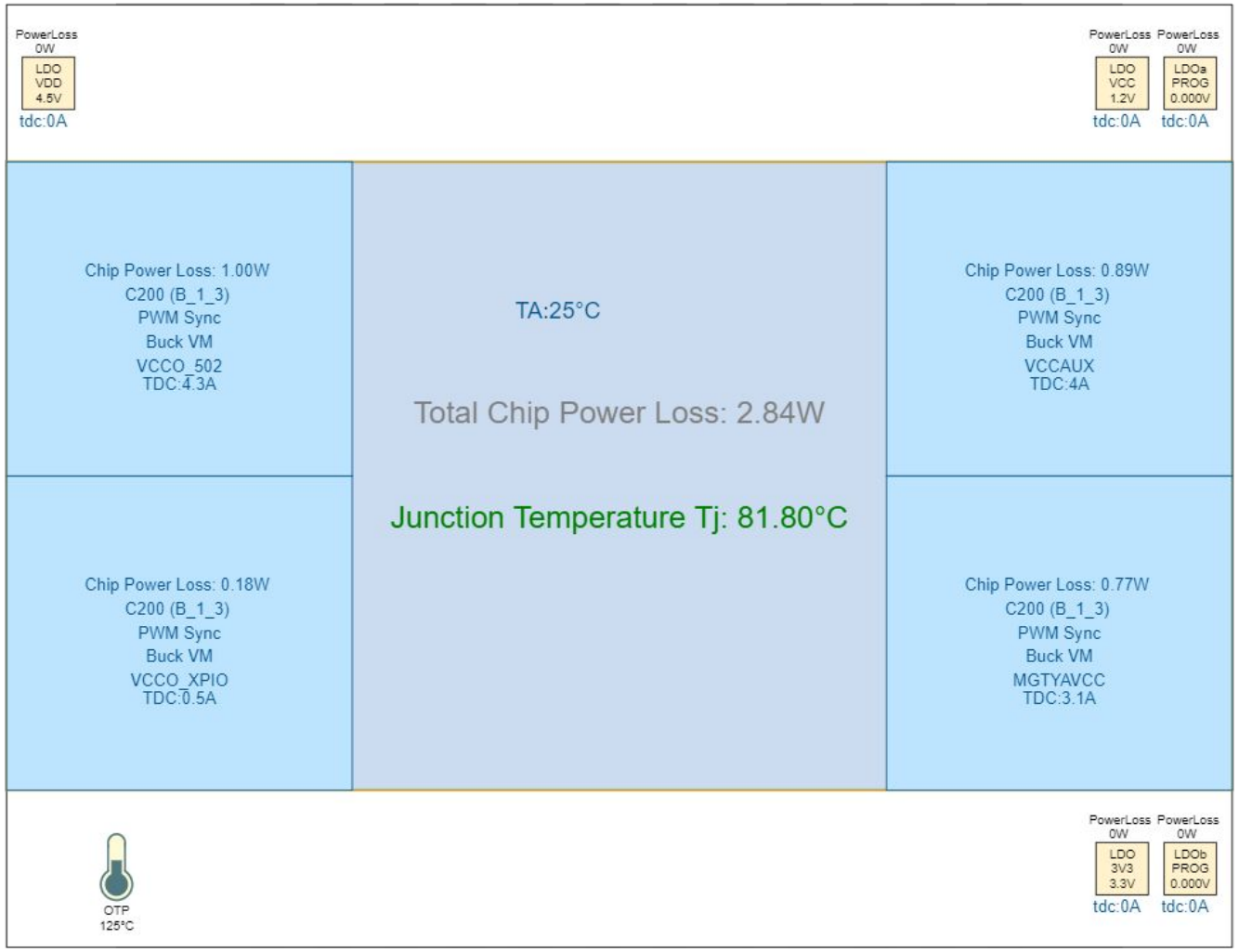


Estimated total area =1092.92 mm^2

Mapping (WebAmP View) Design –IC1

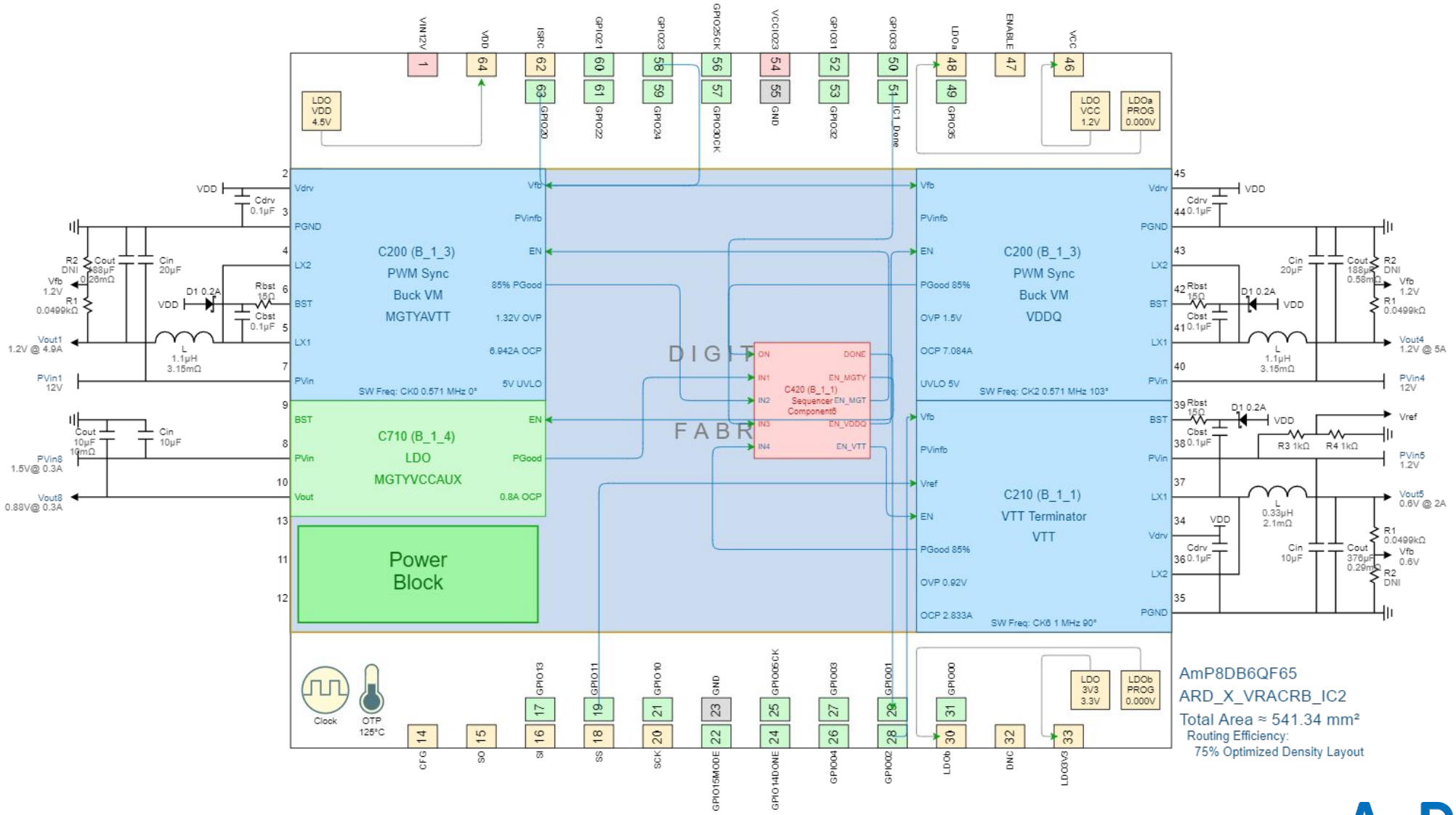


Mapping (Thermal View) –IC1

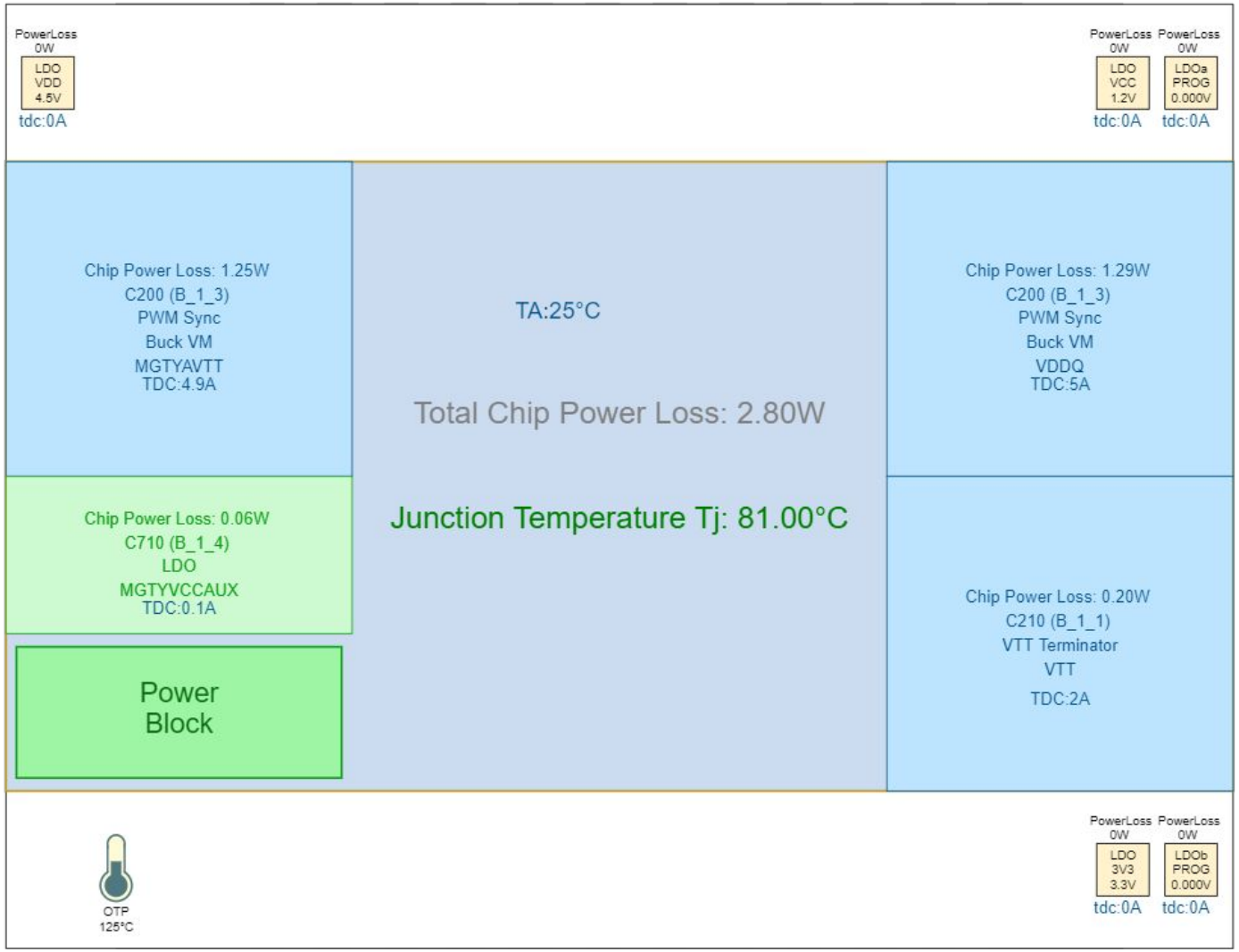


AmP8DB6QF65
ARD_X_VRACRB_IC1
Total Area ≈ 551.58 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (WebAmP View) Design –IC2

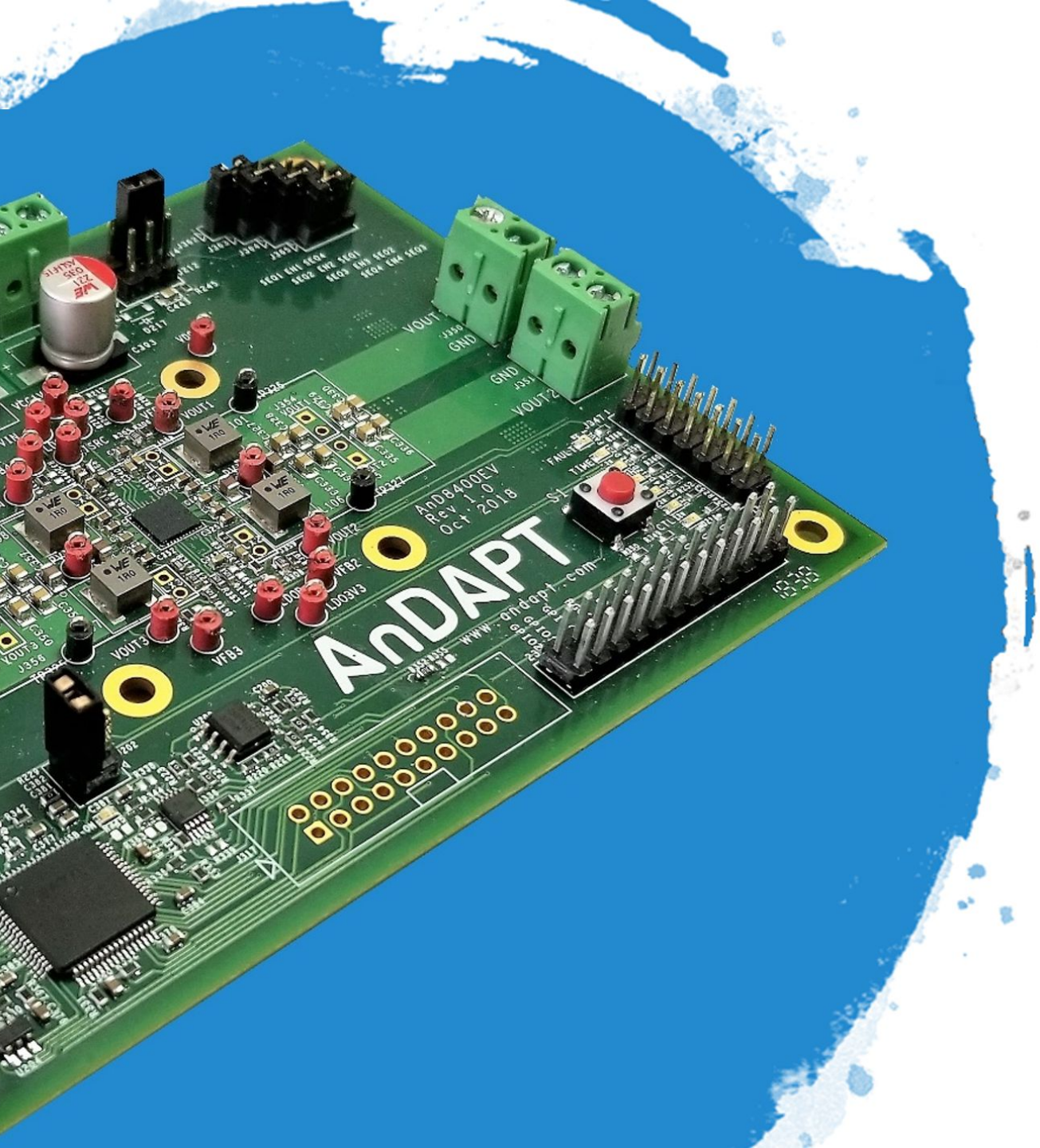


Mapping (Thermal View) –IC2



AmP8DB6QF65
ARD_X_VRACRB_IC2
Total Area ≈ 541.34 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT



Test Data

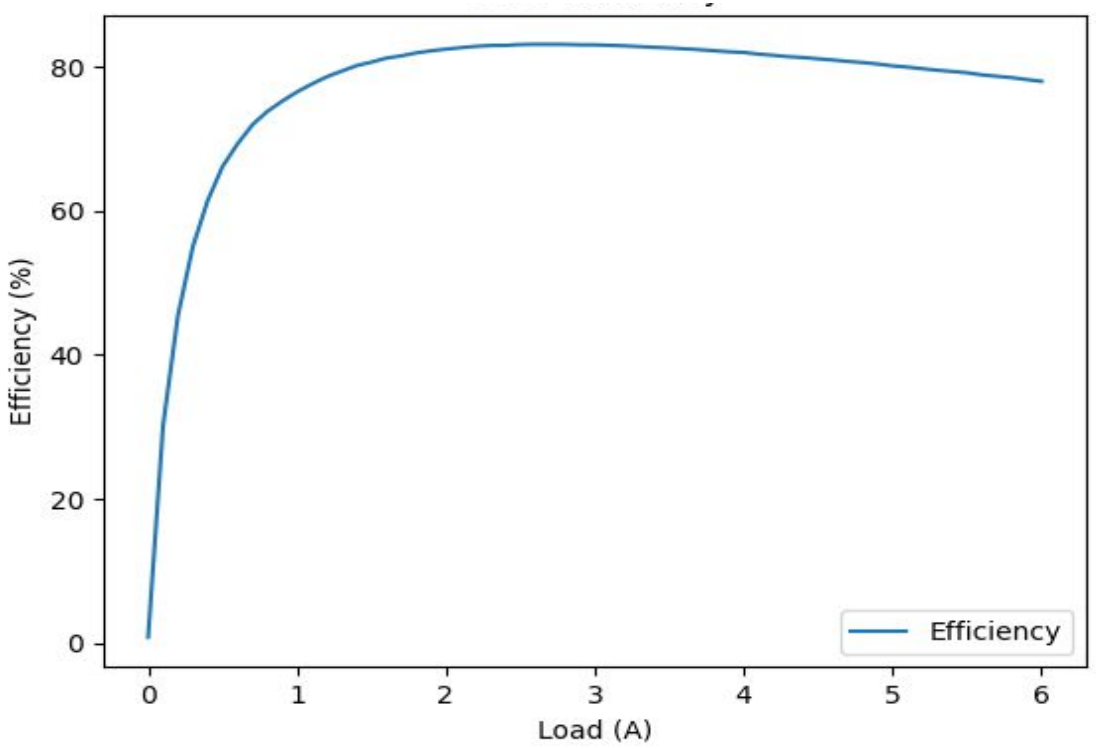
Versal AI Core

AnDAPT

VCCO_XPIO
1.5 V / 6 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 4x47 uF

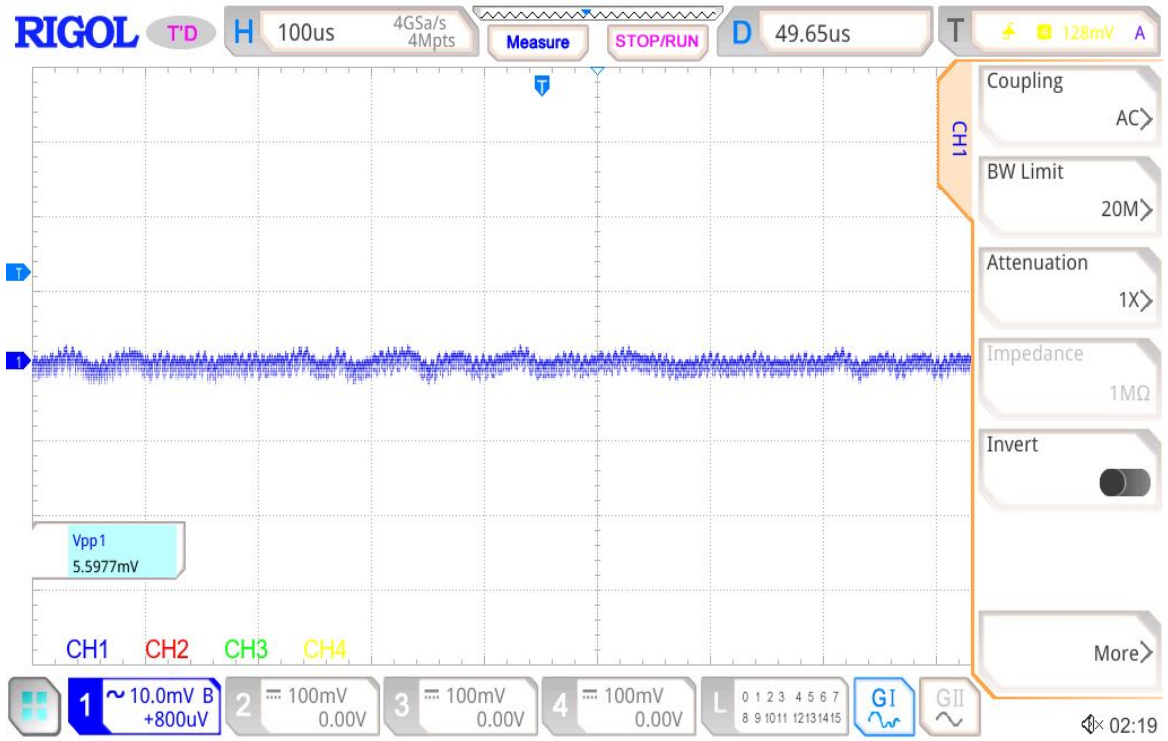
Efficiency & Transient



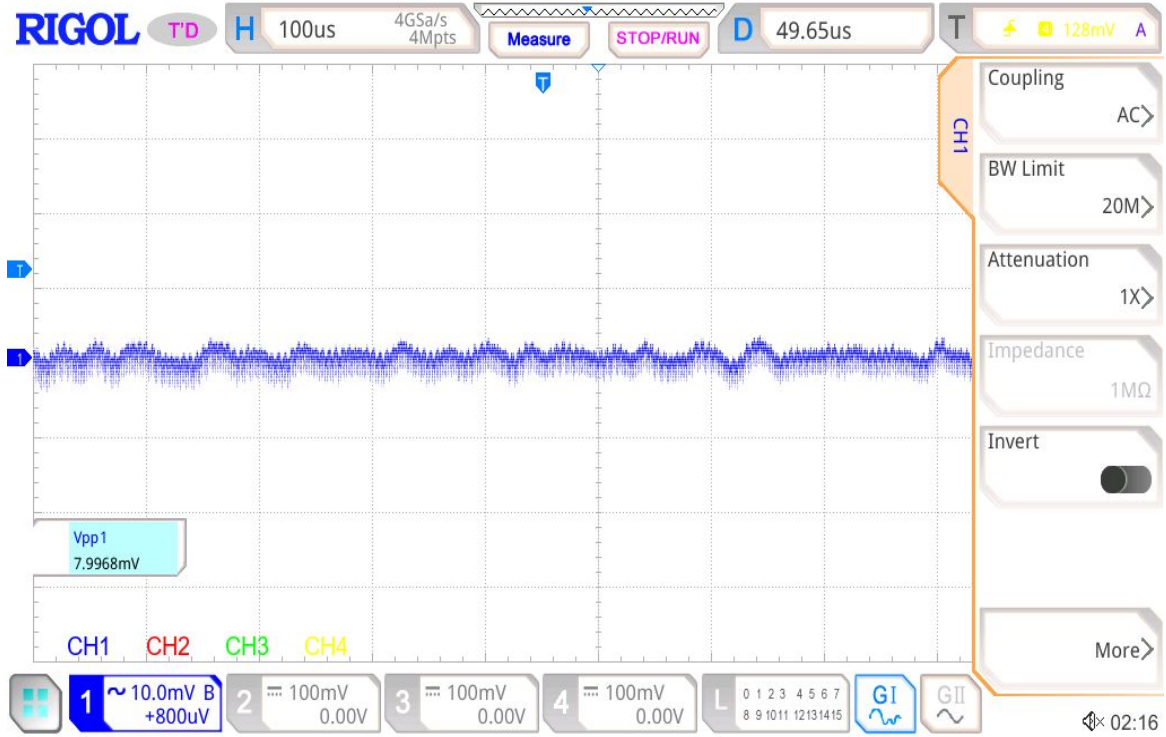
Vout = 1.5V
Transient 4.5 – 6 A@10 A/µs
V_{PP} = 27.18 mV
Fsw = 0.571 MHz
L = 1.1 µH, C= 4x47 uF

AnDAPT

Ripple



No Load
V_{PP} = 5.59 mV



Vout = 1.5 V

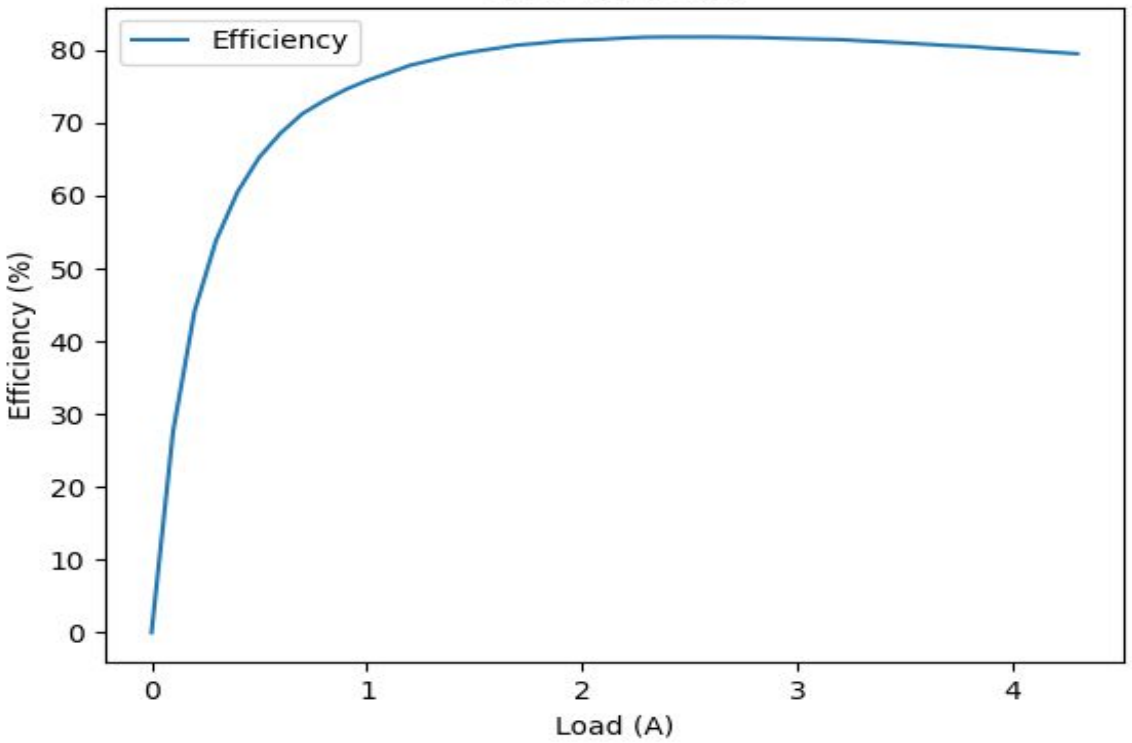
6 A Load
V_{PP} = 7.99 mV

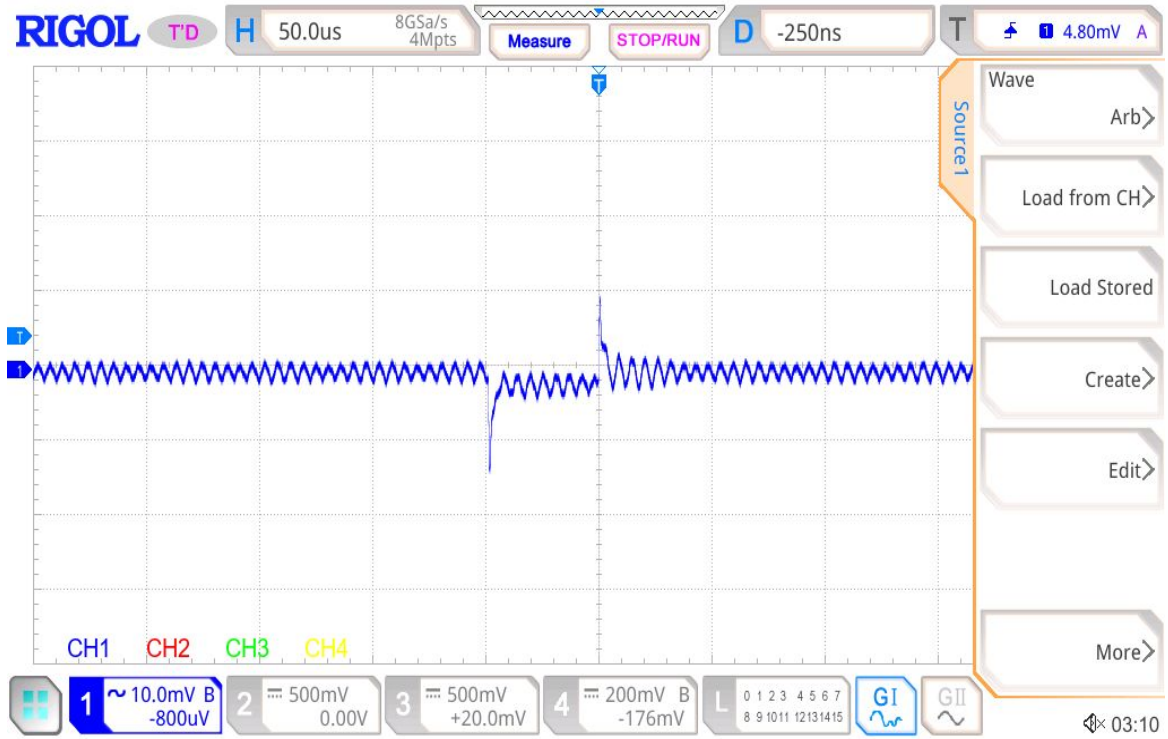
AnDAPT

VCCO_502
1.5 V / 4.3 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

Efficiency & Transient

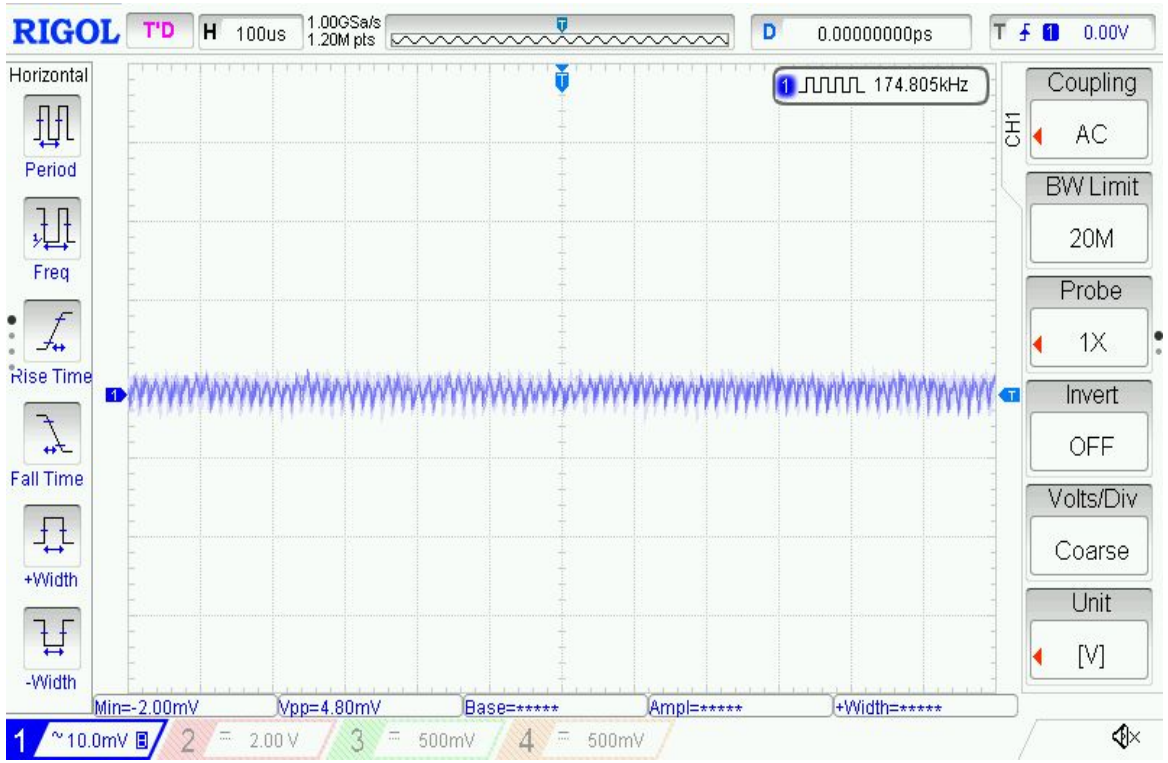




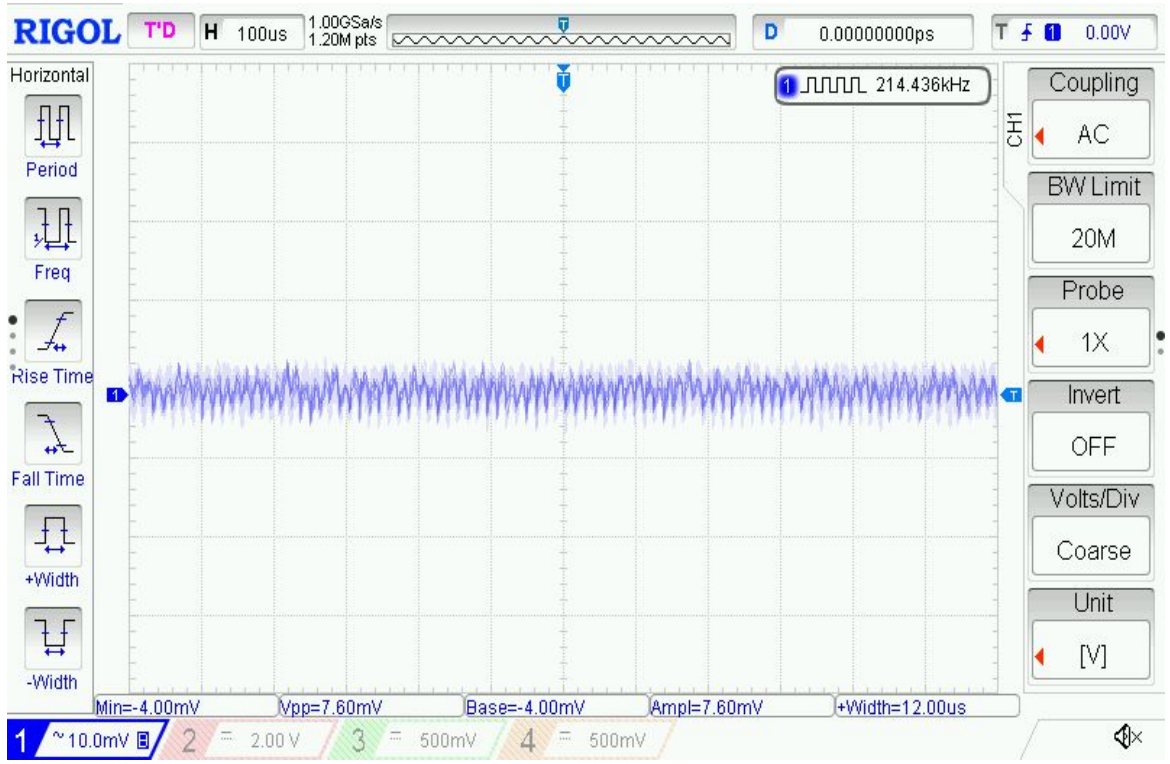
Vout = 1.5V
Transient 2.88A – 4.3A @ 10 A/µs
V_{PP} = 25 mV
Fsw = 0.571 MHz
L = 4.7 µH, C = 1x47 uF

AnDAPT

Ripple



No Load
V_{PP} = 4.80 mV



Vout = 1.5 V

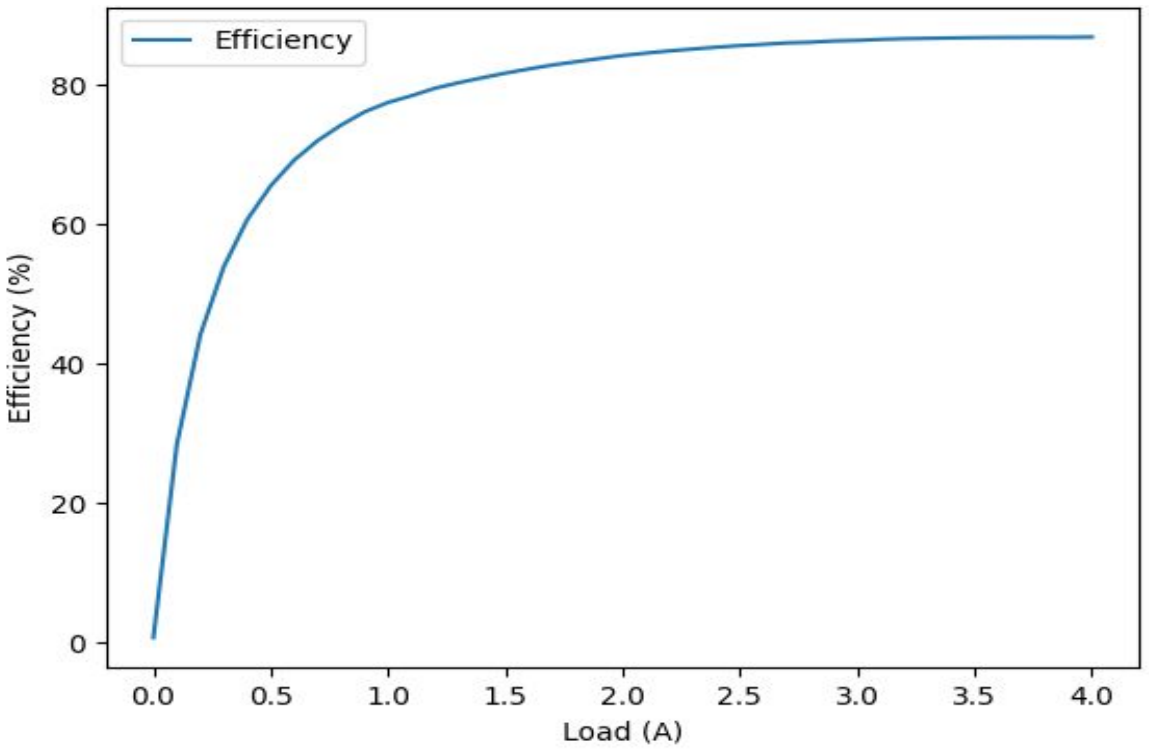
4.3 A Load
V_{PP} = 7.60 mV

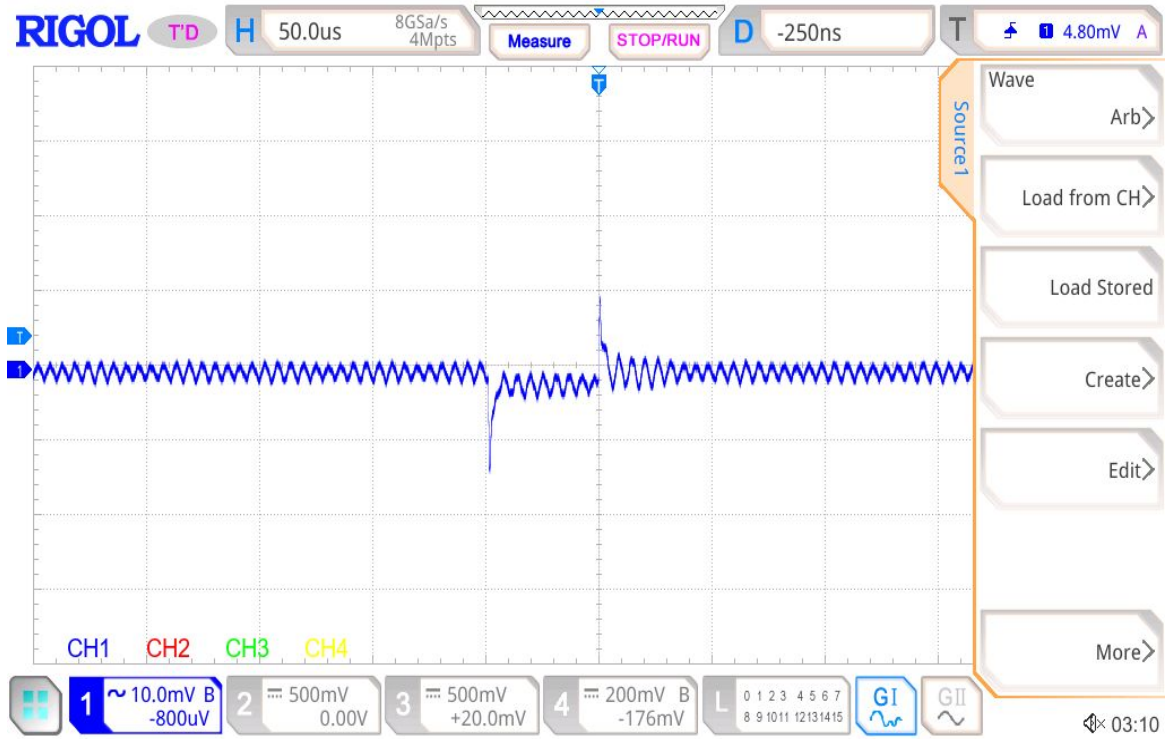
AnDAPT

VCCAUX
1.5 V / 4.2 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

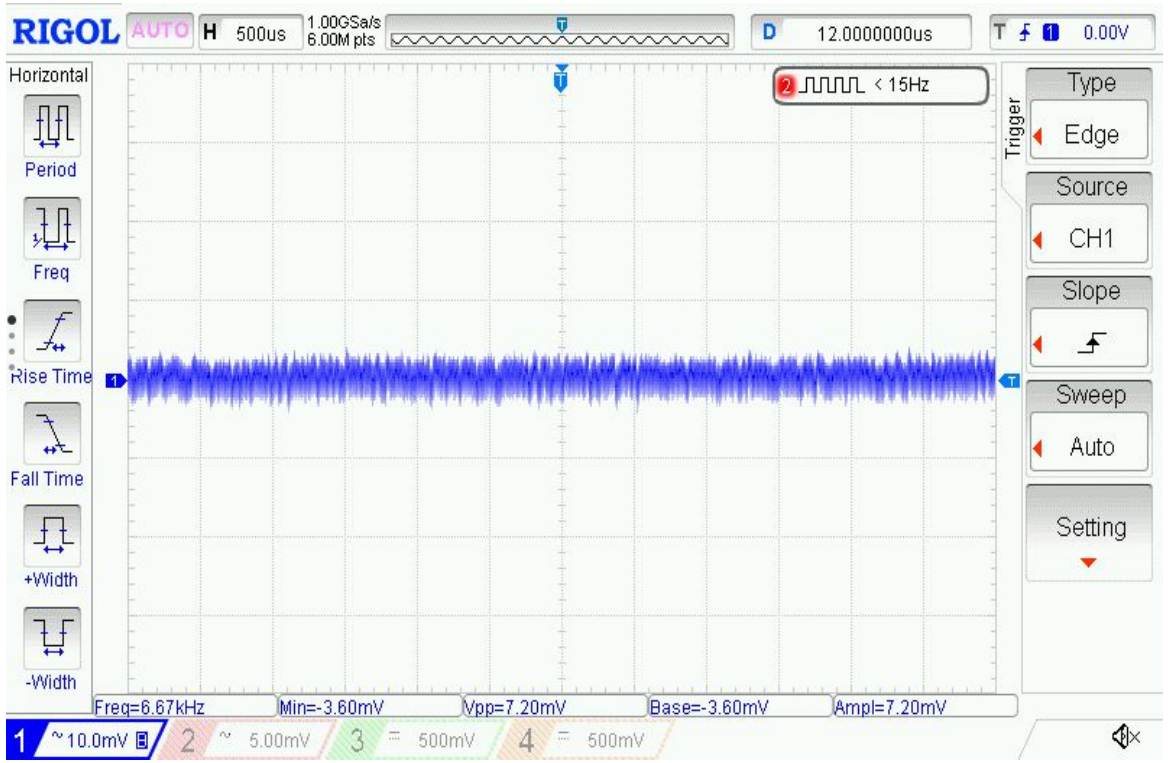
Efficiency & Transient

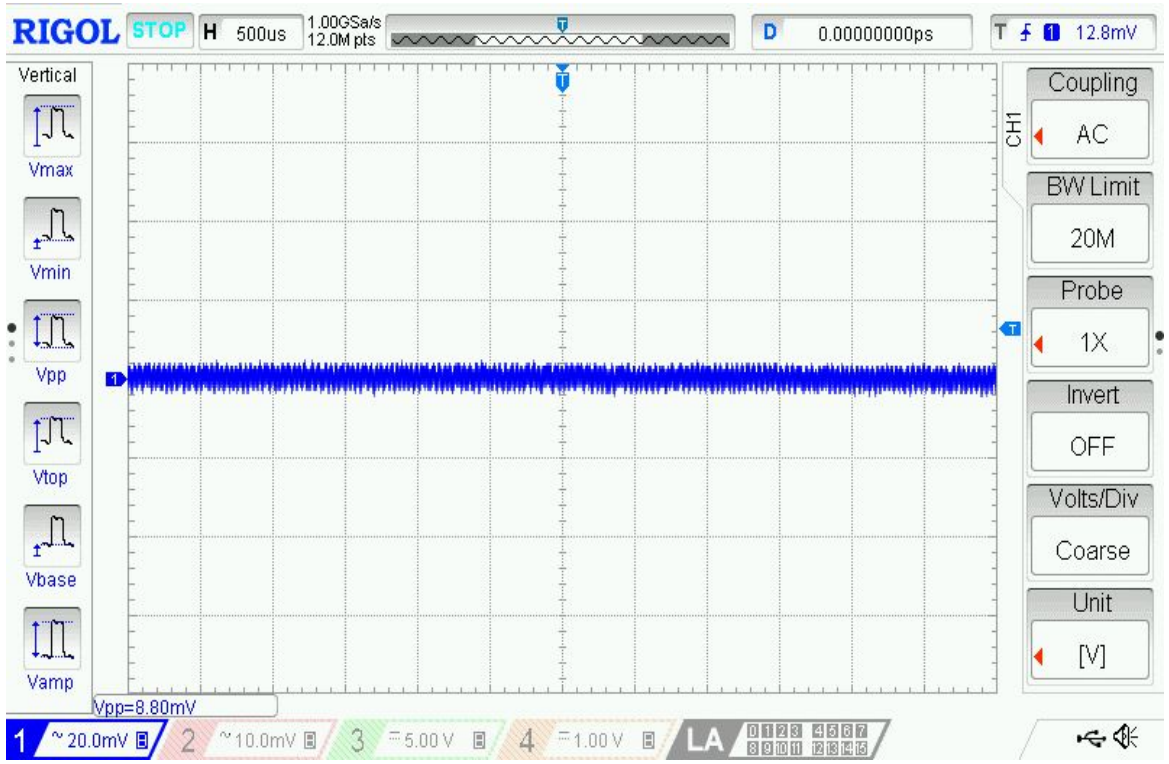




Vout = 1.5 V
Transient 2.81A – 4.2A @ 10 A/µs
V_{PP} = 25 mV
Fsw = 0.571 MHz
L = 4.7 µH, C = 1x47 uF

Ripple





No Load
V_{PP} = 7.20 mV

Vout = 1.5 V

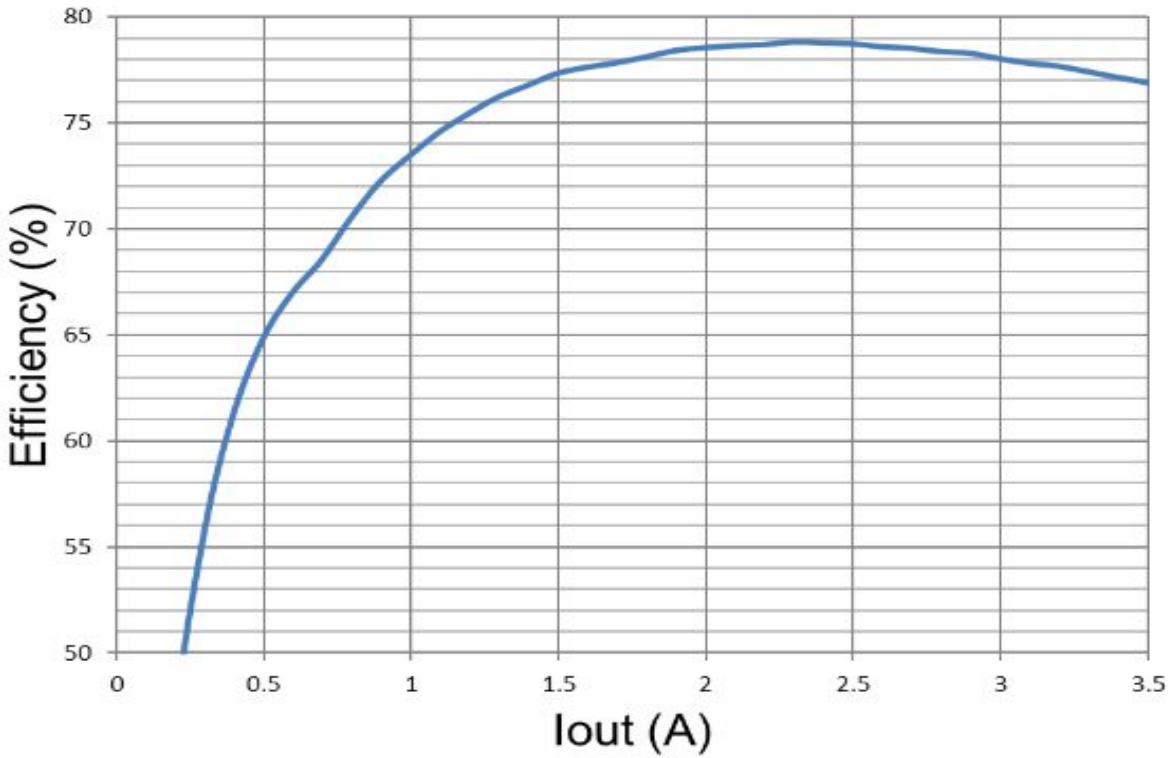
4.2 A Load
V_{PP} = 8.80 mV

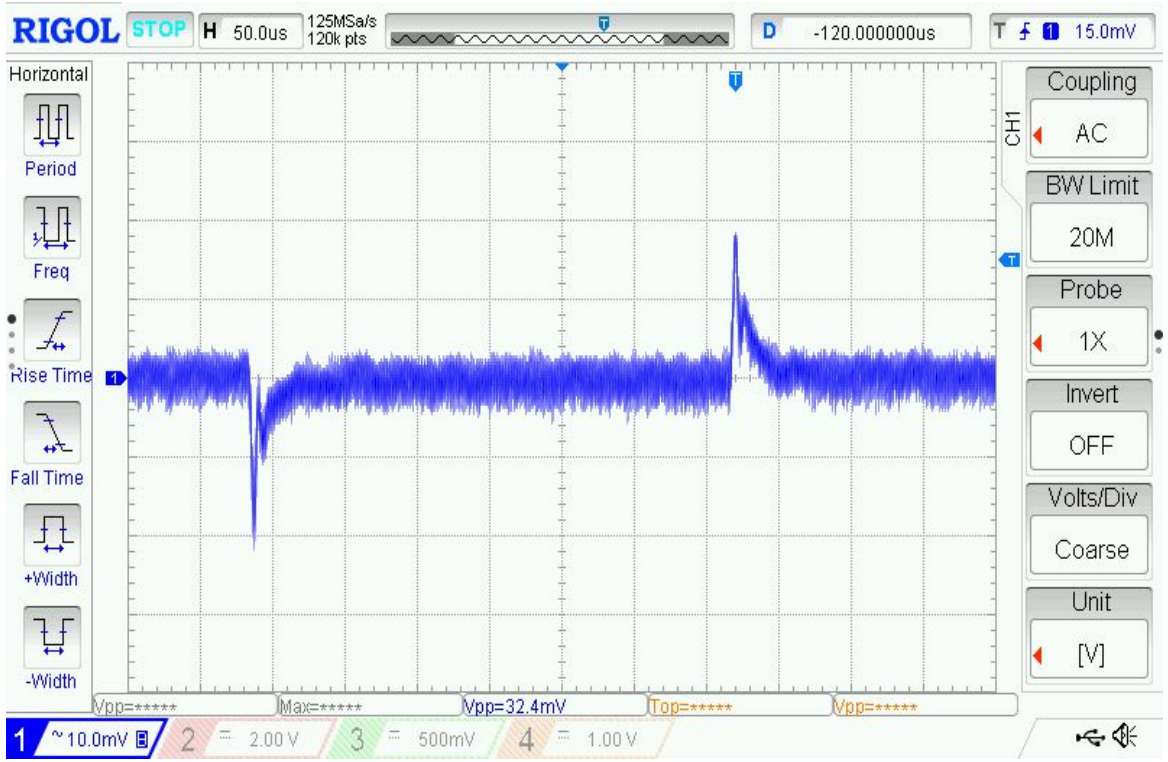
AnDAPT

MGTAVCC
0.88 V / 3.1 A

- C200 (Synchronous Buck)
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 9x47 uF

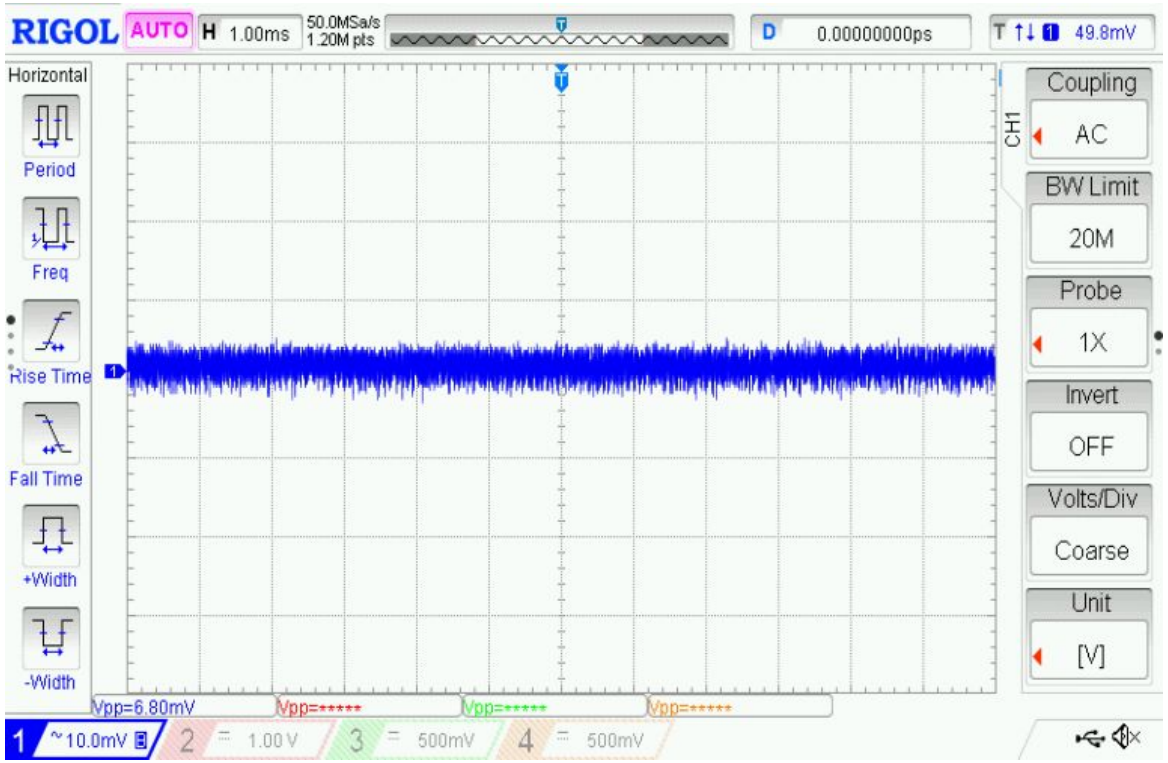
Efficiency & Transient





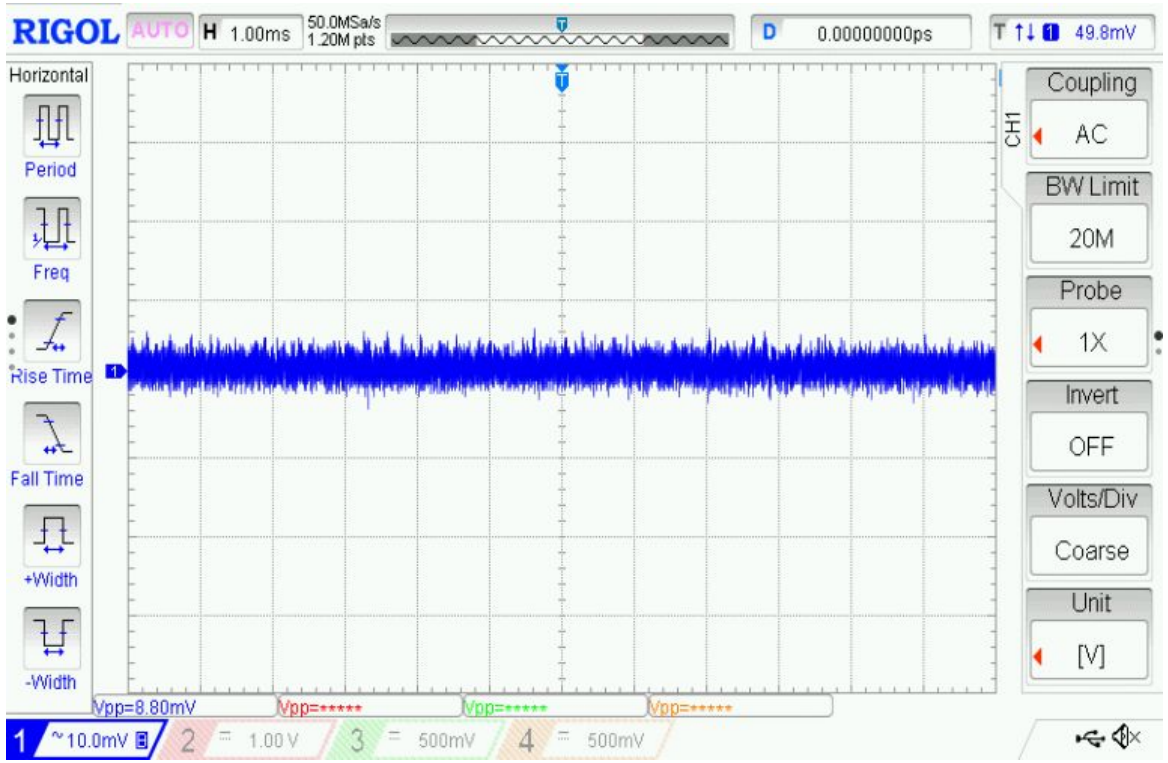
Vout = 0.88 V
Transient 2.625A – 3.5A @ 10 A/µs
V_{PP} = 32.4 mV
Fsw = 1 MHz
L = 0.56 µH, C = 9x47 uF

Ripple



No Load
V_{PP} = 6.80 mV

Vout = 0.88 V



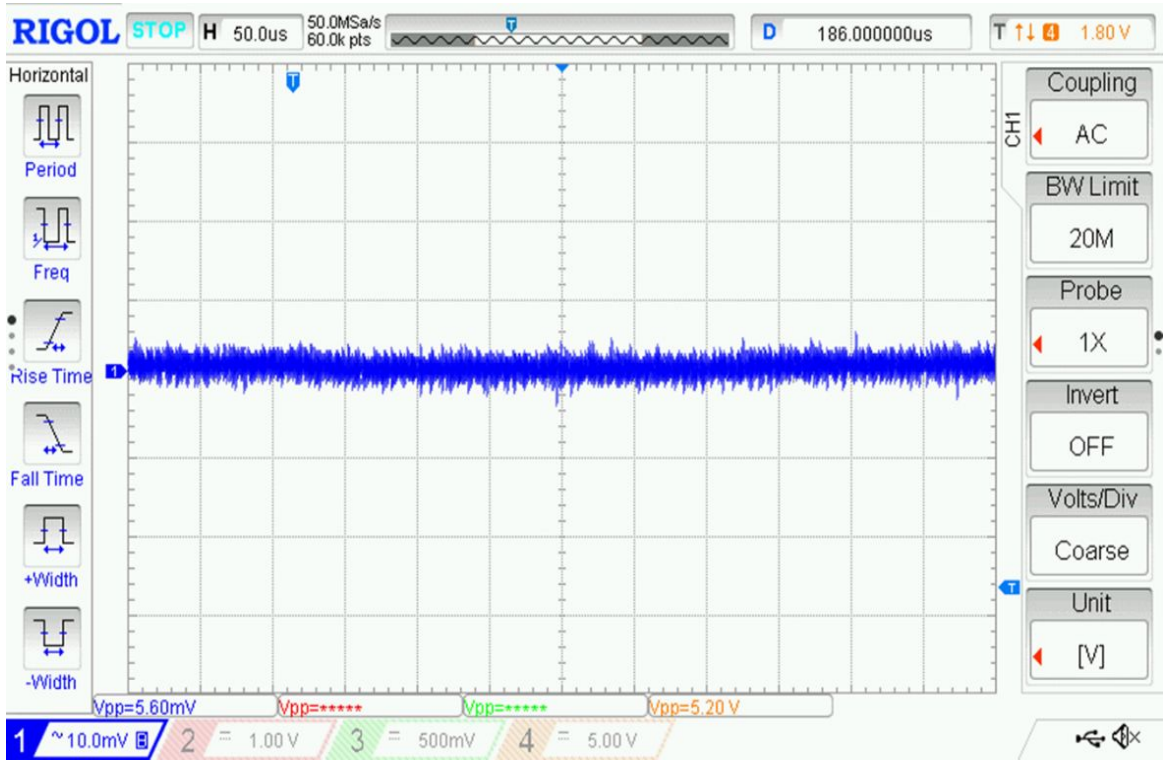
3.1 A Load
V_{PP} = 8.80 mV

AnDAPT

MGTYVCCAUX
0.88 V / 0.3 A

- C710 LDO

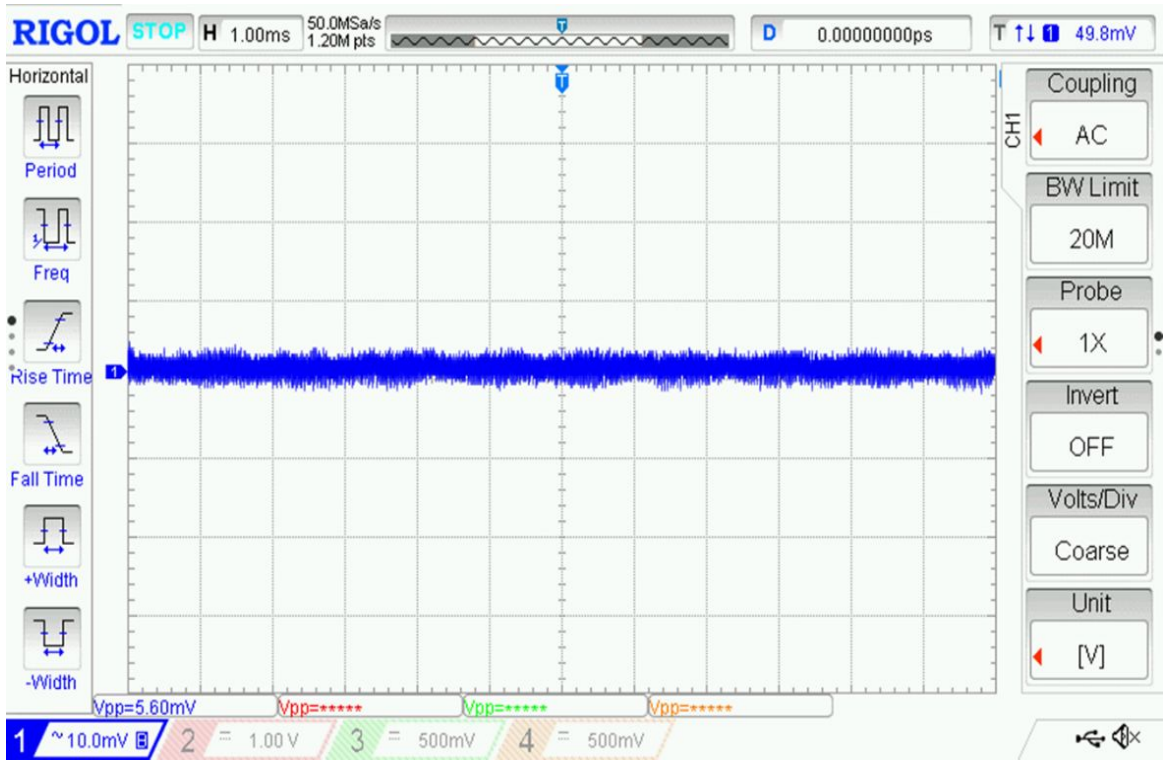
Transient



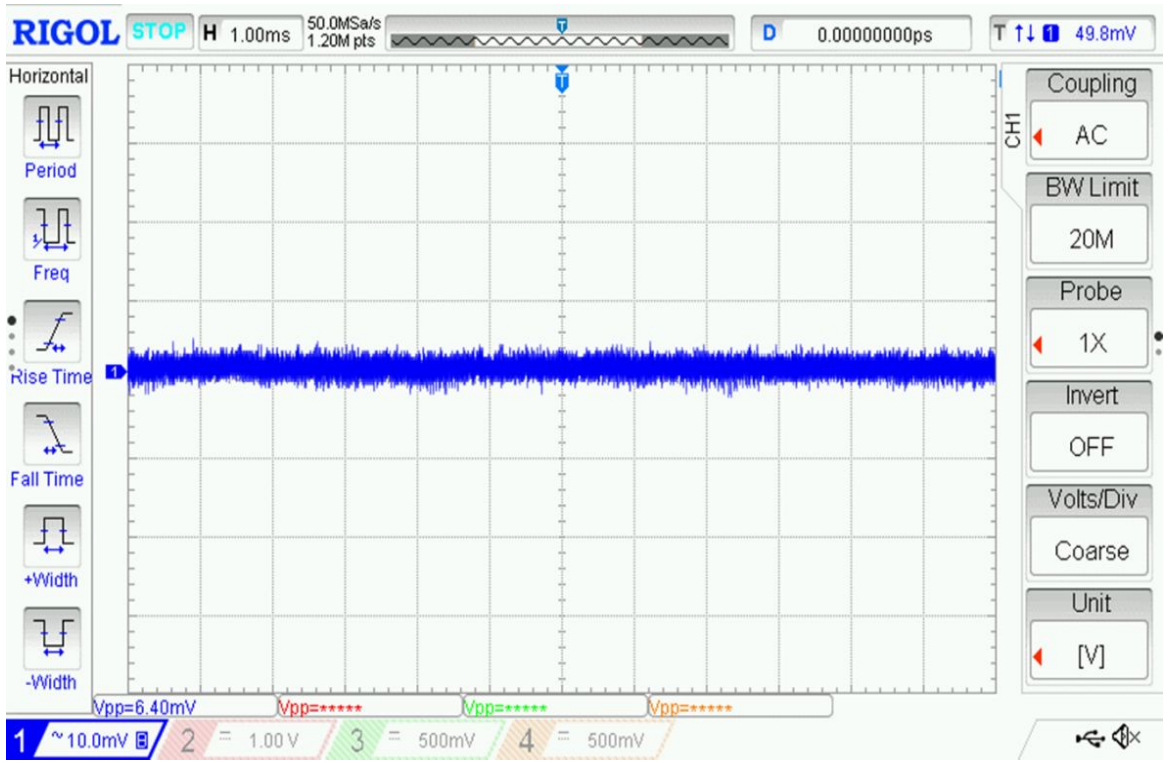
Vout = 0.88 V
Transient 0.21 A – 0.35 A @ 2.5 A/µs
V_{PP} = 5.6 mV

AnDAPT

Ripple



No Load
V_{PP} = 5.6 mV



Vout = 0.88 V

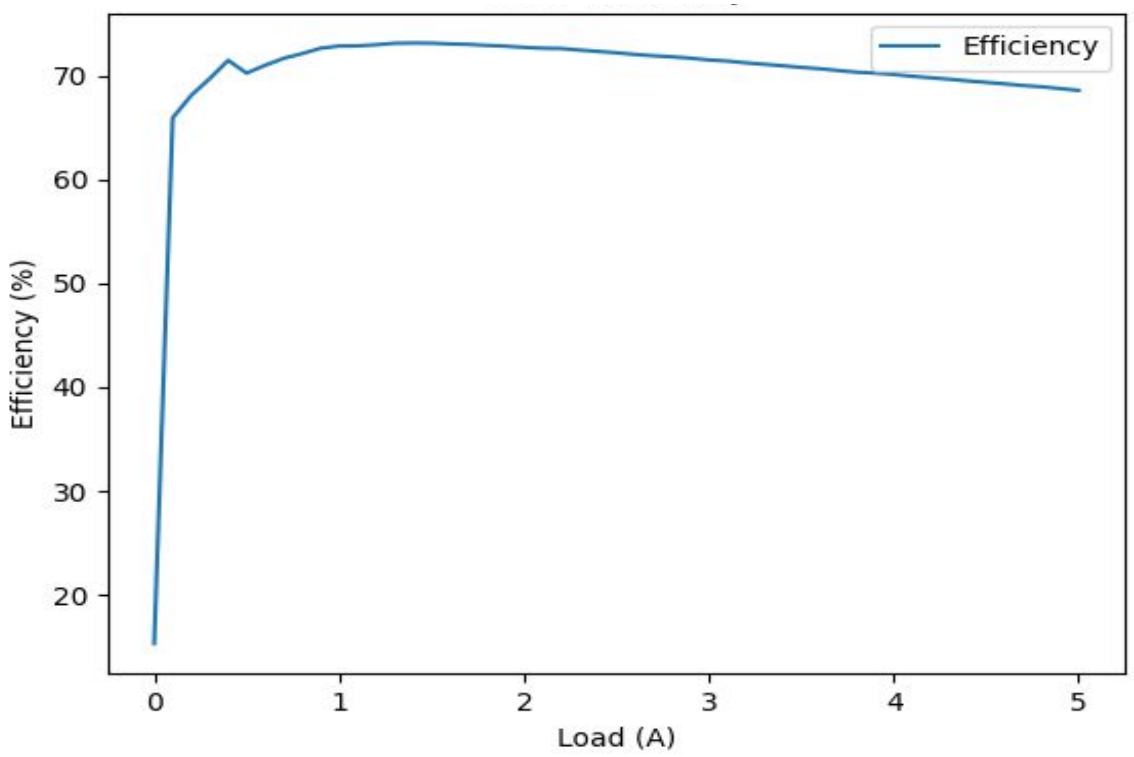
0.3 A Load
V_{PP} = 6.4 mV

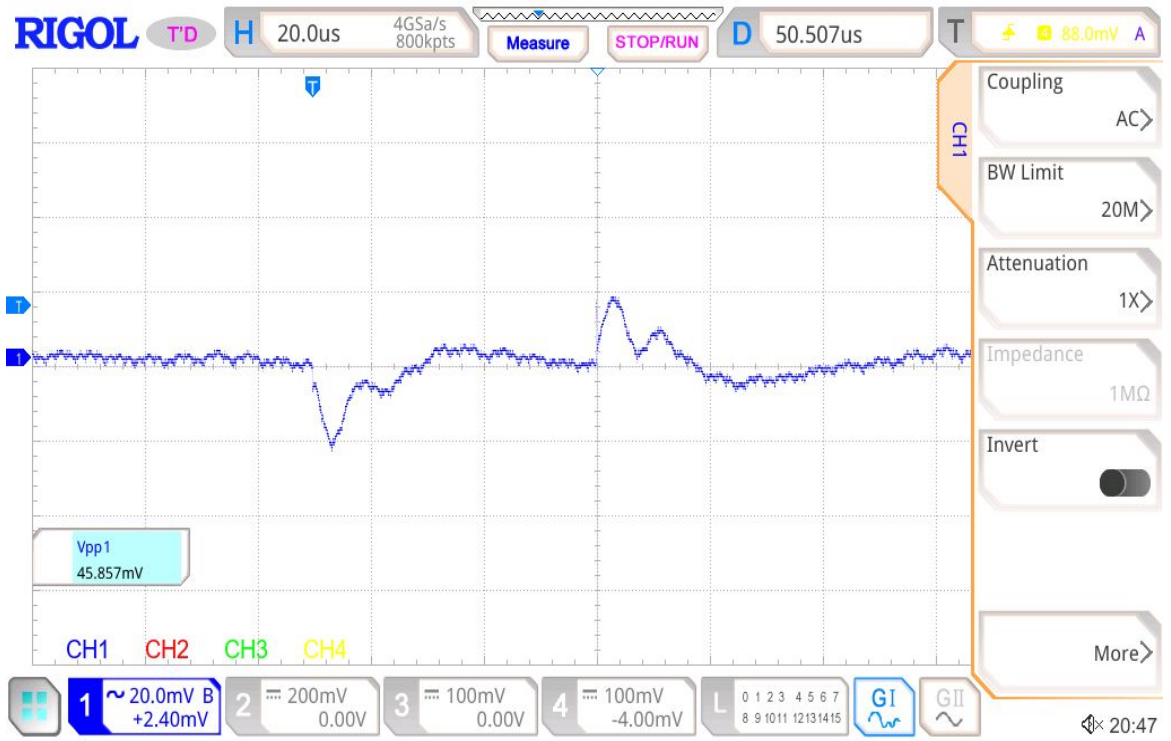
AnDAPT

MGTYAVTT
1.2 V / 4.9 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 4x47 uF

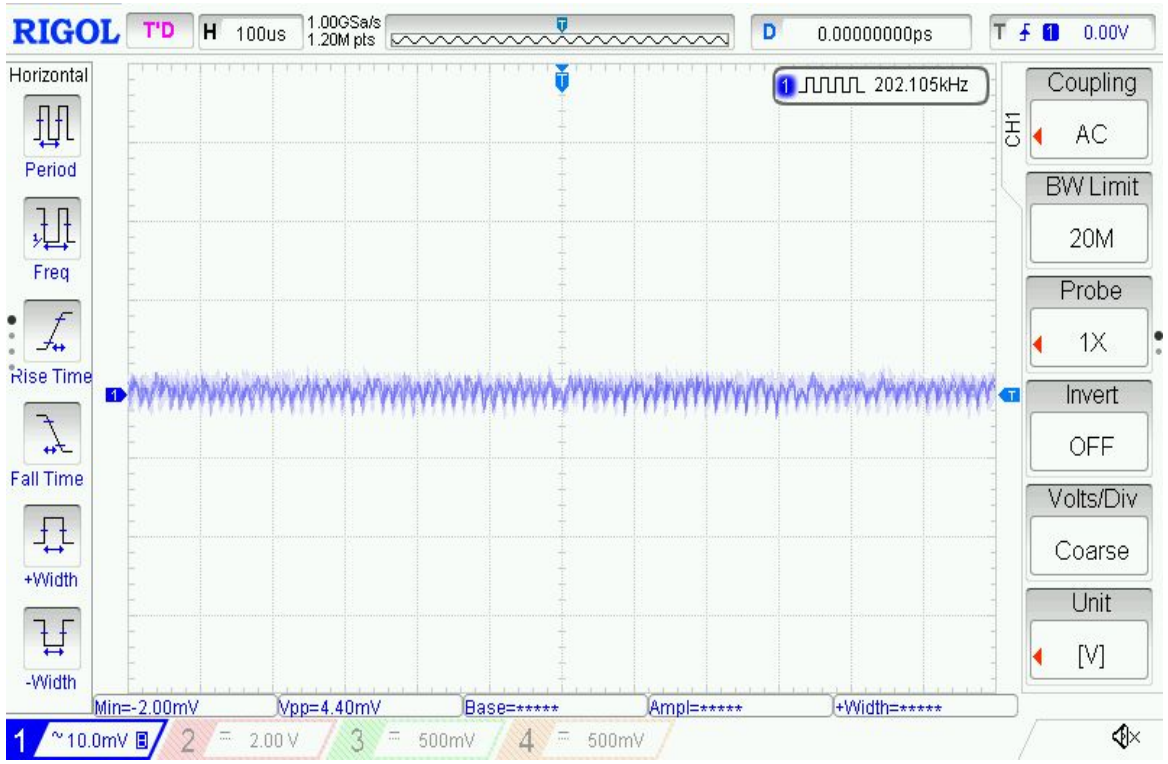
Efficiency & Transient



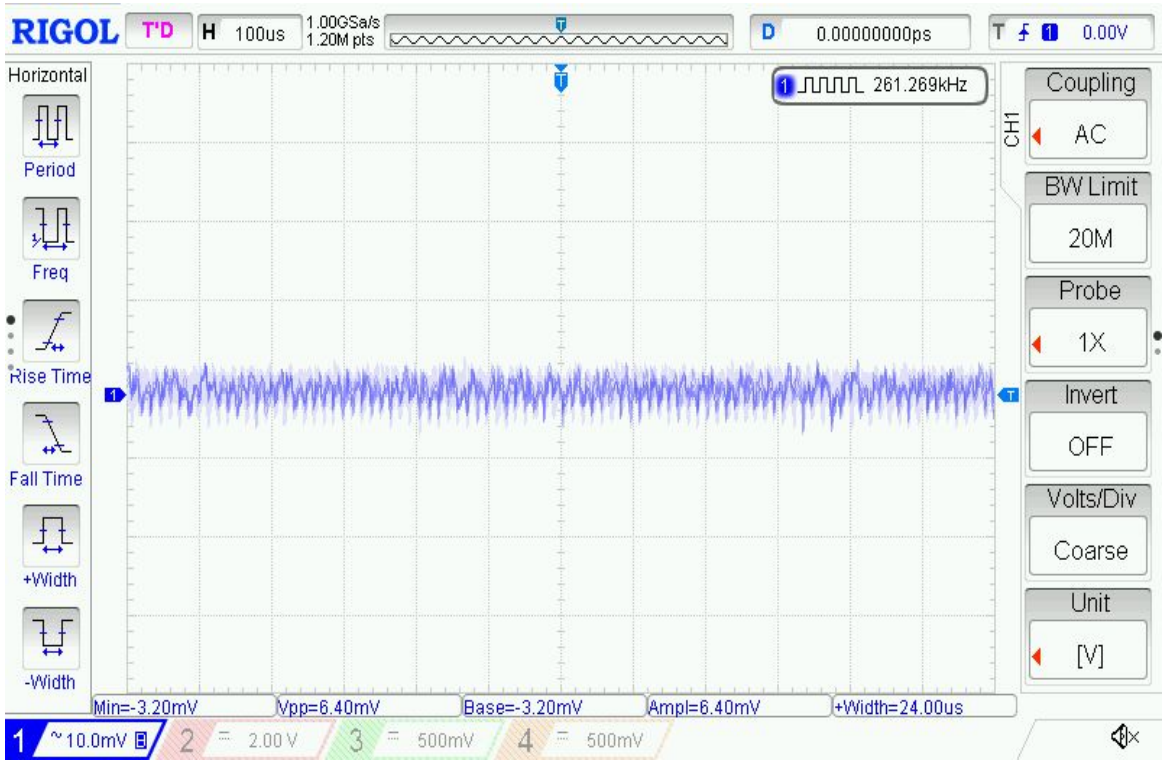


Vout = 1.2 V
Transient 3.675 – 4.9A @ 10 A/µs
V_{PP} = 45.85 mV
Fsw = 0.571 MHz
L = 1.1 µH, C = 4x47 uF

Ripple



No Load
V_{PP} = 4.40 mV



Vout = 1.2 V

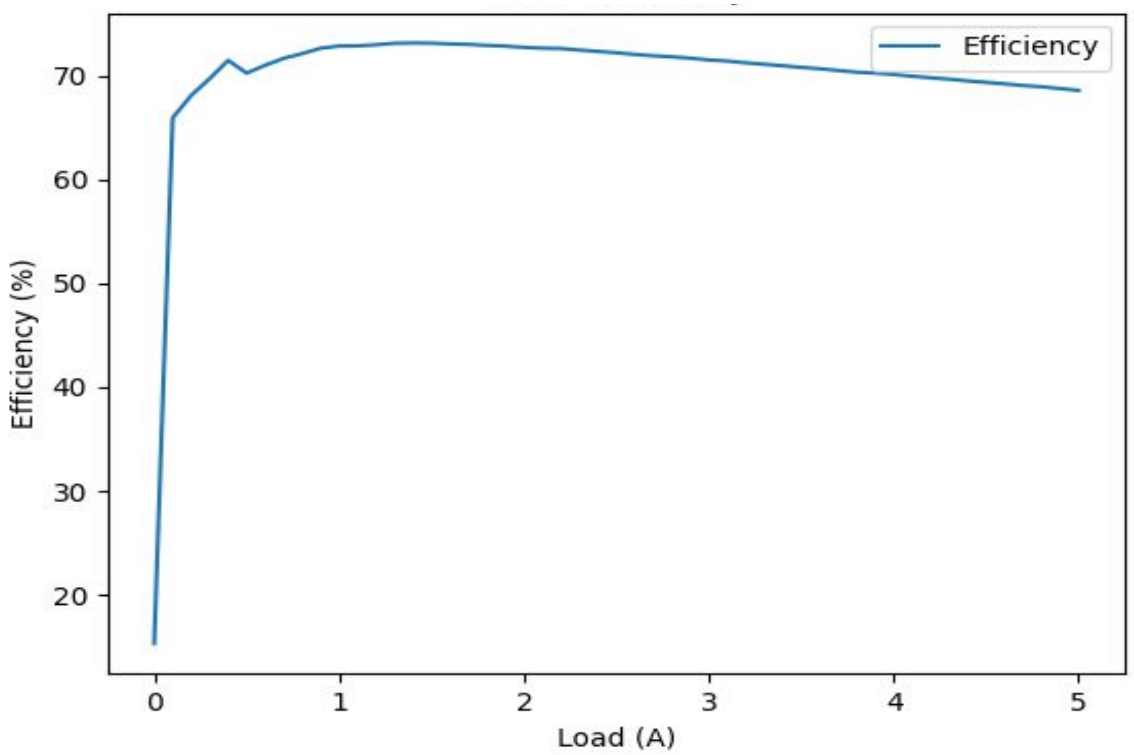
4.9 A Load
V_{PP} = 6.40 mV

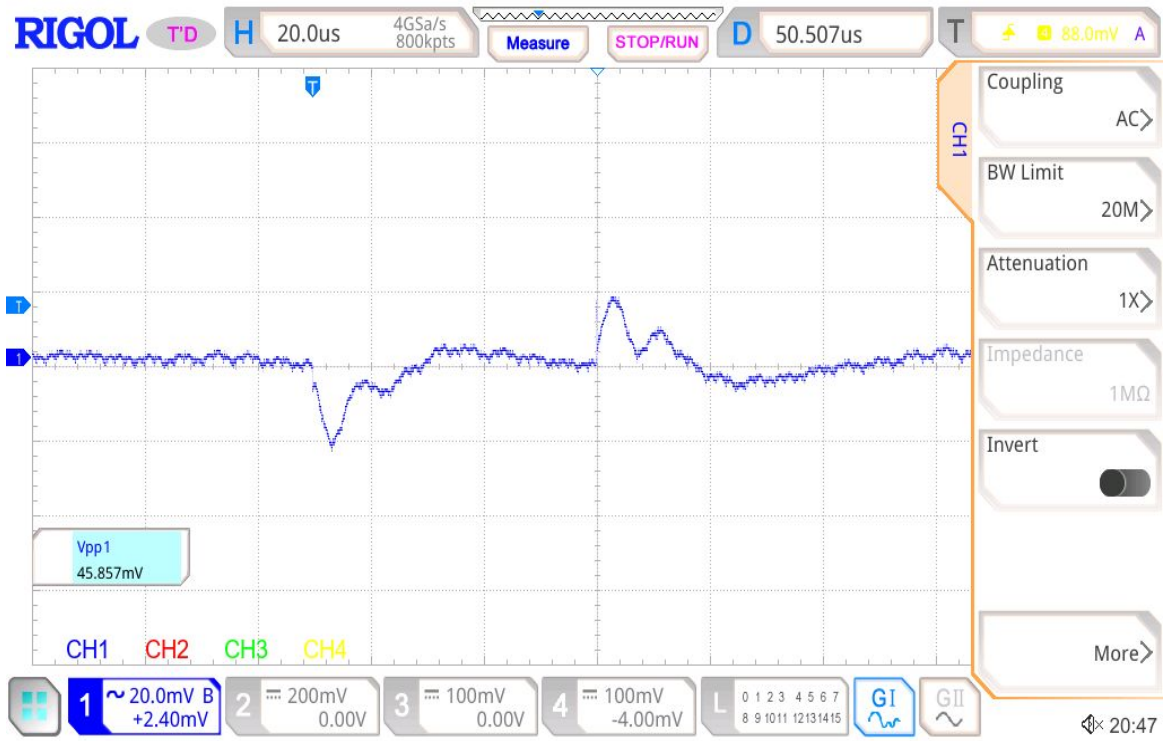
AnDAPT

VDDQ
1.2 V / 5 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1.1µH, P/N Wurth 744314110
- C = 4x47 uF

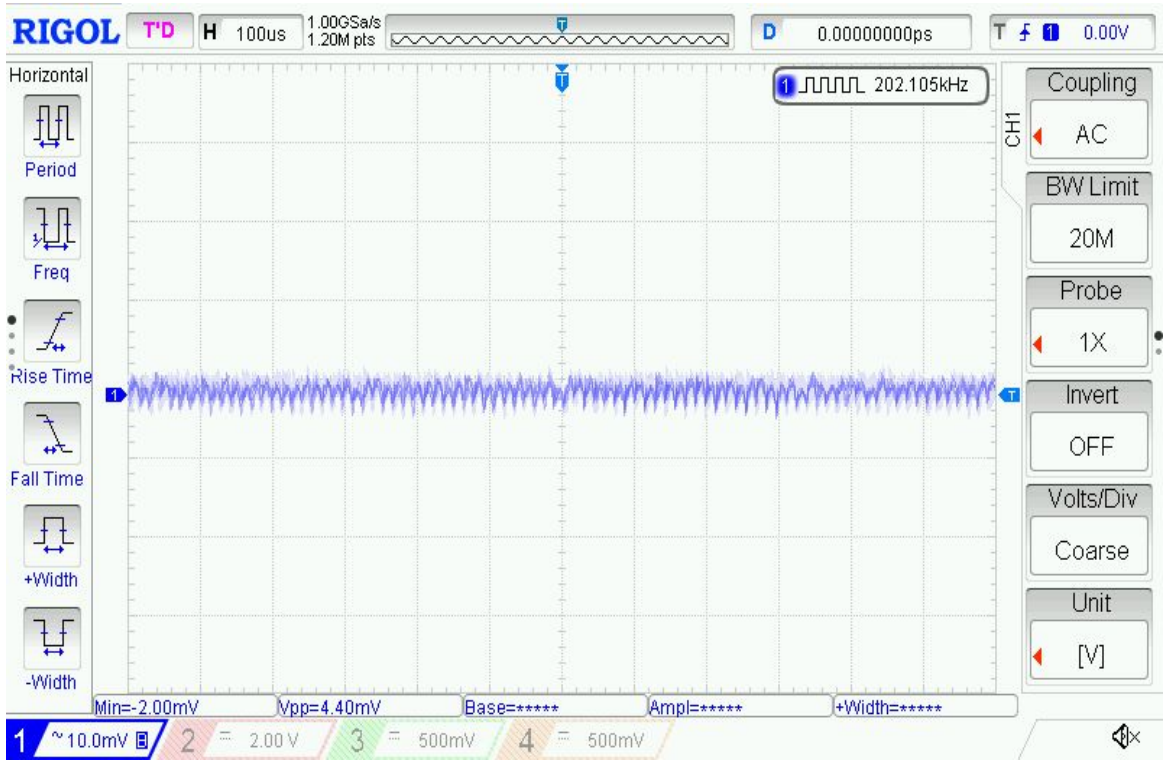
Efficiency & Transient

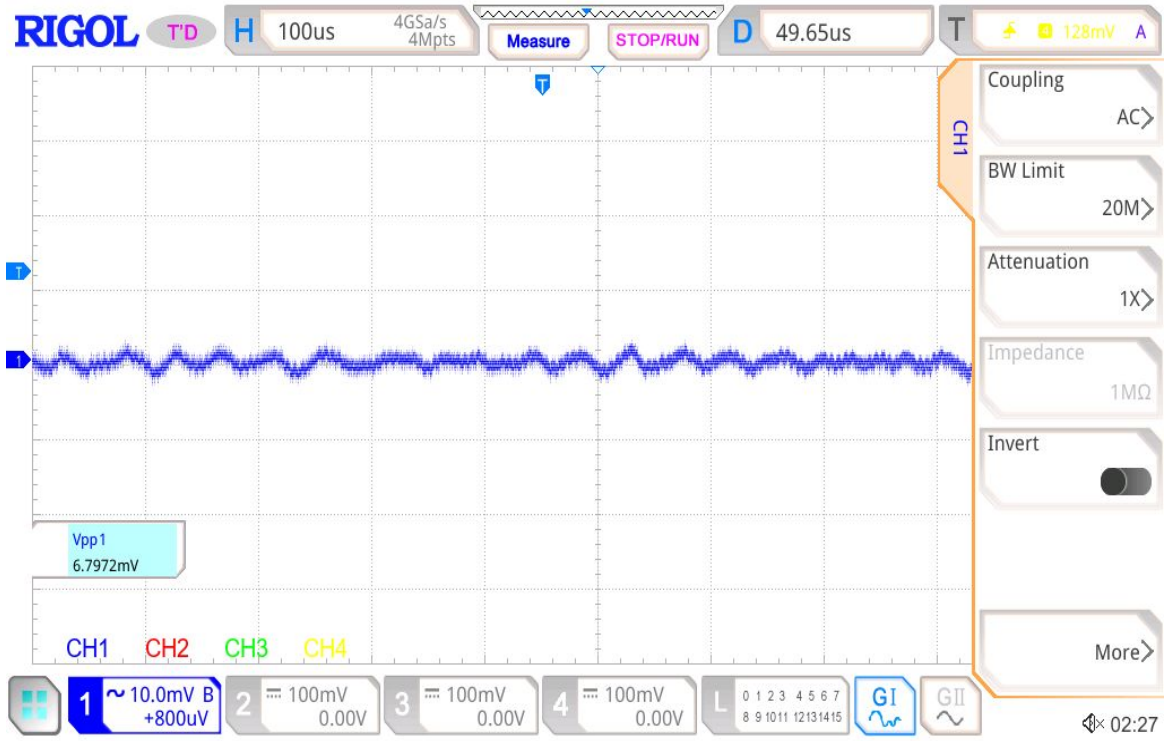




Vout = 1.2 V
Transient 3.75 – 5A @ 10 A/µs
V_{PP} = 45.85 mV
Fsw = 0.571 MHz
L = 1.1 µH, C = 4x47 uF

Ripple





No Load
V_{PP} = 4.40 mV

Vout = 1.2 V

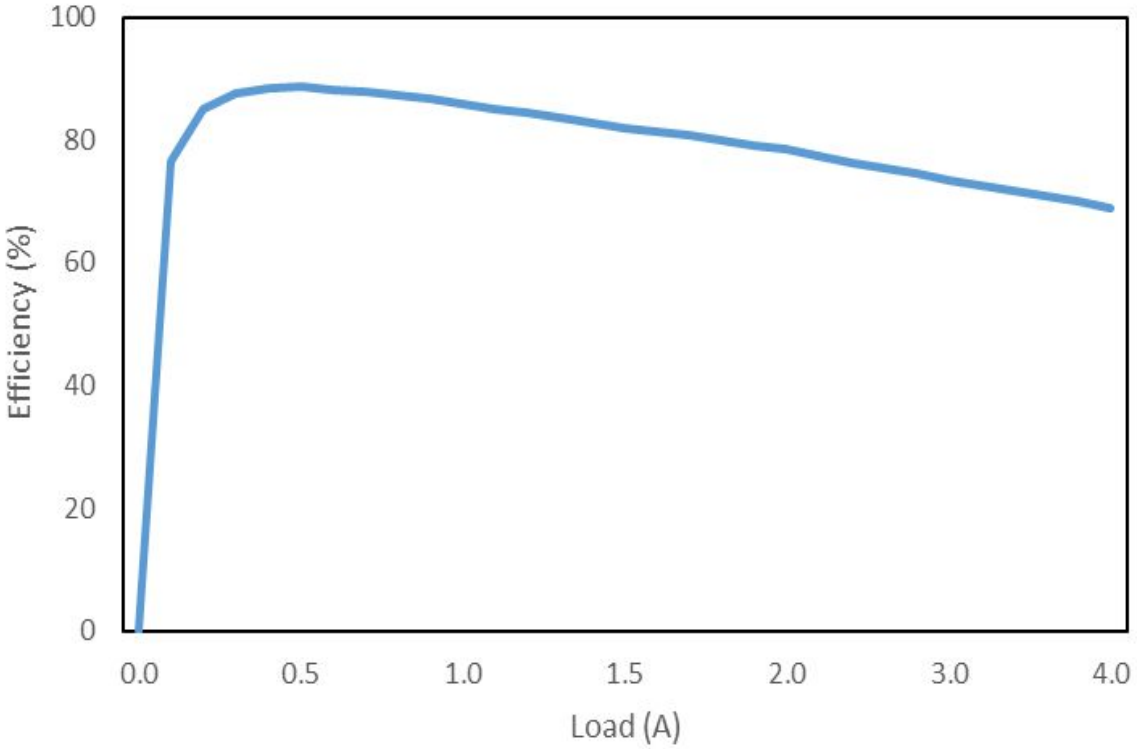
5 A Load
V_{PP} = 6.79 mV

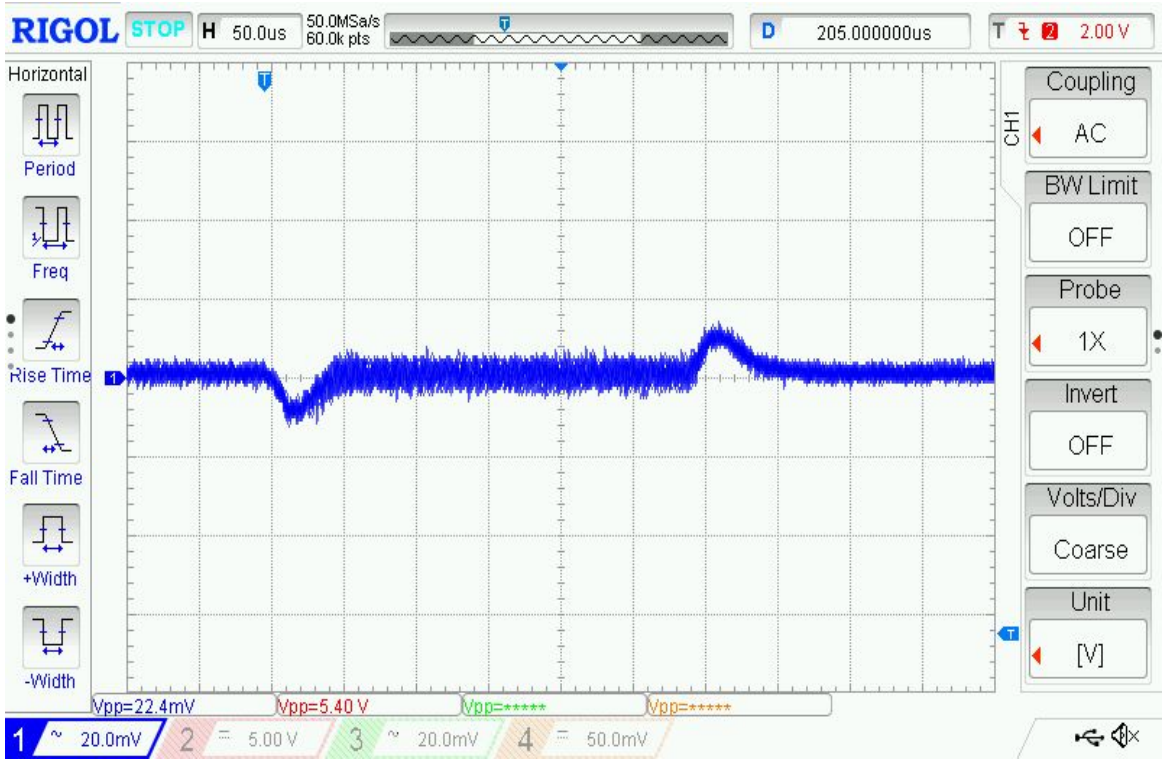
AnDAPT

VTT
0.6 V / 2 A

- C210 (VTT Terminator)
- Fsw = 1 MHz
- L = 0.33 µH, P/N Wurth 744393440033
- C = 8x47 uF

Efficiency & Transient

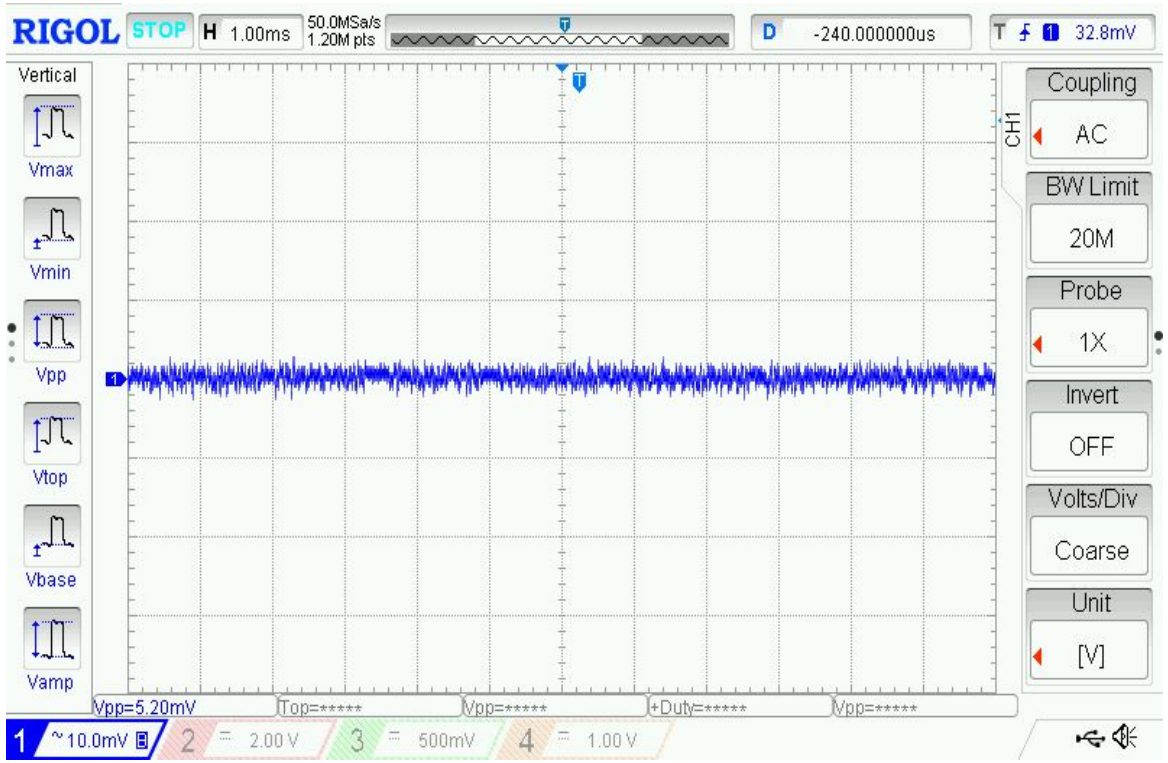




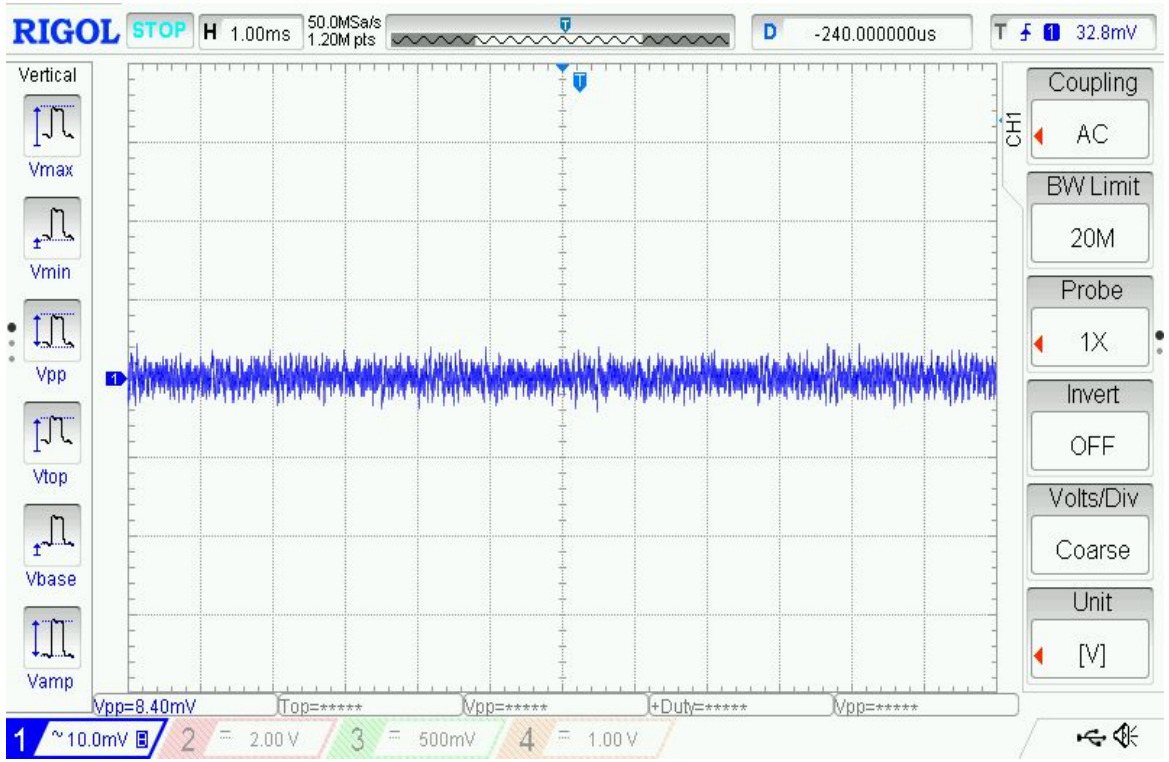
Vout = 0.6V
Transient 3 – 4A @ 10 A/µs
V_{PP} = 22.4 mV
Fsw = 1 MHz
L = 0.33 µH, C = 8x47 uF

AnDAPT

Ripple



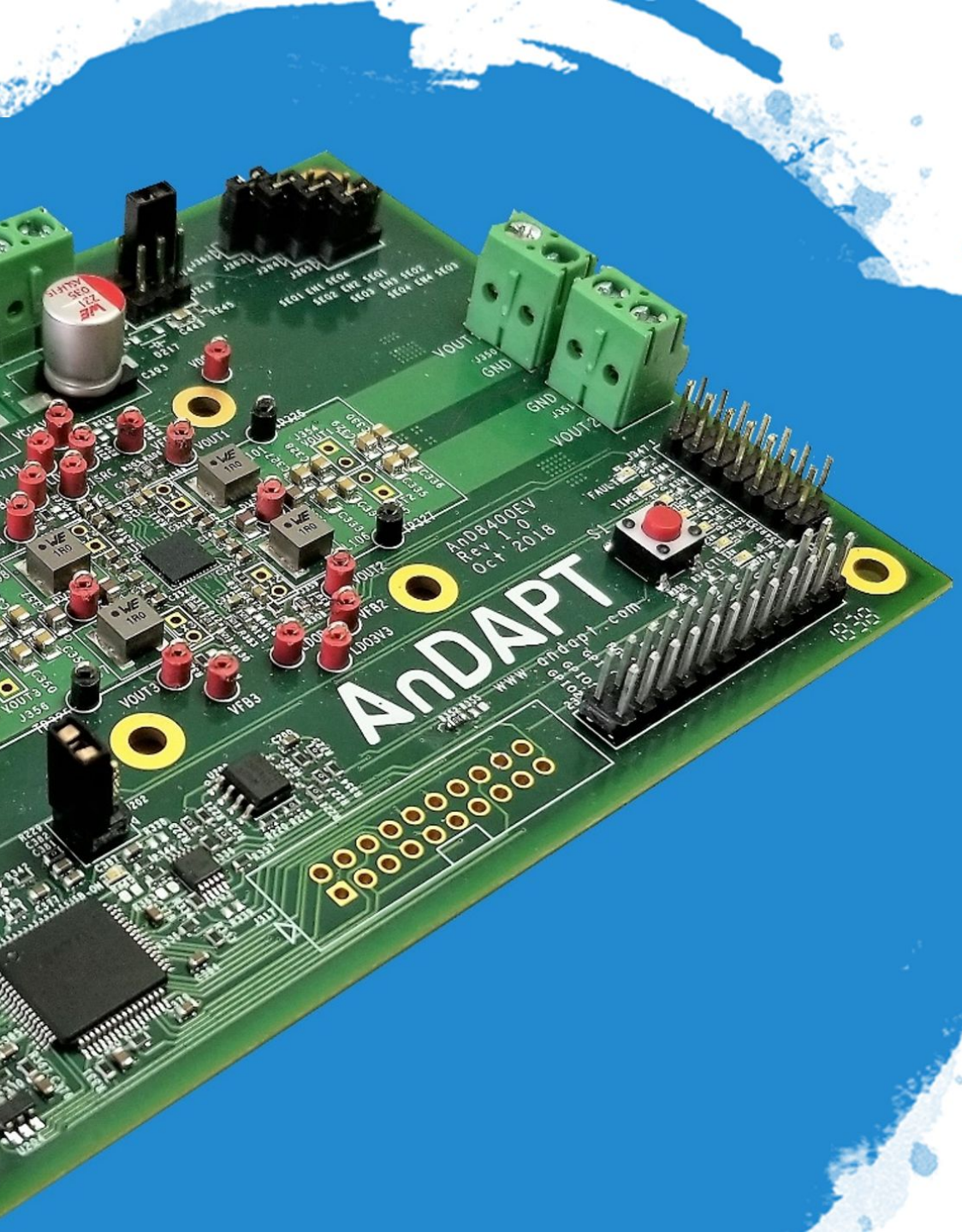
No Load
V_{PP} = 5.20 mV



Vout = 0.6 V

4 A Load
V_{PP} = 8.40 mV

AnDAPT



Thank You

AnDAPT