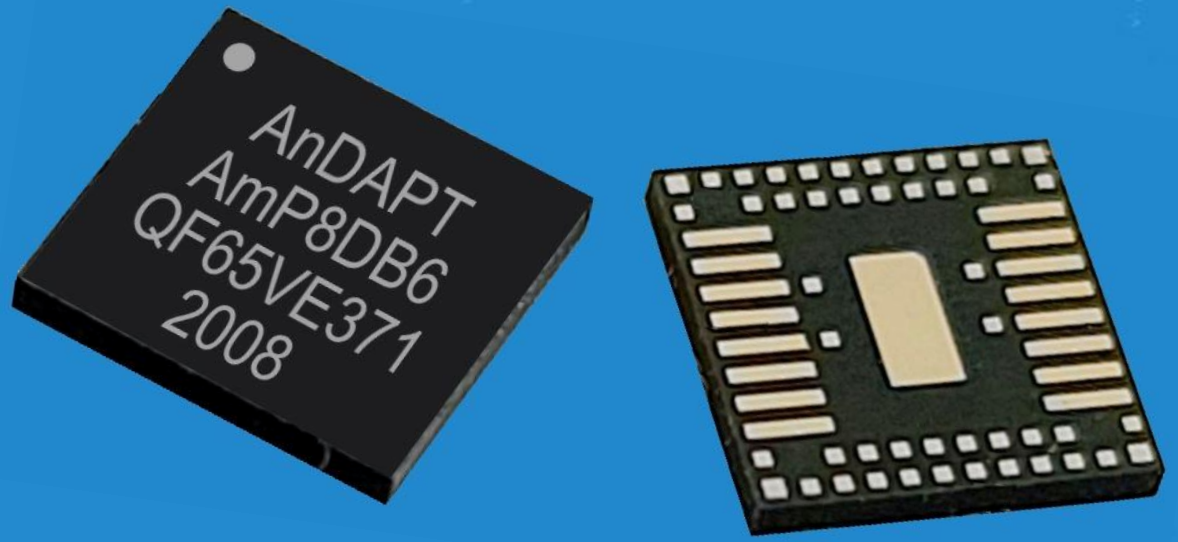

Xilinx Versal Premium –M Devices (Minimum Rails) Upper Loading Use-case

Power Mappings

AnDAPT Marketing Team

AnDAPT

Contents

- Versal Premium power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx

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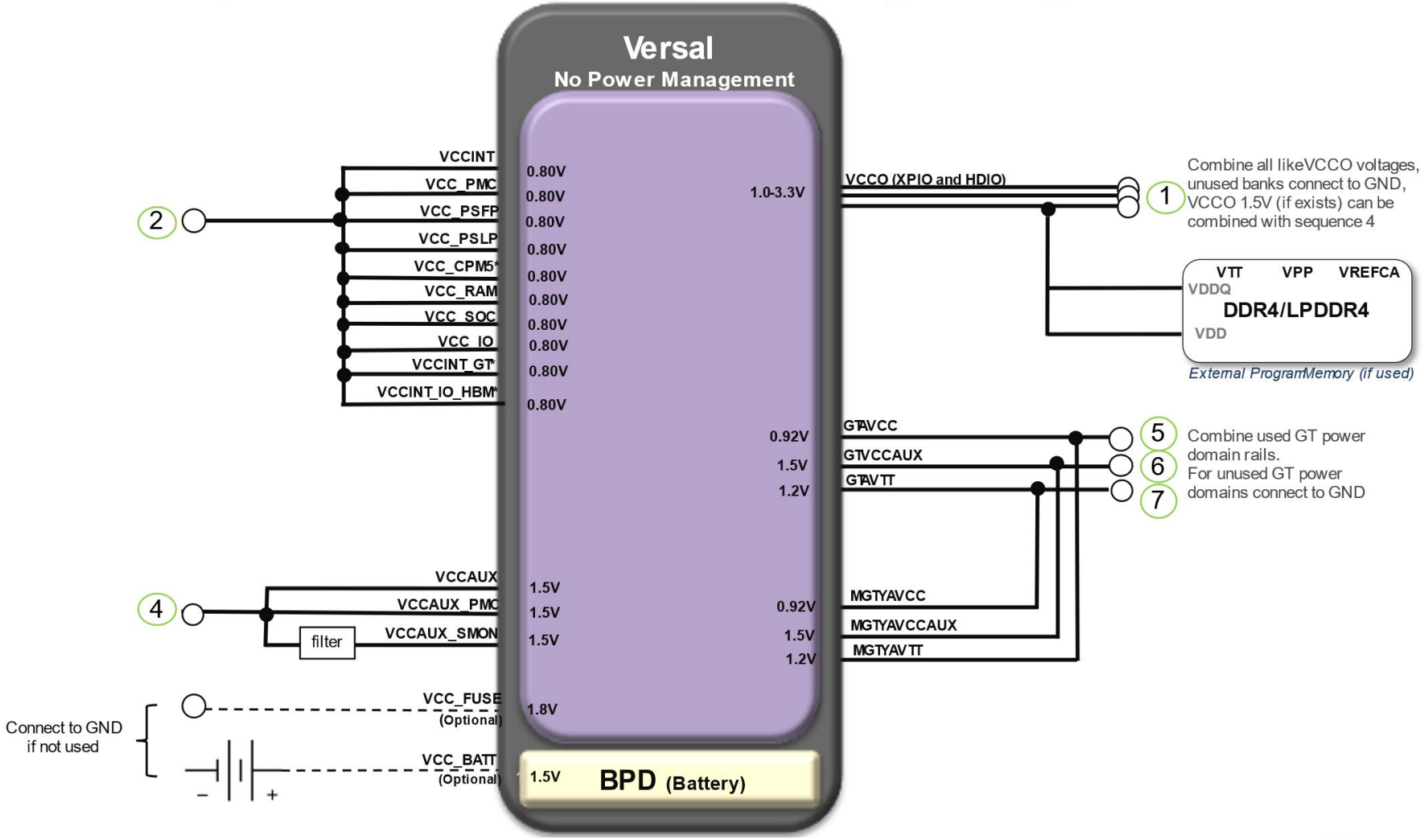
Xilinx Versal Premium Power Tree

Minimum Rails (No Power Management) – Mid/High Voltage



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Power Tree Mapping: Versal Premium –M (Minimum Rails, Upper Loading)

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCO_HDIO (VCCO_HDIO, VCCO_500, VCCO_501, VCCO_502, VCCO_503)	1	C200	Integ. Sync Buck	PVIN	12	1.8	0.1-3	ARD_X_VRPM_B_IC1
2	VCCO_XPIO	1	C200	Integ. Sync Buck	PVIN	12	1.5	0.1-3	
3	VCCINT (VCCINT, VCC_PMC, VCC_PSFP, VCC_PSLP, VCC_CPM5, VCC_RAM, VCC_GT, VCC_SOC, VCC_IO)	2	Ext.	Ext.	PVIN	12	0.8/0.88	80-180	
4	VCCAUX (VCCAUX, VCCAUX_PMC, VCCAUX_SMON)	2	C220	Integ. Sync Buck	PVIN	12	1.5	1.5-10	
5	MGTYAVCC (MGTYAVCC, GTAVCC)	3	C865	1-ph DrMOS Ctrl	PVIN	12	0.88/0.92	6-15	ARD_X_VRPM_B_IC2
6	MGTYAVCCAUX (MGTYAVCCAUX, GTAVCCAUX)	4	C200	Integ. Sync Buck	PVIN	12	1.5	1	
7	MGTYAVTT (MGTYAVTT, GTAVTT)	5	C860	1-ph DrMOS Ctrl	PVIN	12	1.2	8-24	

PVIN = 12V

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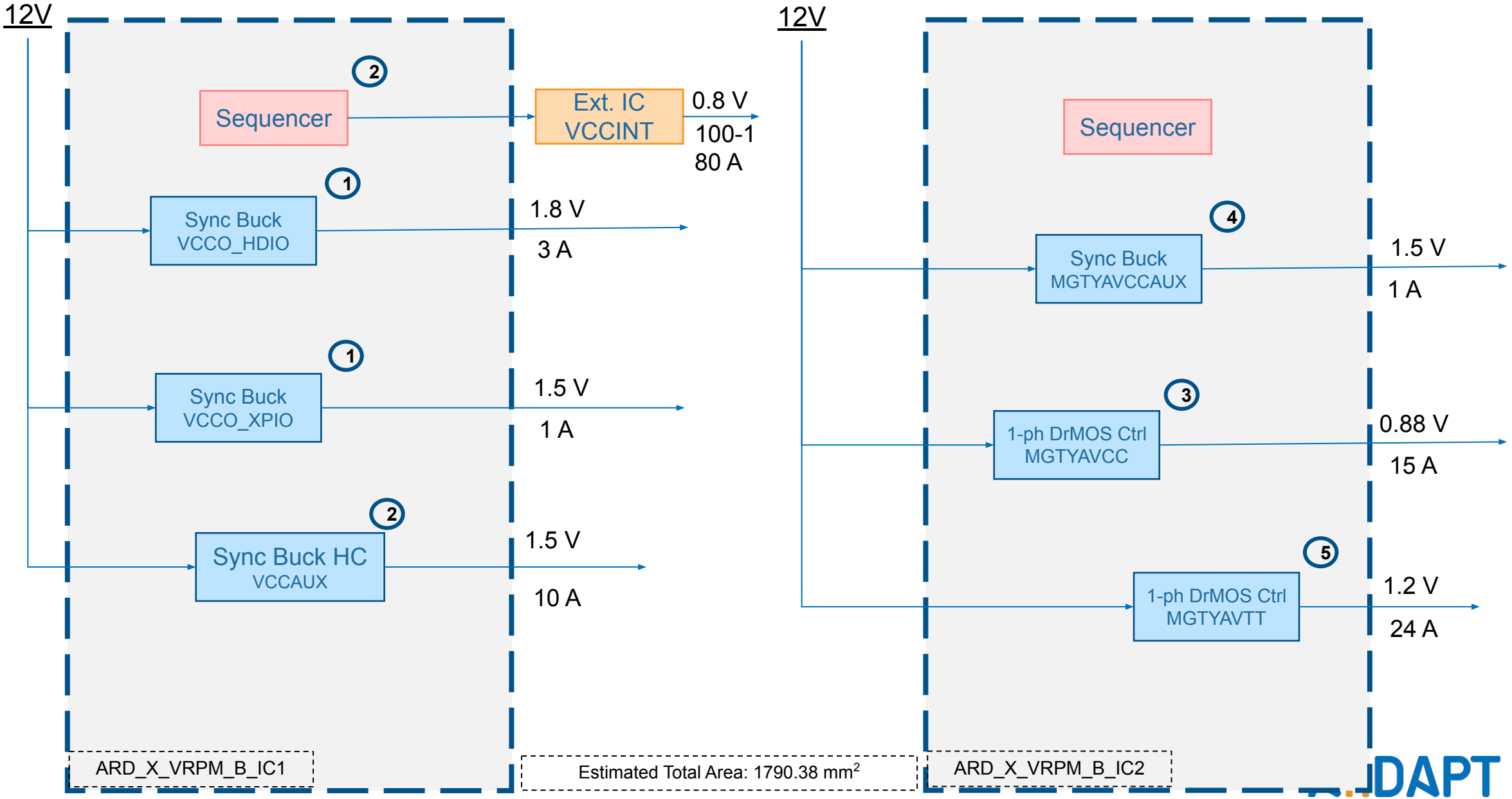
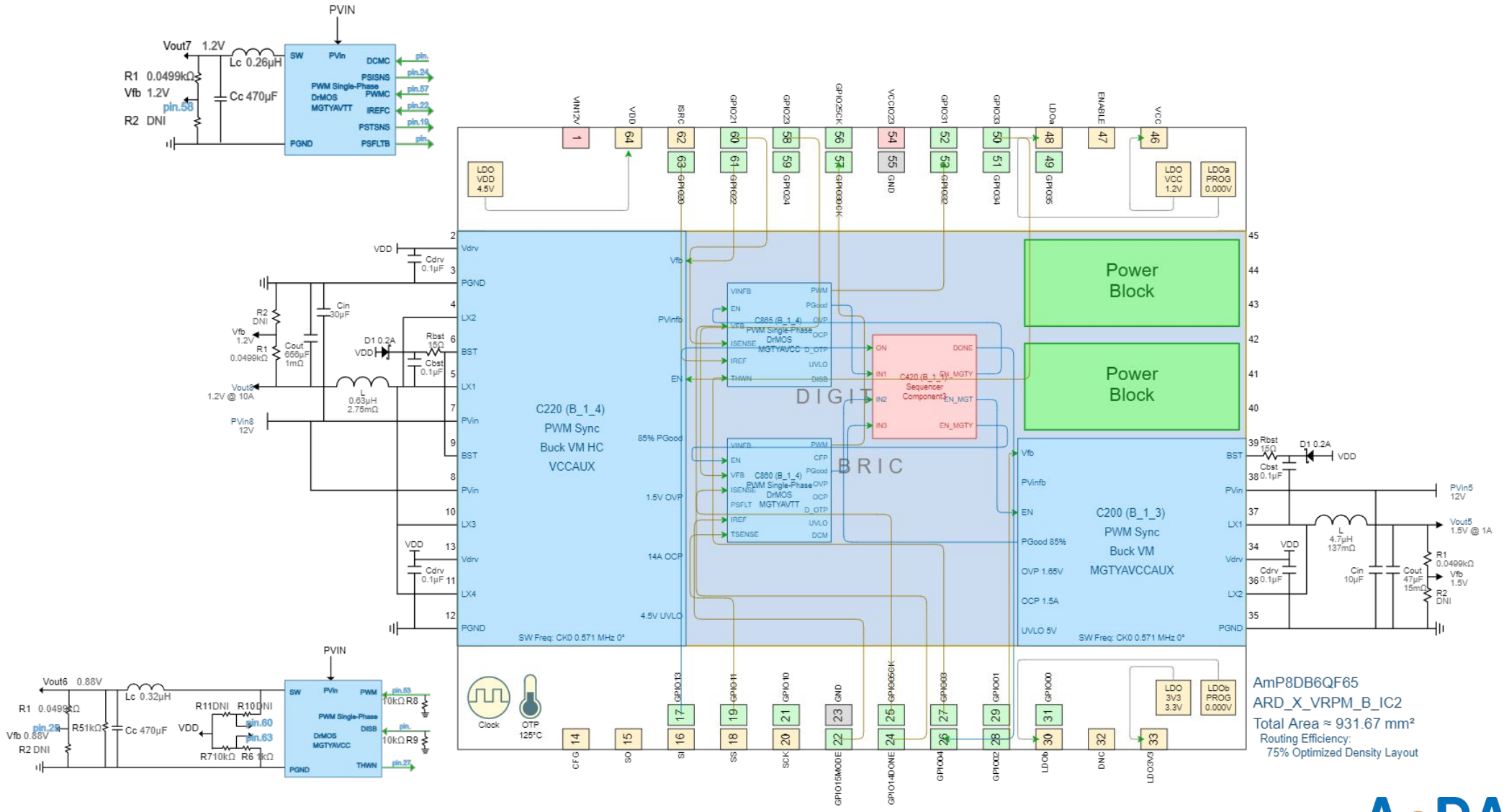
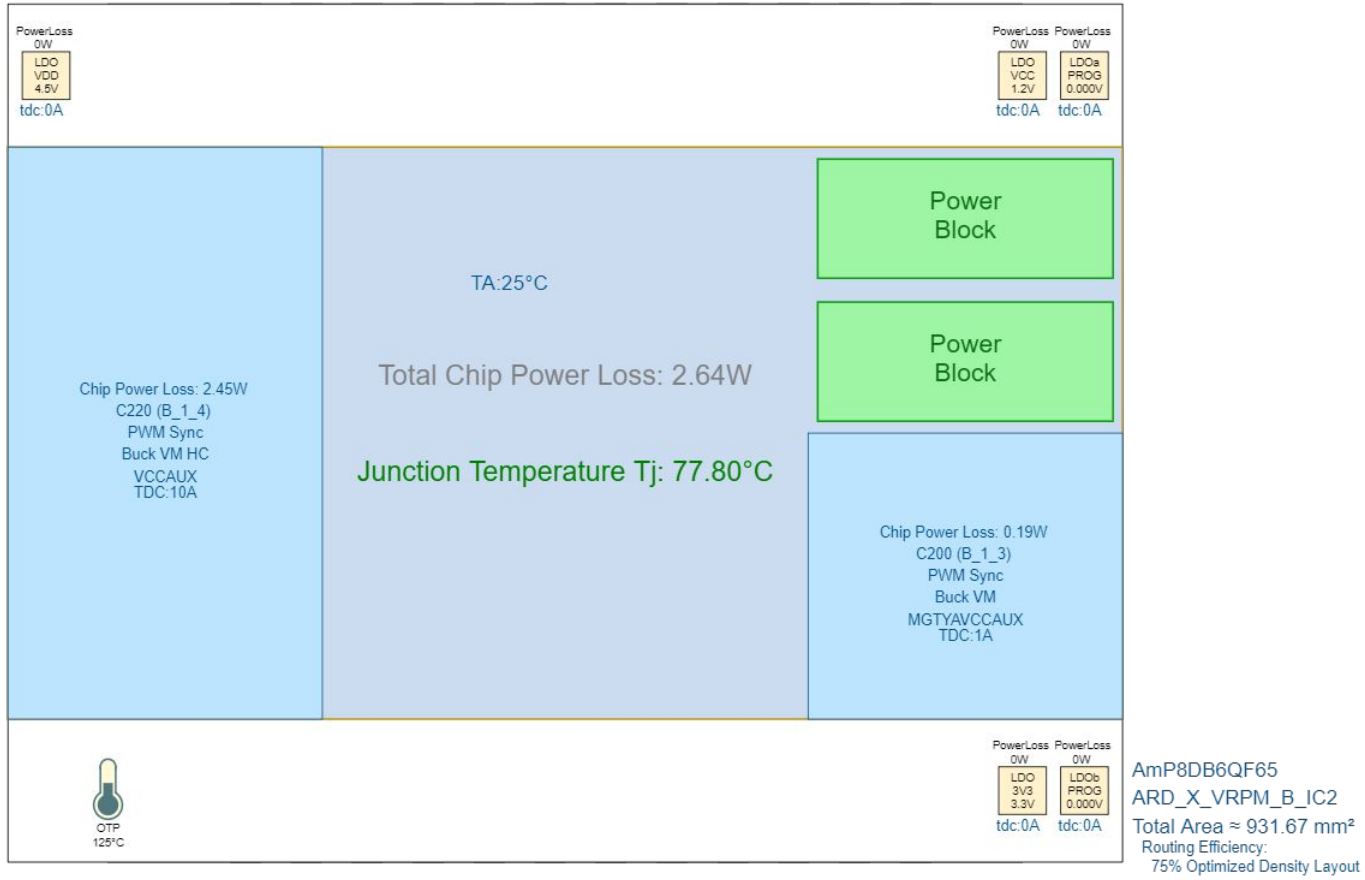
Power Tree Mapping- Design Upper Loading



Mapping (WebAmP View) Design Upper Loading–IC1

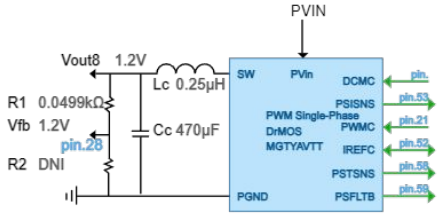


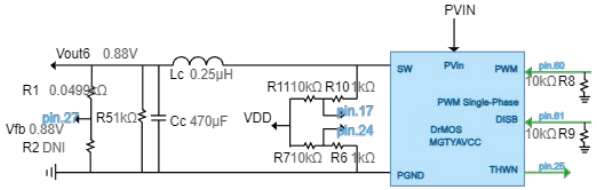
Mapping (Thermal View) Design Upper Loading–IC1

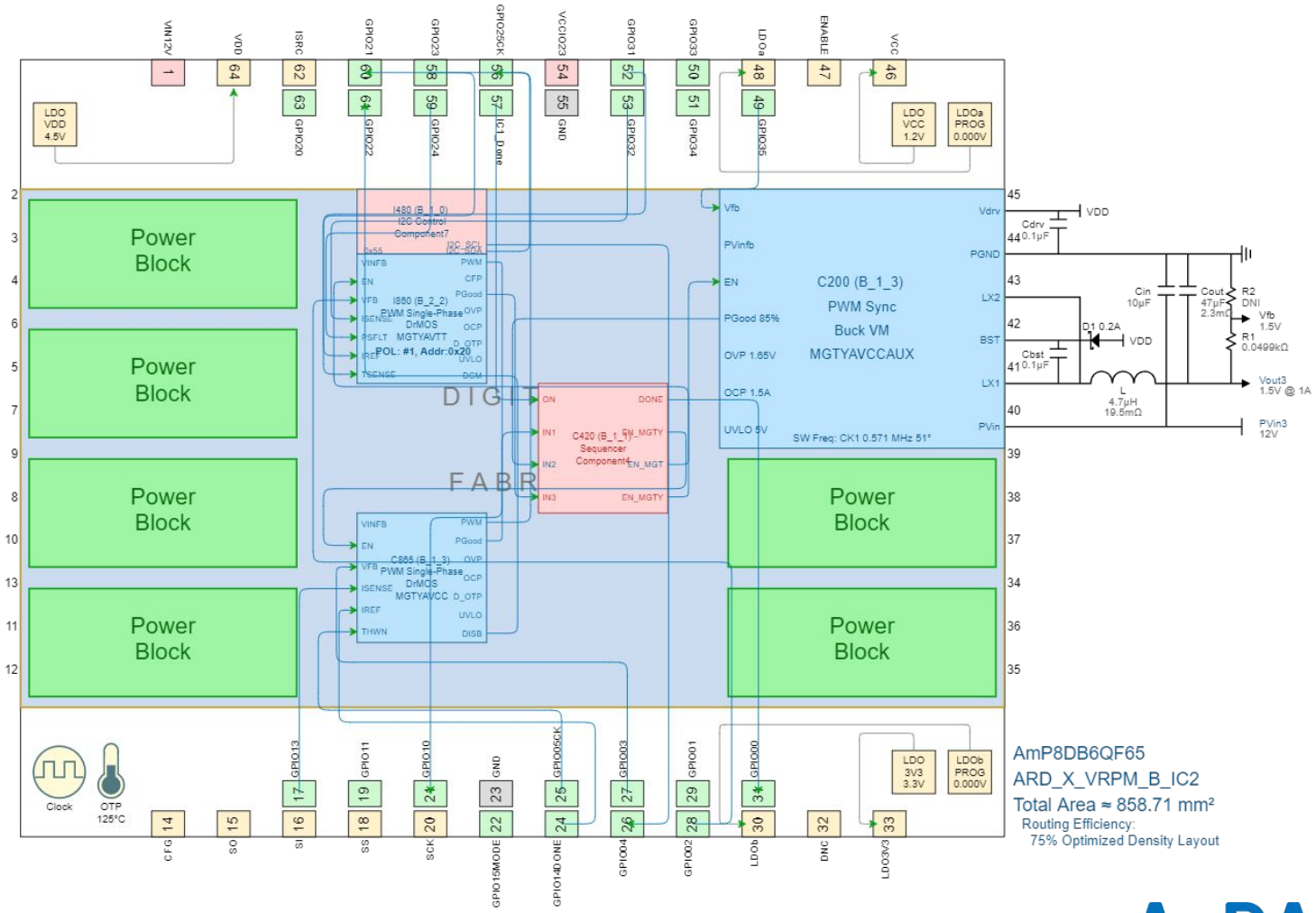


AmP8DB6QF65
ARD_X_VRPM_B_IC2
Total Area ≈ 931.67 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (WebAmP View) Design Upper Loading–IC2

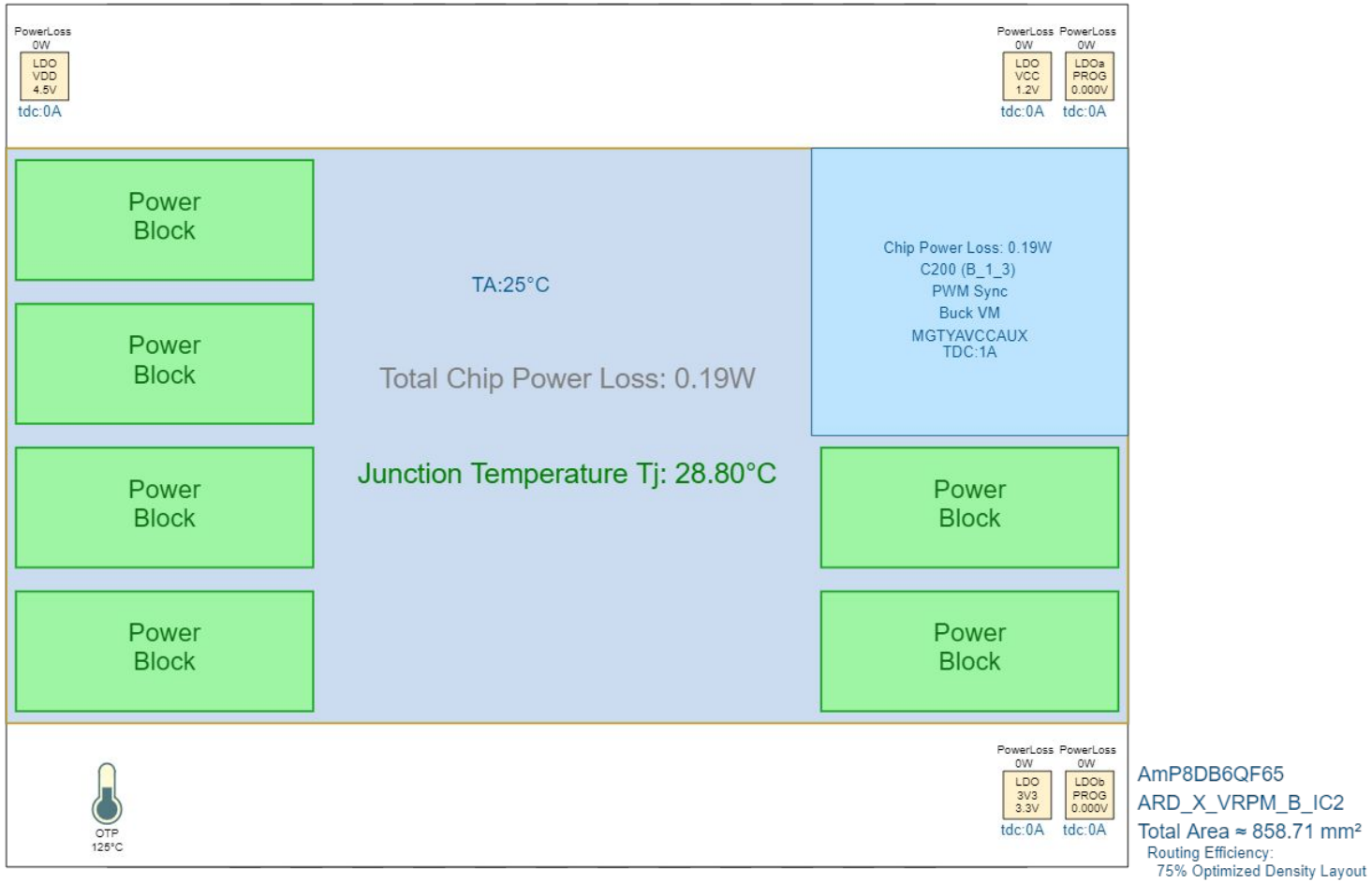


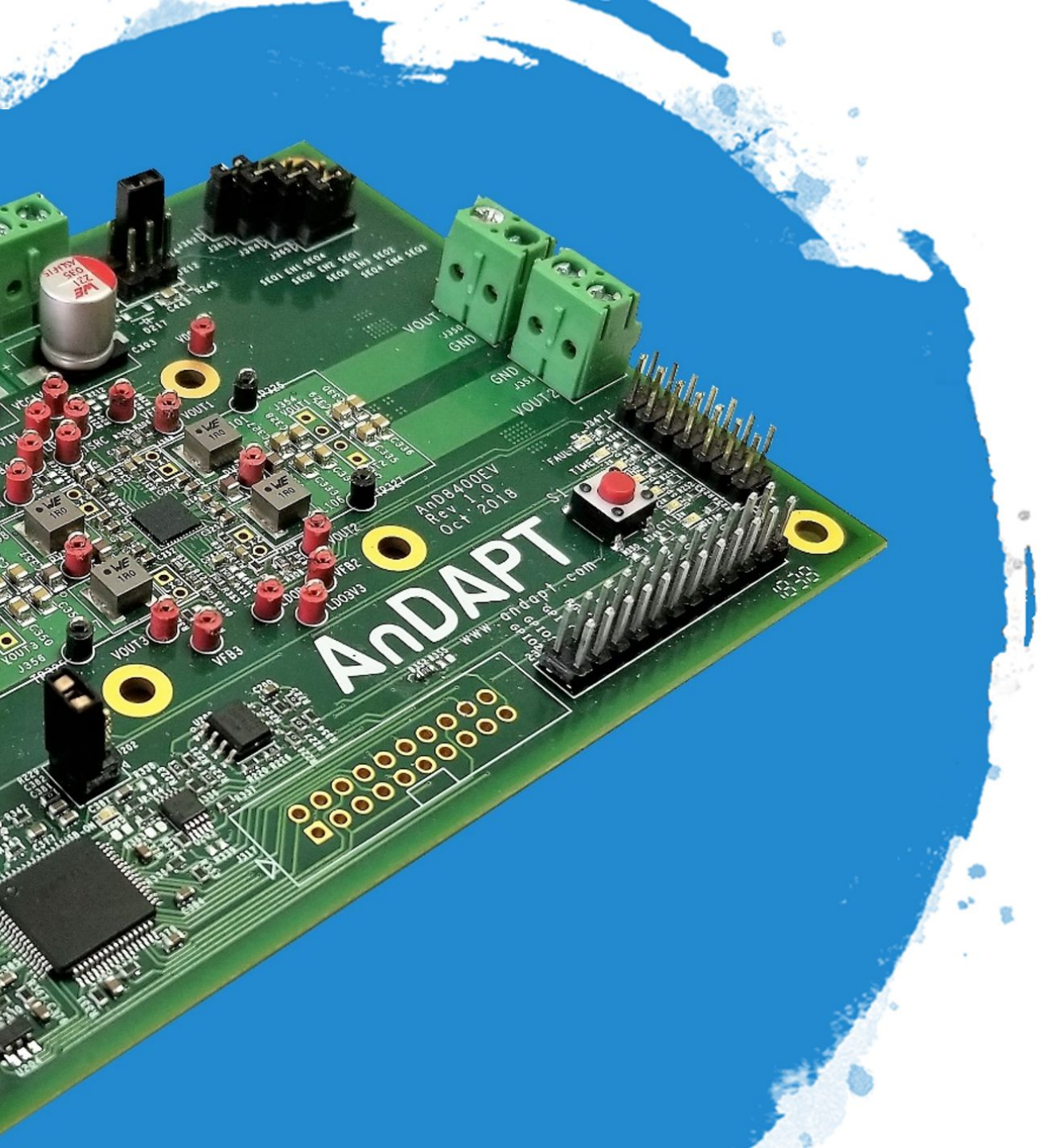




AmP8DB6QF65
ARD_X_VRPM_B_IC2
Total Area ≈ 858.71 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (Thermal View) Design Upper Loading–IC2





Test Data

Xilinx Versal Premium - M

AnDAPT

VCCO_HDIO 1.8 V / 3 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

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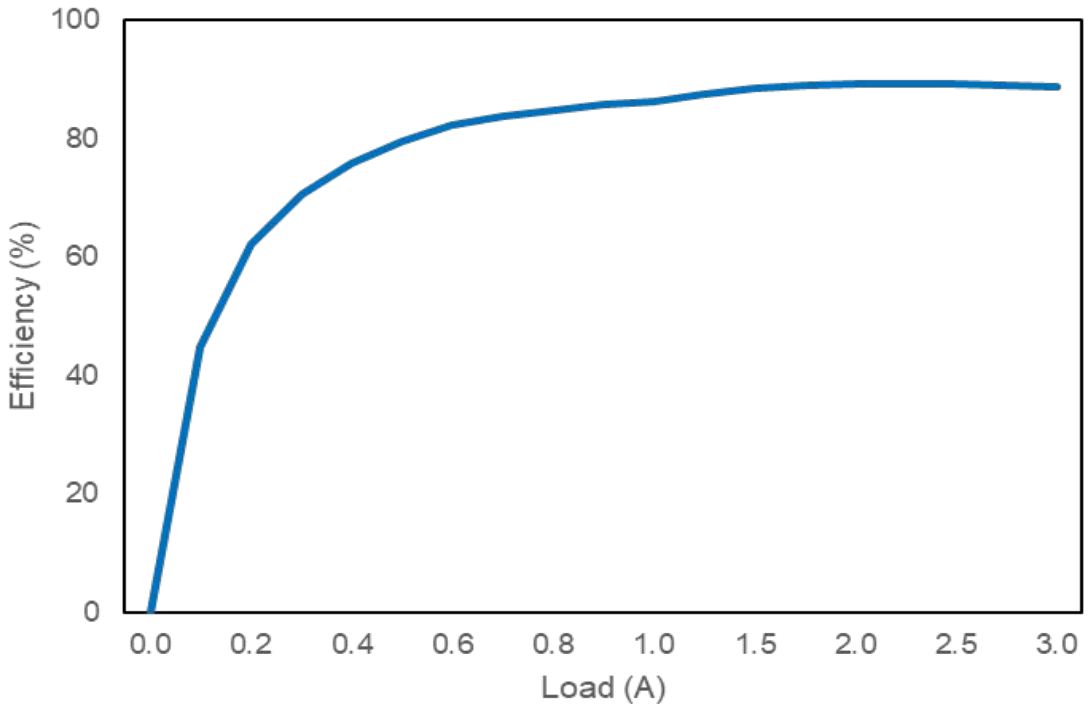
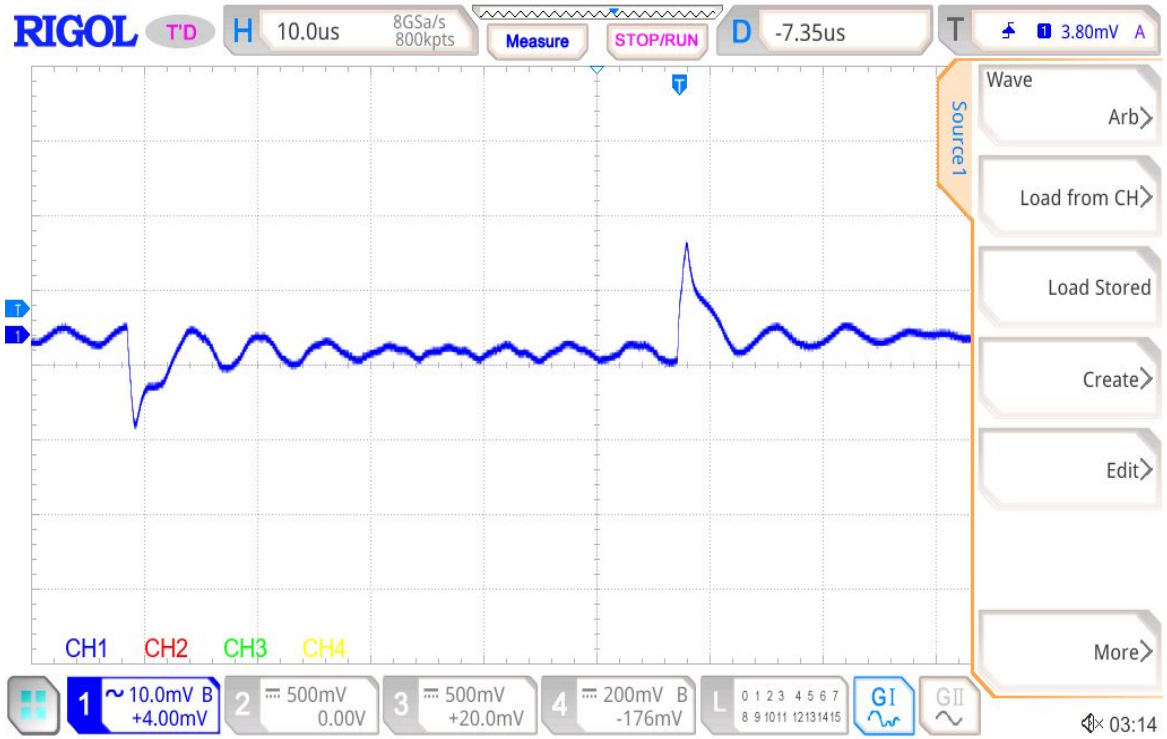
Efficiency & Transient





Vout = 1.8 V
Transient 0 A – 3 A @ 10 A/µs
V_{PP} = 32 mV
Fsw = 0.571 MHz
L = 1.1 µH, C = 3x47 uF

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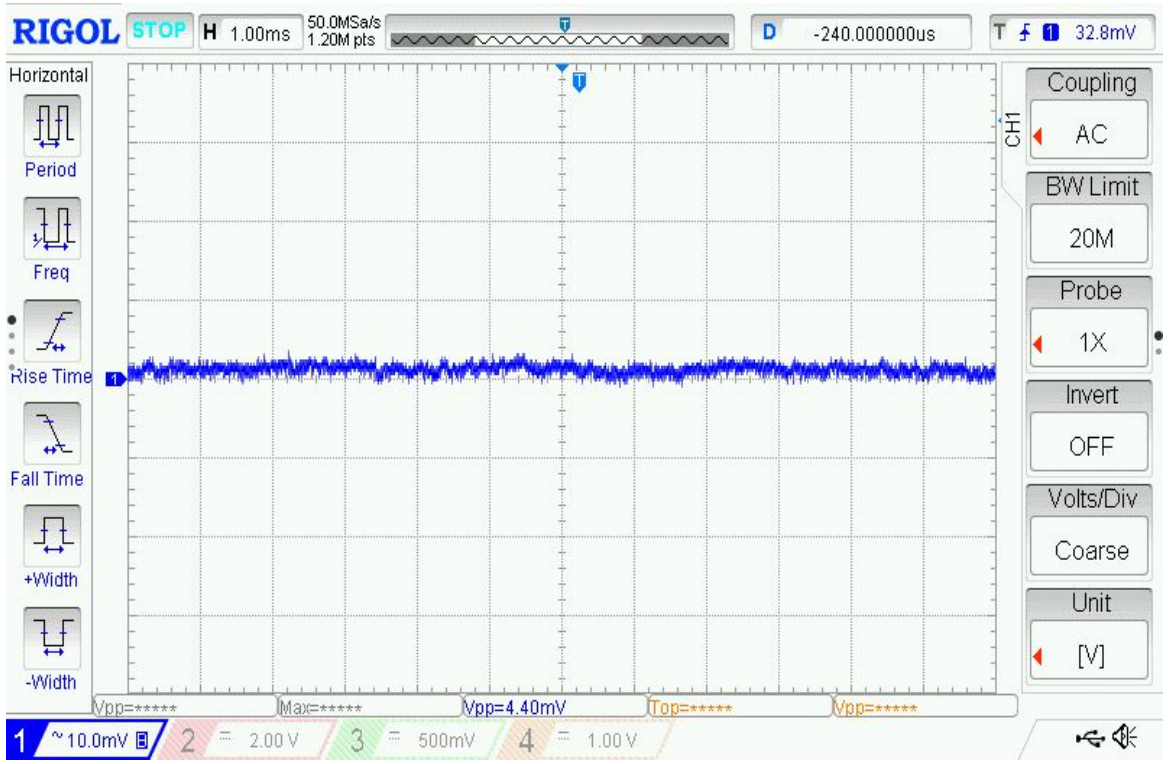
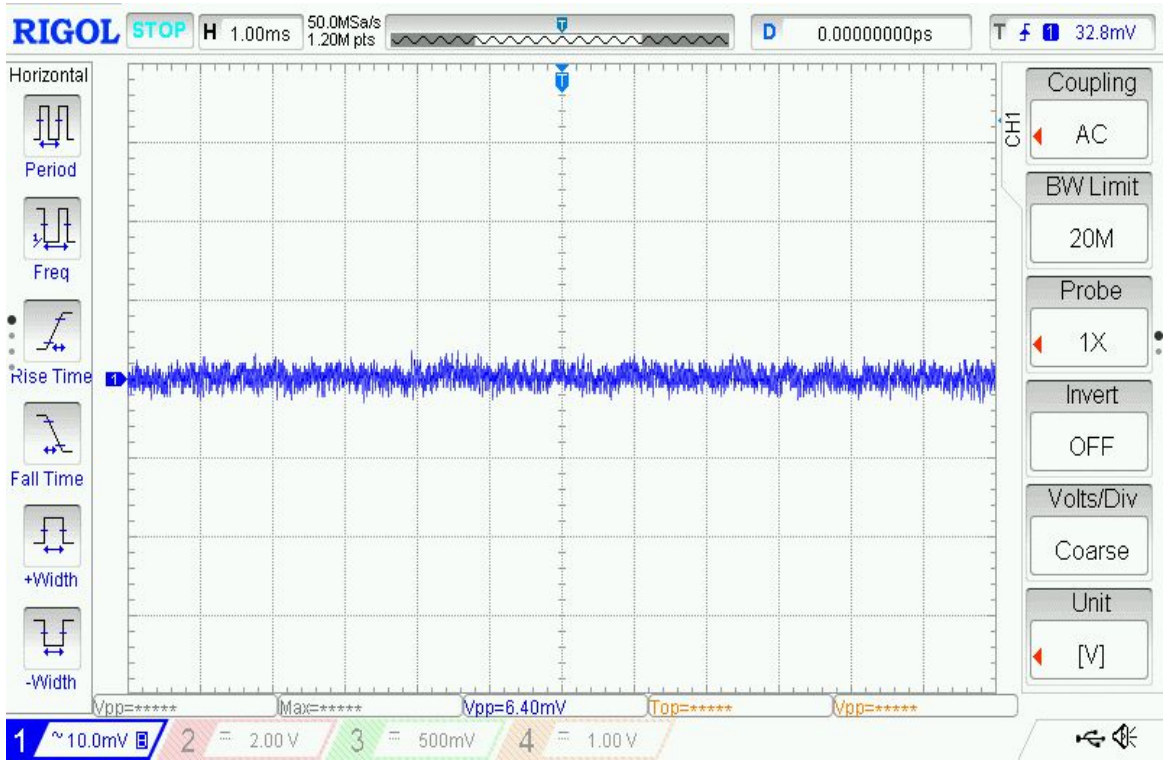
Ripple





No Load
V_{PP} = 4.40 mV

Vout = 1.8 V

3 A Load
V_{PP} = 6.4 mV

AnDAPT Confidential

VCCO_XPIO
1.5 V / 1 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

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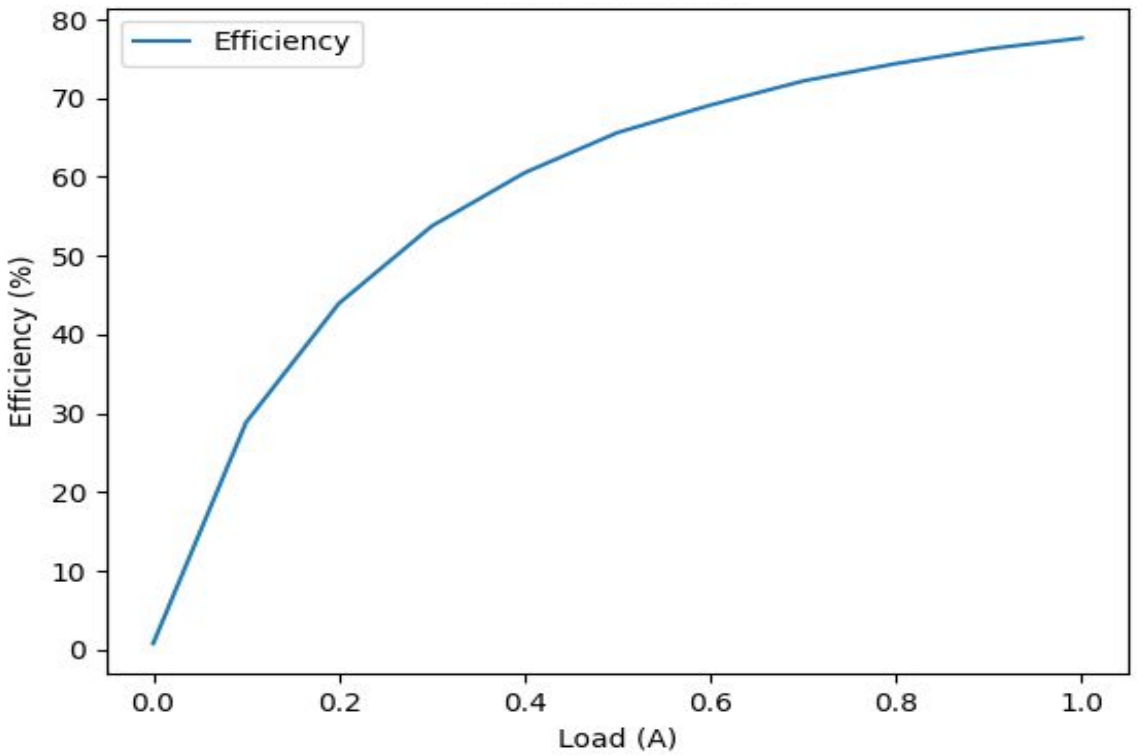
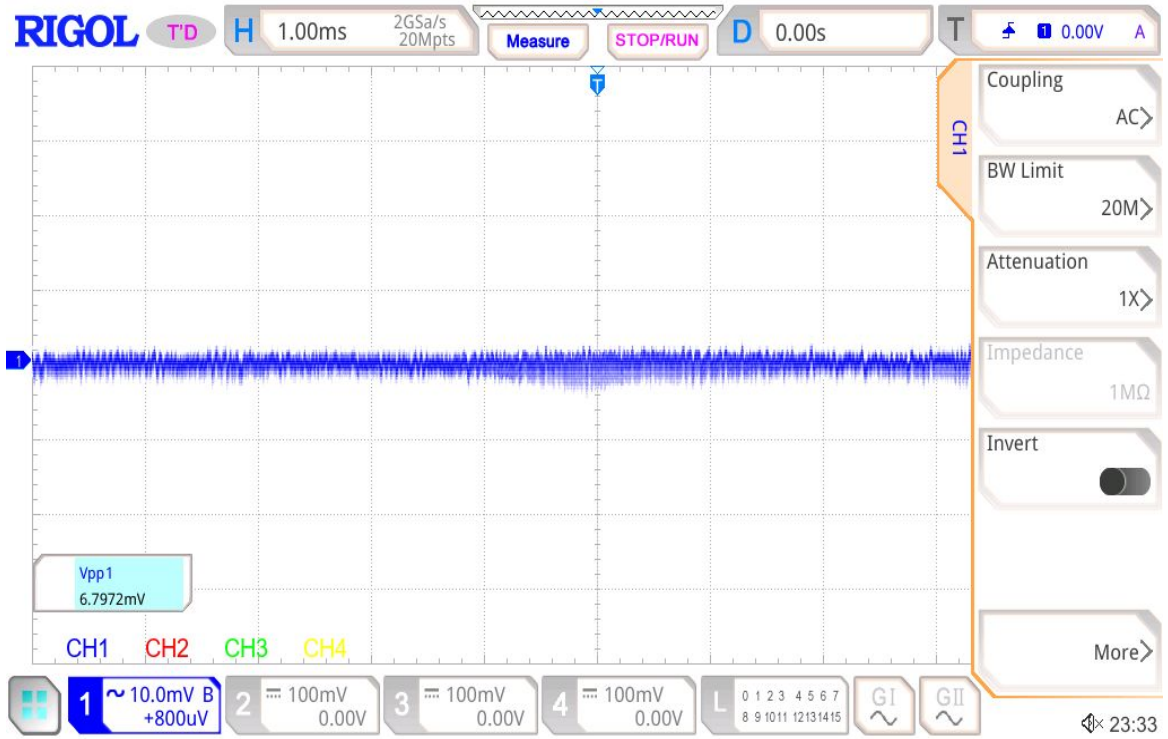
Efficiency & Transient

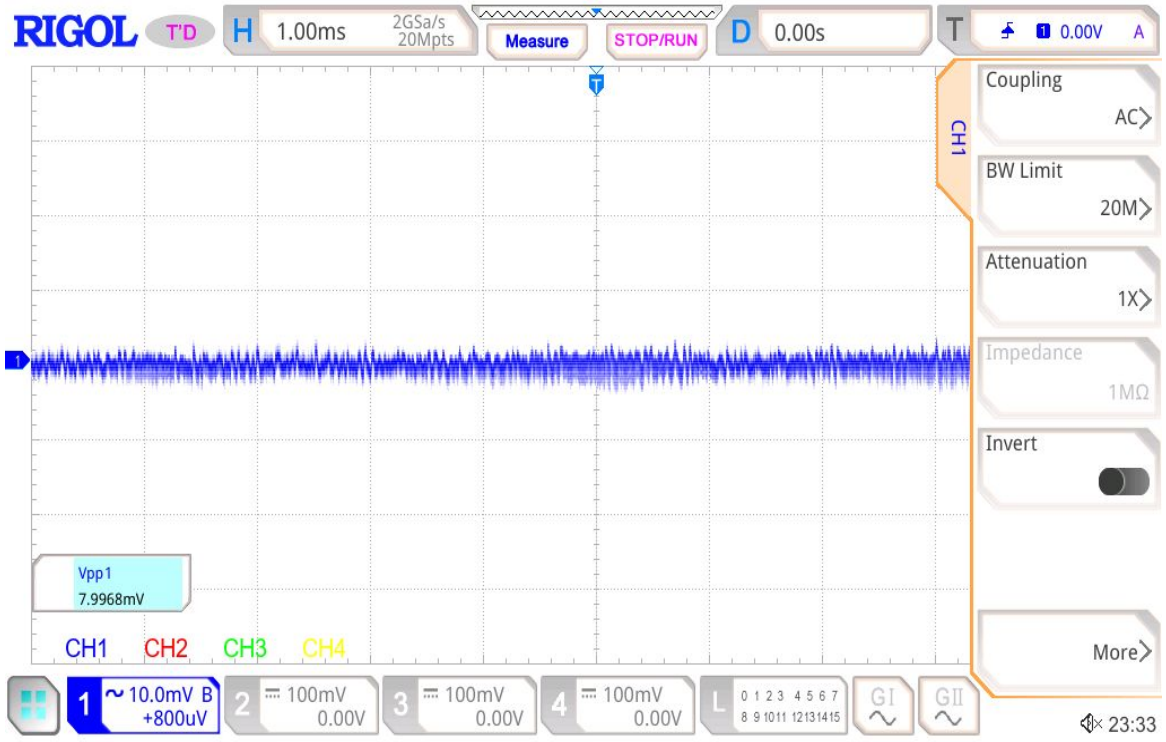


Vout = 1.5V
Transient 0.67 – 1 A@10 A/µs
V_{PP} = 24 mV
Fsw = 0.571 MHz
L = 4.7 µH, C = 1x47 uF

AnDAPT Confidential

Ripple





No Load
V_{PP} = 6.79 mV

Vout = 1.5 V

1 A Load
V_{PP} = 7.99 mV

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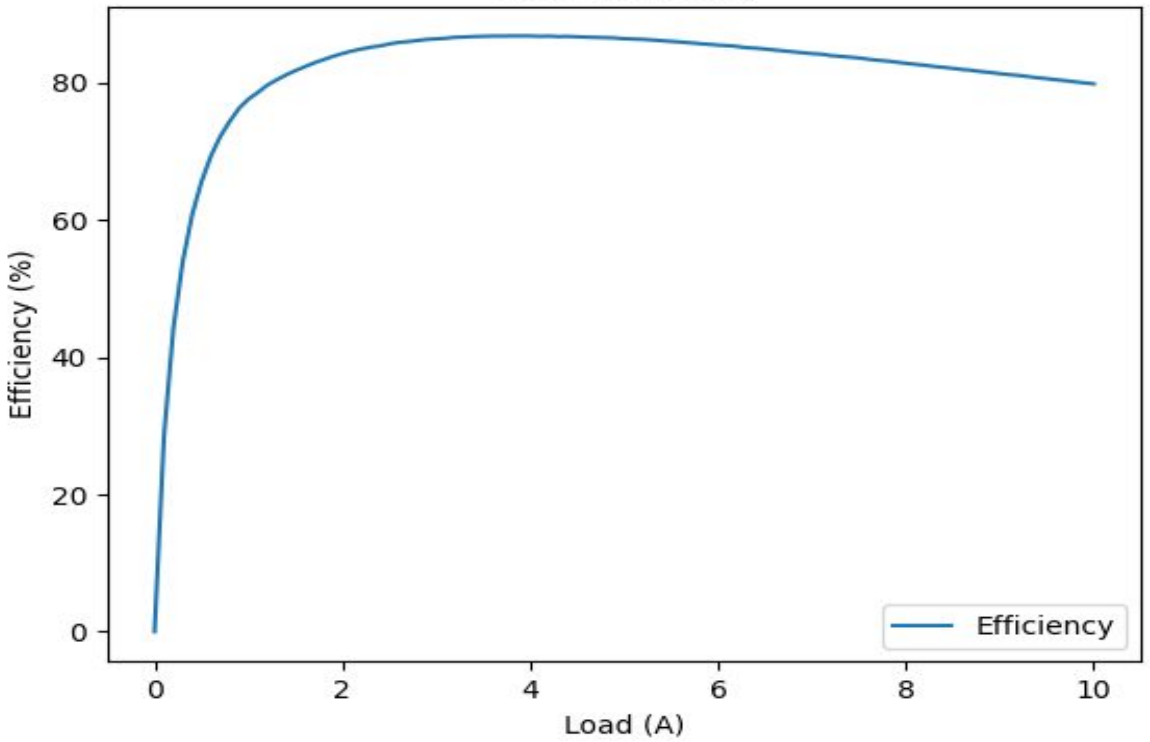
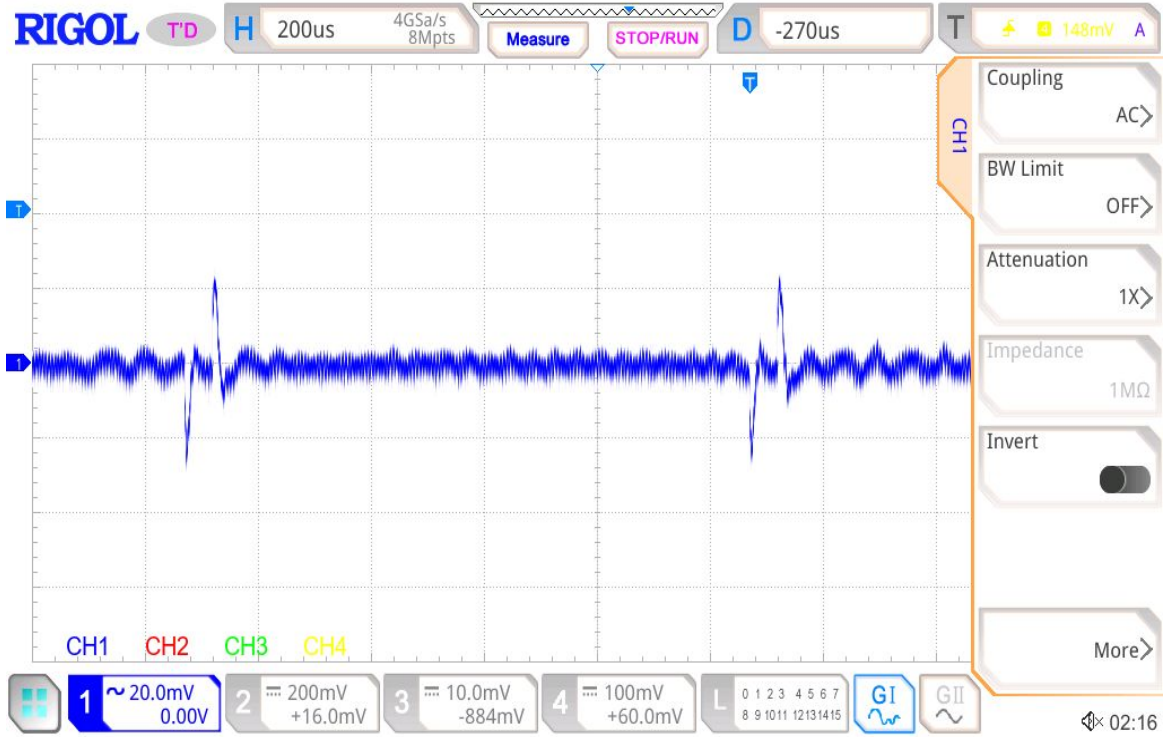
VCCAUX
1.5 V / 10 A

- C220 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 0.33 µH, P/N Wurth 744308033
- C = 7x47 uF

AnDAPT Confidential

Efficiency & Transient

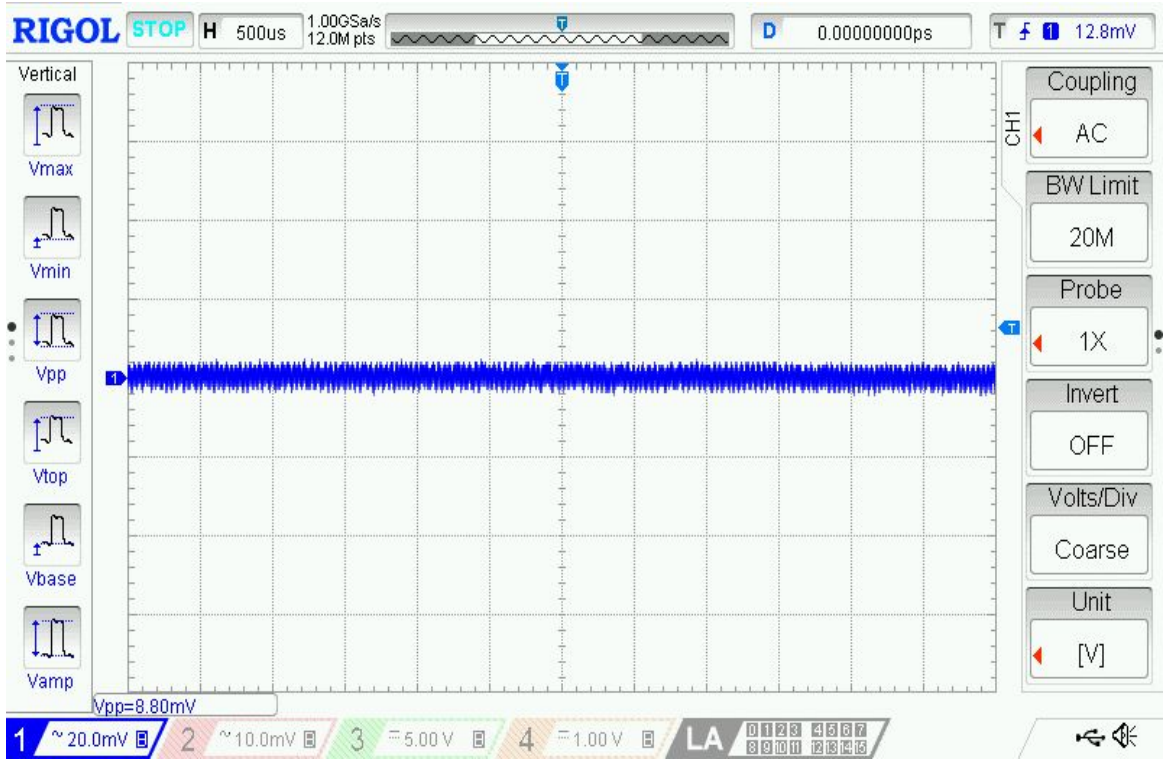


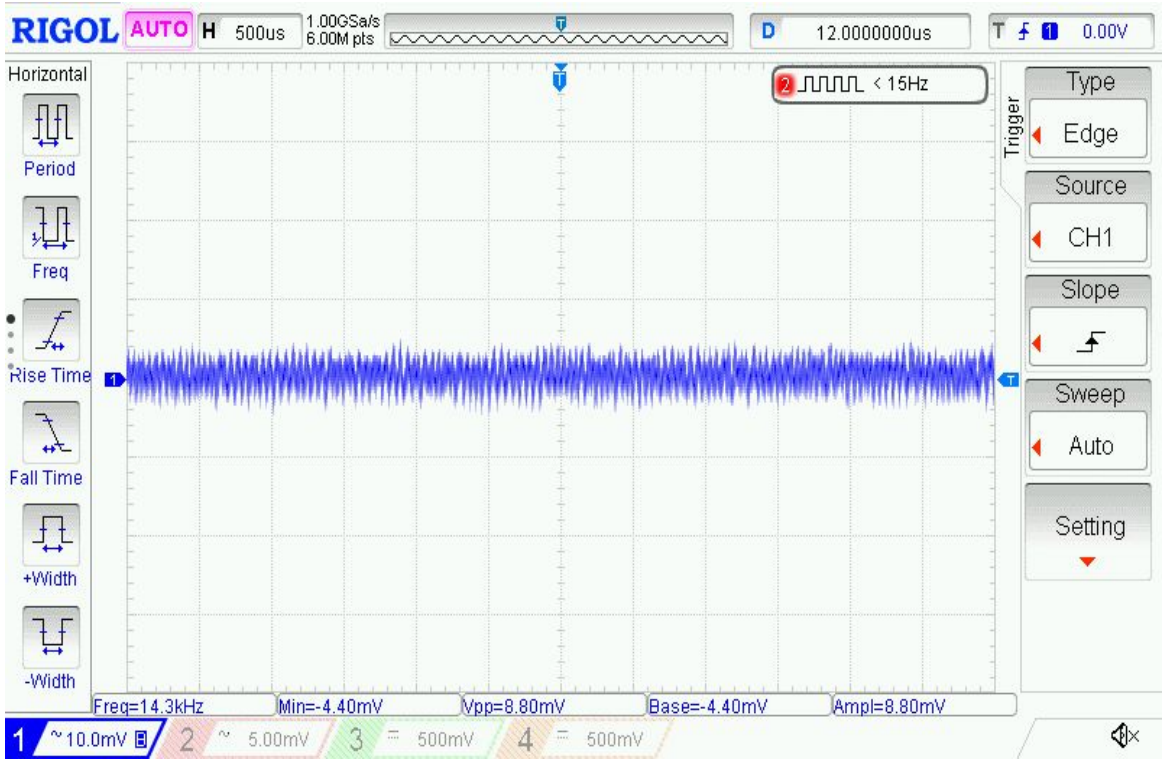


Vout = 1.5V
Transient 0.67 – 1 A@10 A/μs
V_{PP} = 52 mV
Fsw = 0.571 MHz
L = 0.33 μH, C= 7x47 uF

AnDAPT Confidential

Ripple





No Load
V_{PP} = 8.80 mV

Vout = 1.5 V

10 A Load
V_{PP} = 8.80 mV

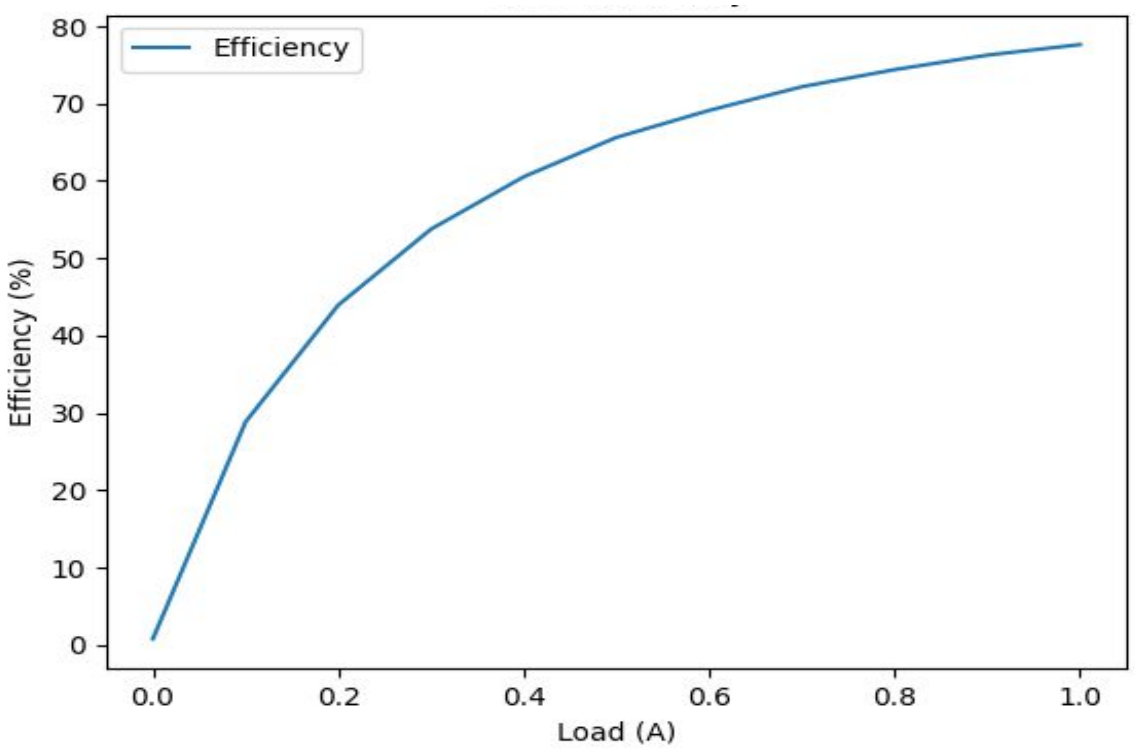
AnDAPT Confidential

MGTYAVCCAUX 1.5 V / 1 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

AnDAPT Confidential

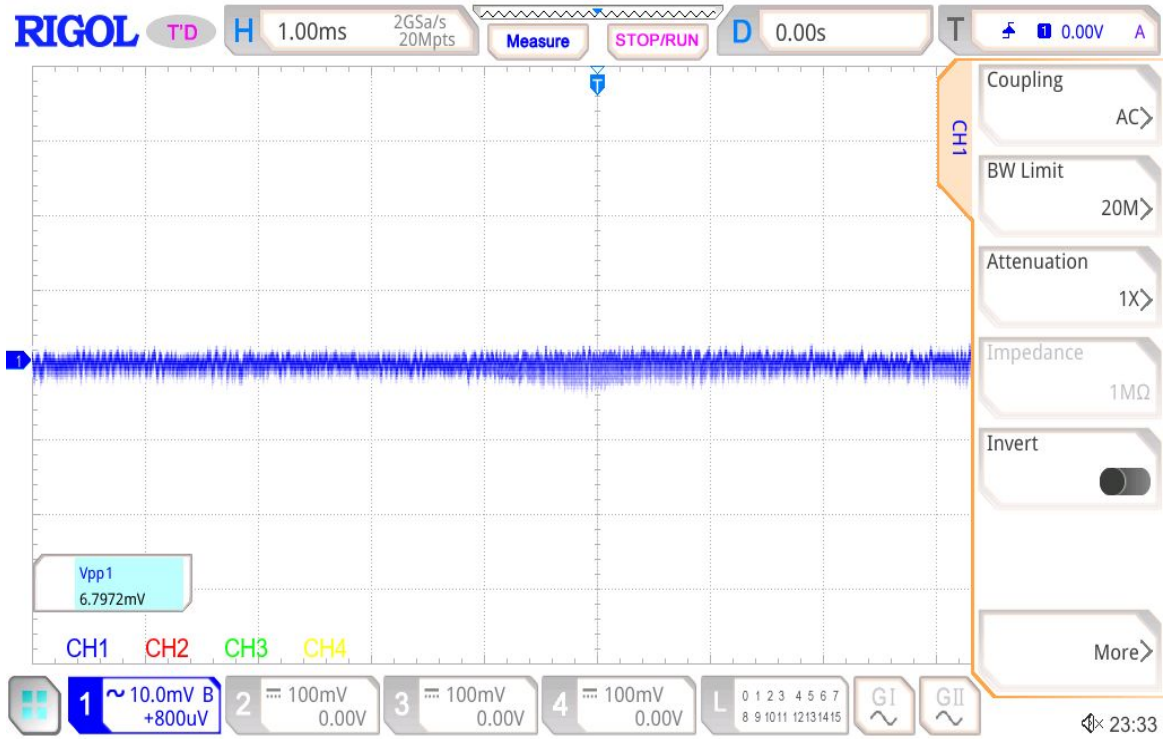
Efficiency & Transient

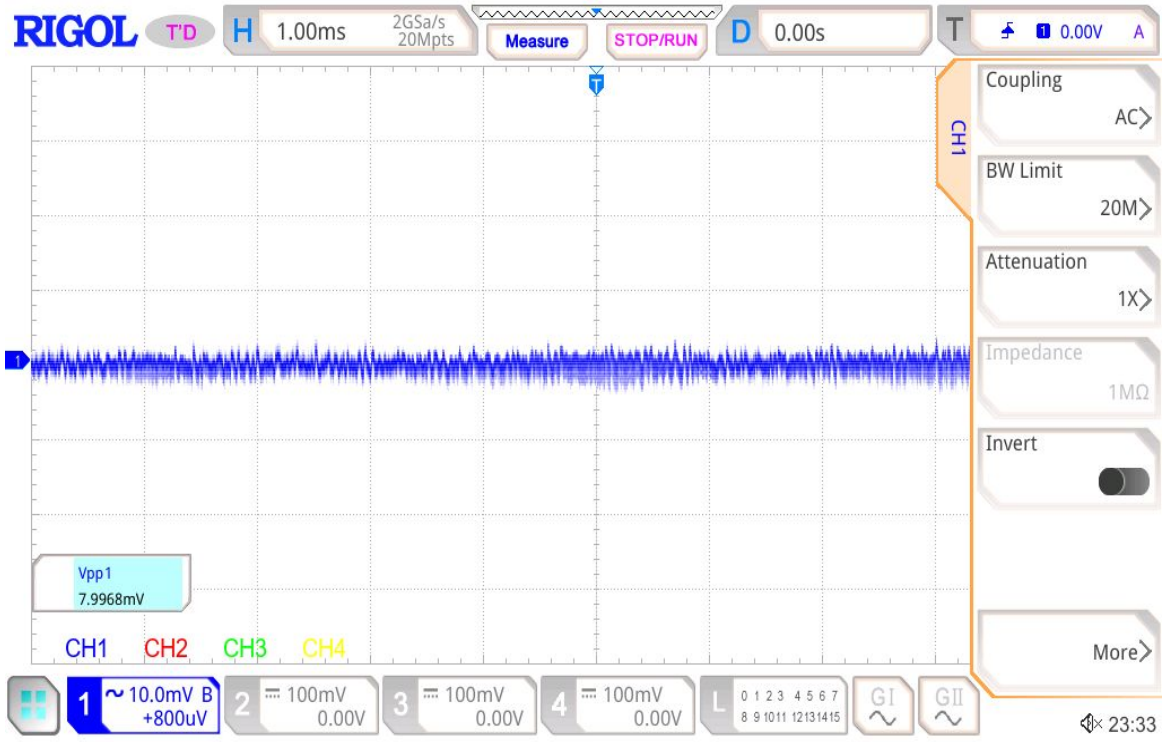


Vout = 1.5V
Transient 0.67 – 1 A@10 A/µs
V_{PP} = 24 mV
Fsw = 0.571 MHz
L = 4.7 µH, C = 1x47 uF

AnDAPT Confidential

Ripple





No Load
V_{PP} = 6.79 mV

Vout = 1.5 V

1 A Load
V_{PP} = 7.99 mV

AnDAPT Confidential

MGTYAVCC
0.88 V / 15 A

- C865 (Single-Phase DrMOS)
- Fsw = 0.571 MHz
- L = 0.25 µH, P/N Wurth 744301025
- C = 10x47 uF

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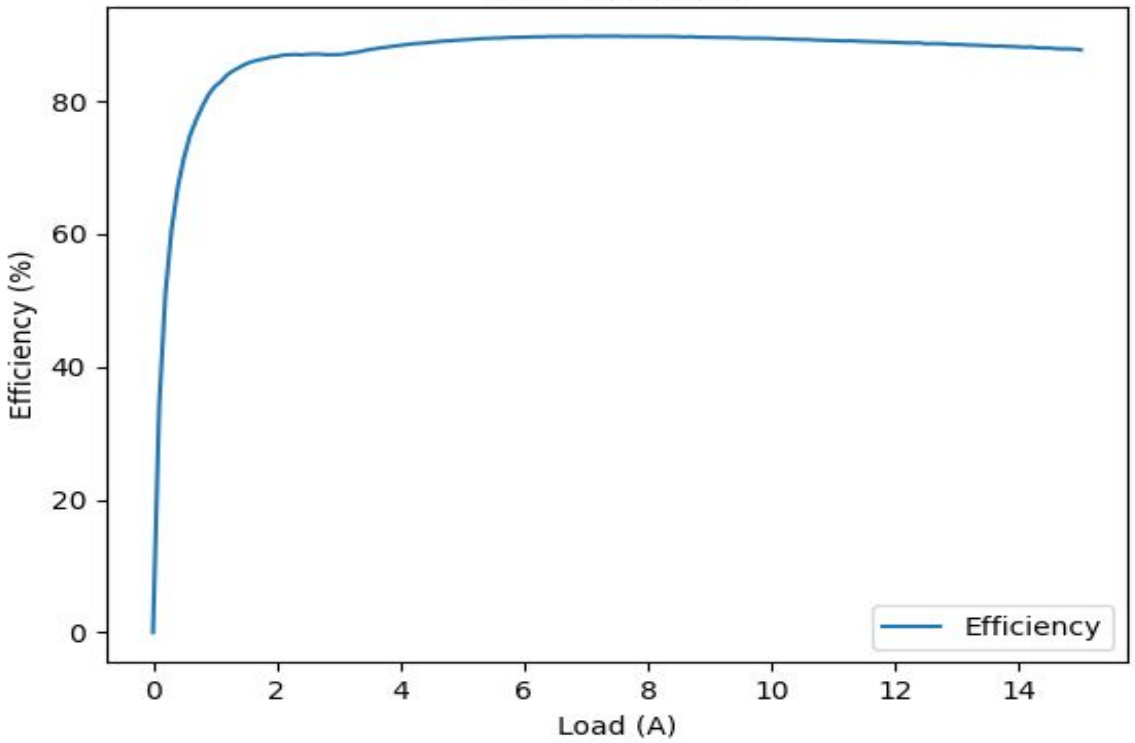
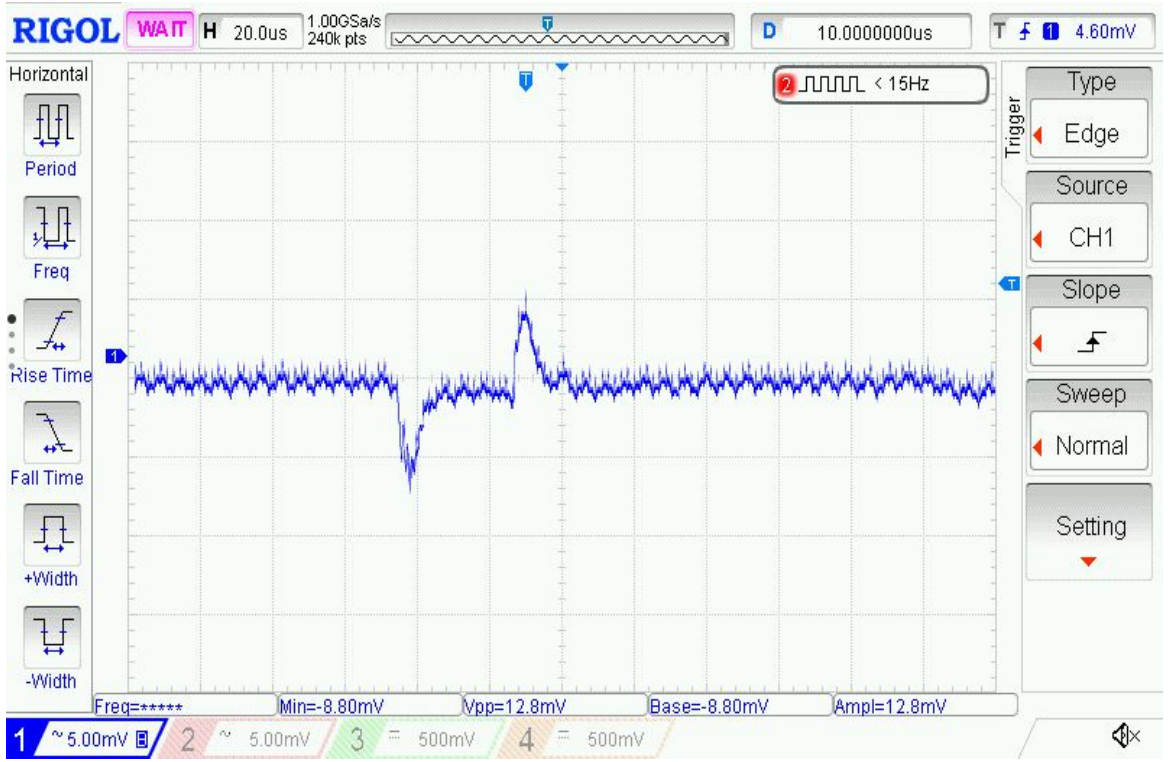
Efficiency & Transient





Vout = 0.88 V
Transient 10.05 – 15 A@10 A/μs
V_{PP} = 12.80 mV
Fsw = 0.571 MHz
L = 0.25 μH, C = 10x47 uF

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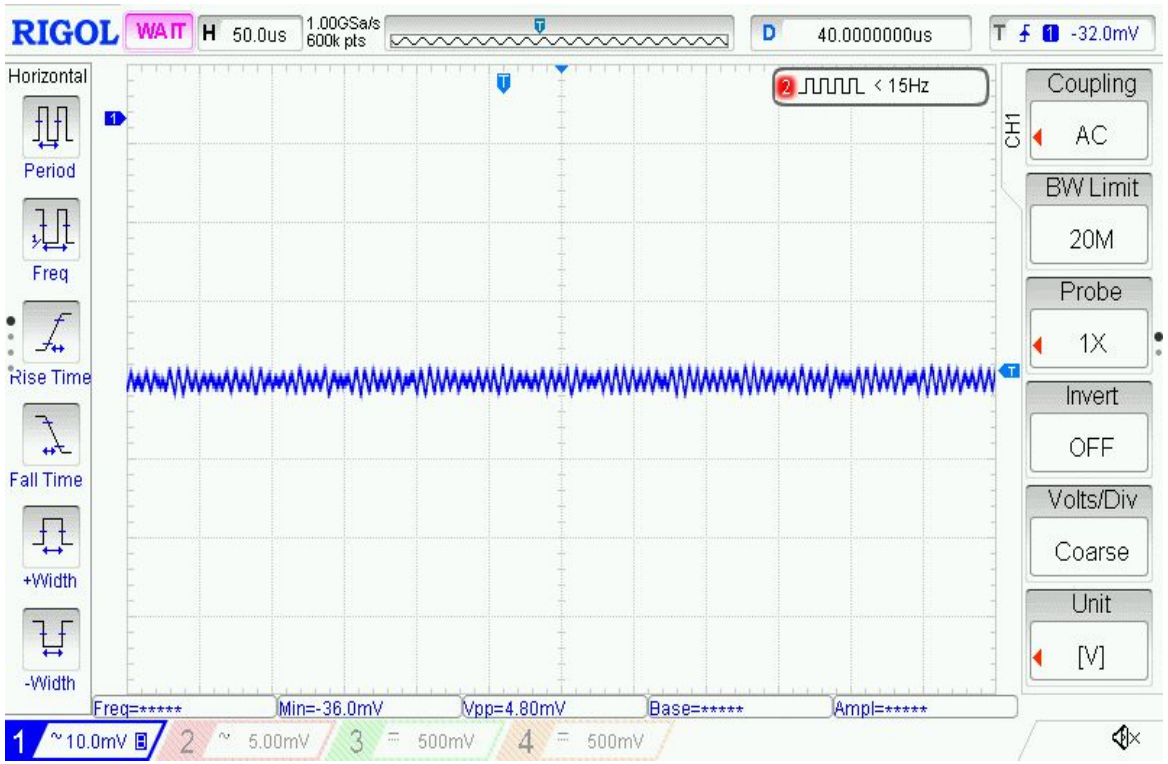
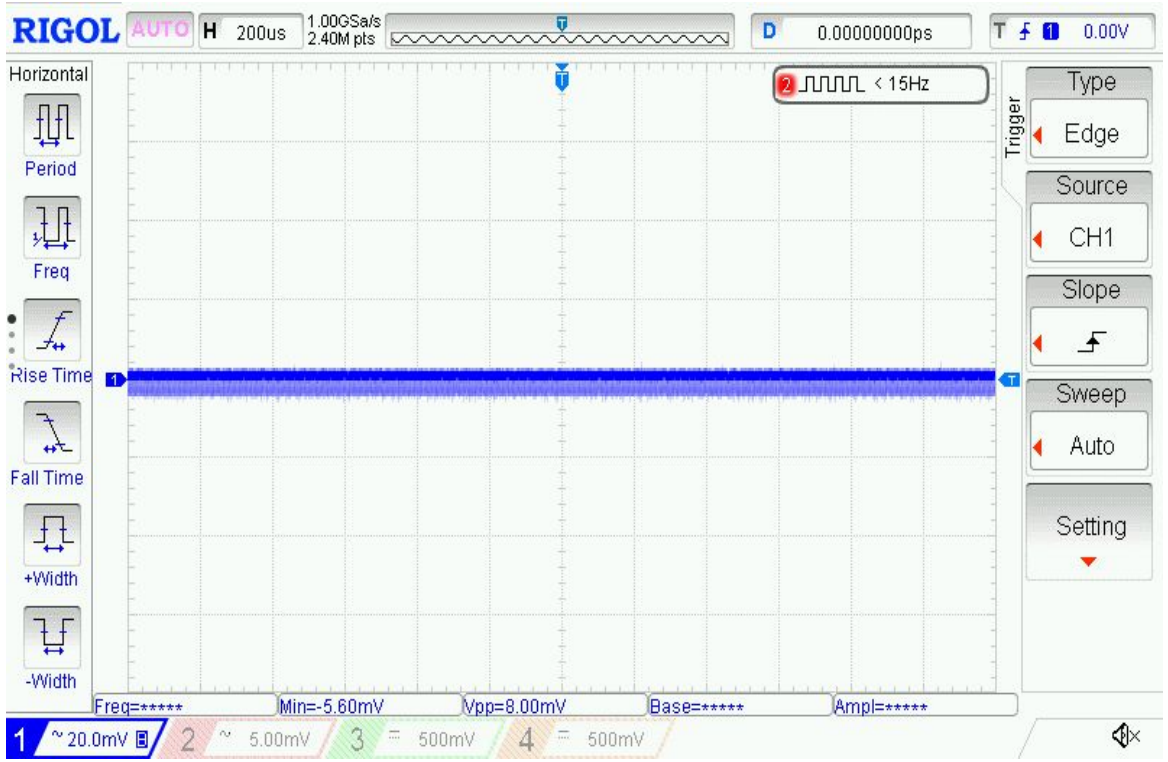
Ripple





No Load
V_{PP} = 4.80 mV

Vout = 0.88 V

15 A Load
V_{PP} = 8 mV

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MGTYAVTT
1.2 V /24 A

- C860 (Single-Phase DrMOS)
- Fsw = 0.571 MHz
- L = 0.25 µH, P/N Wurth 744301025
- C = 10x47 uF + 1x47 uF

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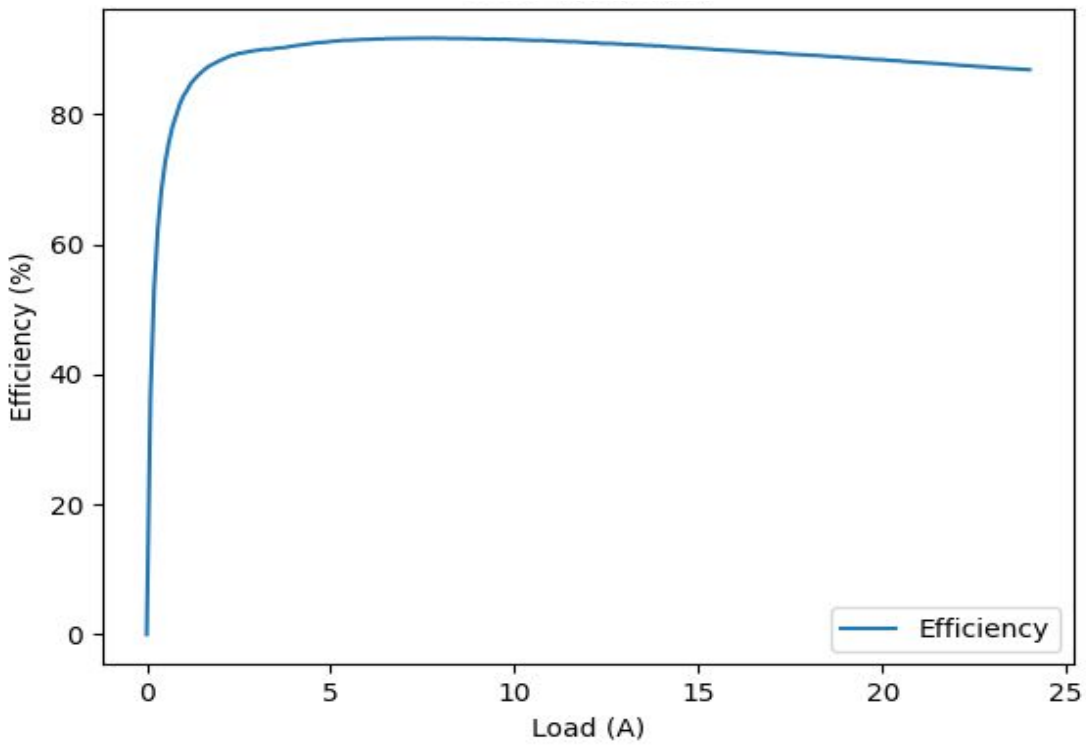
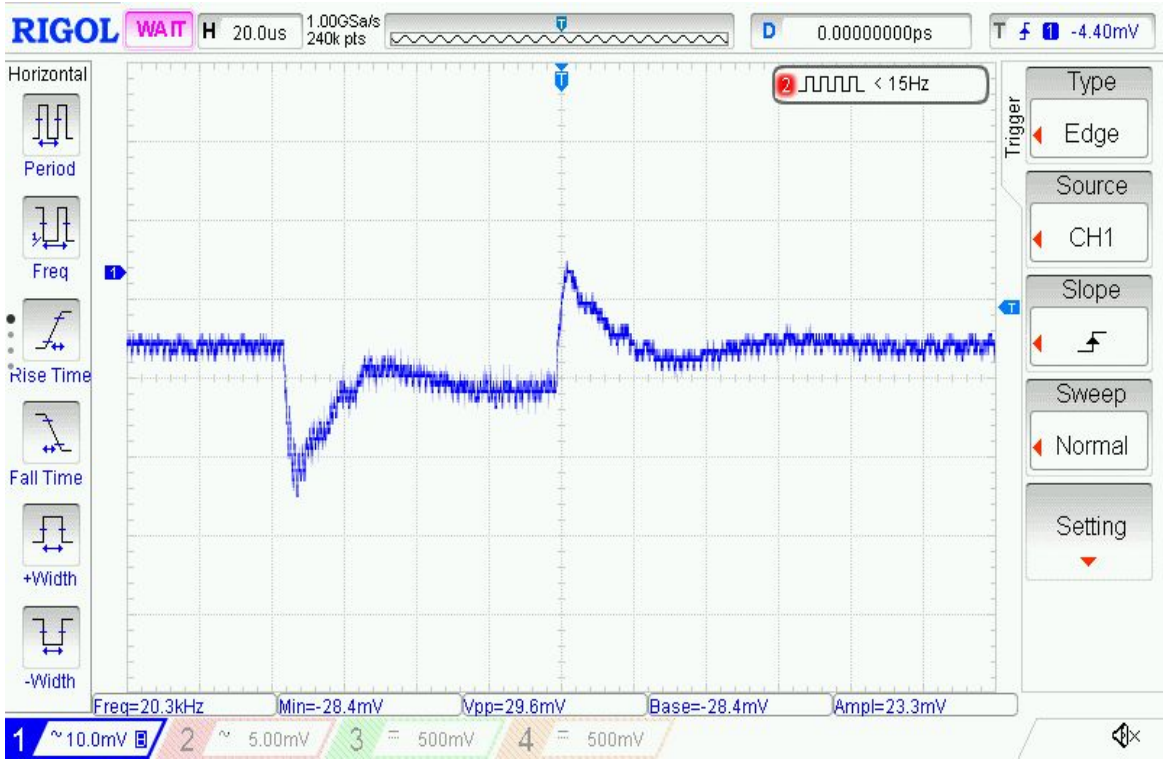
Efficiency & Transient

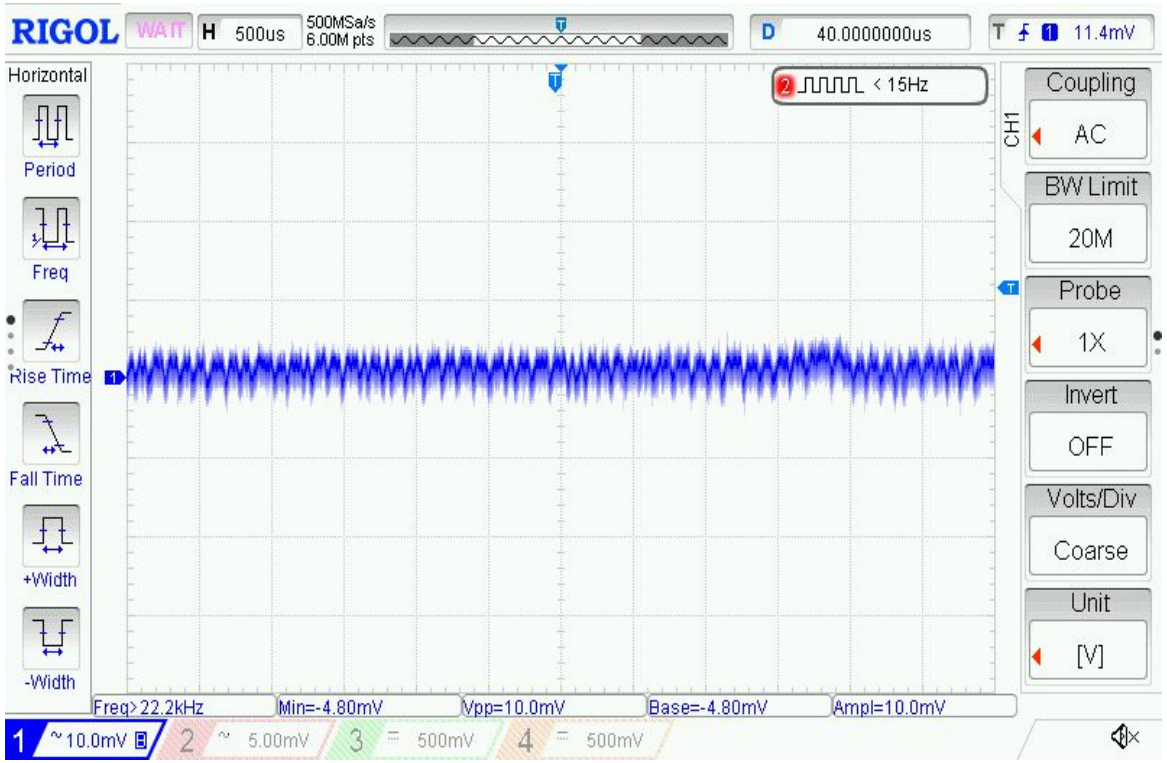


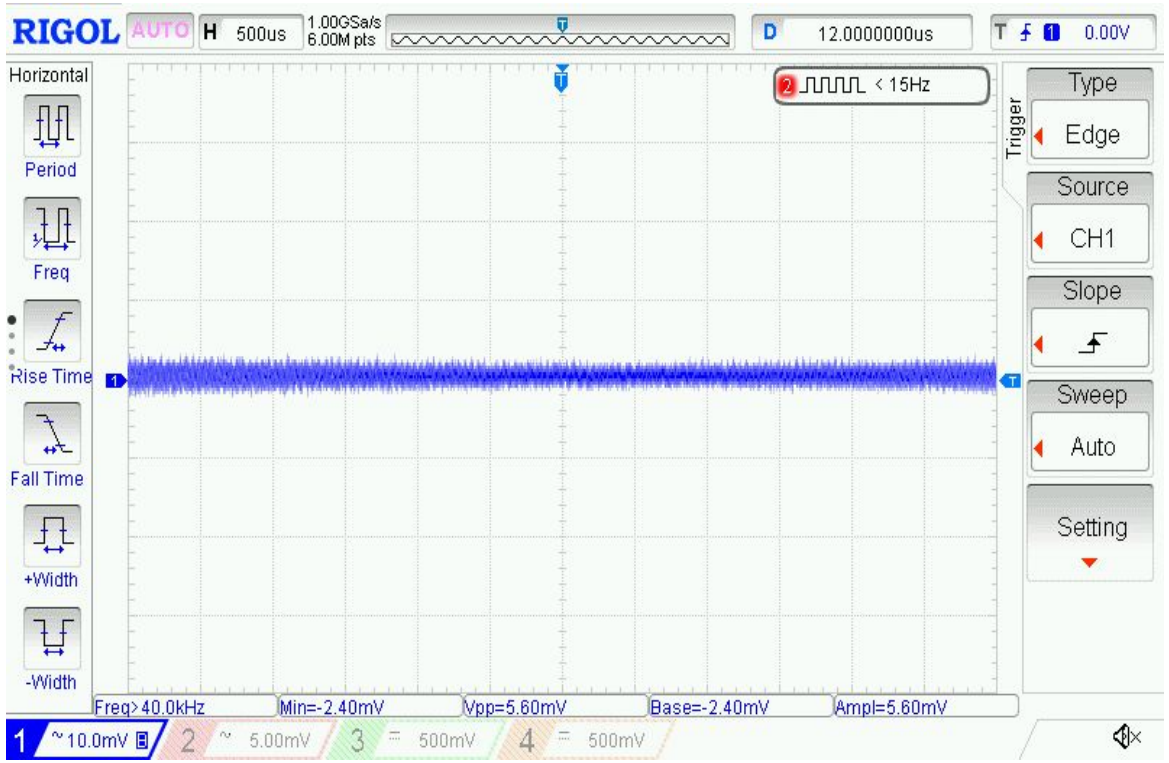


Vout = 1.2V
Transient 16.08 – 24 A@10 A/µs
V_{PP} = 29.6 mV
Fsw = 0.571 MHz
L = 0.25 µH, C = 10x47 uF + 1x47 uF

AnDAPT Confidential

Ripple





No Load
V_{PP} = 10 mV

Vout = 1.2 V

24 A Load
V_{PP} = 5.60 mV

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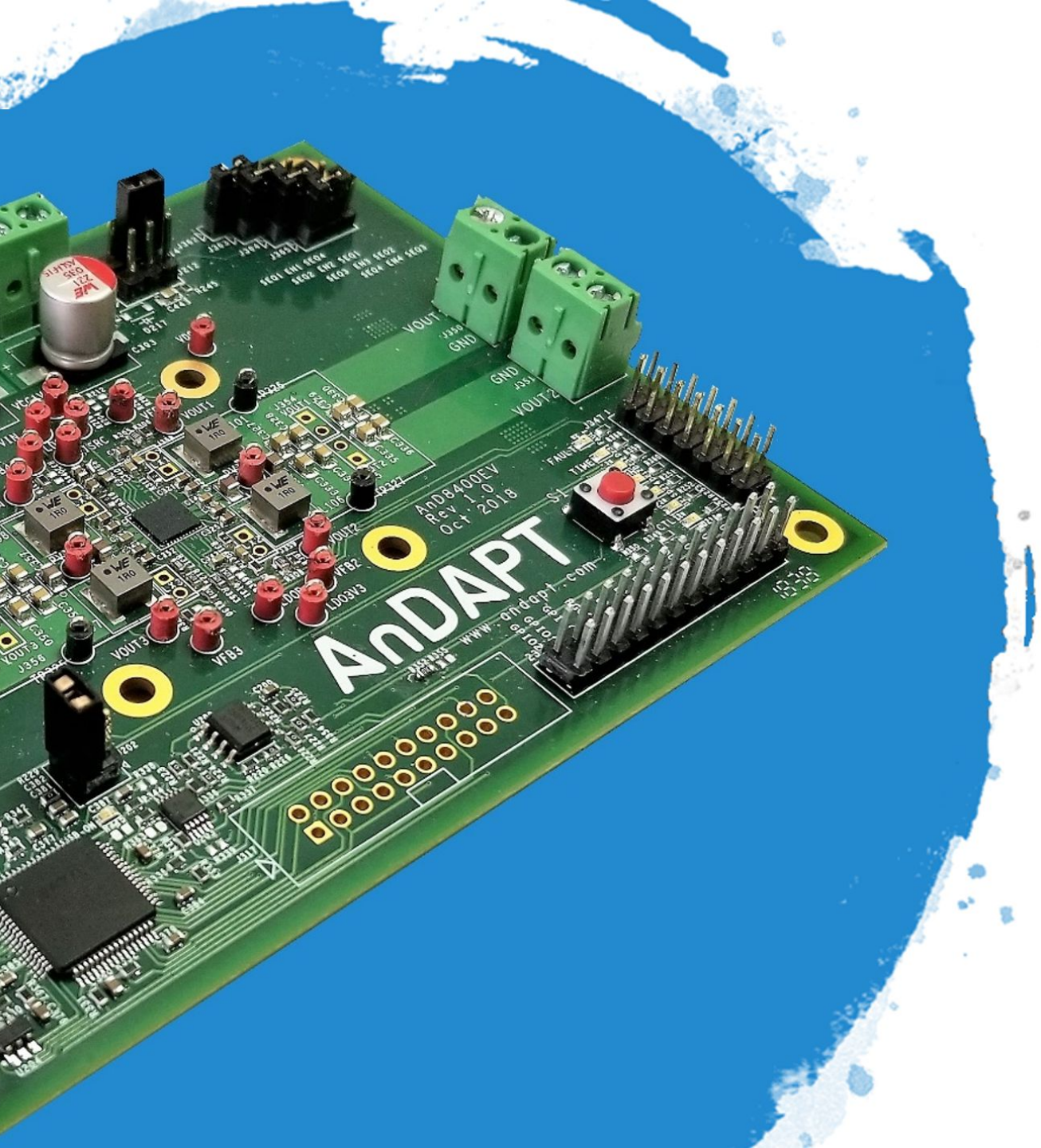

Thank You

AnDAPT