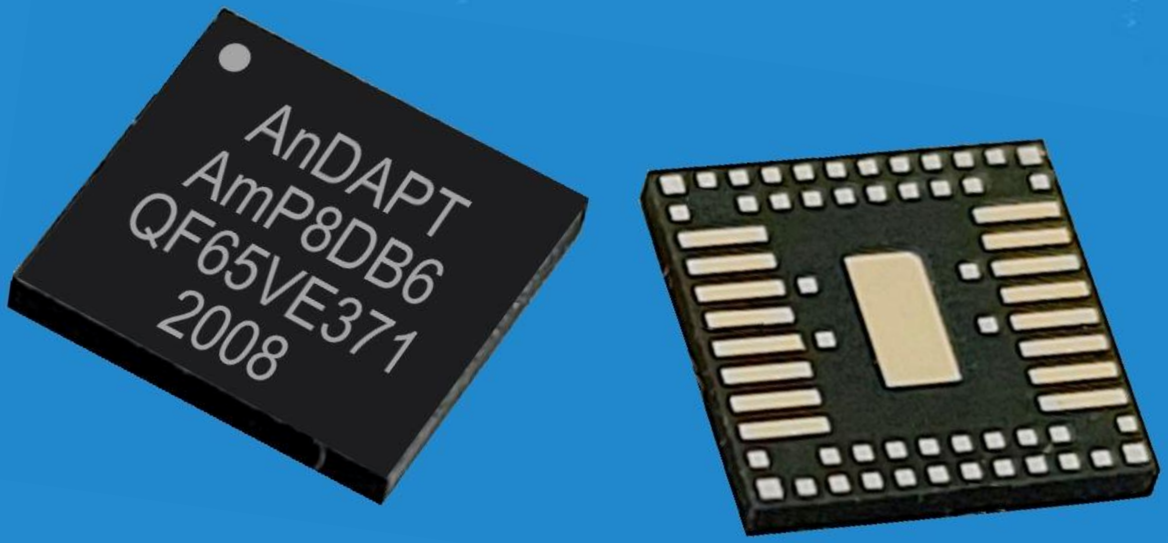

Xilinx Versal Prime (Minimum Rails, Low Voltage) Power Solution

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Versal Prime (Minimum Rails, Low Voltage) Power Mapping Highlights

- Power tree mappings completed as per data received from Xilinx Power Management team.
- Both Typical and Upper use-cases are served by the same design.
- Data gathered and bench tested by the applications team at AnDAPT.
  - Data meets or exceeds Xilinx power and timing specifications.
- Total 10 power rails covered by 2x AmP ICs including memory and termination rails.
- Total solution area is 1625.47 mm^2.
- Presentation contains thermal views of both ICs.

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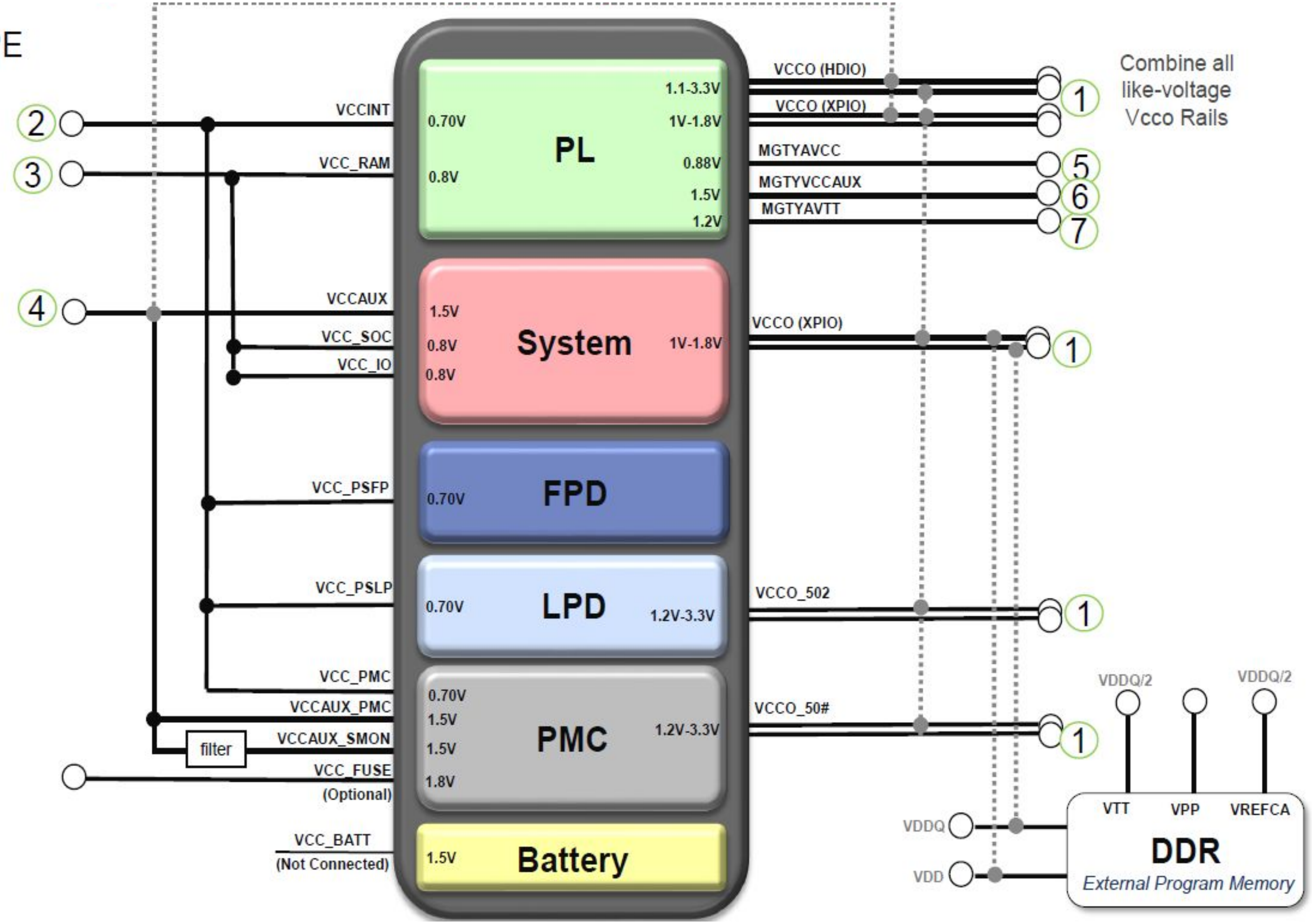
Xilinx Versal Prime Power Tree

Check the latest XPE on Xilinx.com for supported rail groupings and sequences



Versal Prime (Minimum Rails, Low Voltage)Power Rails: Typical and Upper

Sequence	Rail Name	Voltage (V)	Prime	
			Typical (A)	Upper (A)
Rail 1	VCCINT, VCC_PSLP, VCC_PSFP, VCC_PMC	0.7V	45.45	54.54
Rail 2	VCC_IO, VCCRAM, VCC_SOC	0.8V	4.88	5.856
Rail 3	VCCAUX, VCCAUX_SMON, VCCAUX_PMC	1.5V	3.1	3.72
Rail 4	MGTAVCC	.88V	2.47	3.08
Rail 5	MGTAVAUX	1.5V	0.23	0.29
Rail 6	MGTAVTT	1.2V	3.85	4.81
Rail 7	VCCO[0....] (HDIO)	1.1V-3.3V, 1V-1.8V, 1.2V-3.3V	3.39	4.068
Current Total (A)			**56.82**	**68.184**

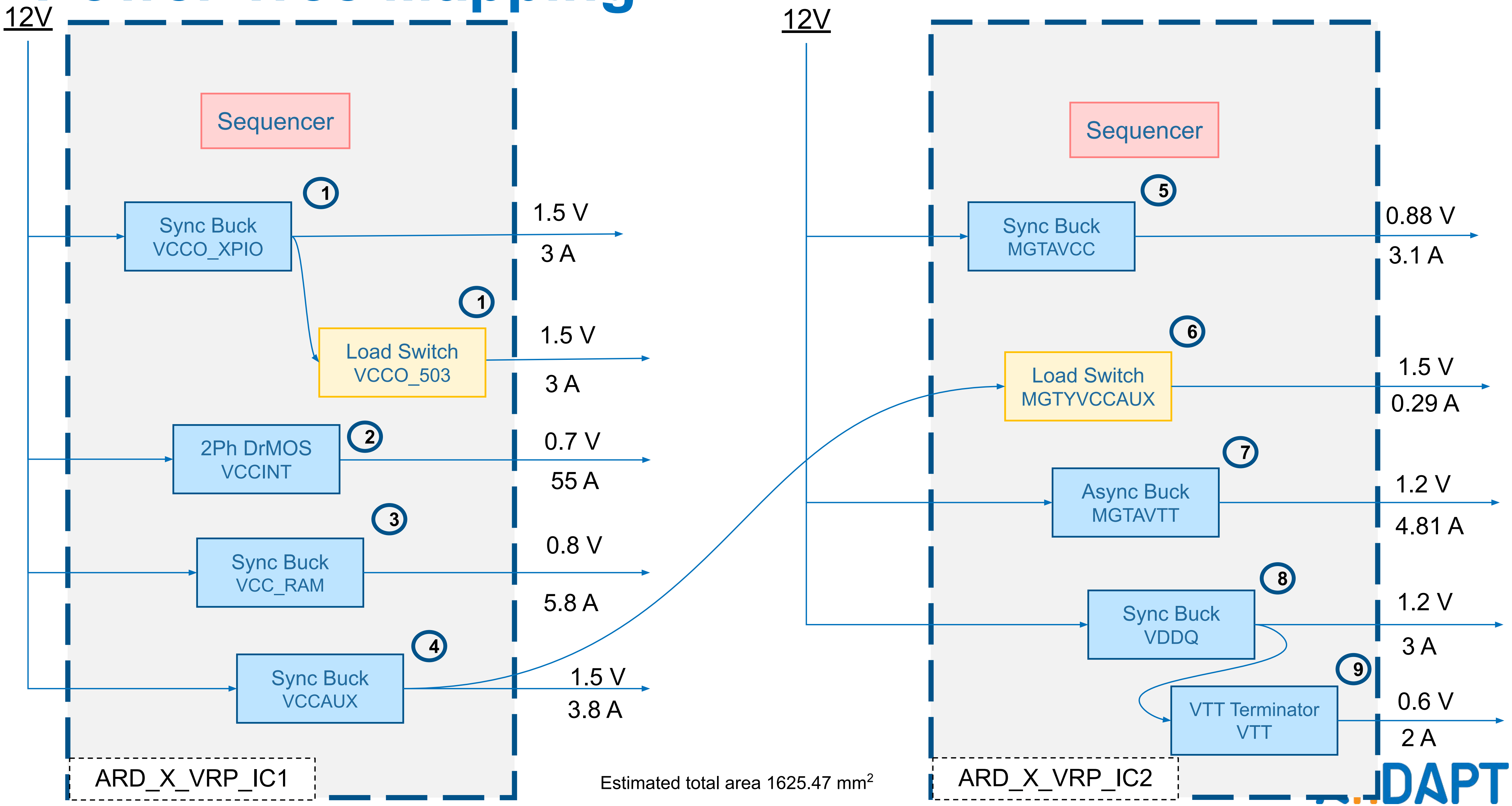
Versal Prime (Minimum Rails, Low Voltage) Power Tree Mapping

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCO_XPIO (VCCO_XPIO, VCCO_HDIO)	1	Sync Buck	C200	PVIN	12	1.5	3+3	ARD_X_VRP_IC1
2	VCCO_503 (VCCO_502, VCCO_50X)	1	Load Switch	C200	VCCO_XPIO	12	1.5	3	
3	VCCINT (VCCINT, VCC_PMC, VCC_PSFP, VCC_PSLP)	2	Two-Phase DrMOS	C870	PVIN	12	0.7	55	
4	VCC_RAM (VCC_RAM, VCC_SOC, VCC_IO)	3	Sync Buck	C200	PVIN	12	0.8	5.8	
5	VCCAUX (VCCAUX, VCCAUX_PMC, VCCAUX_SMON)	4	Sync Buck	C200	PVIN	12	1.5	3.8 + 0.29	
6	MGTAVCC	5	Sync Buck	C200	PVIN	12	0.88	3.1	ARD_X_VRP_IC2
7	MGTYVCCAUX	6	Load Switch	C750	VCCAUX	1.5	1.5	0.29	
8	MGTAVTT	7	Async Buck	C150	PVIN	12	1.2	4.81	
9	VDDQ	8	Sync Buck	C200	PVIN	12	1.2	3 + 2	
10	VTT	9	VTT Terminator	C210	VDDQ	1.2	0.6	2	

PVIN = 12V

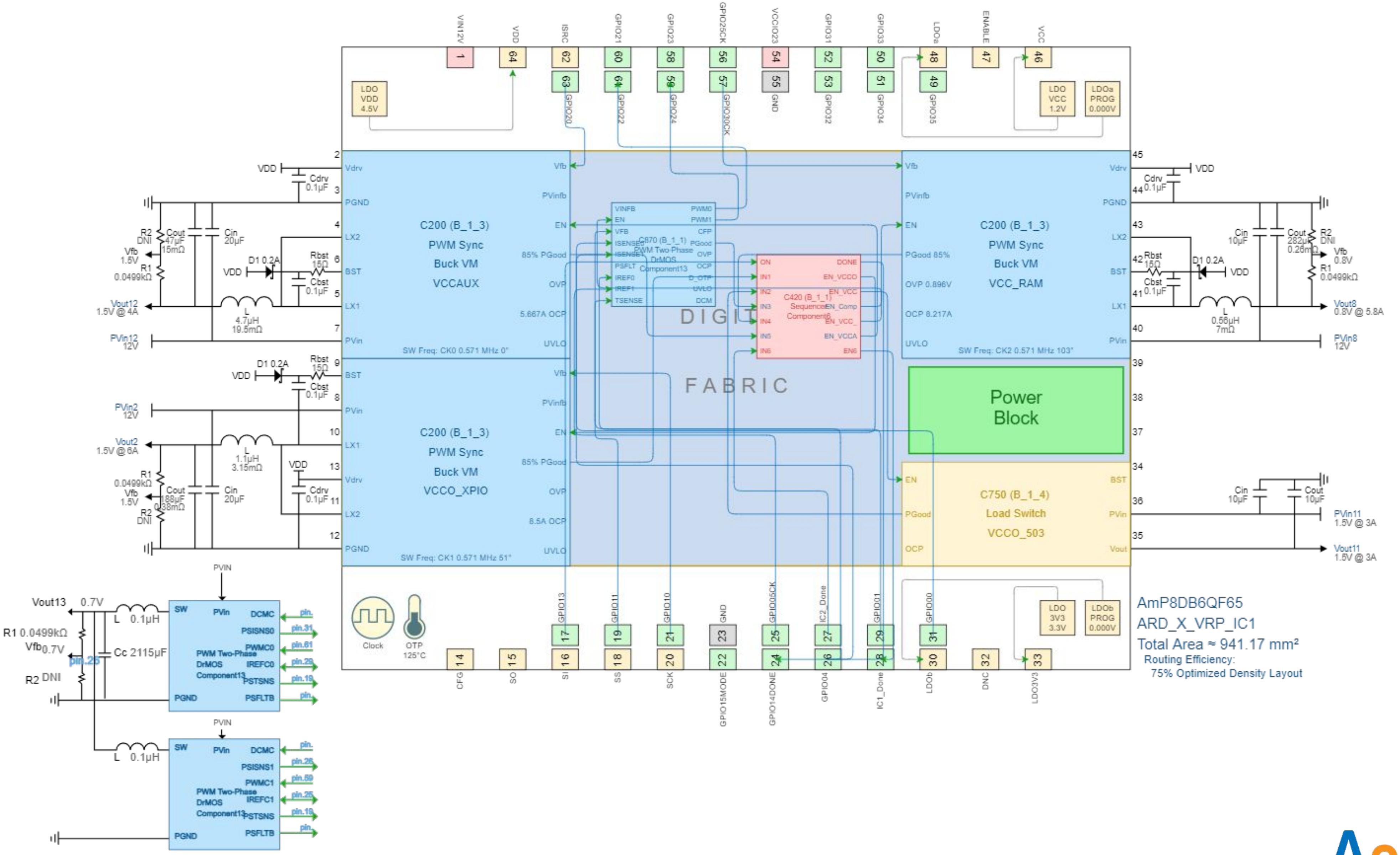
Total estimated solution area = 1625.47 mm^2

Versal Prime (Minimum Rails, Low Voltage) Power Tree Mapping

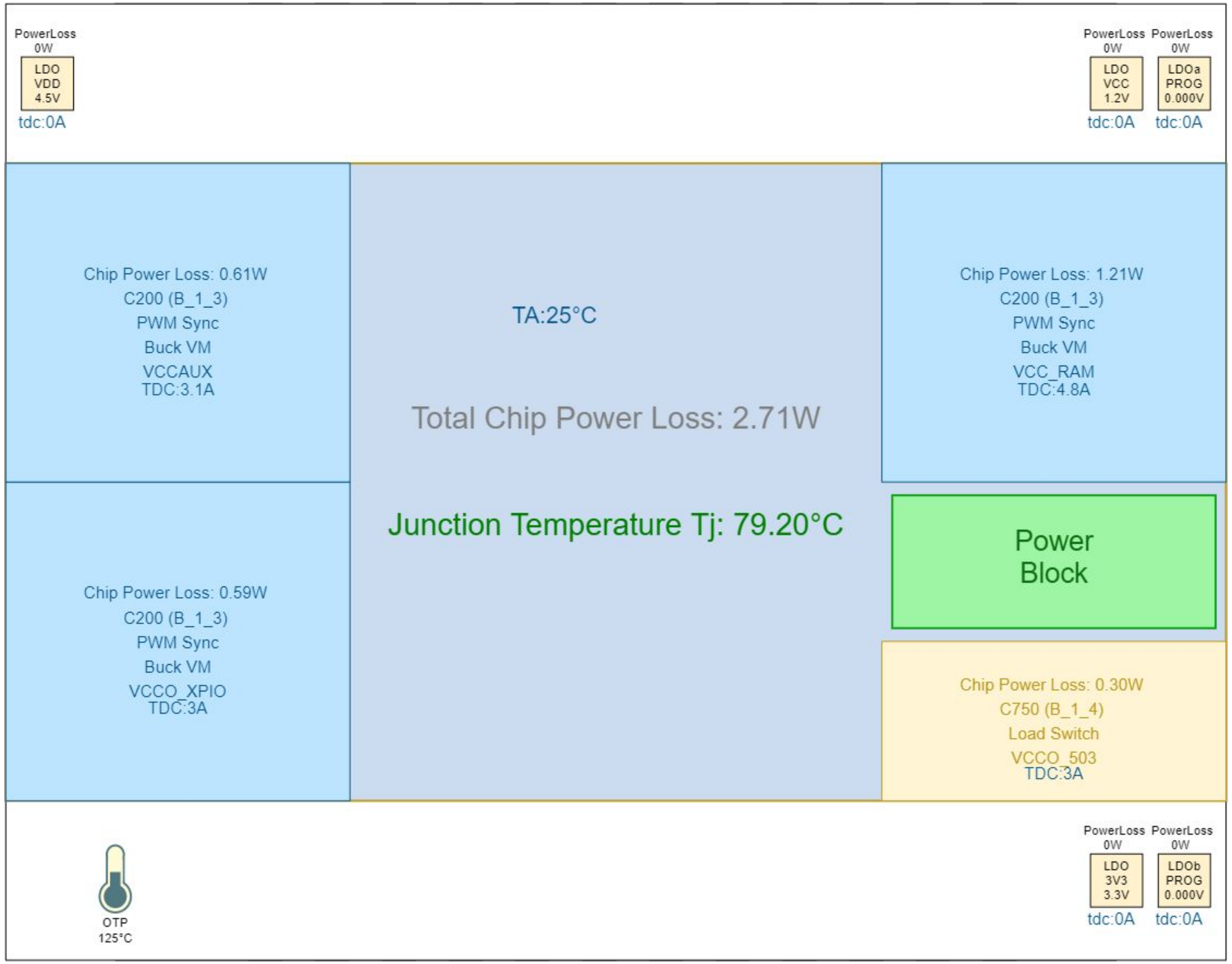


Estimated total area 1625.47 mm^2

Mapping (WebAmP View) Design –IC1

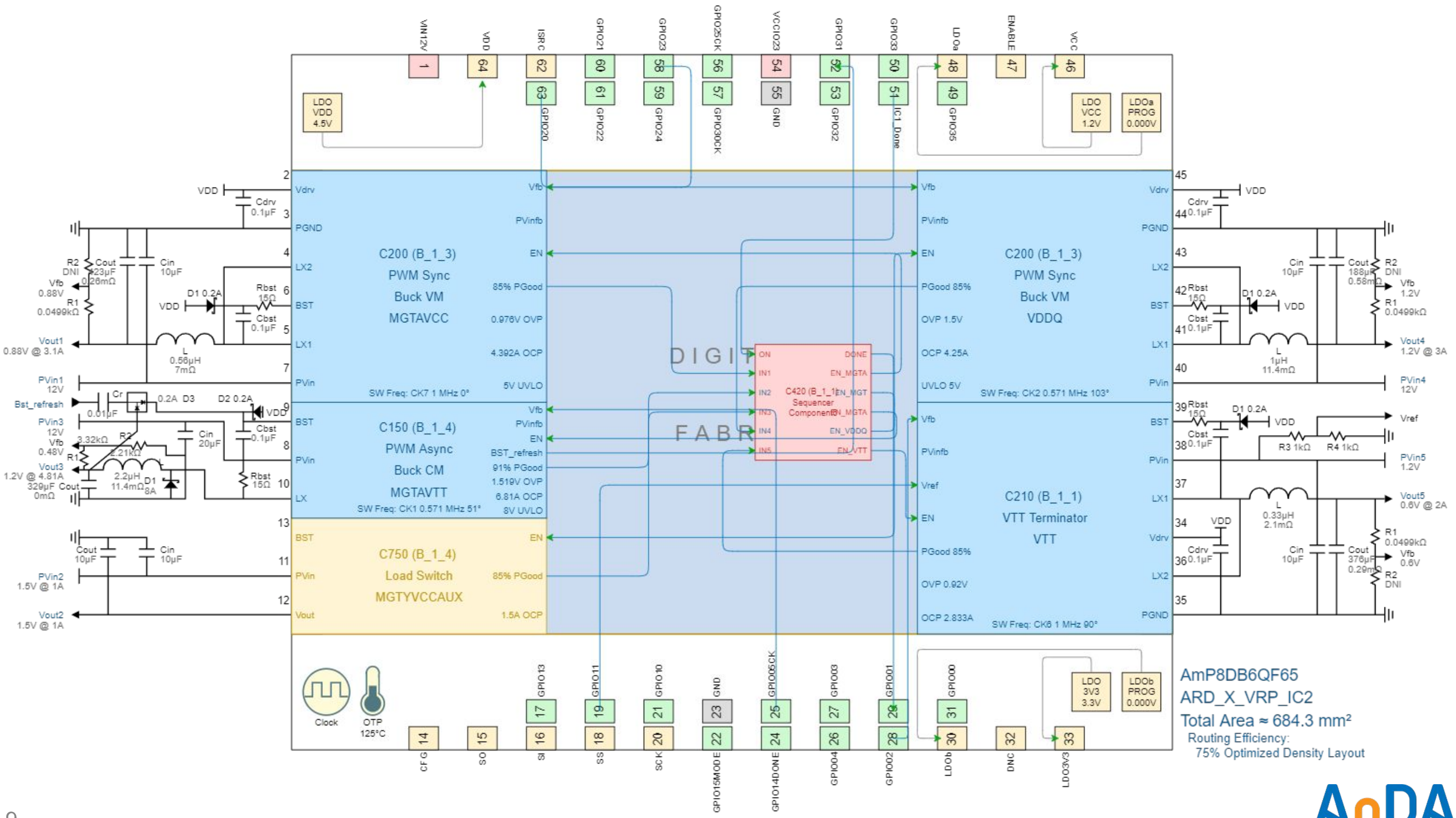


Mapping (Thermal View) –IC1



AmP8DB6QF65
ARD_X_VRP_IC1
Total Area ≈ 941.17 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (WebAmP View) Design –IC2



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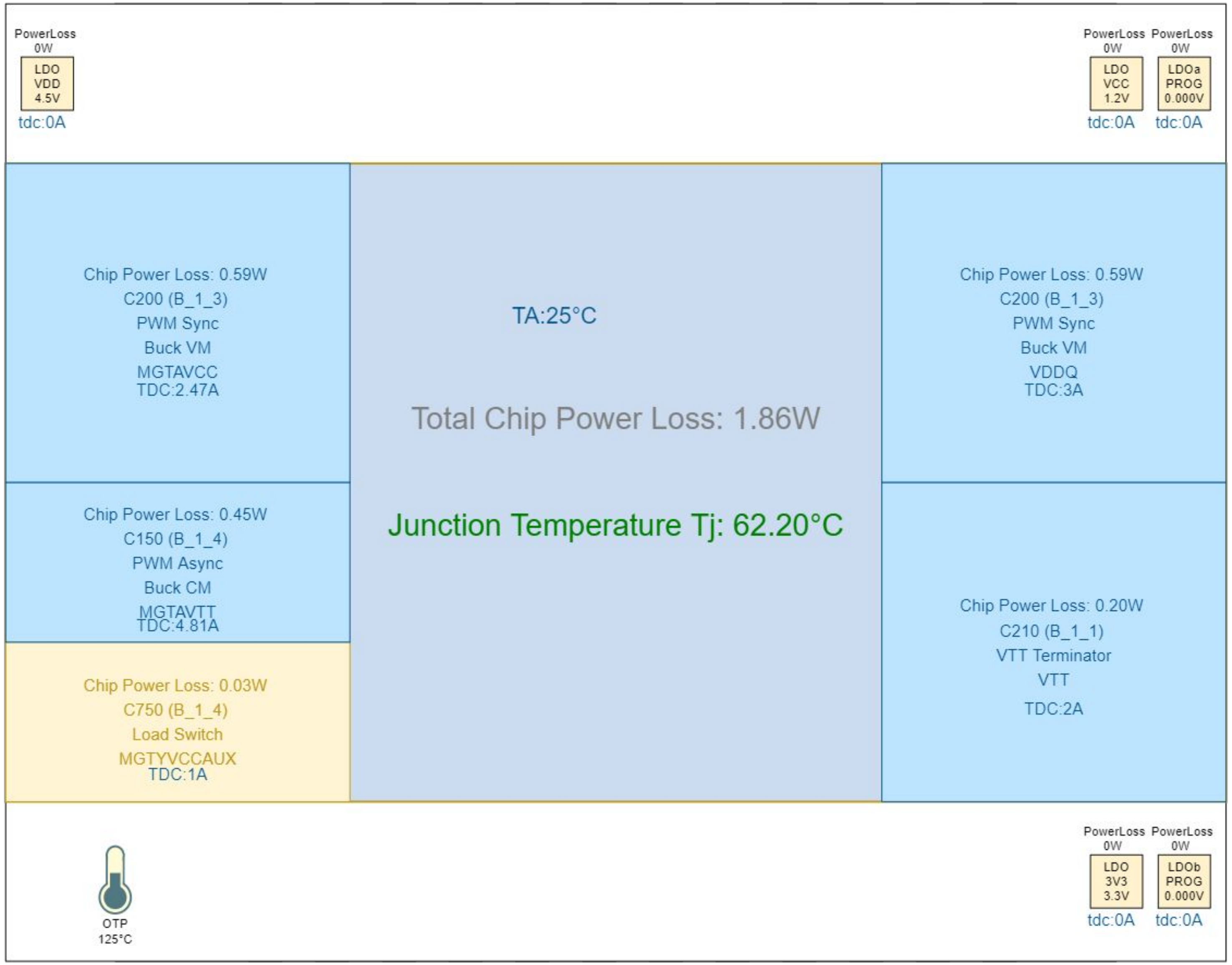
Mapping (Thermal View) –IC2



AmP8DB6QF65
ARD_X_VRP_IC2
Total Area ≈ 684.3 mm²
Routing Efficiency:
75% Optimized Density Layout

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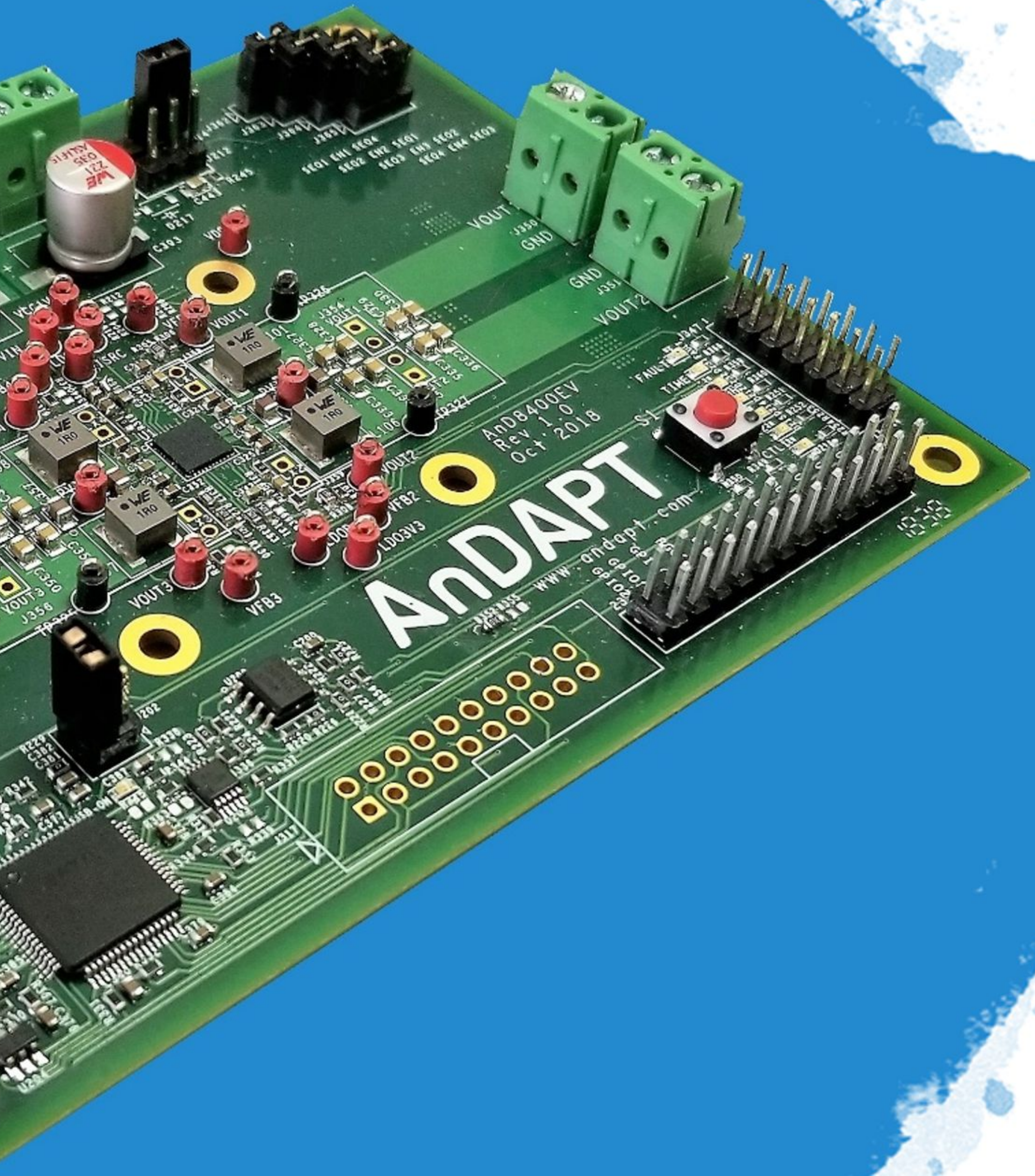

Test Data

Versal Prime (Minimum Rails, Low Voltage)

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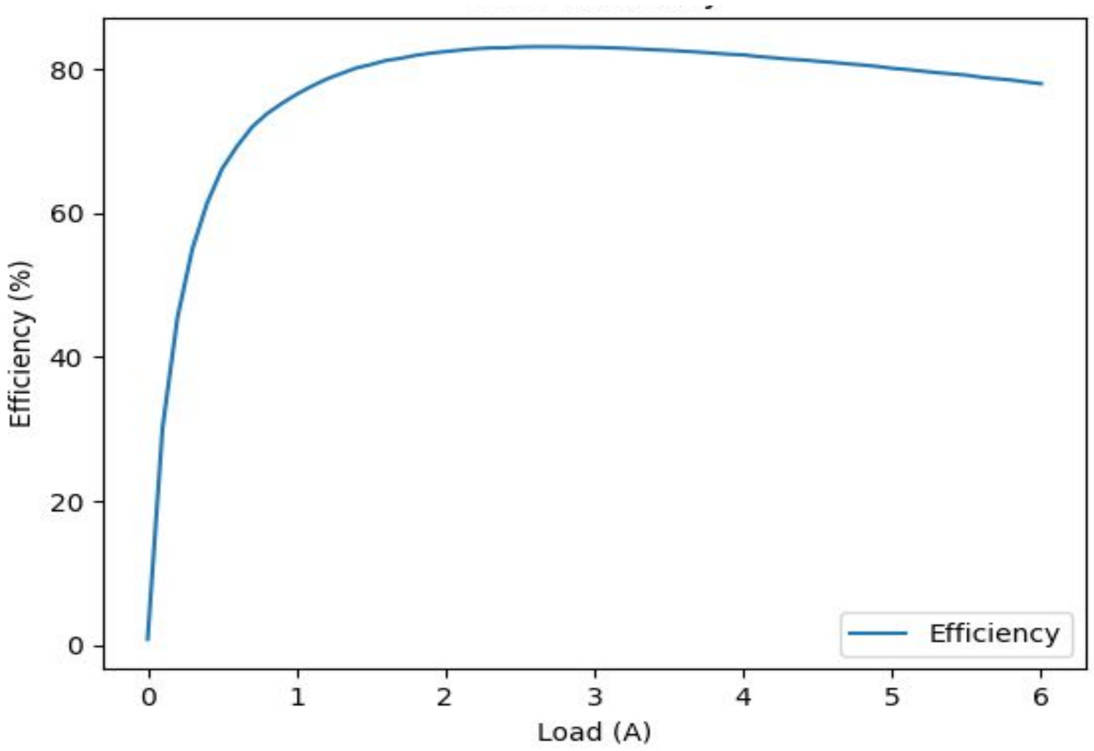
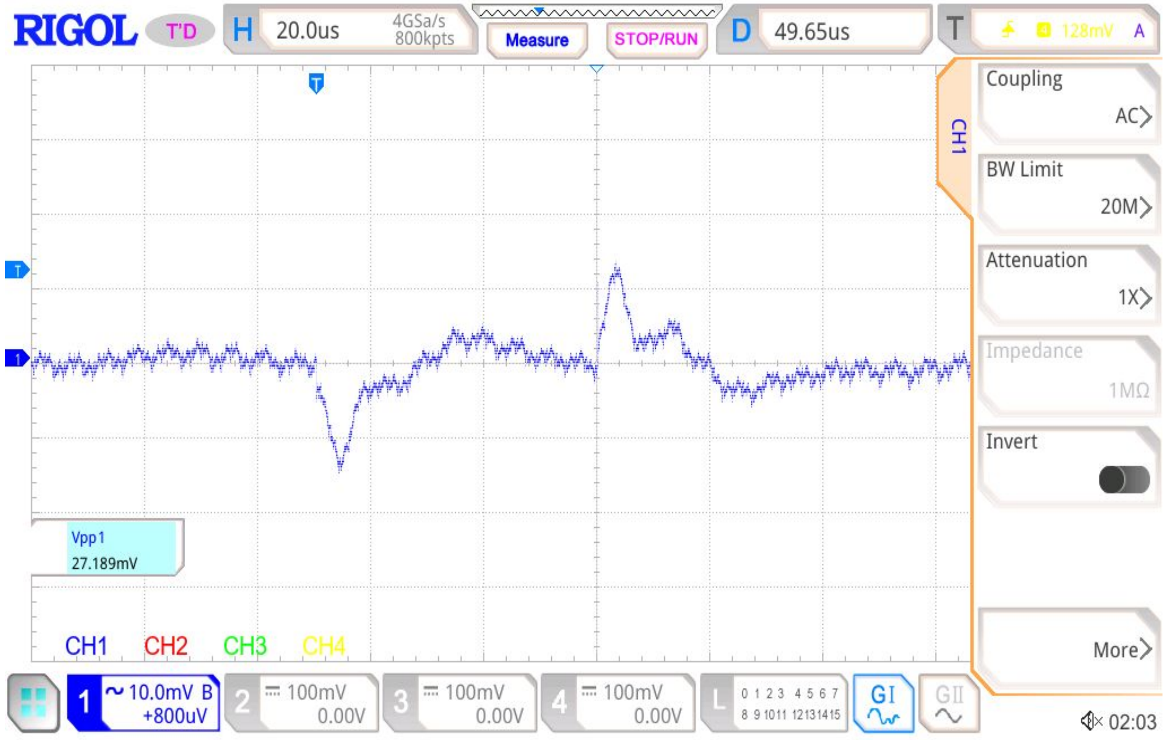
VCCO_XPIO
1.5 V / 6 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 4x47 uF

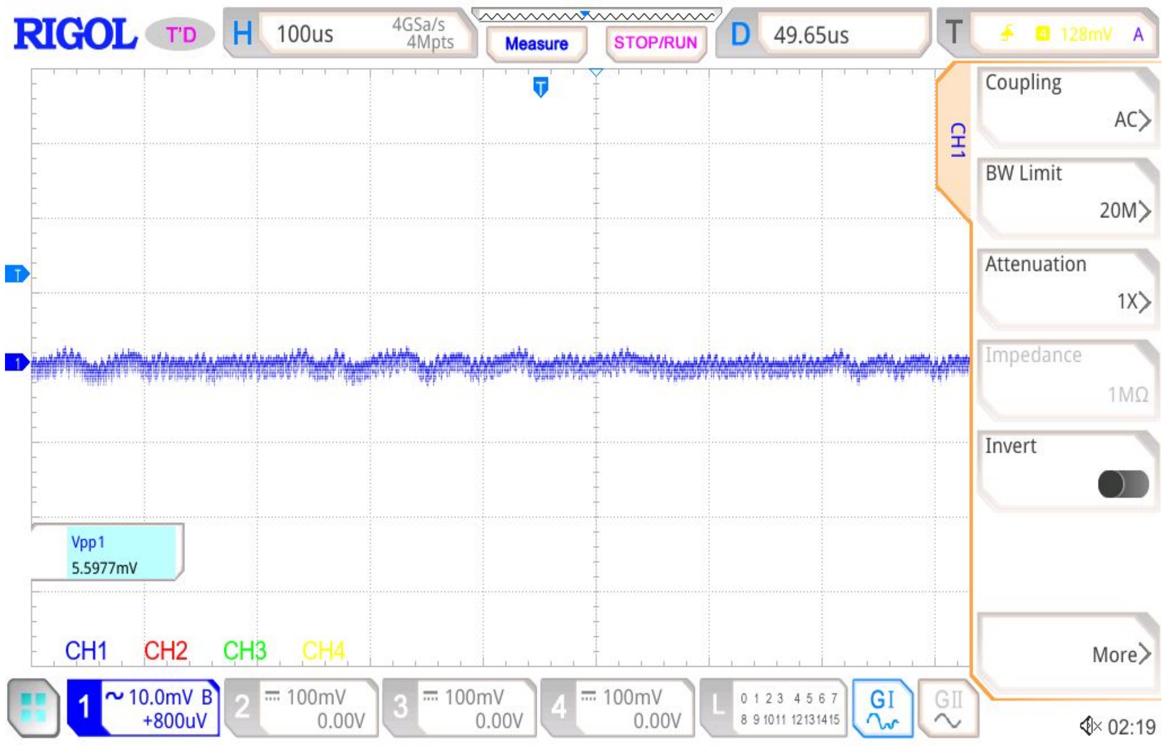
Efficiency & Transient

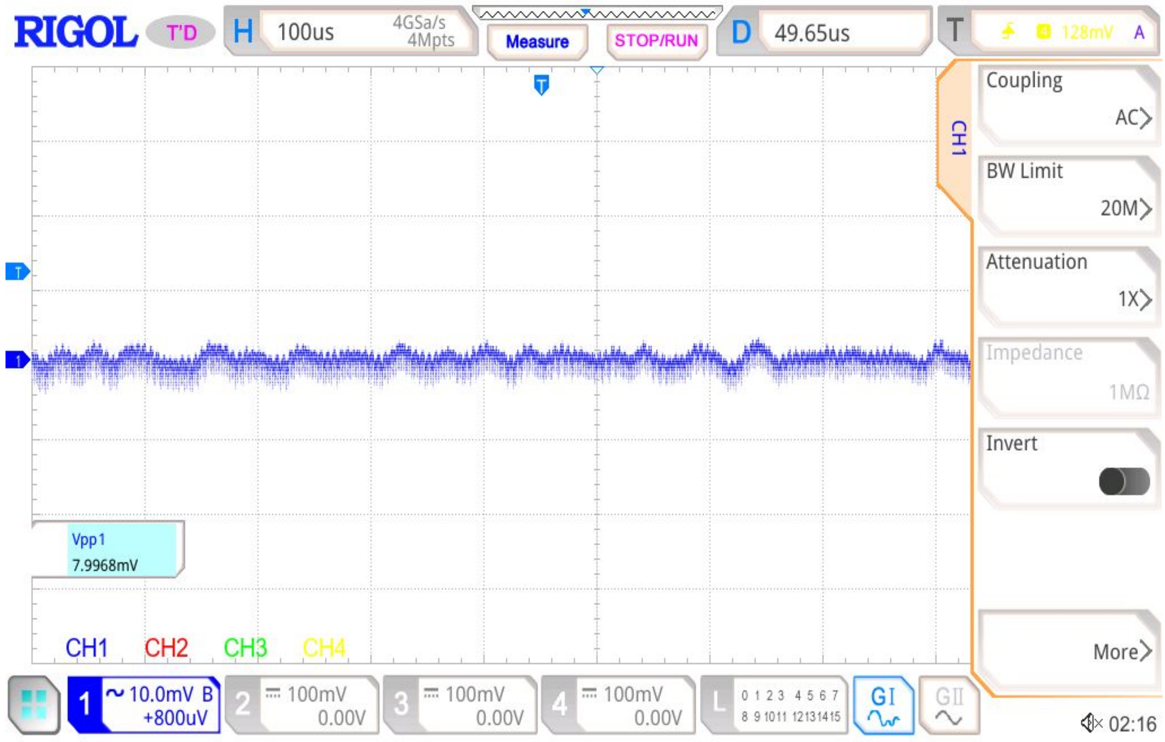




Vout = 1.5V
Transient 4.5 – 6 A@10 A/μs
V_{PP} = 27.18 mV
Fsw = 0.571 MHz
L = 1.1 μH, C= 4x47 uF

Ripple





No Load
V_{PP} = 5.59 mV

Vout = 1.5 V

6 A Load
V_{PP} = 7.99 mV

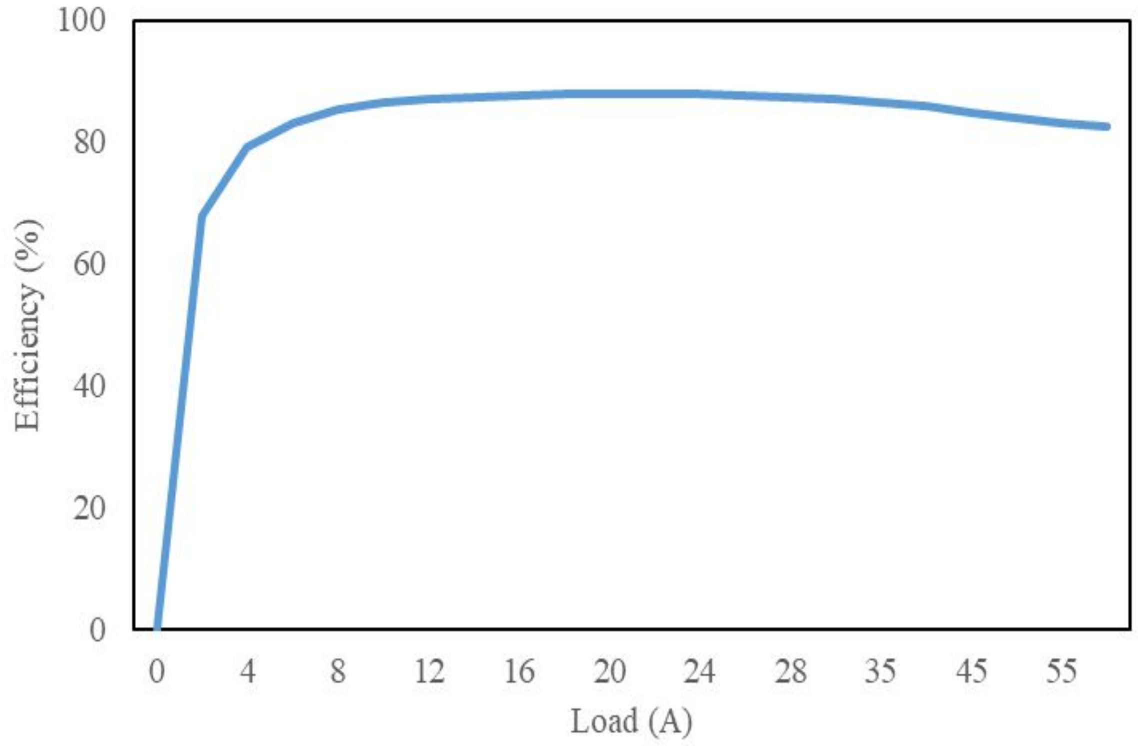
VCCO_503
1.5 V / 3 A

- C750 (Load switch)

VCCINT
0.7 V / 55 A

- C870 (Two Phase DrMOS)
- Fsw = 1 MHz
- L = 0.1 μH, P/N Wurth 7443081010
- C = 45x47 uF + 4x470 uF

Efficiency & Transient



Vout = 0.7V
Transient 22A – 55A @ 100 A/µs
V_{PP} = 26 mV
Fsw = 1 MHz
L = 0.1 µH, C = 45x47 uF + 4x470 uF

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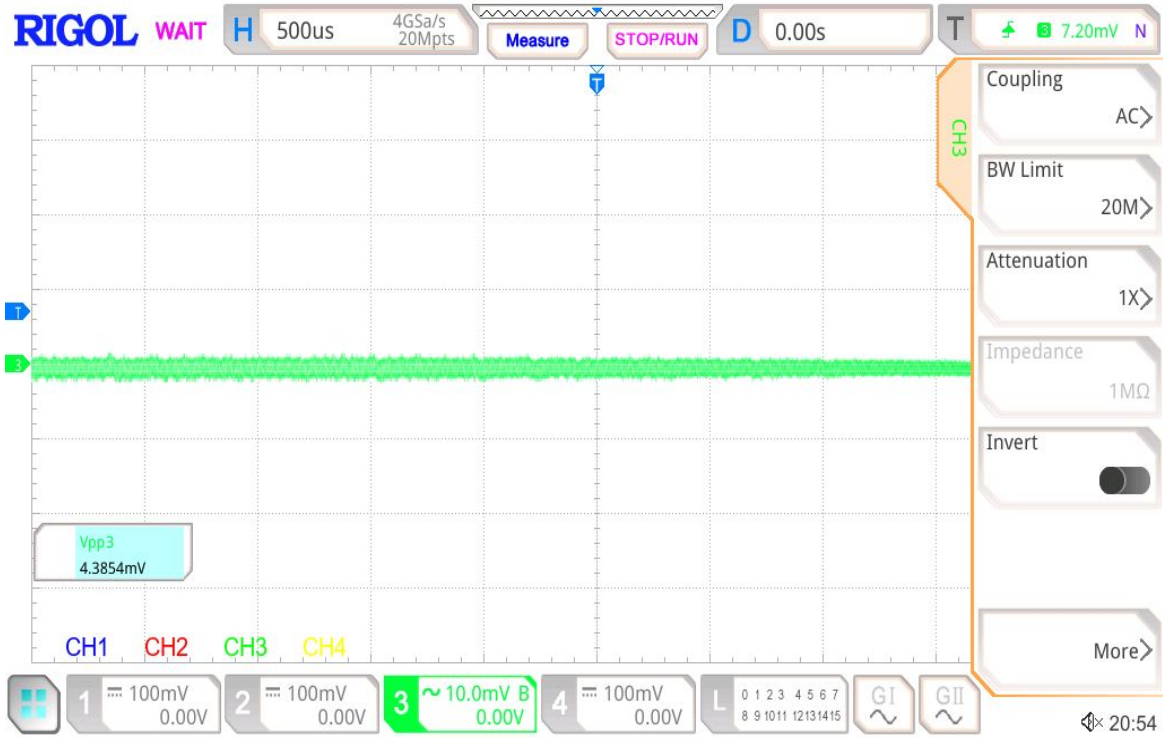
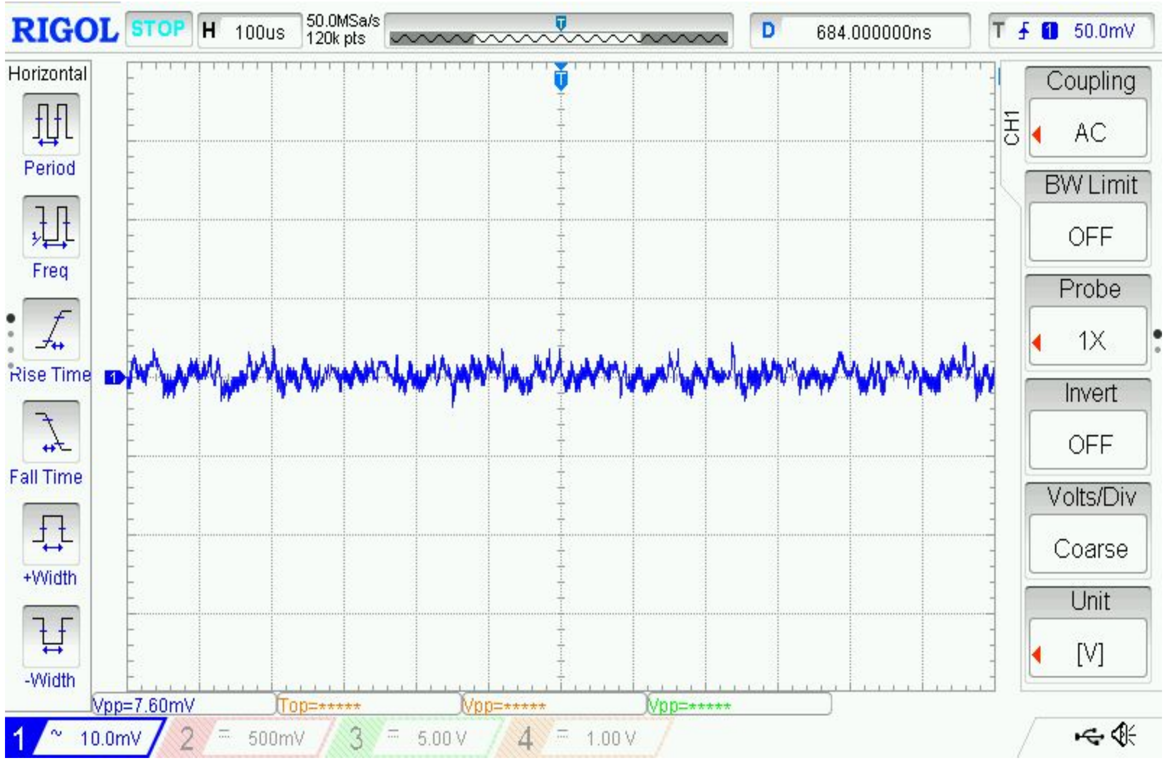
Ripple





No Load
V_{PP} = 4.38 mV

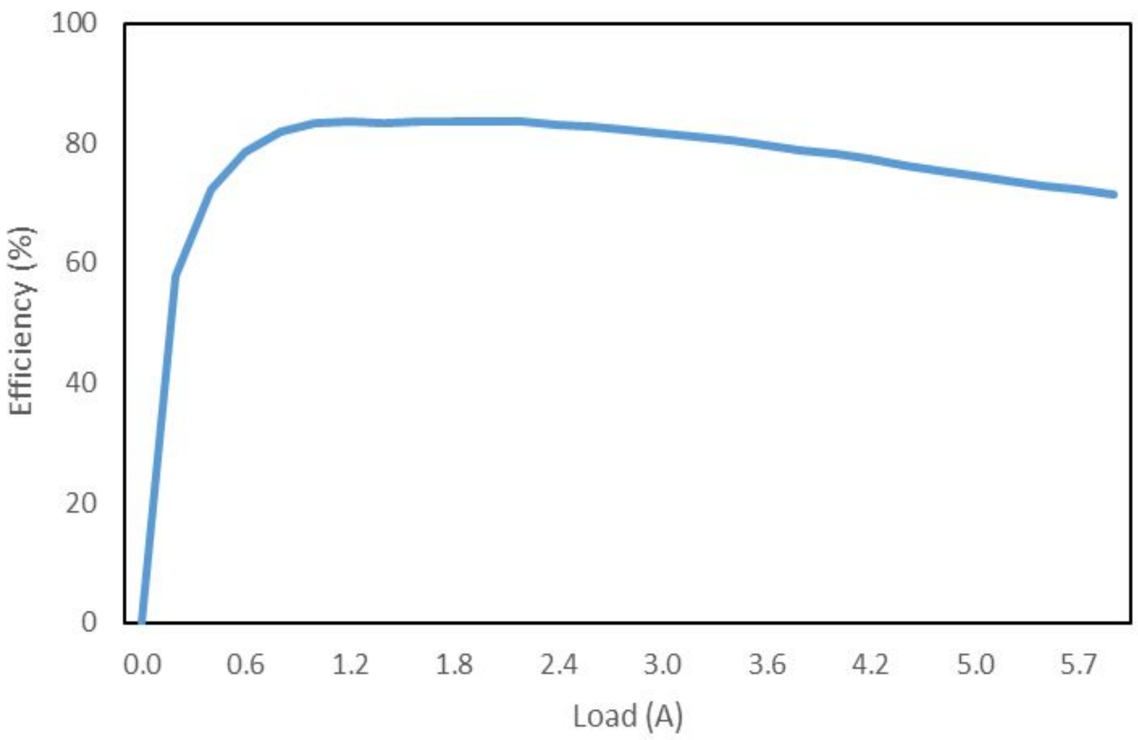
Vout = 0.7 V

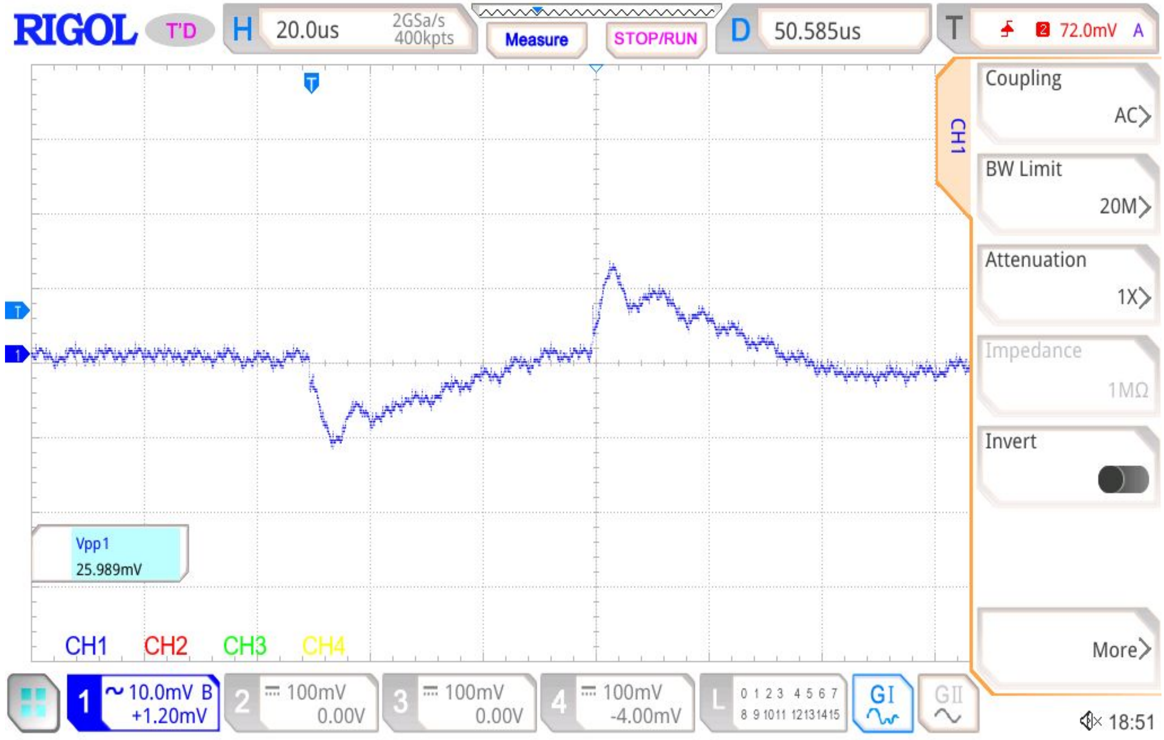
55 A Load
V_{PP} = 7.60 mV

VCC_RAM
0.8 V / 5.8 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 6x47 uF

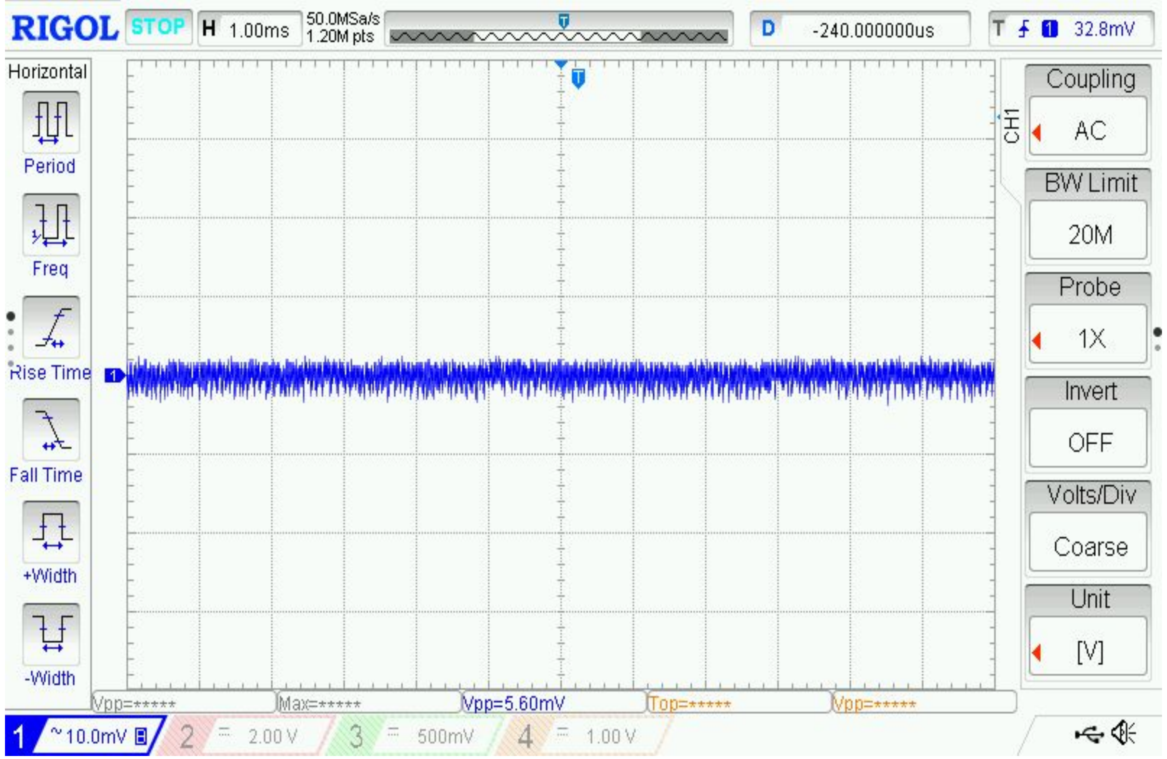
Efficiency & Transient

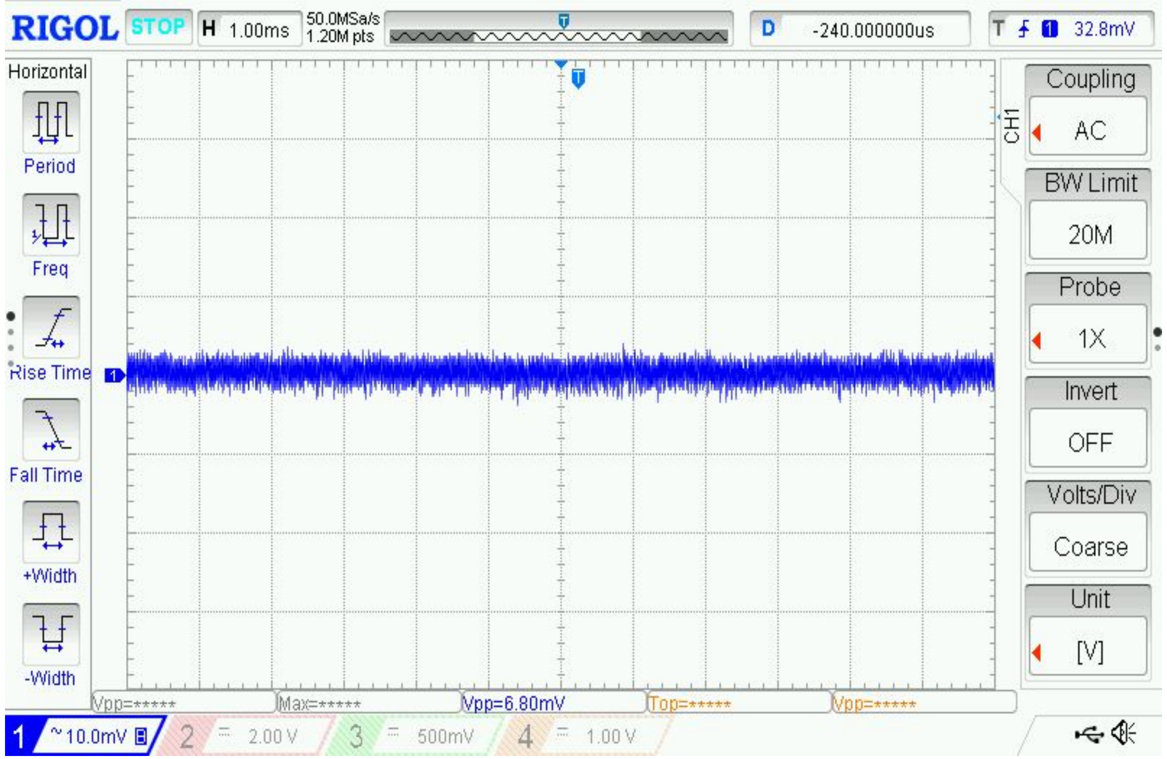




Vout = 0.8V
Transient 3.48A – 5.8A @ 10 A/μs
V_{PP} = 25.98 mV
Fsw = 0.571 MHz
L = 0.56 μH, C = 6x47 uF

Ripple





No Load
V_{PP} = 5.60 mV

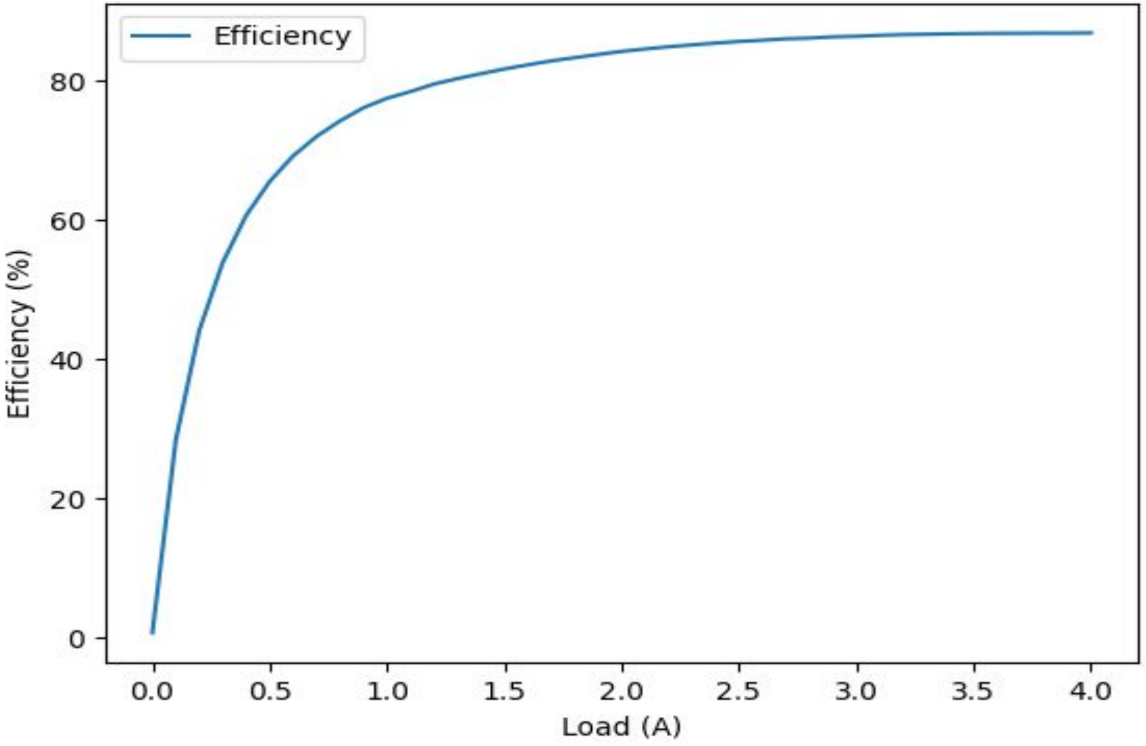
Vout = 0.8 V

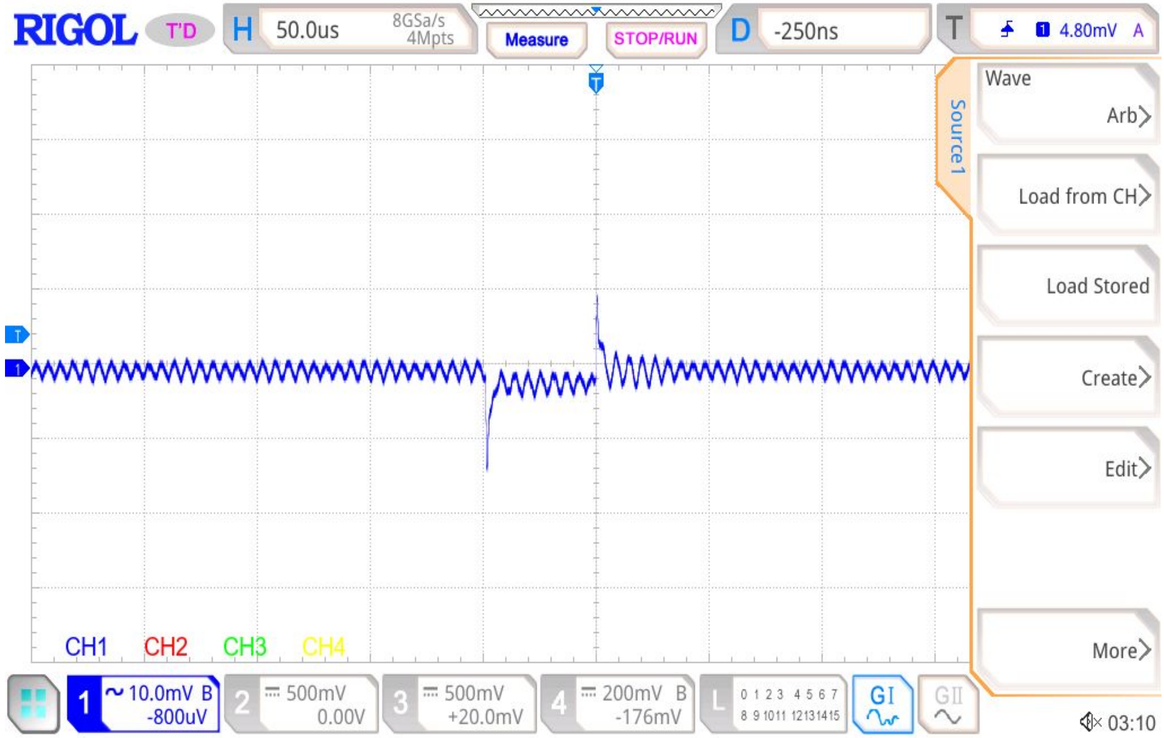
5.8 A Load
V_{PP} = 6.80 mV

VCCAUX
1.5 V / 4 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 4.7 µH, P/N Wurth 744311470
- C = 1x47 uF

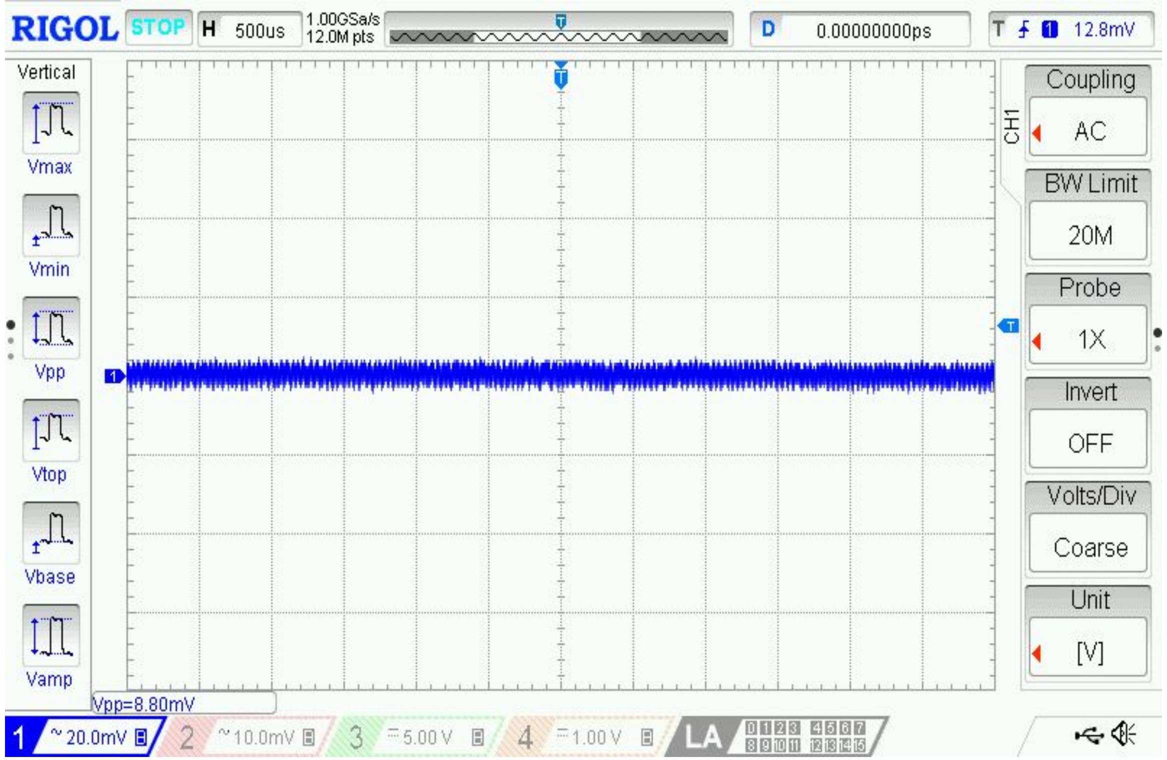
Efficiency & Transient

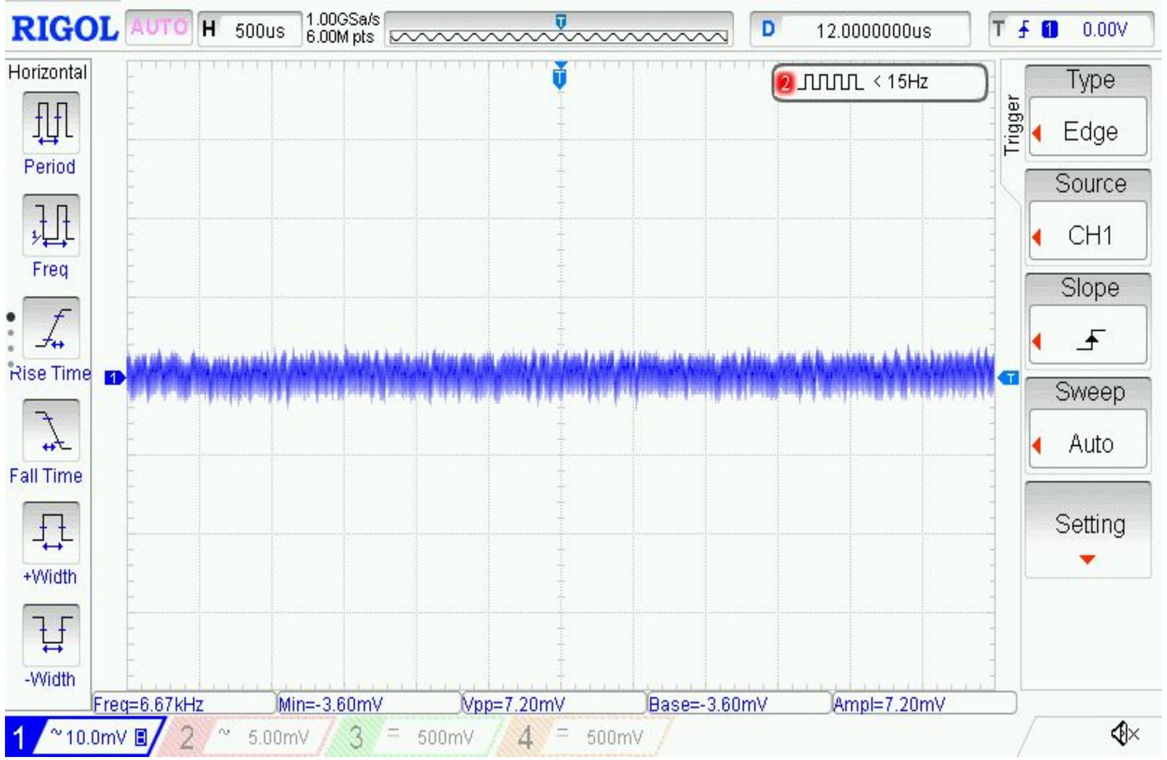




Vout = 1.5V
Transient 2.68A – 4A @ 10 A/µs
V_{PP} = 25 mV
Fsw = 0.571 MHz
L = 4.7 µH, C = 1x47 uF

Ripple





No Load
V_{PP} = 8.80 mV

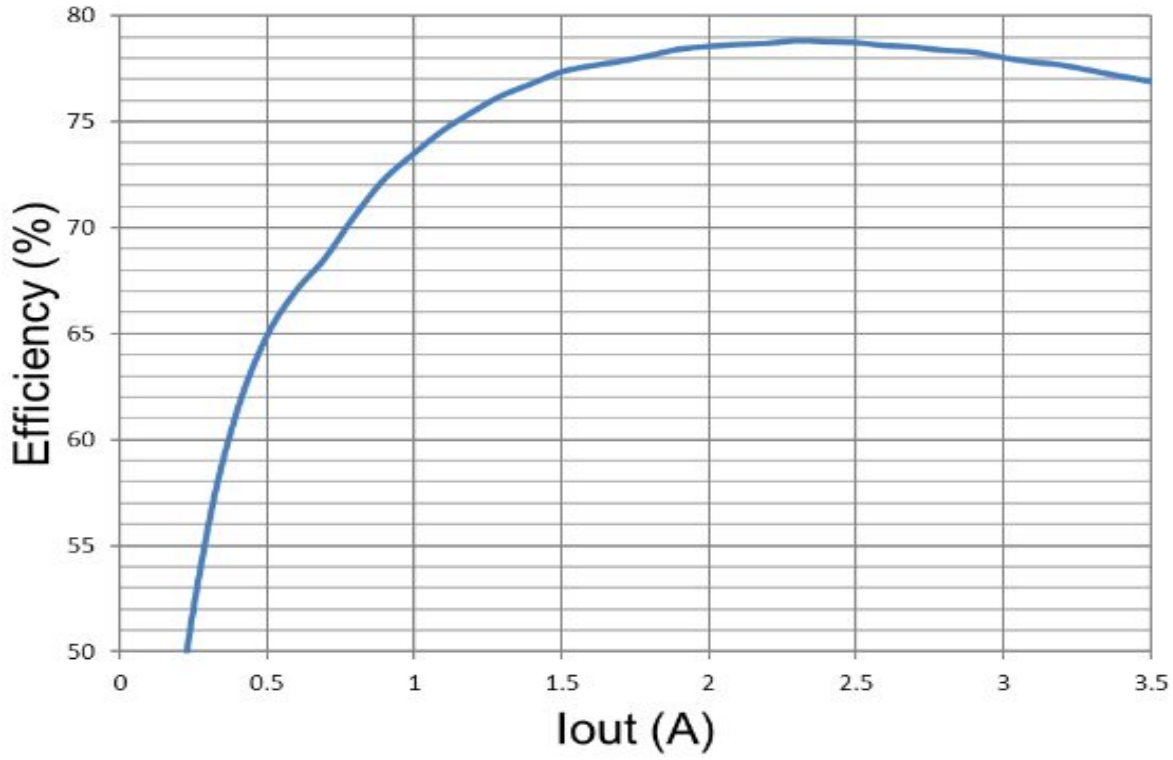
Vout = 1.5 V

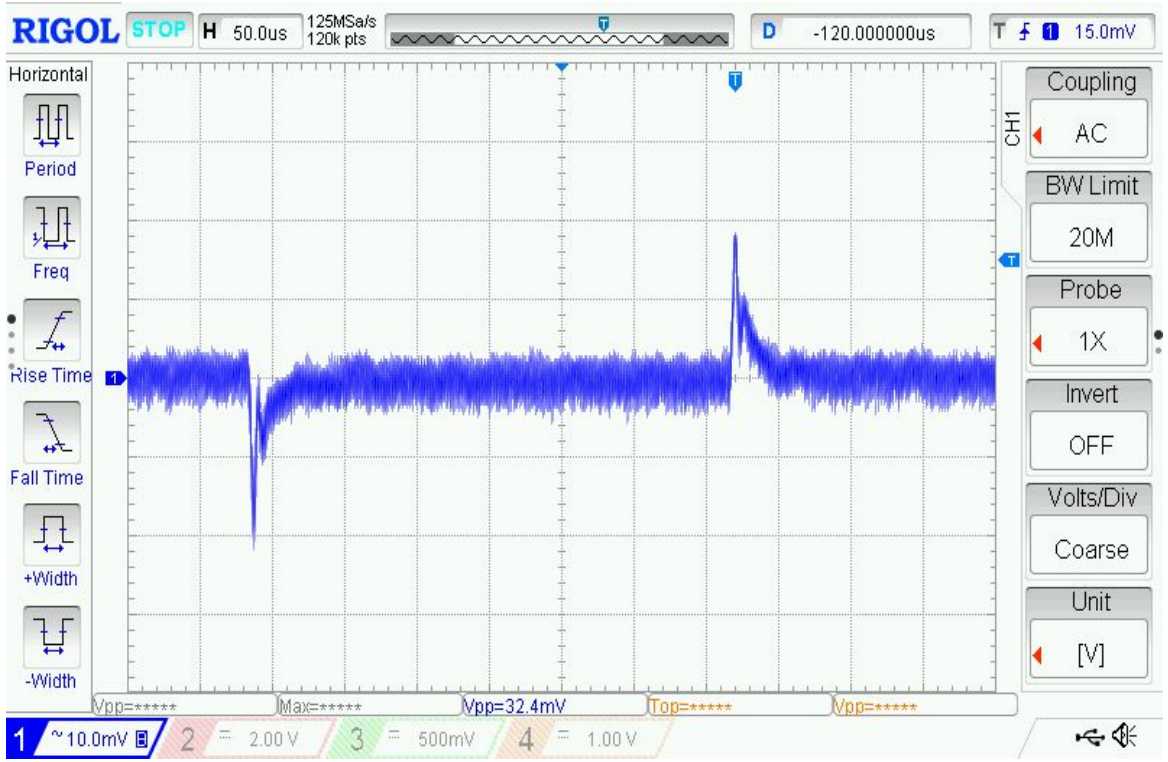
4 A Load
V_{PP} = 7.20 mV

MGTAVCC
0.88 V / 3.1 A

- C200 (Synchronous Buck)
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 9x47 uF

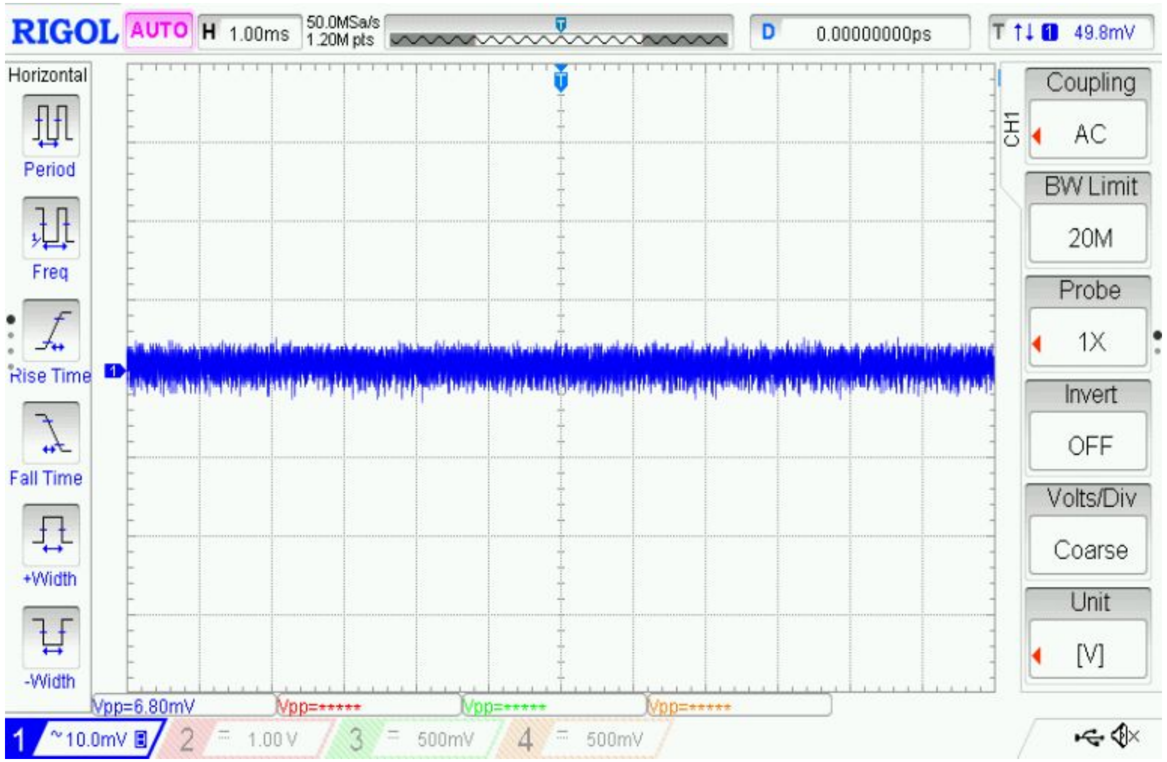
Efficiency & Transient

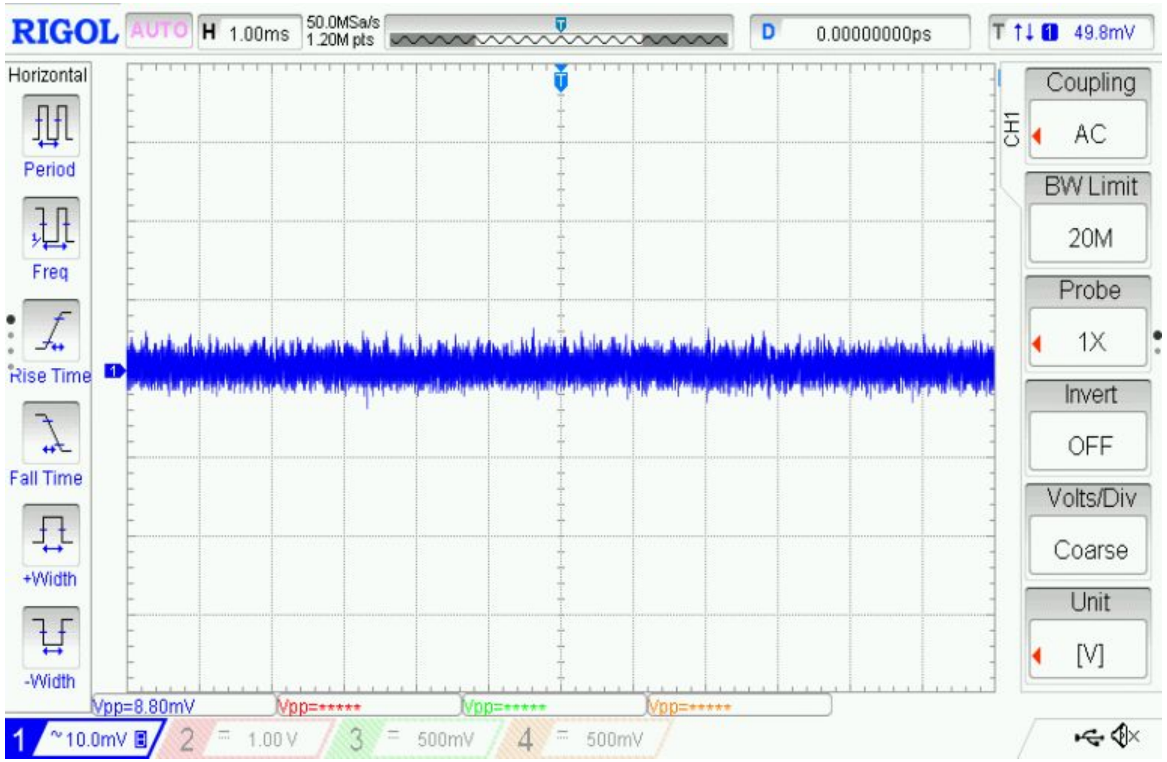




Vout = 0.88V
Transient 2.625A – 3.5A @ 10 A/μs
V_{PP} = 32.4 mV
Fsw = 0.571 MHz
L = 0.56 μH, C = 9x47 uF

Ripple





No Load
V_{PP} = 6.80 mV

Vout = 0.88 V

3.1 A Load
V_{PP} = 8.80 mV

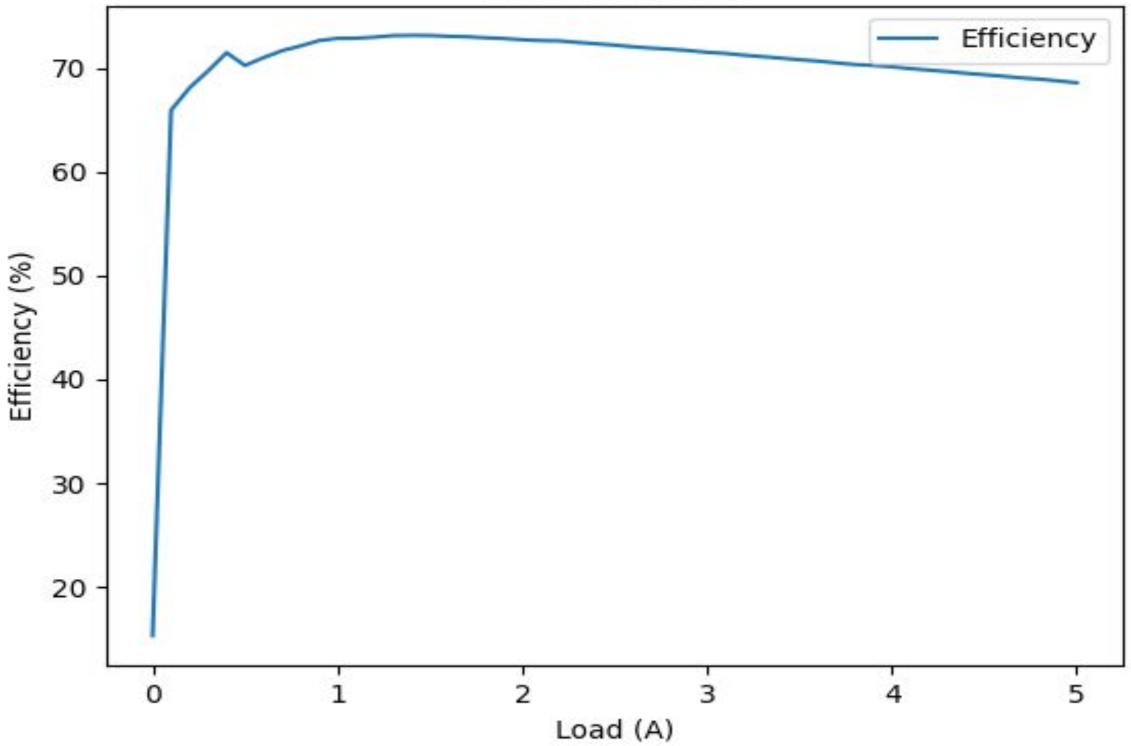
MGTYVCCAUX
1.5 V / 0.29 A

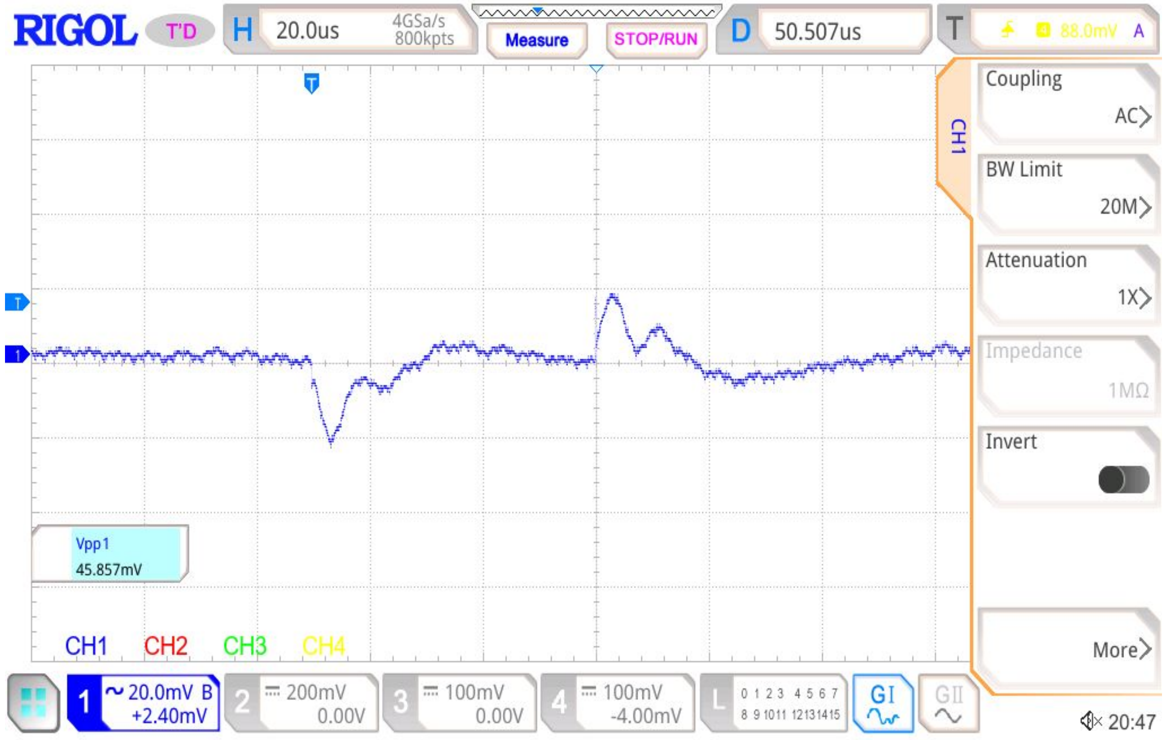
- C750 (Load switch)

MGTAVTT
1.2 V / 4.81 A

- C150 (Asynchronous Buck)
- Fsw = 0.571 MHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 7x47 uF

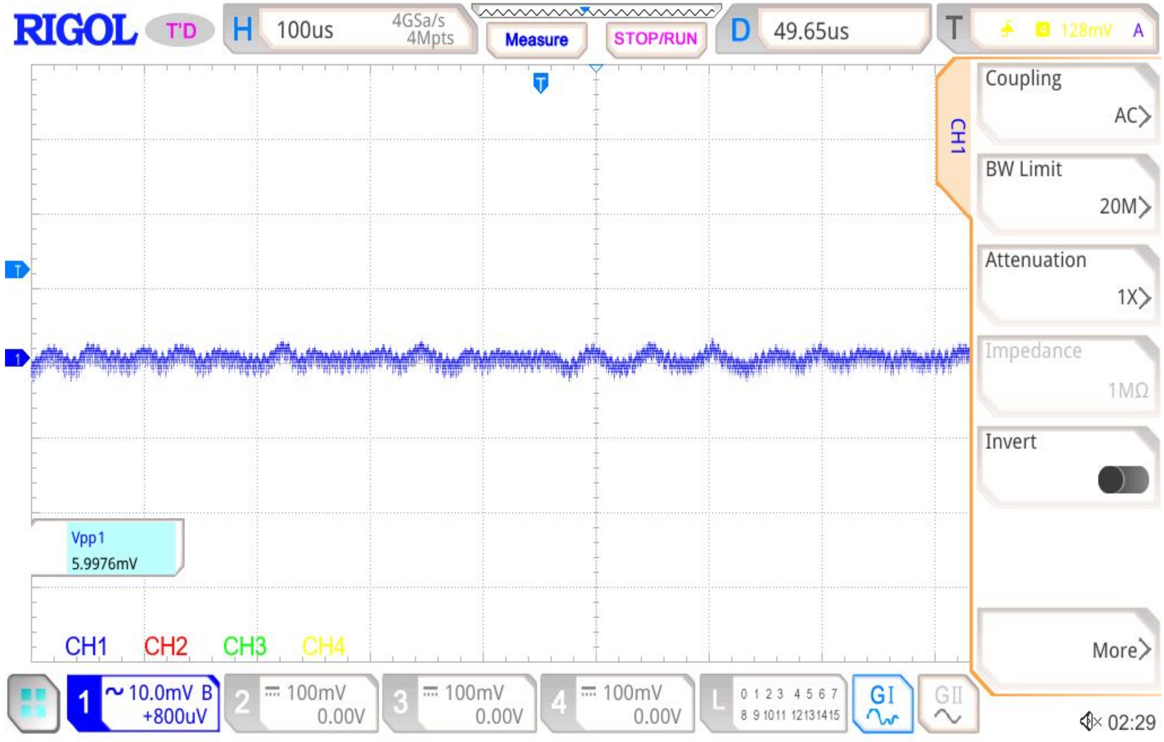
Efficiency & Transient

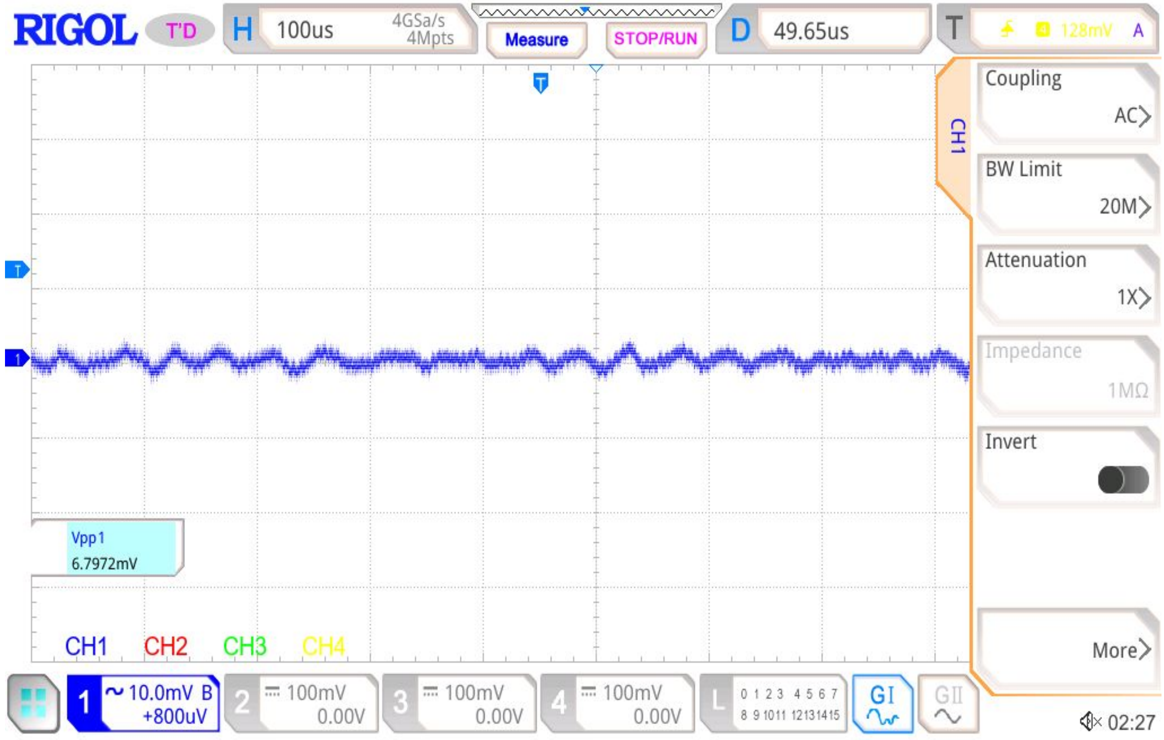




Vout = 1.2V
Transient 3.61 – 4.81A @ 10 A/µs
V_{PP} = 45.85 mV
Fsw = 0.571 MHz
L = 2.2 µH, C = 7x47 uF

Ripple





No Load
V_{PP} = 5.99 mV

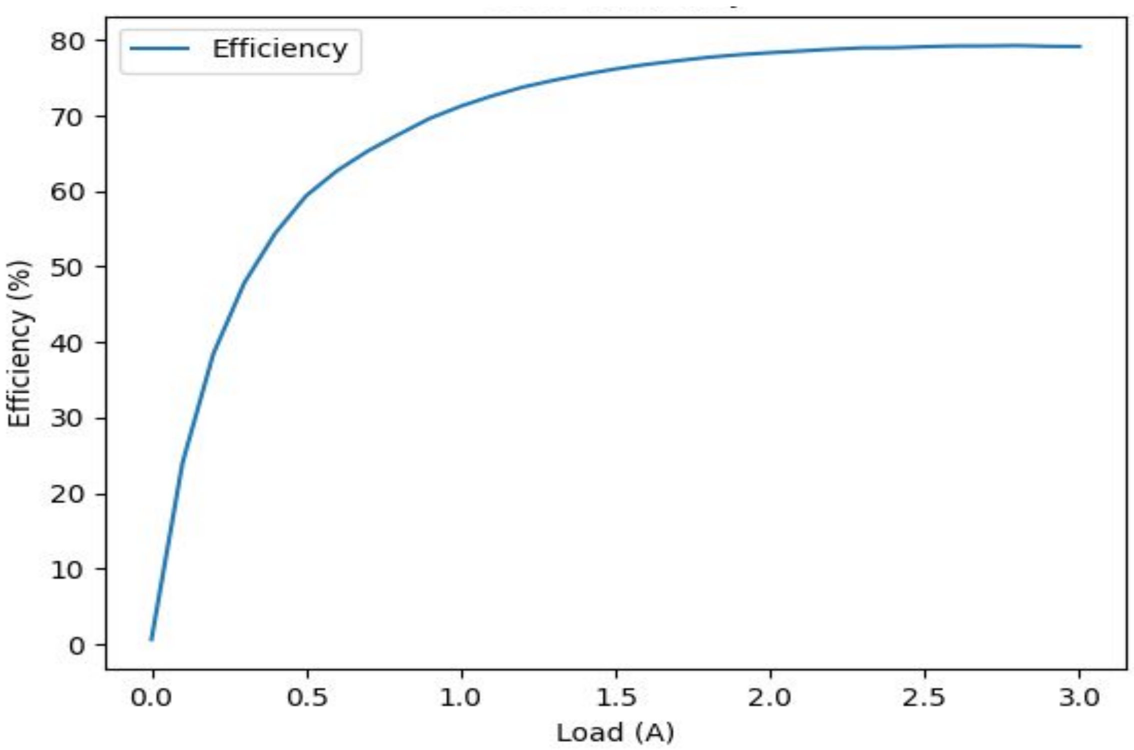
Vout = 1.2 V

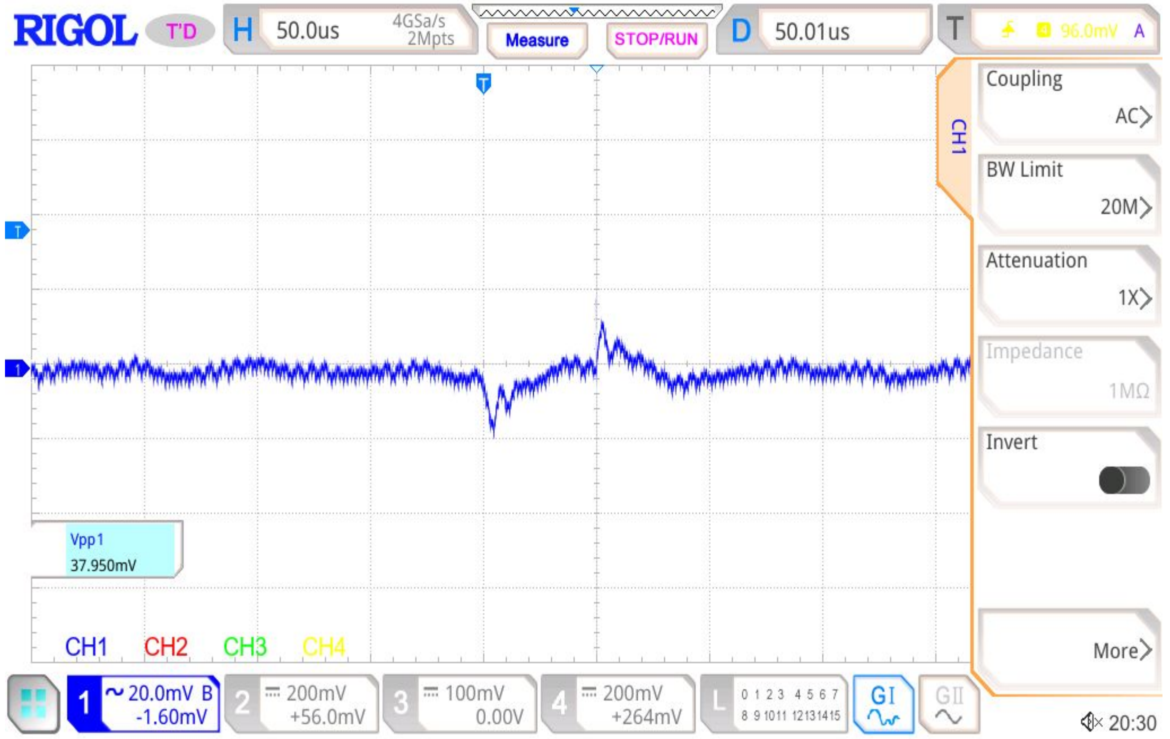
4.81 A Load
V_{PP} = 6.79 mV

VDDQ
1.2 V / 3 A

- C200 (Synchronous Buck)
- Fsw = 0.571 MHz
- L = 1 µH, P/N Wurth 74438366010
- C = 4x47 uF

Efficiency & Transient





Vout = 1.2V
Transient 0.3 – 3A @ 10 A/μs
V_{PP} = 37.95 mV
Fsw = 0.571 MHz
L = 1 μH, C = 4x47 uF

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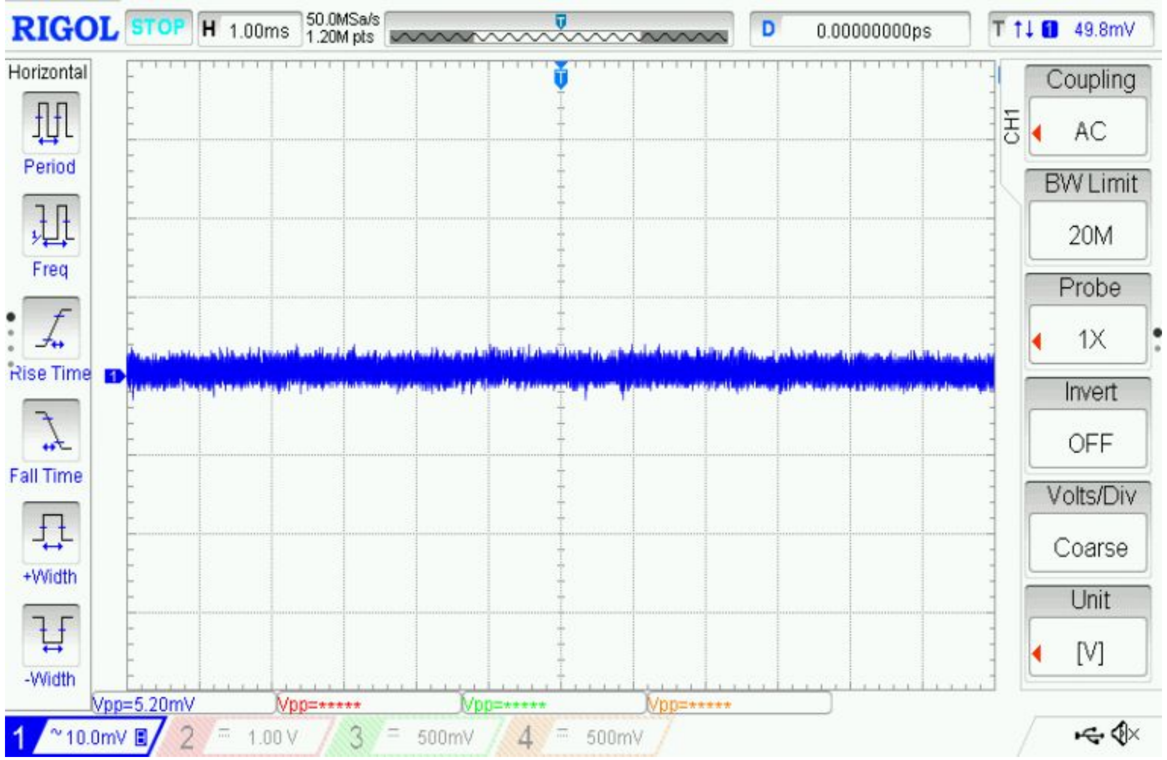
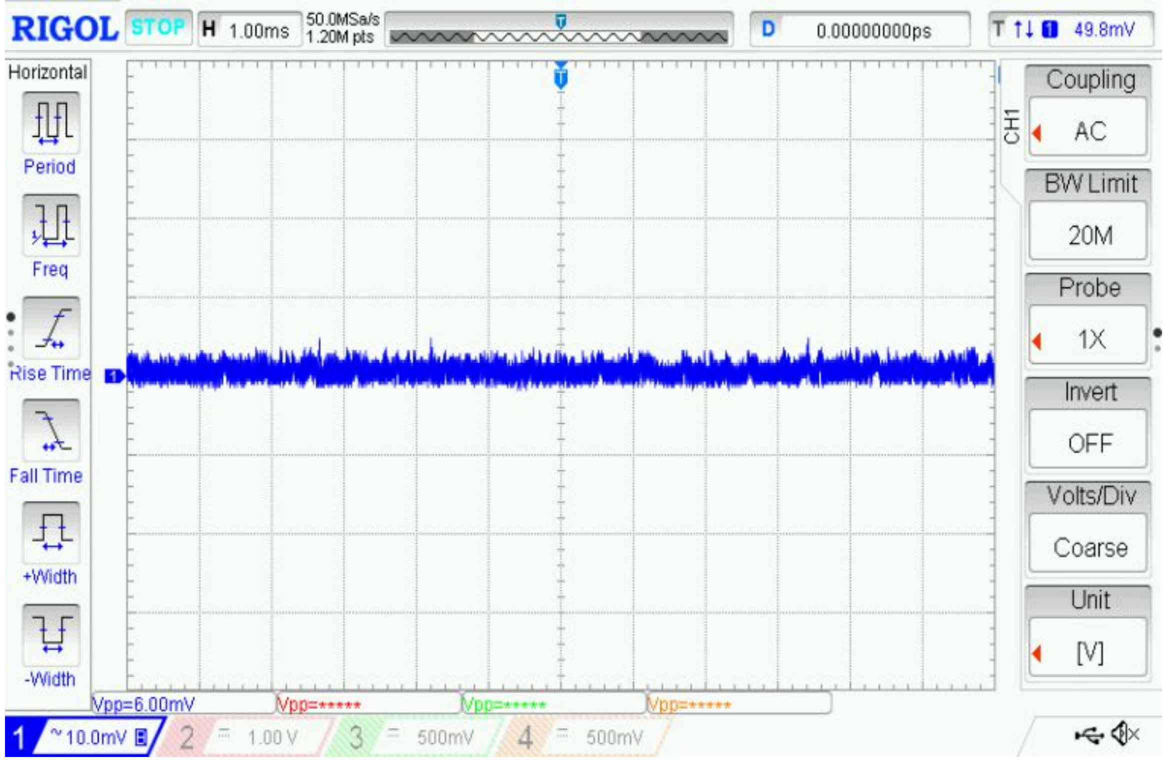
Ripple





No Load
V_{PP} = 5.20 mV

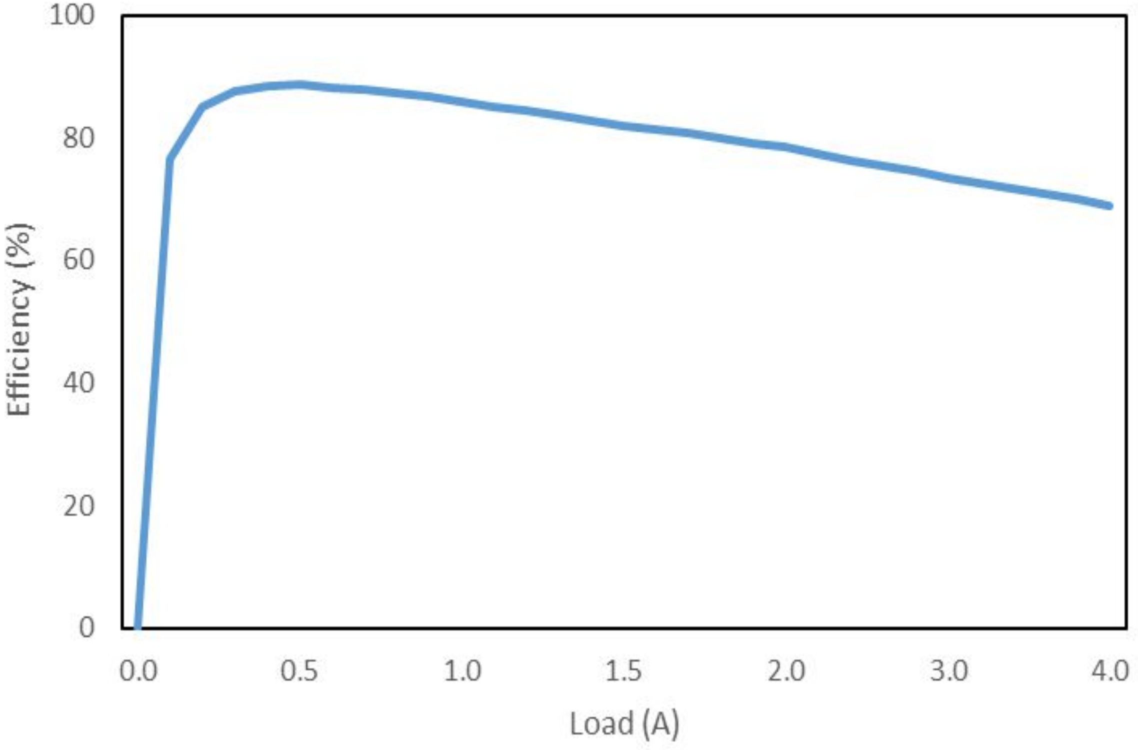
Vout = 1.2 V

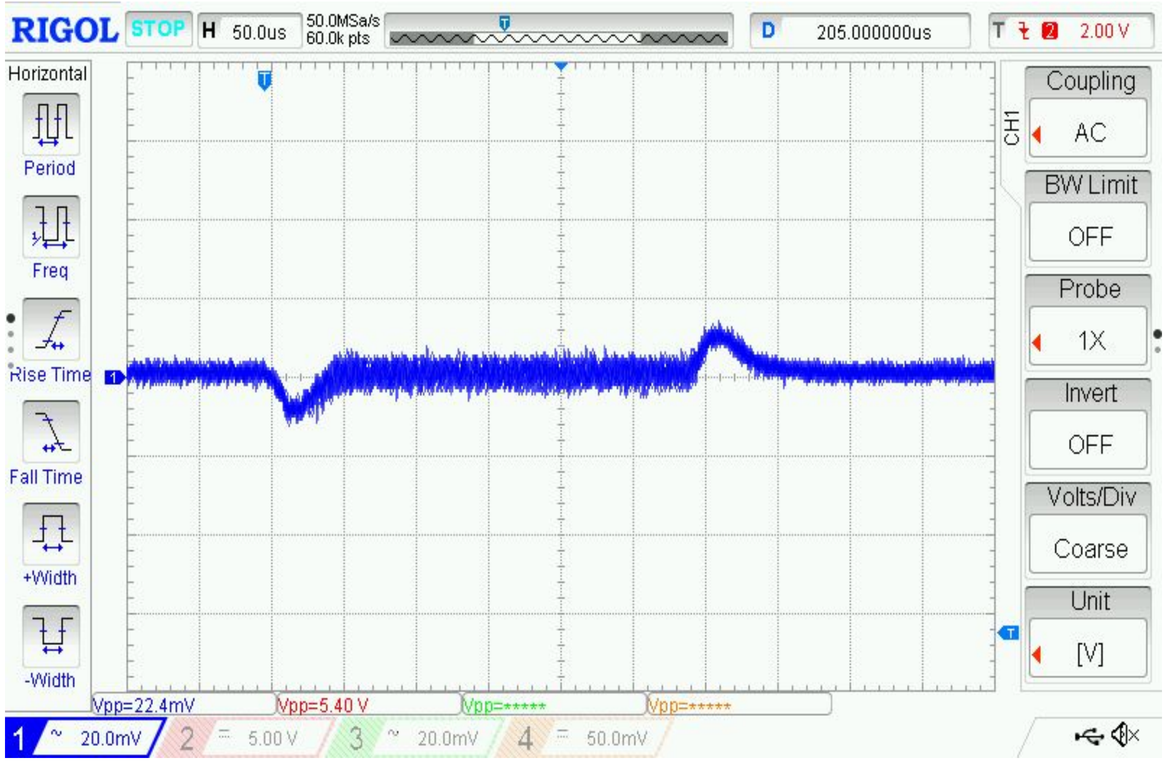
3 A Load
V_{PP} = 6.00 mV

VTT
0.6 V / 2 A

- C210 (VTT Terminator)
- Fsw = 1 MHz
- L = 0.33 µH, P/N Wurth 744393440033
- C = 8x47 uF

Efficiency & Transient

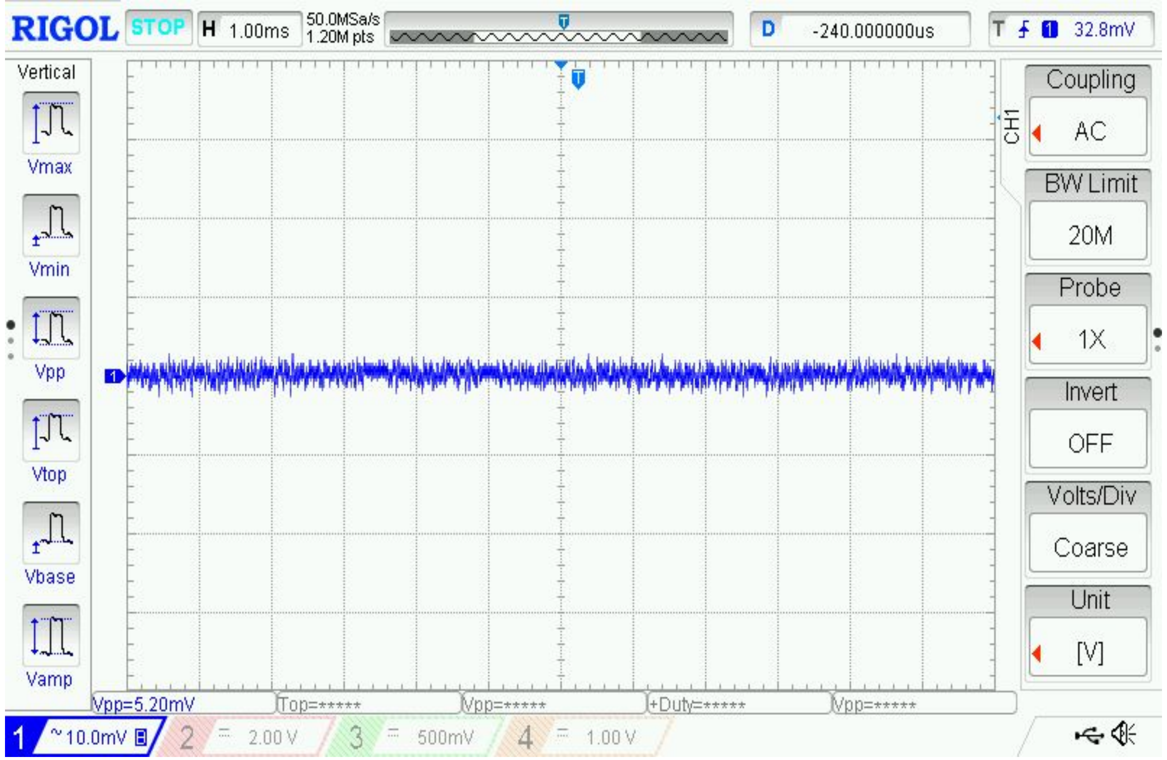


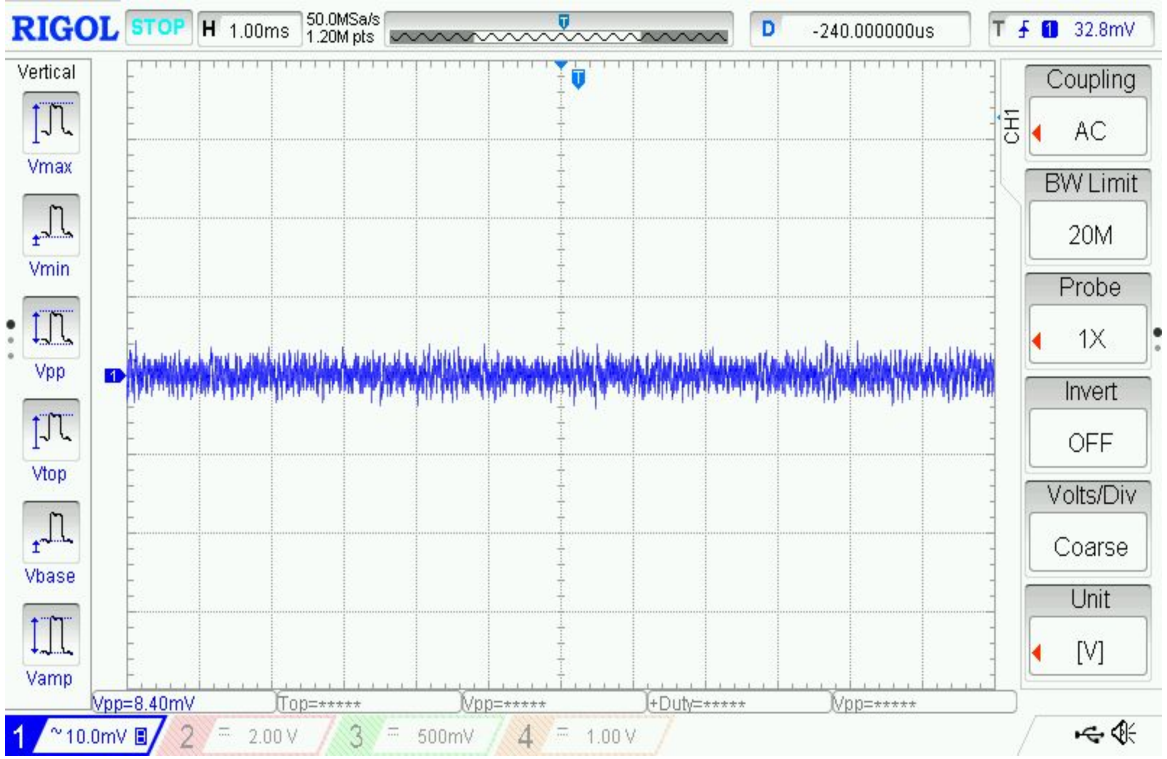


Vout = 0.6V
Transient 3 – 4A @ 10 A/µs
V_{PP} = 22.4 mV
Fsw = 1 MHz
L = 0.33 µH, C = 8x47 uF

AnDAPT

Ripple

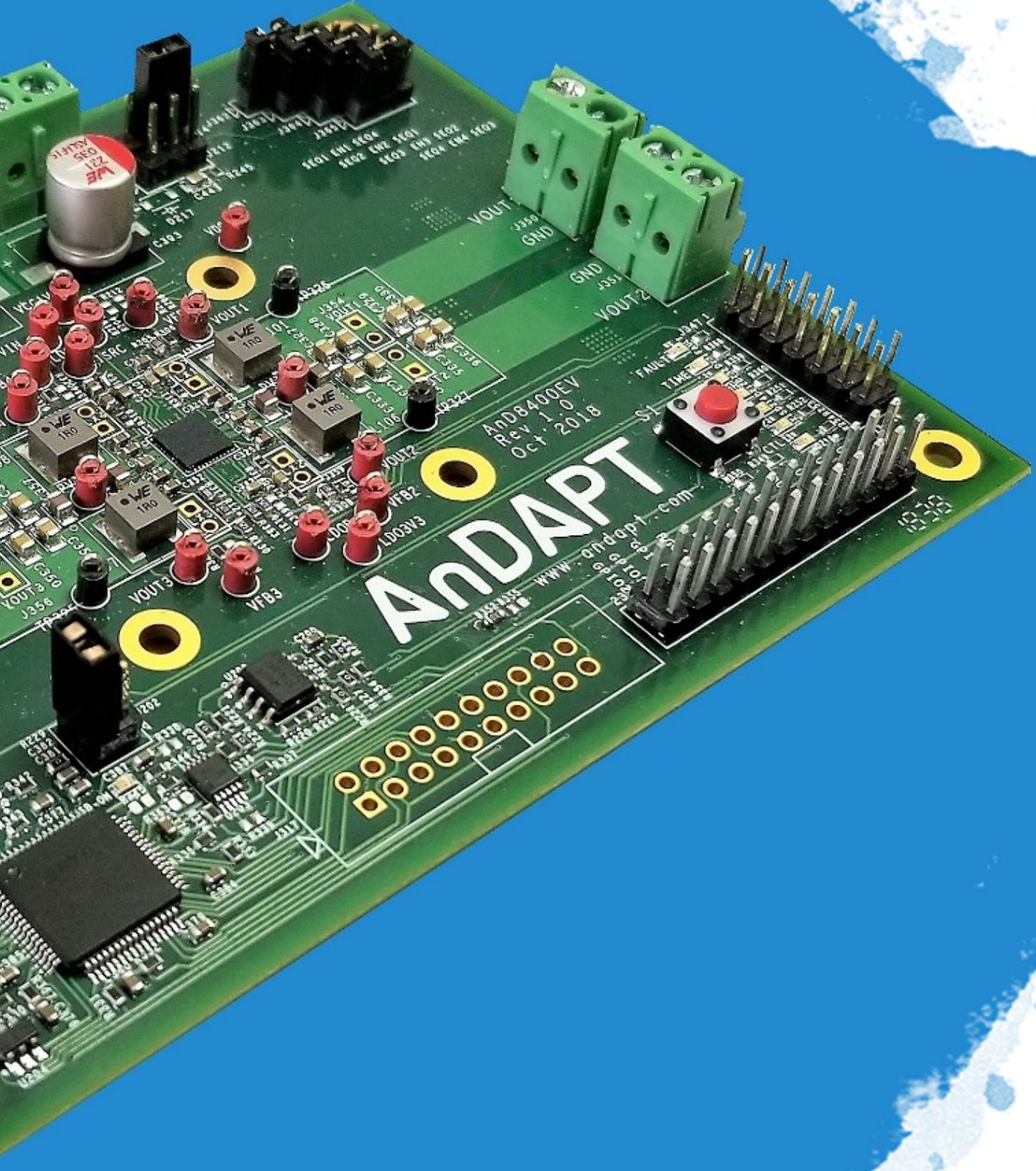




No Load
V_{PP} = 5.20 mV

Vout = 0.6 V

4 A Load
V_{PP} = 8.40 mV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VOUT1
VOUT2
VOUT3
GND
VFB2
VFB3
LDO3V3

Thank You