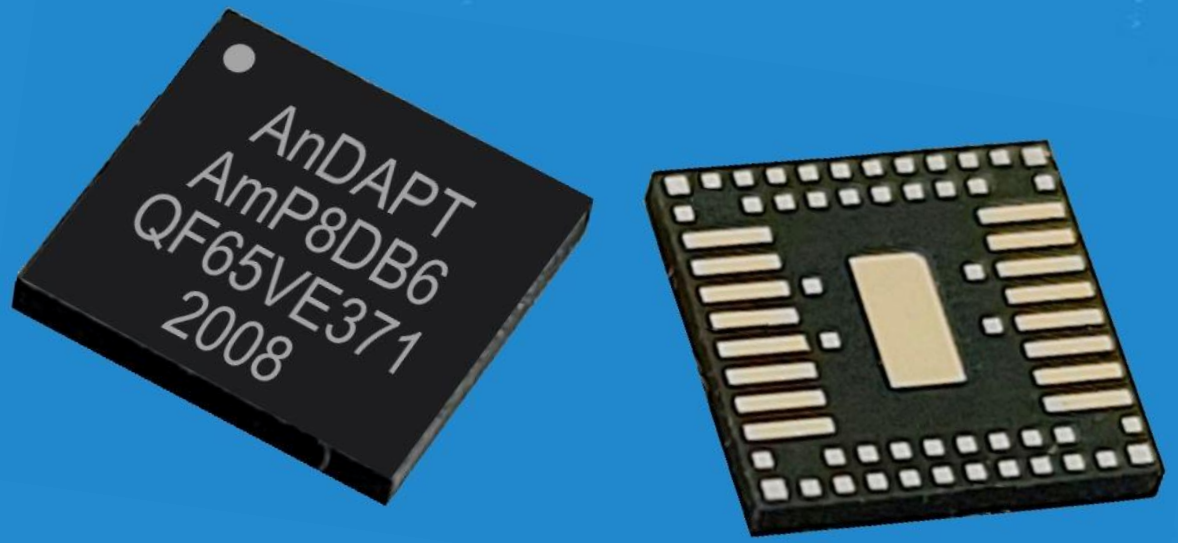


Virtex UltraScale+ (Minimum Rails)

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Virtex UltraScale+ family of devices SKUs (Minimum rails) in cost-optimized portfolio
- Virtex US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Virtex UltraScale + family FPGAs

Virtex UltraScale+ Device SKUs Covered- Minimum Rails

Supported SKUs
XCVU3P
XCVU5P
XCVU7P
XCVU9P
XCVU11P
XCVU13P
XCVU19P

Virtex UltraScale+ (Minimum Rails)

Can be combined if voltage same

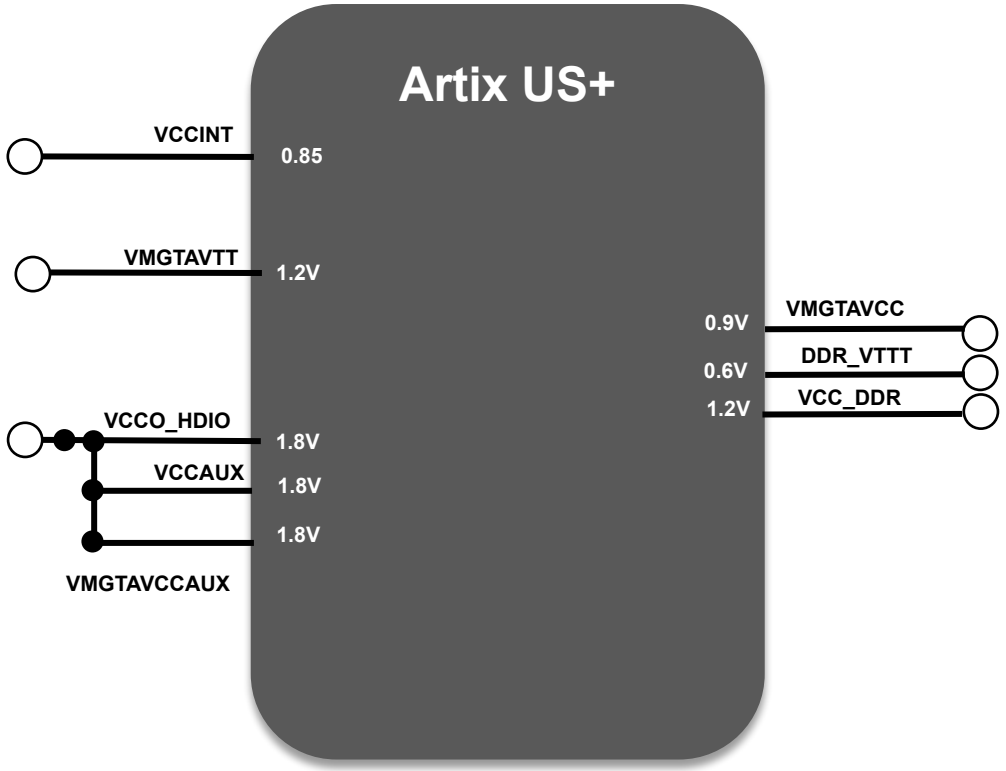


Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree: Virtex UltraScale+ (Min Rails)

PVIN = 12V

#	Rail	Seq	Vout (V)	Iout (A)
1	VCCINT, VCCINT_IO, VCCBRAM	1	0.85	60
2	VCCAUX, VCCAUX_IO, VCCADC	2	1.8	3
3	VMGTAVTT	3	1.2	10
4	VMGTAVCCAUX	4	1.8	0.5
5	VMGTACCC	5	0.9	6
6	VCCO_HDIO, VCCO_HPIO	6	1.8	6
7	VCC_DDR	6	1.2	4
8	DDR_VTT, DDR_VREF	7	0.6	2

Power Tree Mapping: Virtex UltraScale+ (Min Rails)

PVIN = 12V

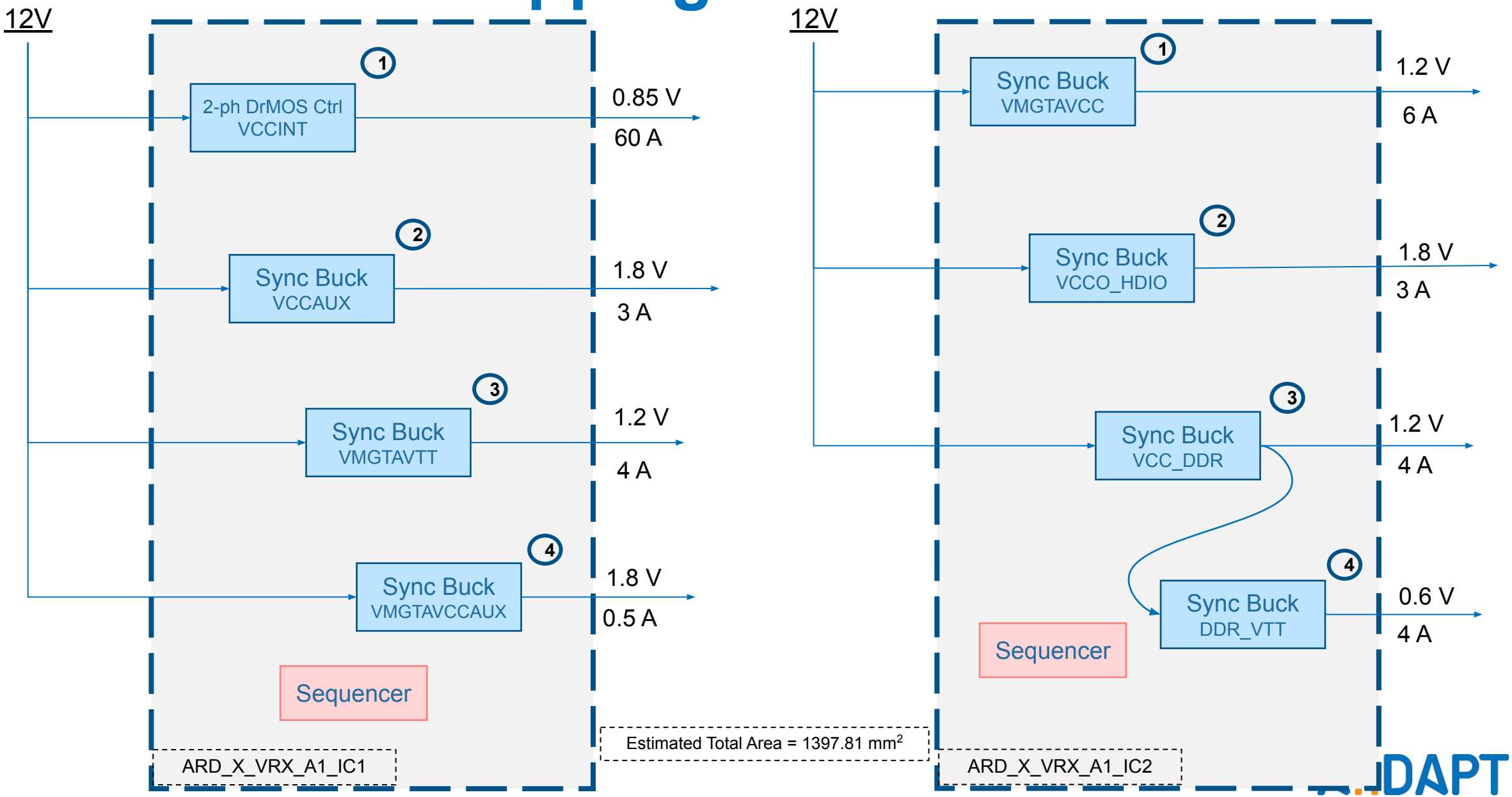
#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT Product
1	VCCINT (VCCINT, VCCINT_IO, VCCBRAM)	1	C870	2-ph DrMOS Ctrl	PVIN	12	0.85	60	ARD_X_VRX_A1_IC1
2	VCCAUX (VCCAUX, VCCAUX_IO, VCCADC)	2	C200	Sync Buck	PVIN	12	1.8	3	
3	VMGTAVTT	3	C200	Sync Buck	PVIN	12	1.2	4	
4	VMGTAVCCAUX	4	C200	Sync Buck	PVIN	12	1.8	0.5	
5	VMGTAVCC	5	C200	Sync Buck	PVIN	12	0.9	6	ARD_X_VRX_A1_IC2
6	VCCO_HDIO (VCCO_HDIO, VCCO_HPIO)	6	C200	Sync Buck	PVIN	12	1.8	3	
7	VCC_DDR	6	C200	Sync Buck	PVIN	12	1.2	4	
8	DDR_VTT (DDR_VTT, DDR_VREF)	7	C210	VTT Terminator	VCC_DDR	1.2	0.6	4	

Estimated total area estimated* = 864.59 + 533.22 = 1397.81 mm^2

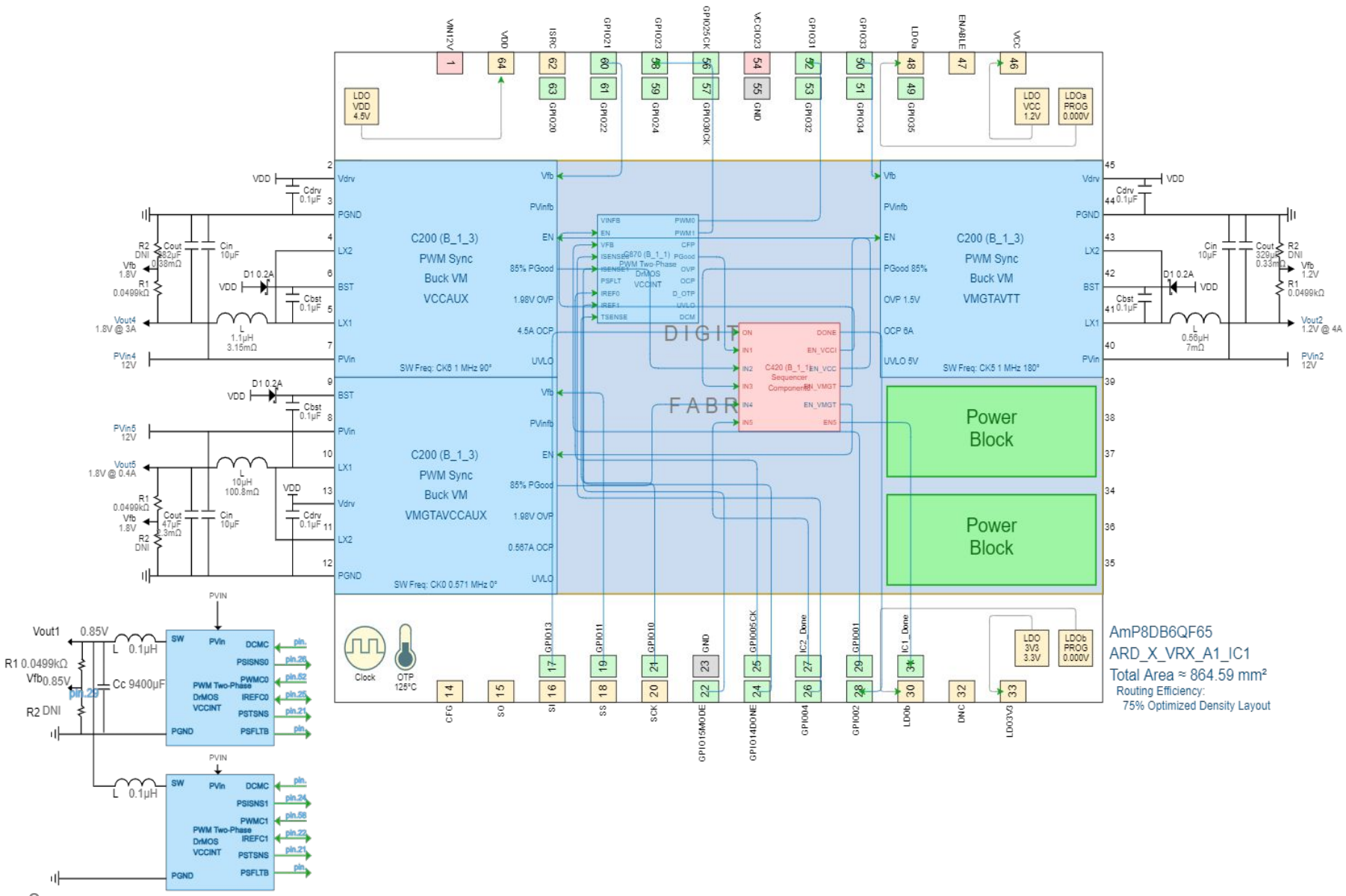
*With 75% Layout optimization density

AnDAPT

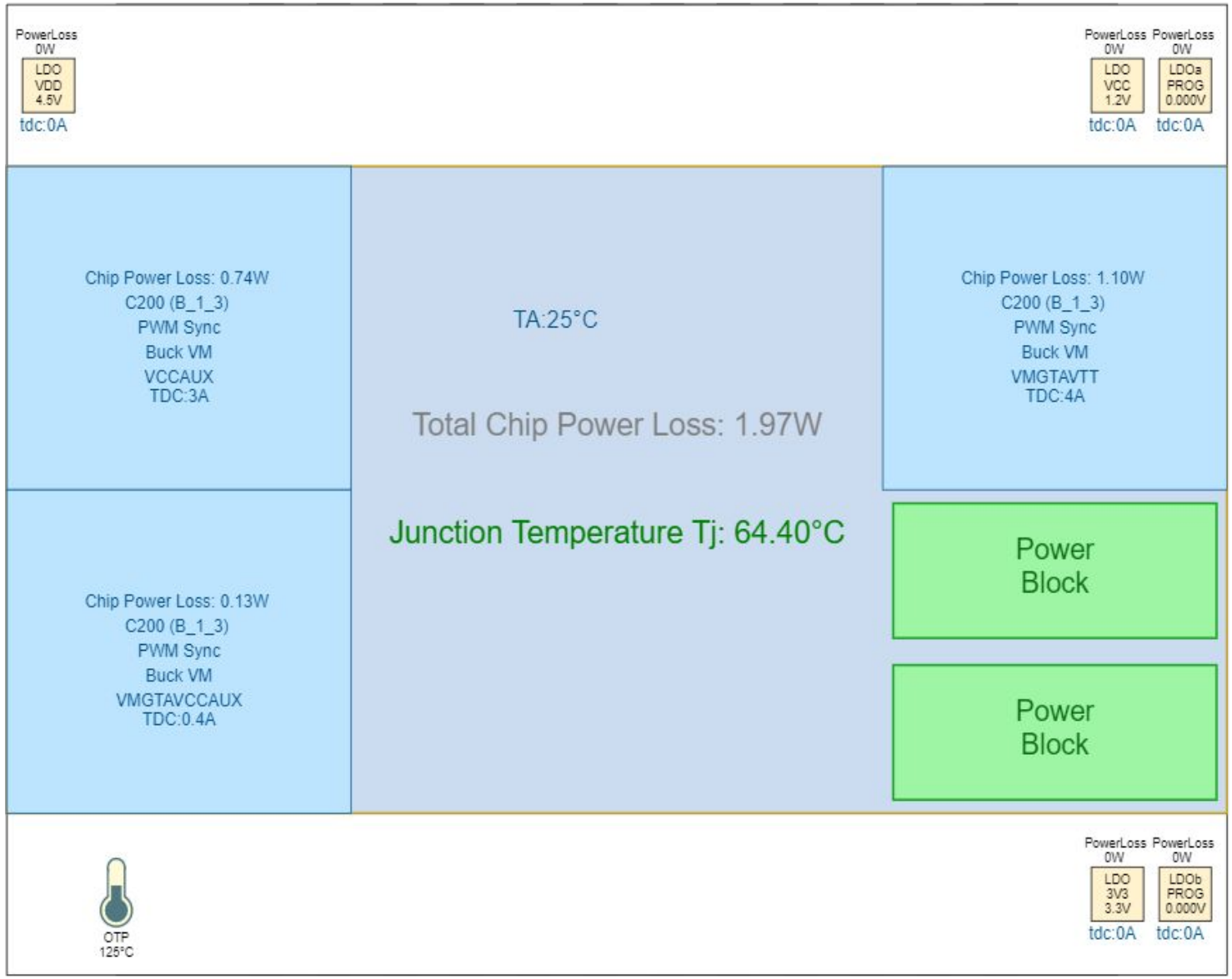
Power Tree Mapping



Mapping (WebAmP View) IC1



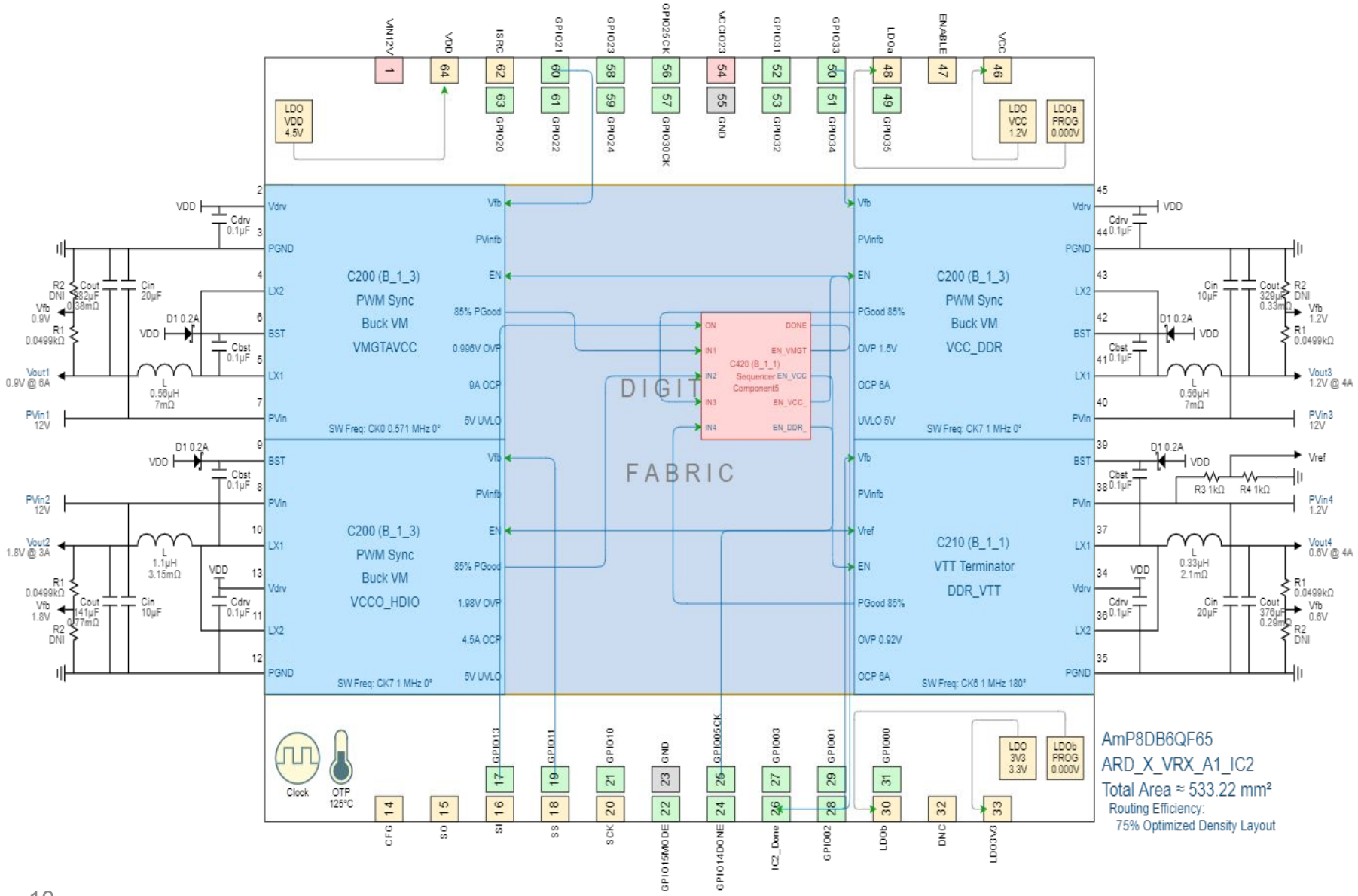
Mapping (Thermal View) IC1



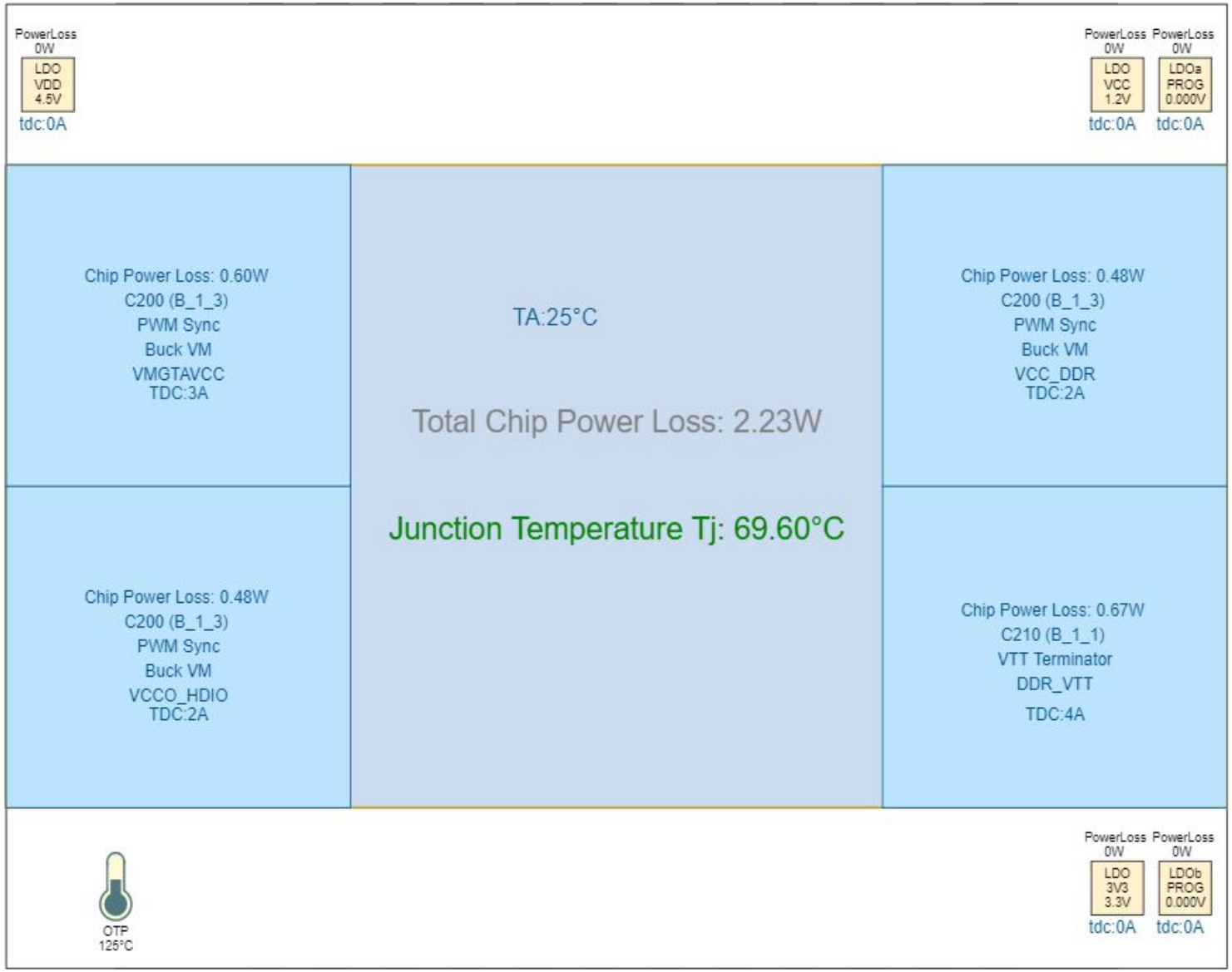
AmP8DB6QF65
ARD_X_VRX_A1_IC1
Total Area ≈ 864.59 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT

Mapping (WebAmP View) IC2

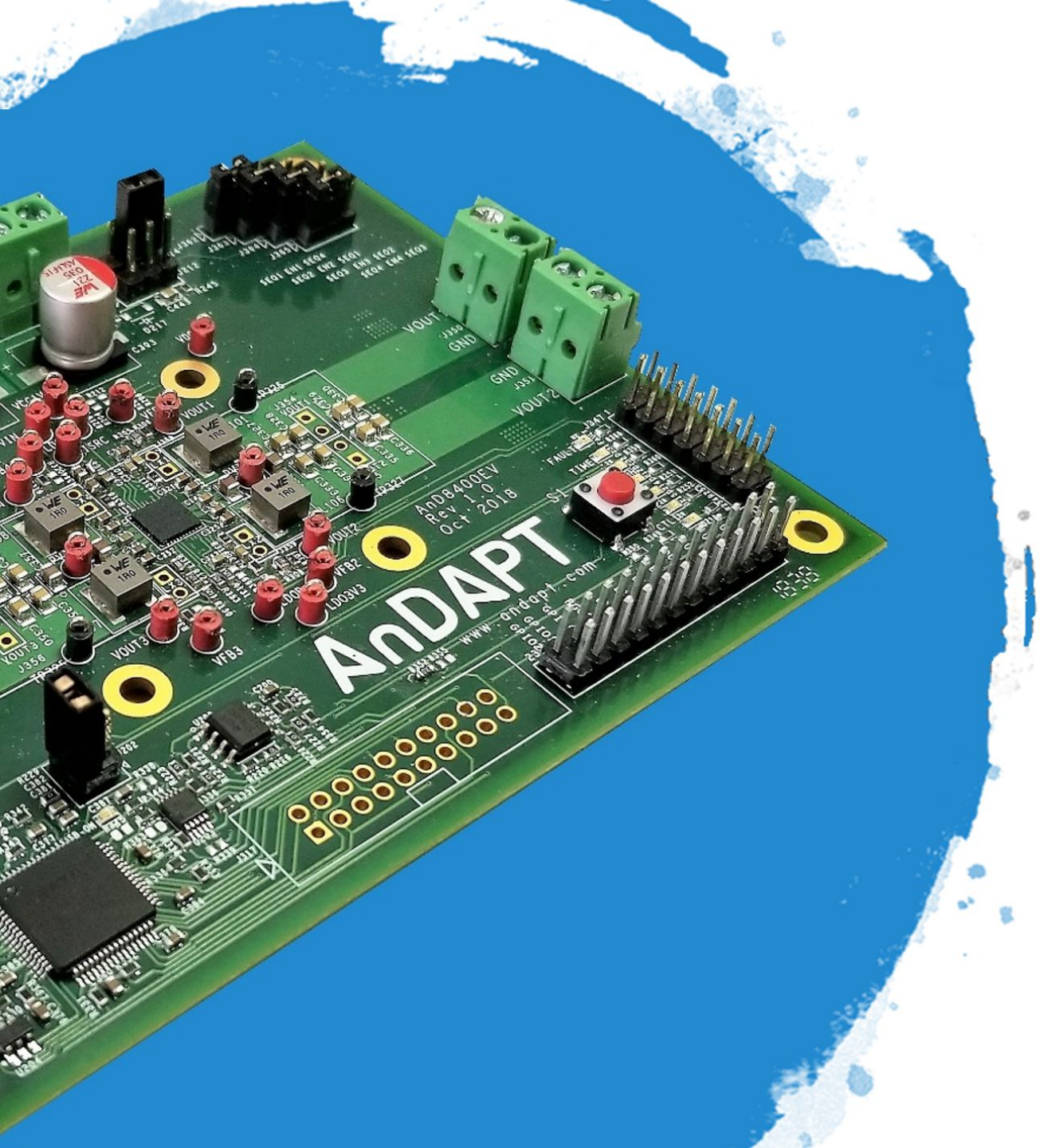


Mapping (Thermal View) IC2



AmP8DB6QF65
ARD_X_VRX_A1_IC2
Total Area ≈ 533.22 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT

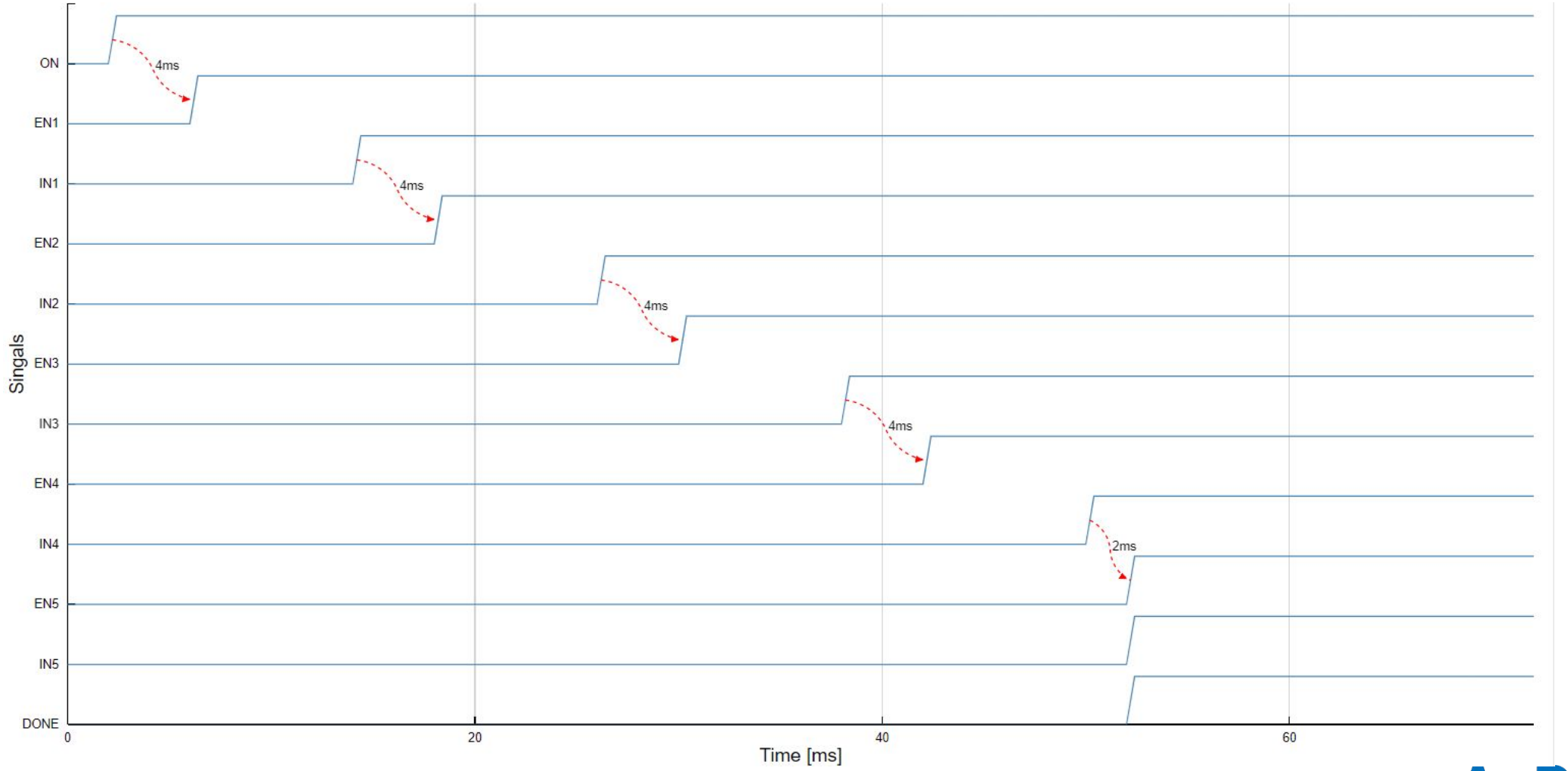


Test Data

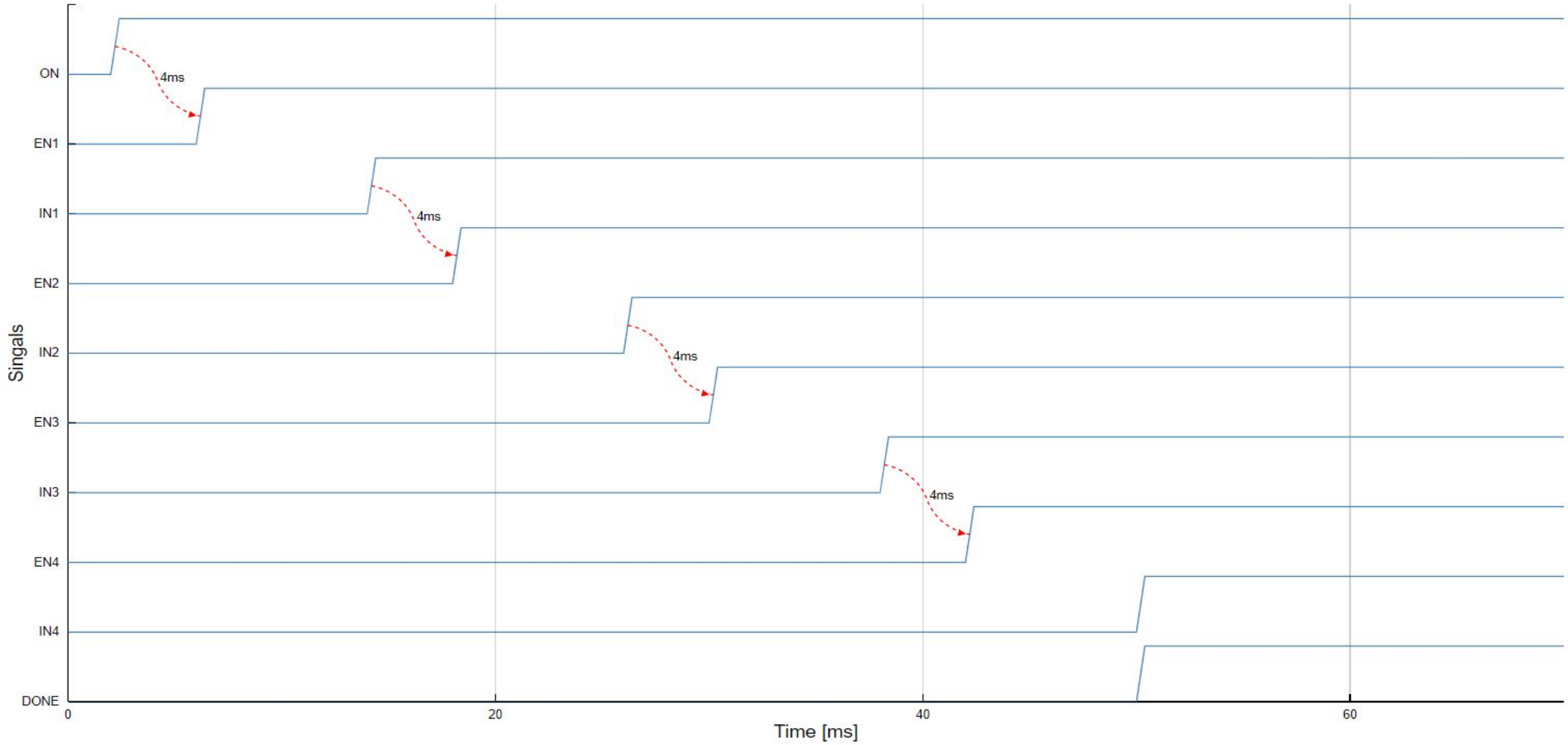
Virtex UltraScale+ (Min Rails)

AnDAPT

Integrated Sequencer Graphic IC1 (Turn ON)



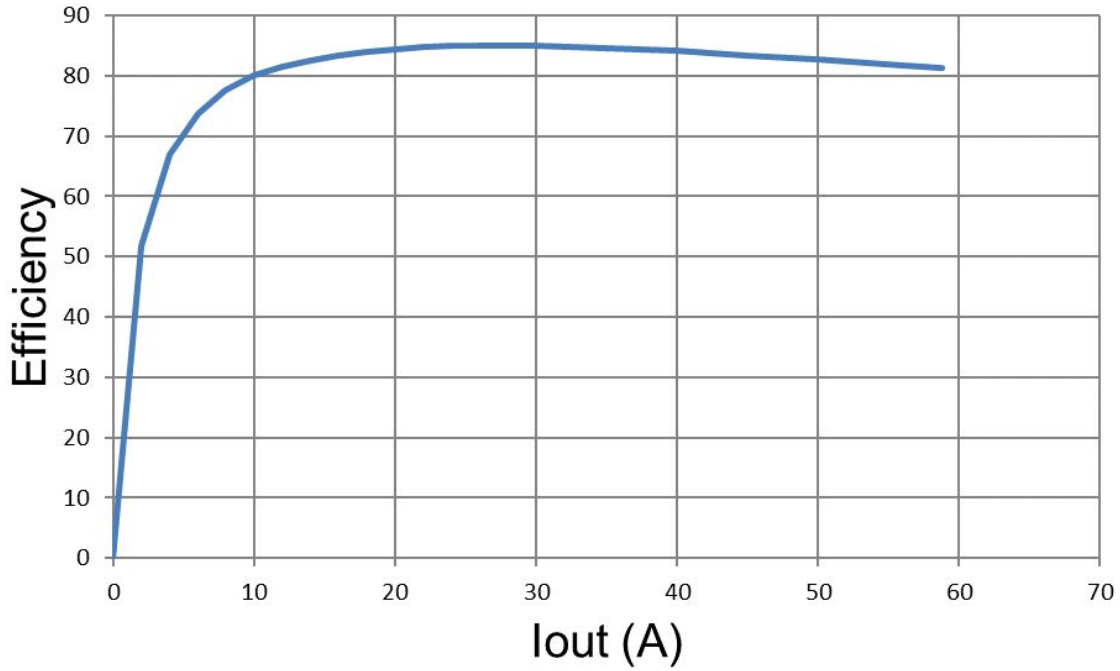
Integrated Sequencer Graphic IC2 (Turn ON)

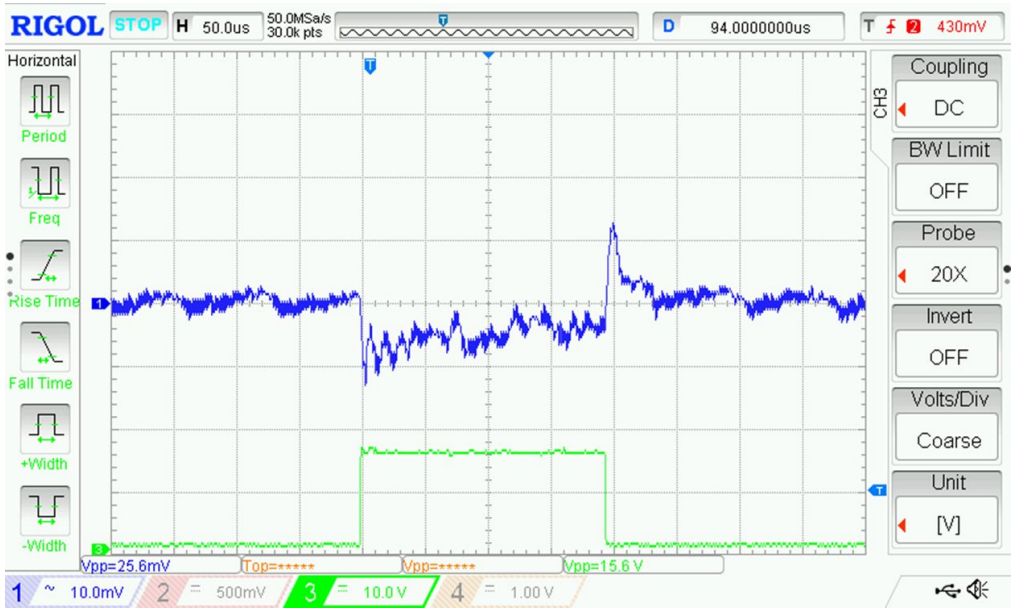


VCCINT, VCCINT_IO, VCCBRAM 0.85 V / 60 A

- C870 2-ph DrMOS Ctrl
- Fsw = 1 MHz
- L = 0.1 µH, P/N Wurth 7443082010
- C = 20x220 uF

Efficiency & Transient

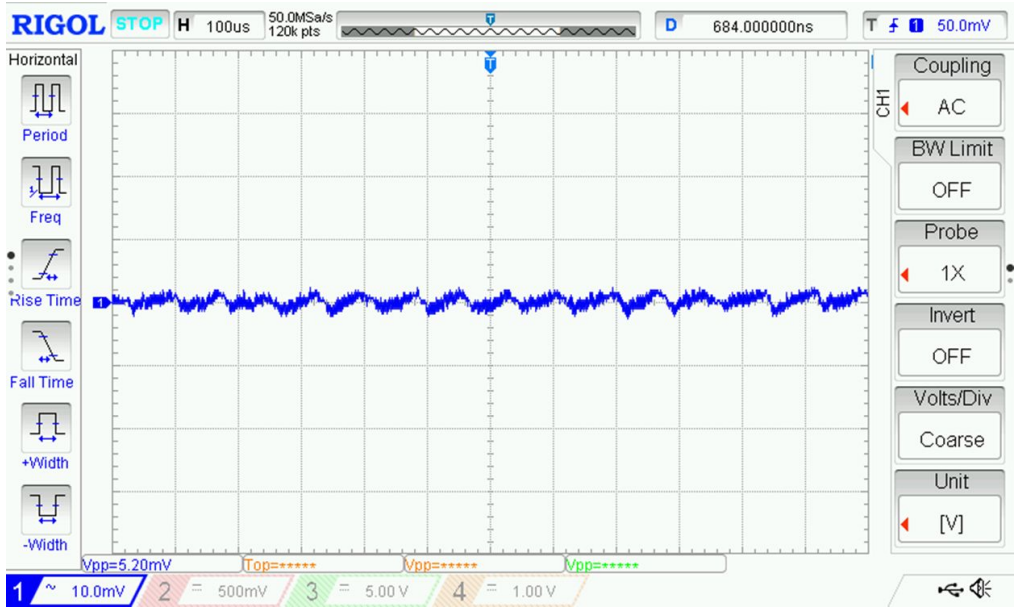




Vout = 0.85 V
Transient 45A – 60A @ 100 A/µs
V_{PP} = 25.6 mV
Fsw = 1 MHz
Lout = 0.1 µH, Cout = 20 x 220 µF

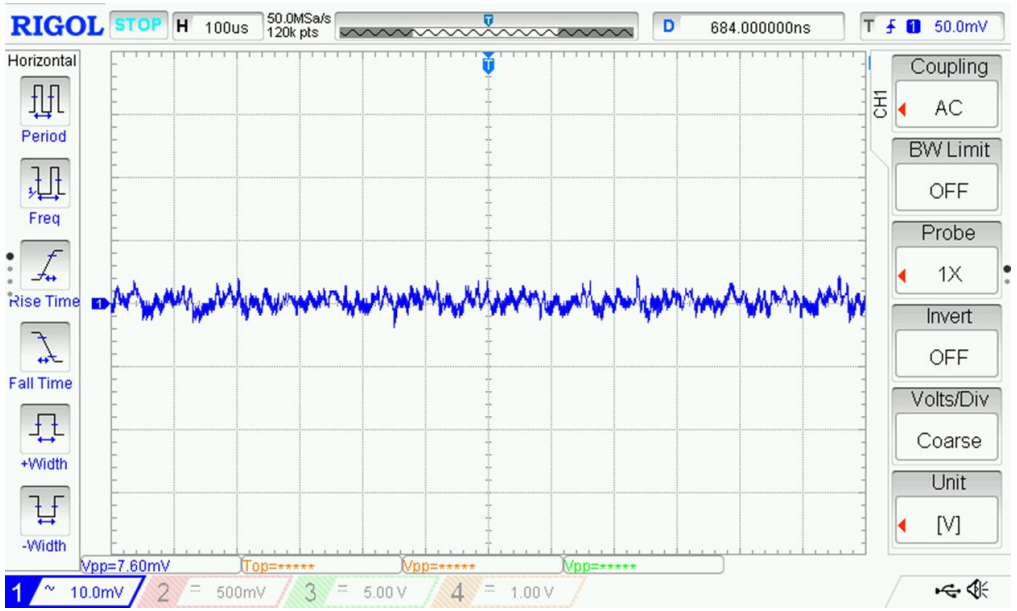
AnDAPT

Ripple



No Load
V_{PP} = 5.2 mV

Vout = 0.85 V



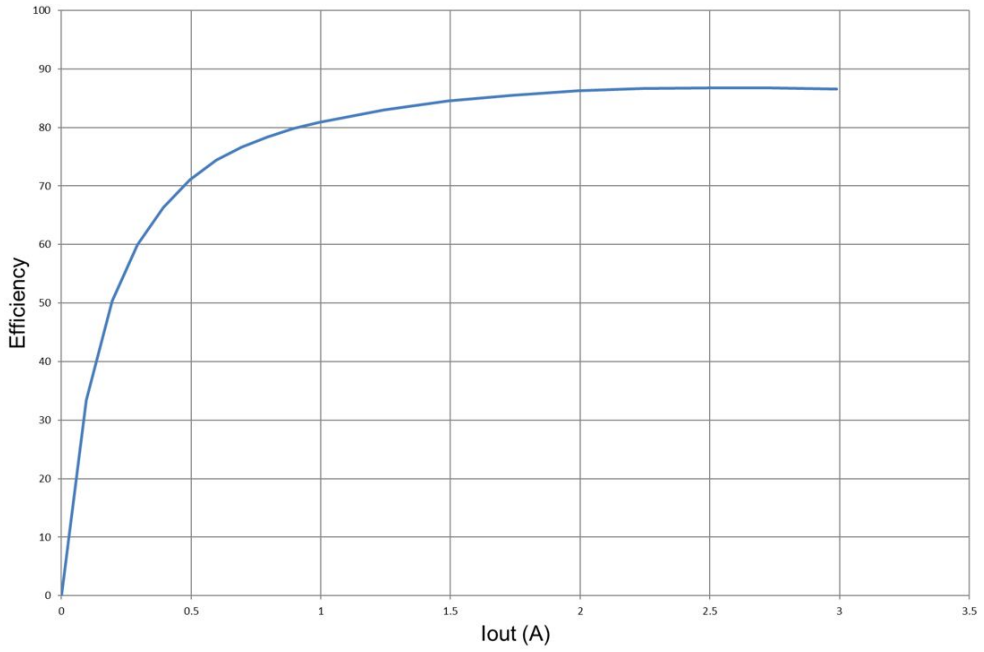
60 A Load
V_{PP} = 7.6 mV

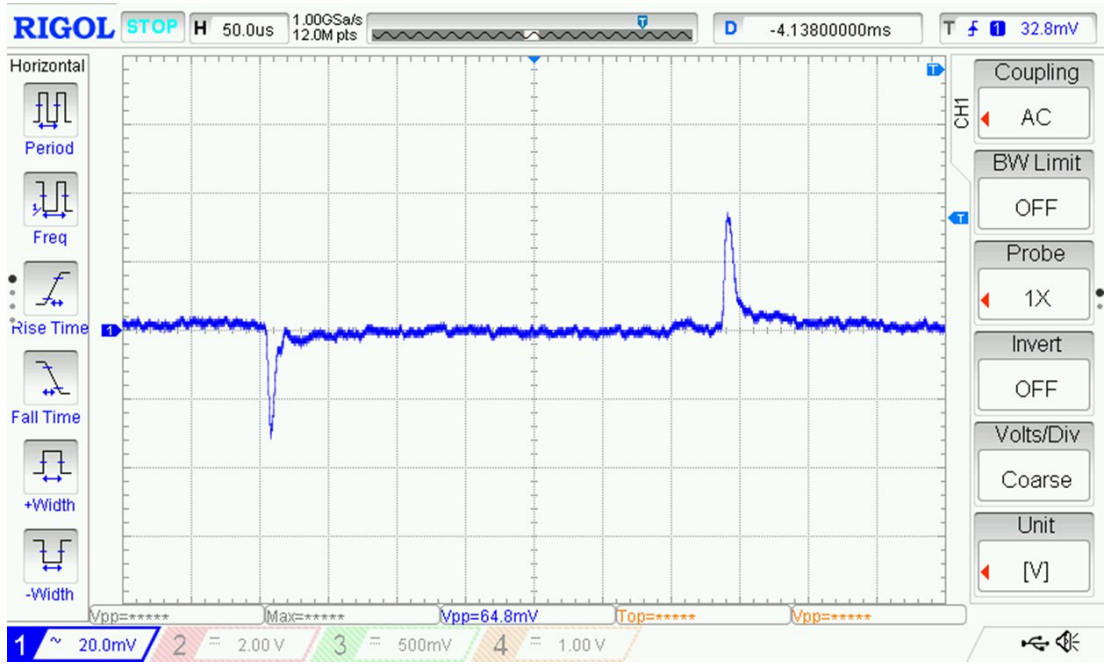
AnDAPT

VCCAUX, VCCAUX_IO, VCCADC 1.8 V / 3 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 6x47 uF

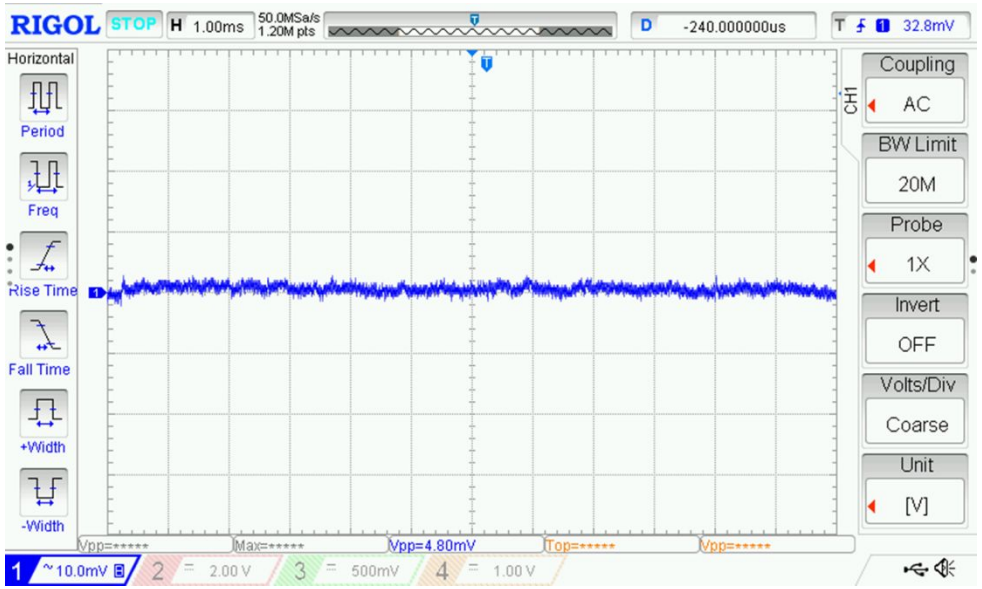
Efficiency & Transient





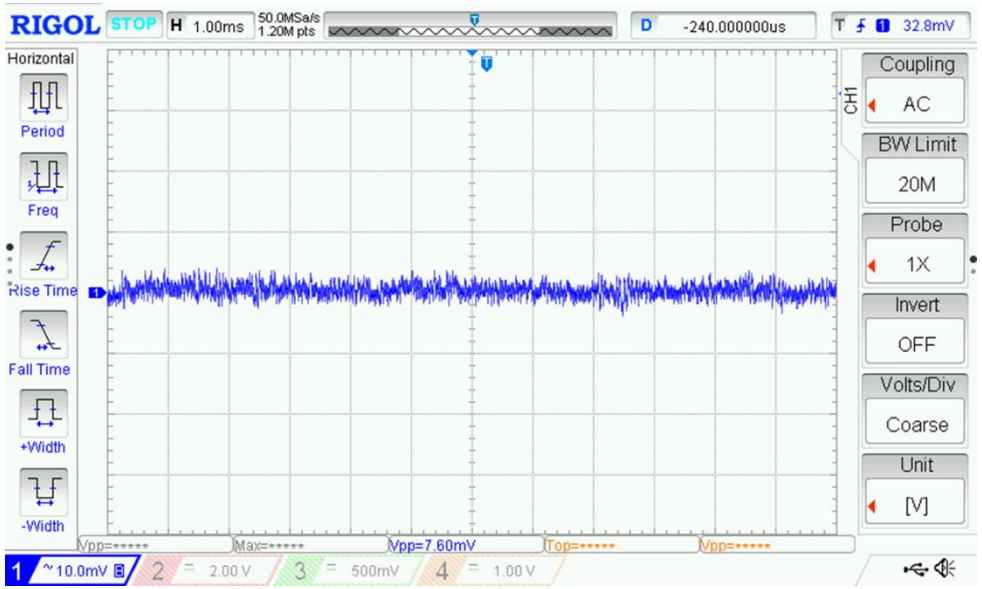
Vout = 1.8 V
Transient 0.3 A – 3 A @ 10 A/µs
V_{PP} = 64.8 mV
Fsw = 1 MHz
Lout = 1.1 µH, Cout = 6 x 47 µF

Ripple



No Load
V_{PP} = 4.8 mV

Vout = 1.8 V



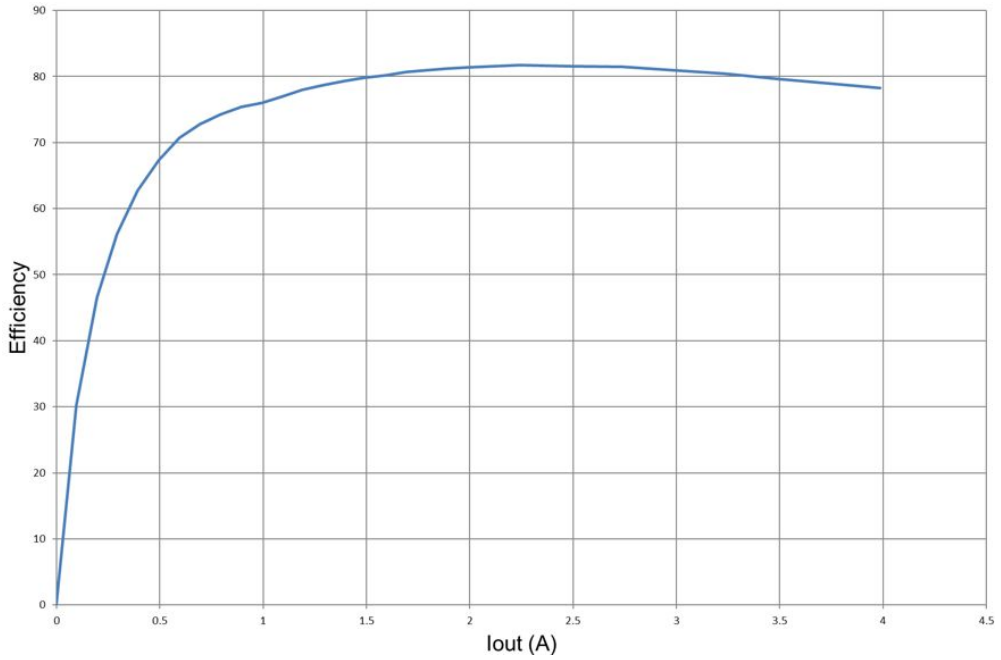
3 A Load
V_{PP} = 7.6 mV

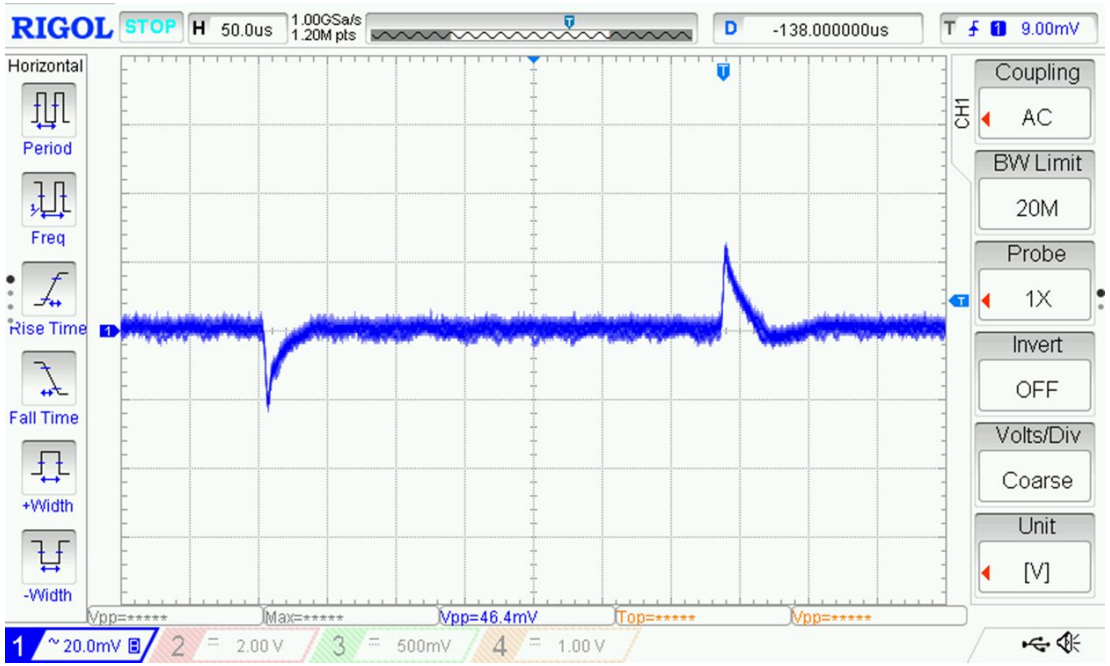
AnDAPT

VMGTAVTT
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

Efficiency & Transient

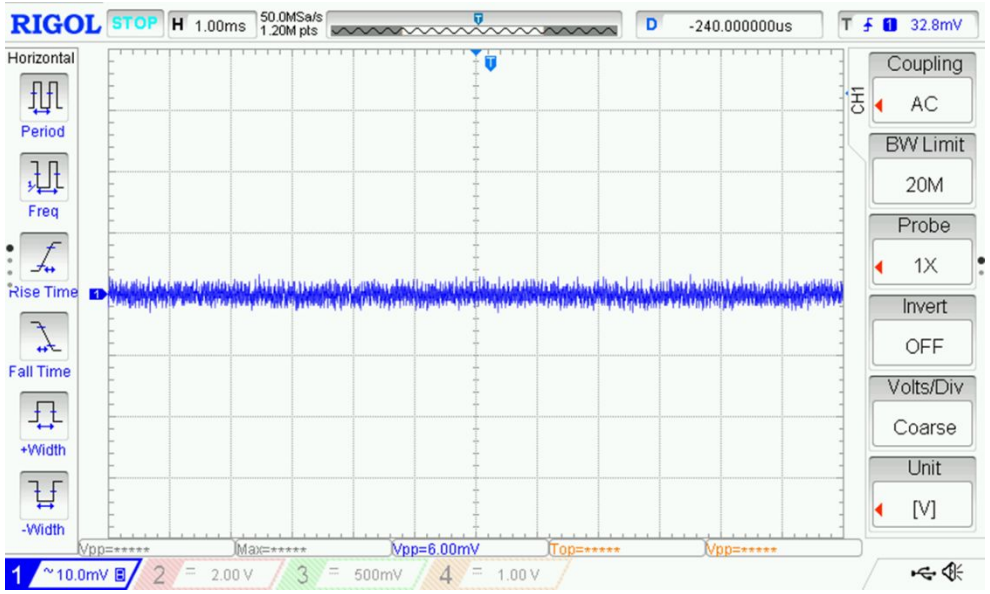




Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

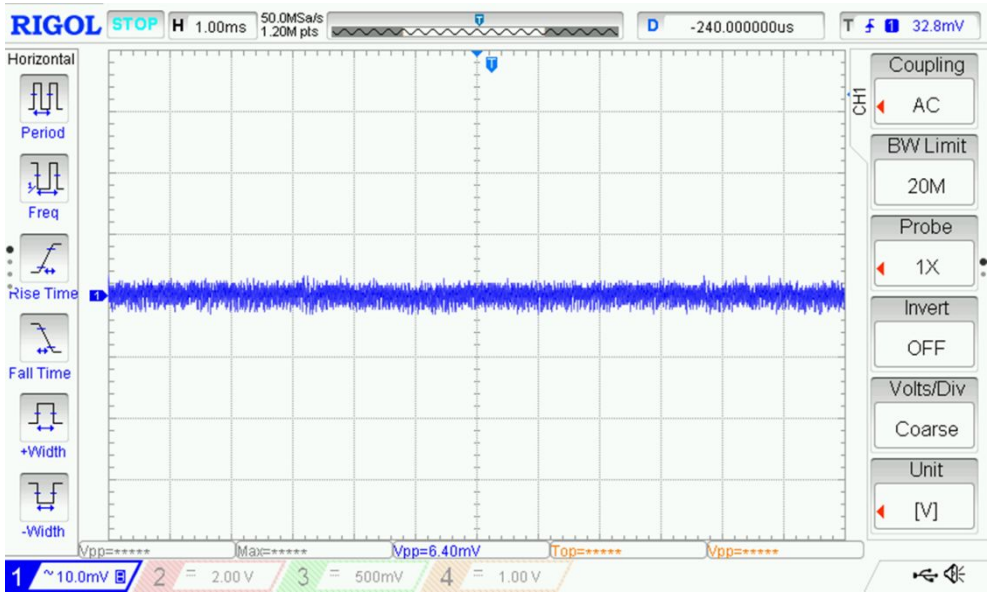
AnDAPT

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



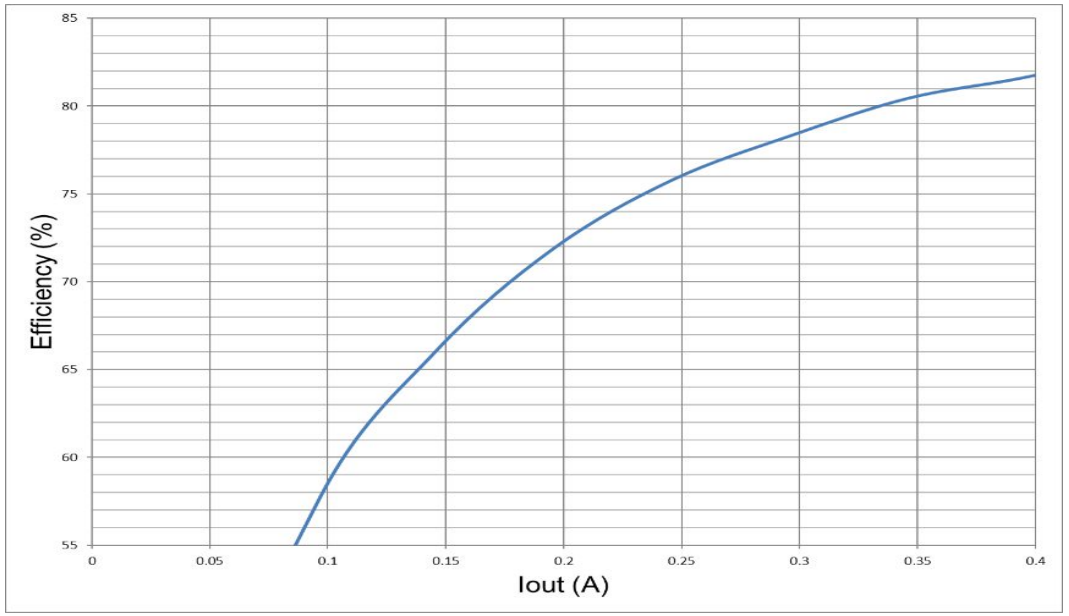
0.035 A Load
V_{PP} = 6.4 mV

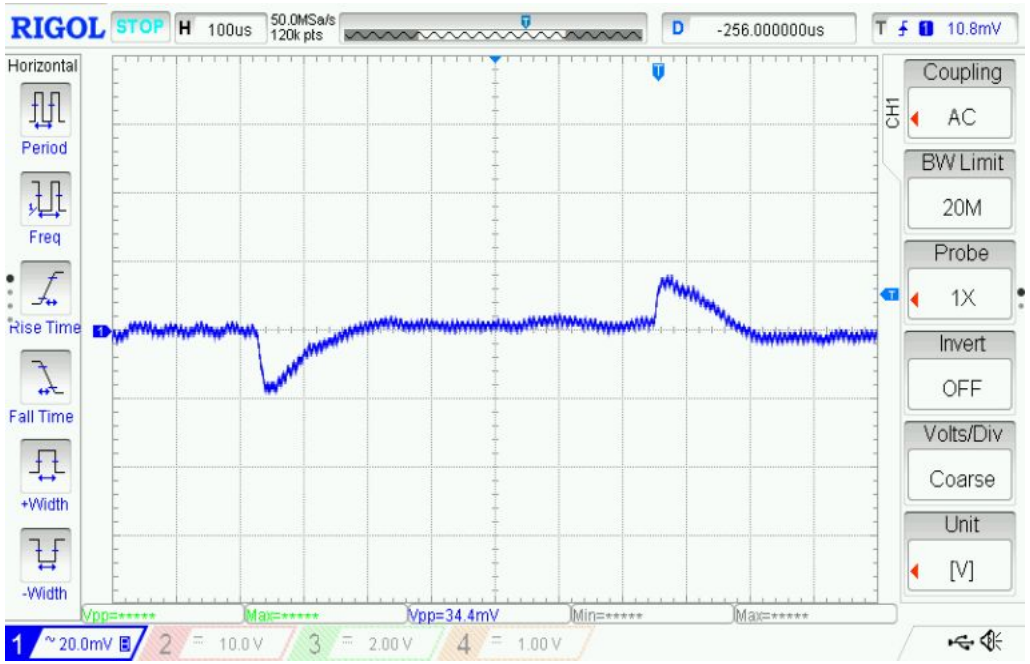
AnDAPT

VMGTAVCCAUX
1.8 V / 0.5 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74438357100
- C = 1x47 uF

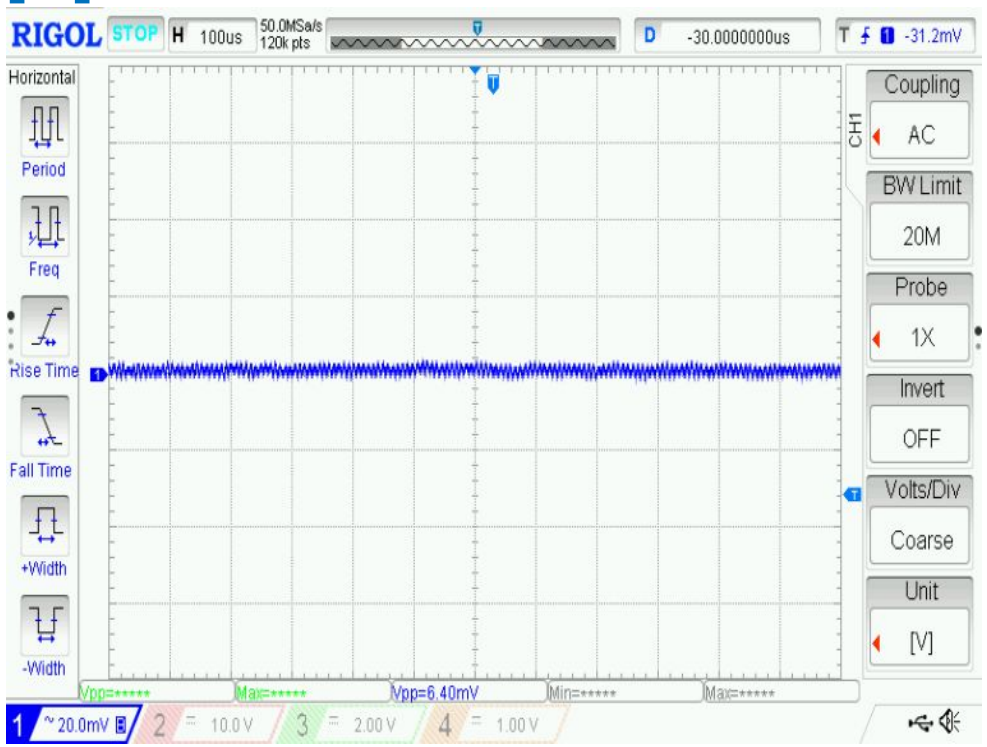
Efficiency & Transient





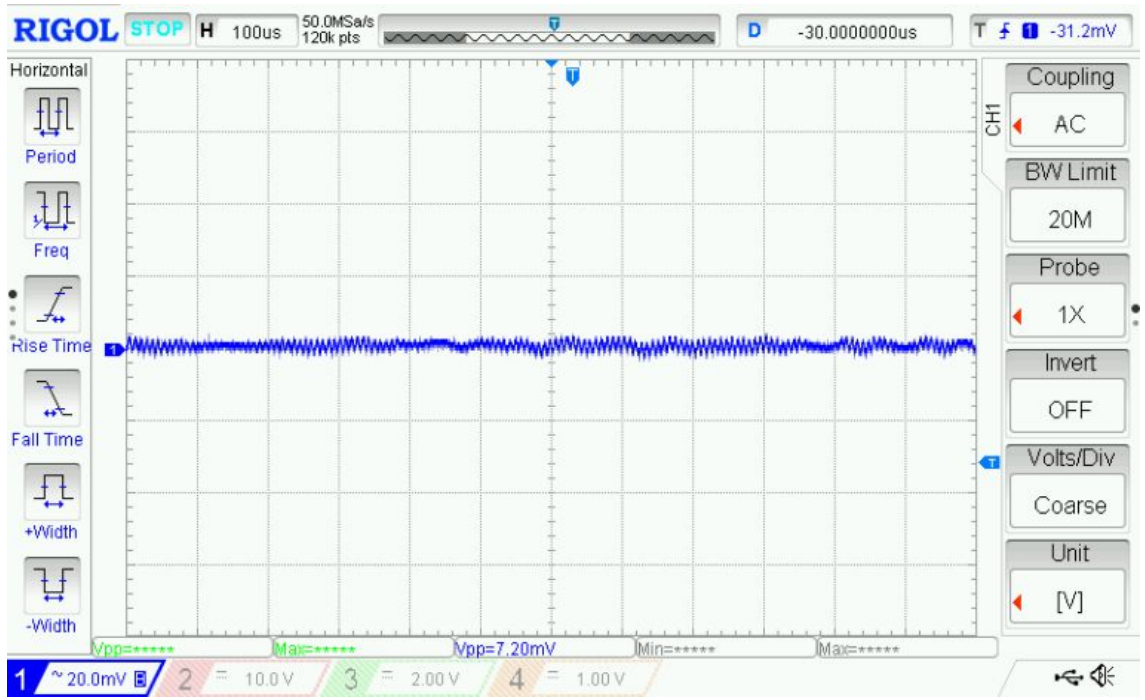
Vout = 1.8 V
Transient 0.12 A – 0.4 A @ 2.5 A/µs
V_{PP} = 34.4 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1 x 47 µF

Ripple



No Load
V_{PP} = 6.4 mV

Vout = 1.8 V



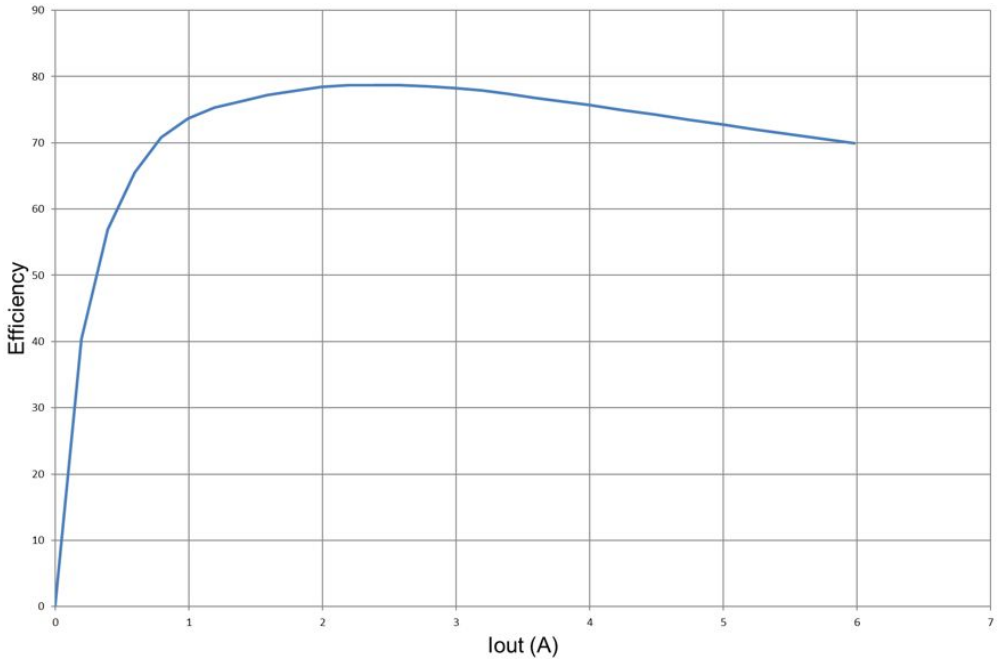
0.4 A Load
V_{PP} = 7.2 mV

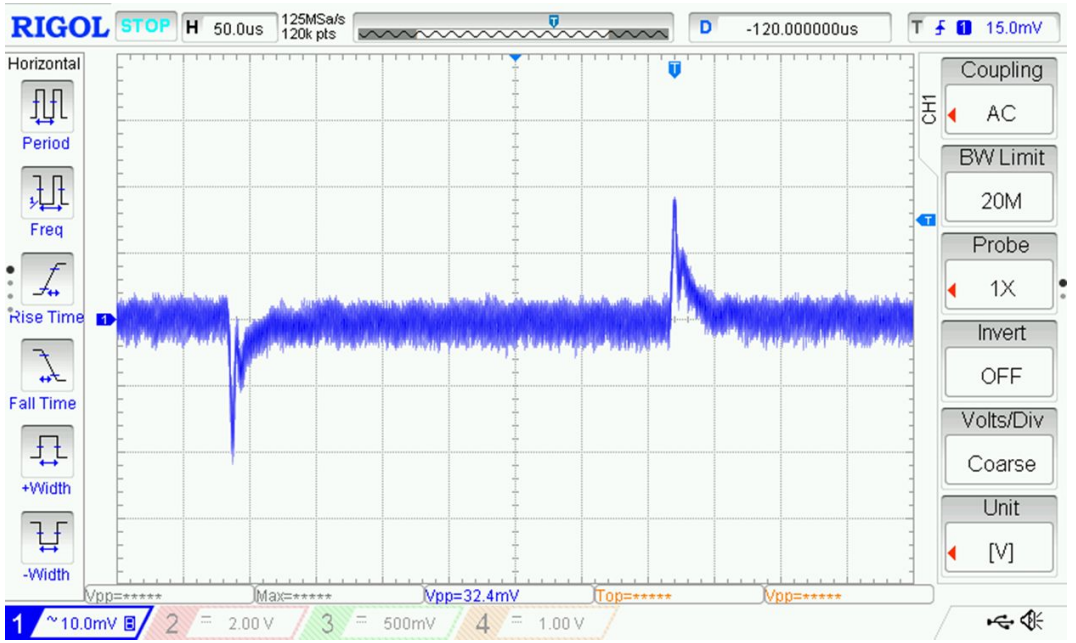
AnDAPT

VMGTAVCC
0.9 V / 6 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 6x47 uF

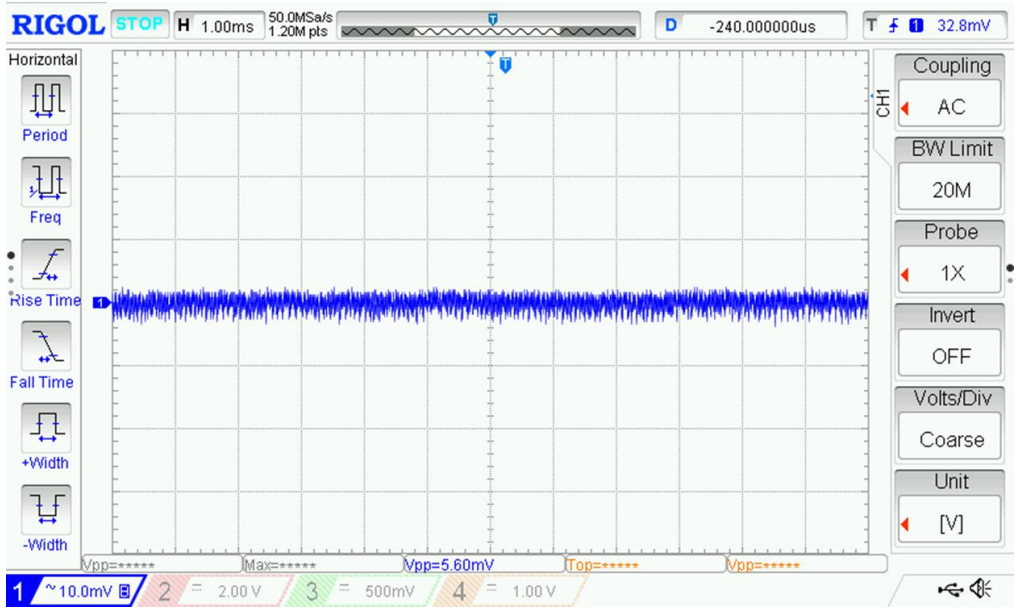
Efficiency & Transient





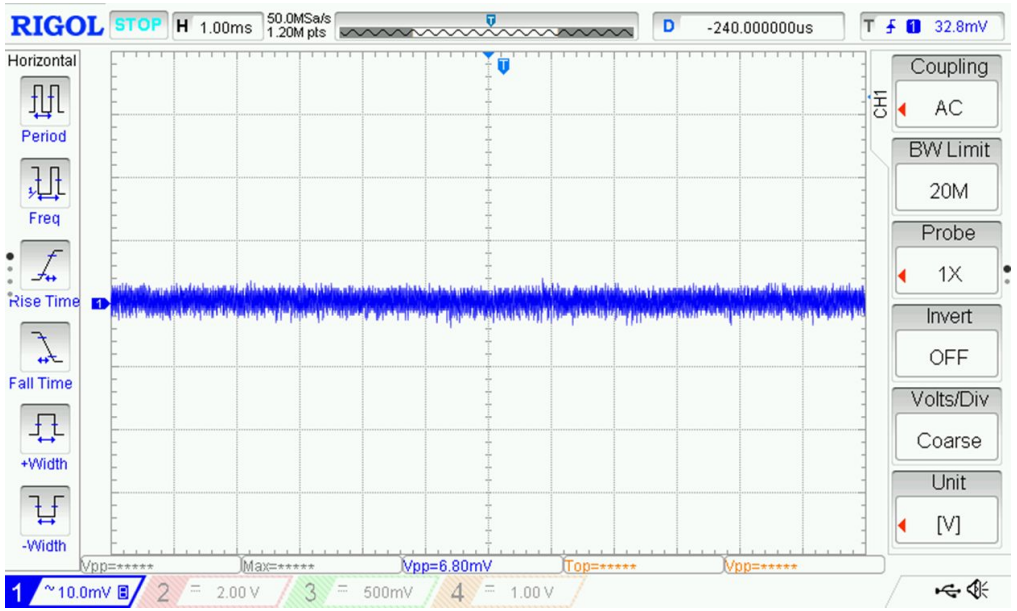
Vout = 0.9V
Transient 4.5 A – 6 A @ 10 A/µs
V_{PP} = 32.4 mV
Fsw = 571 kHz
Lout = 0.56 µH, Cout = 6 x 47 µF

Ripple



No Load
V_{PP} = 5.6 mV

Vout = 0.9 V



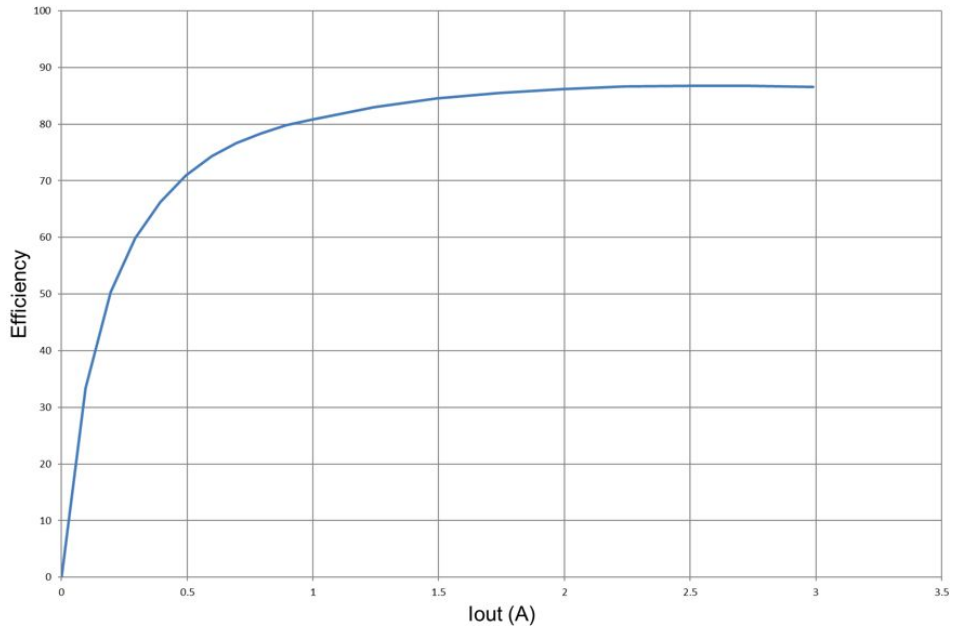
6 A Load
V_{PP} = 6.8 mV

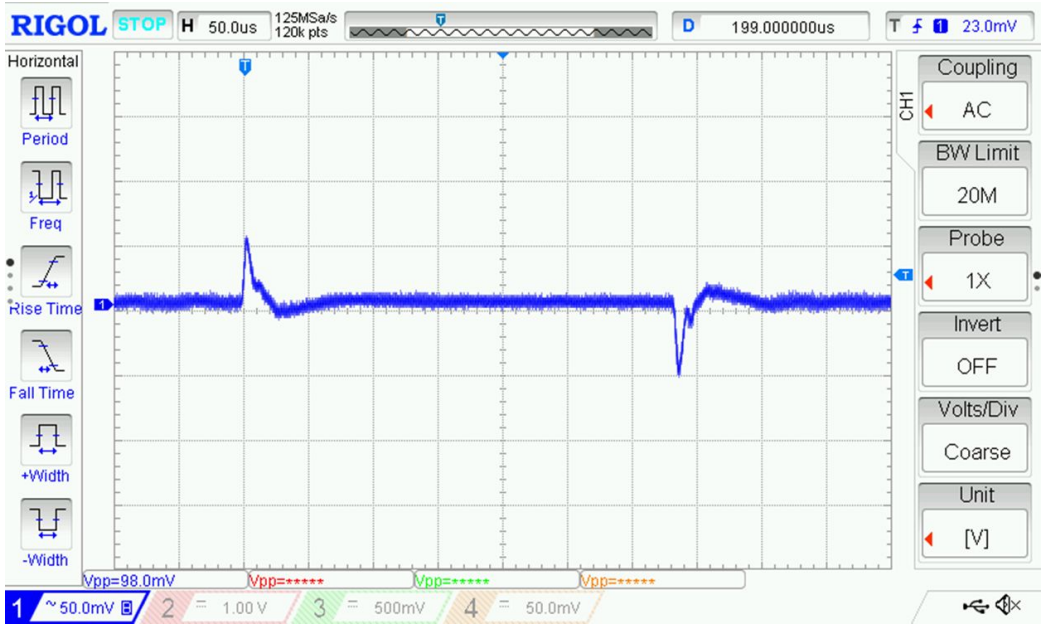
AnDAPT

VCCO_HDIO, VCCO_HPIO 1.8 V / 3 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

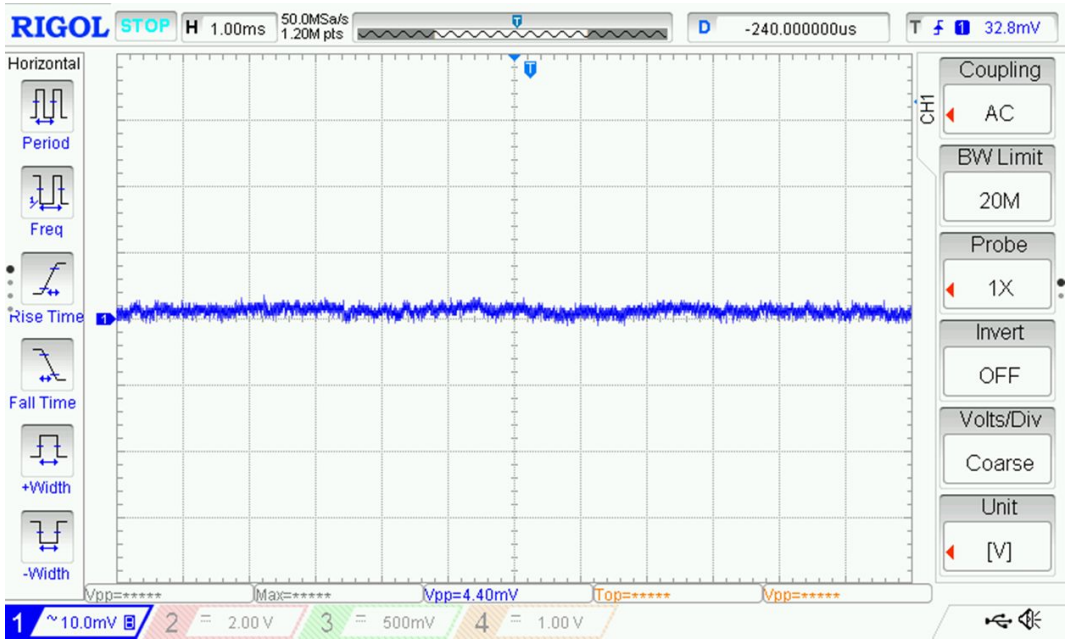
Efficiency & Transient





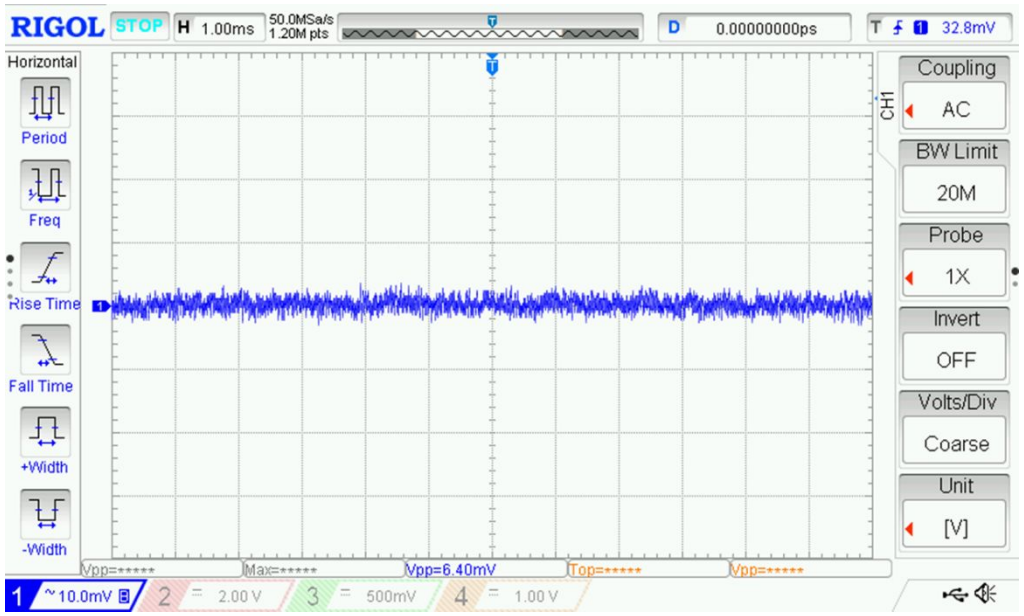
Vout = 1.8 V
Transient 0.3 A – 3A @ 10 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

Ripple



No Load
V_{PP} = 4.4 mV

Vout = 1.8 V



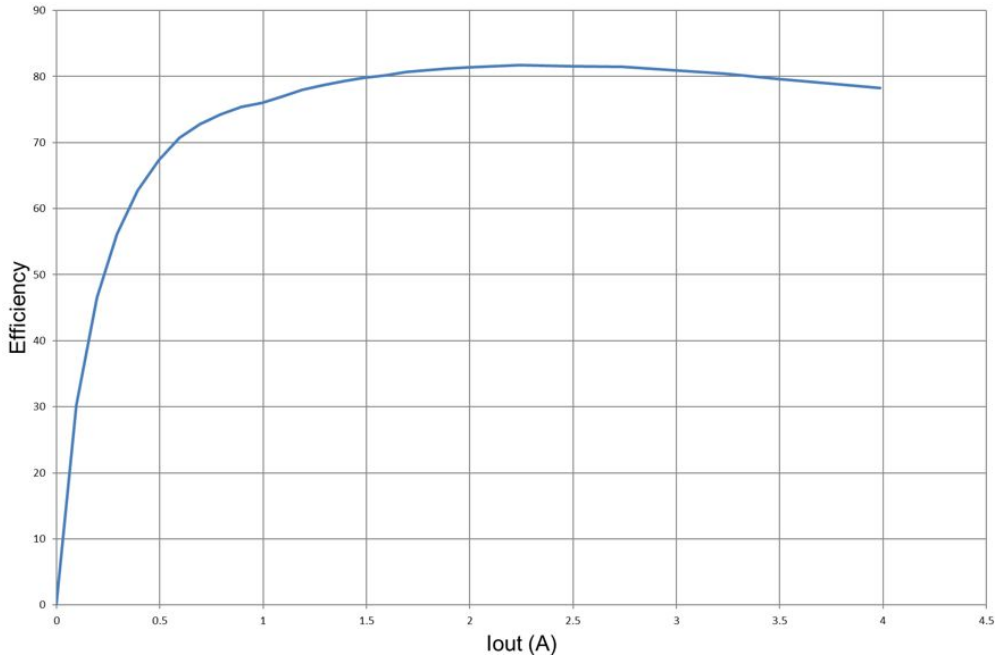
3 A Load
V_{PP} = 6.4 mV

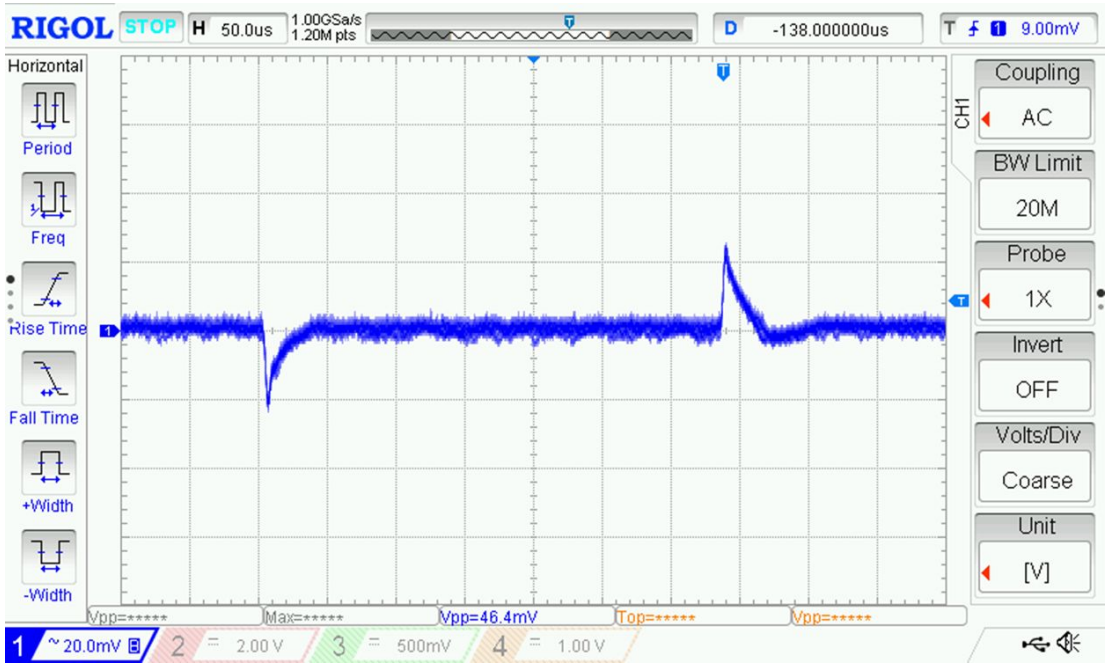
AnDAPT

VCC_DDR
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

Efficiency & Transient

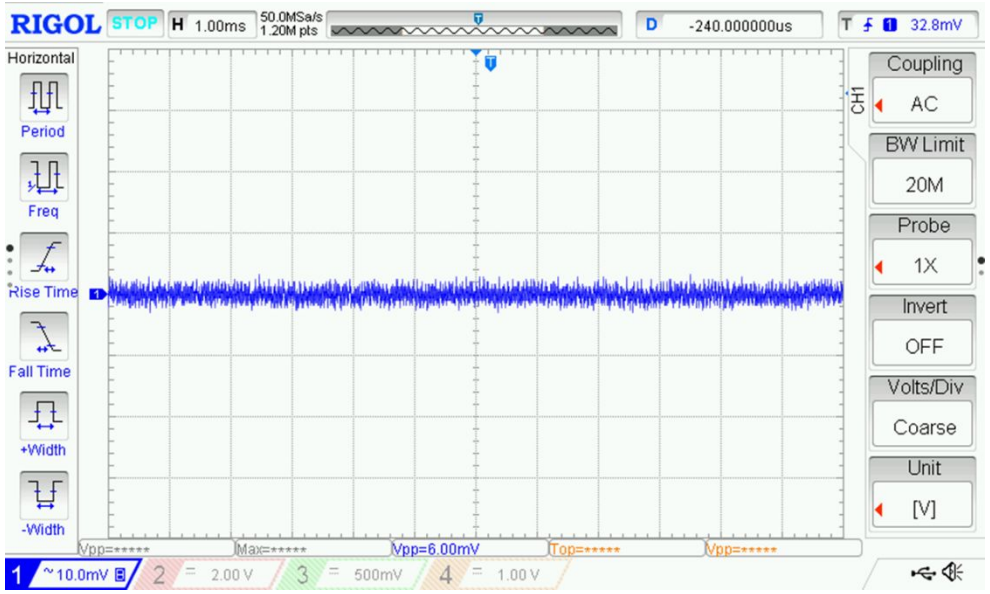




Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

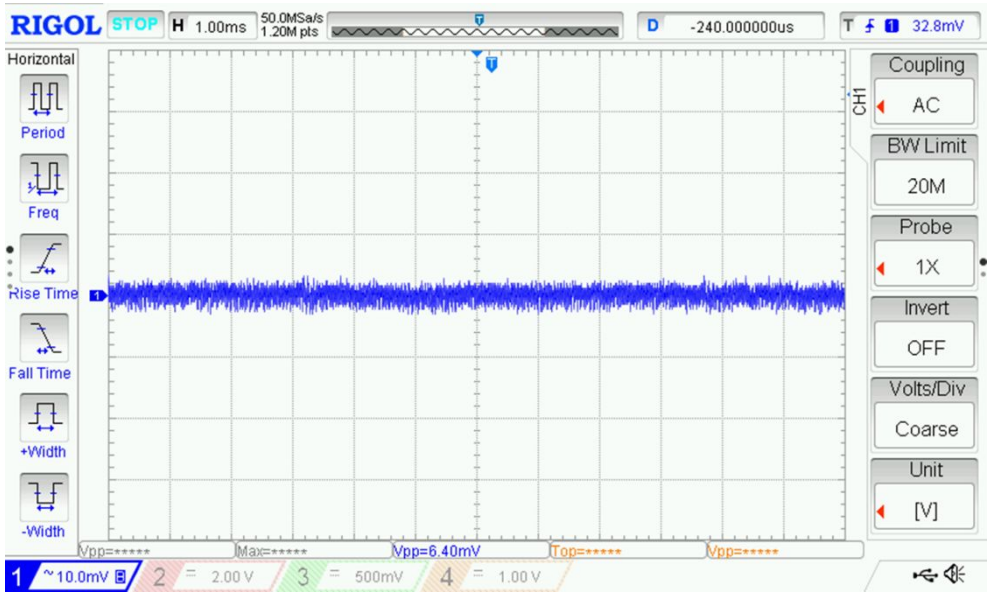
AnDAPT

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



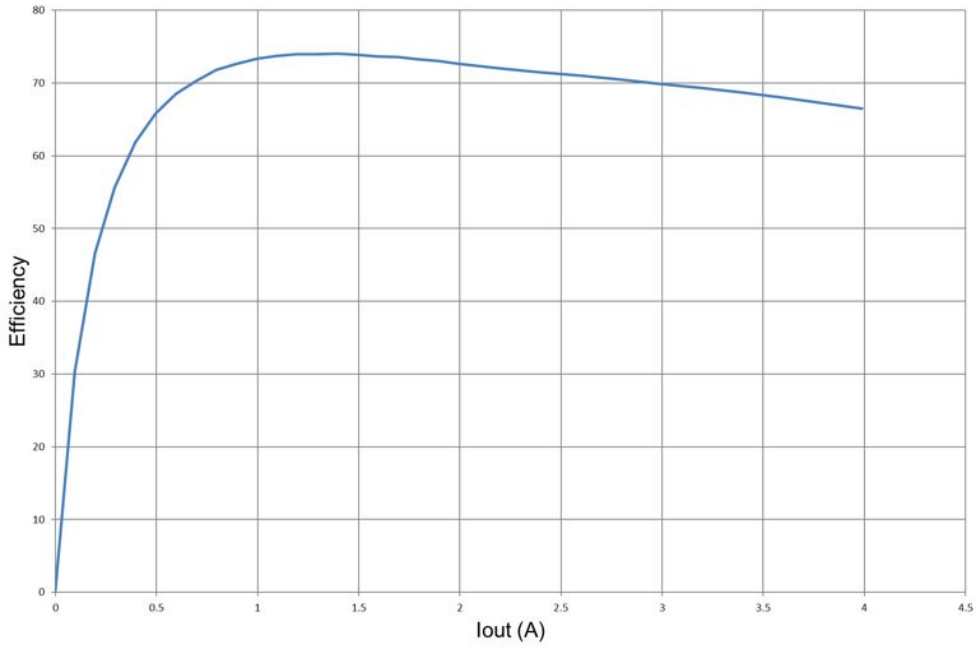
0.035 A Load
V_{PP} = 6.4 mV

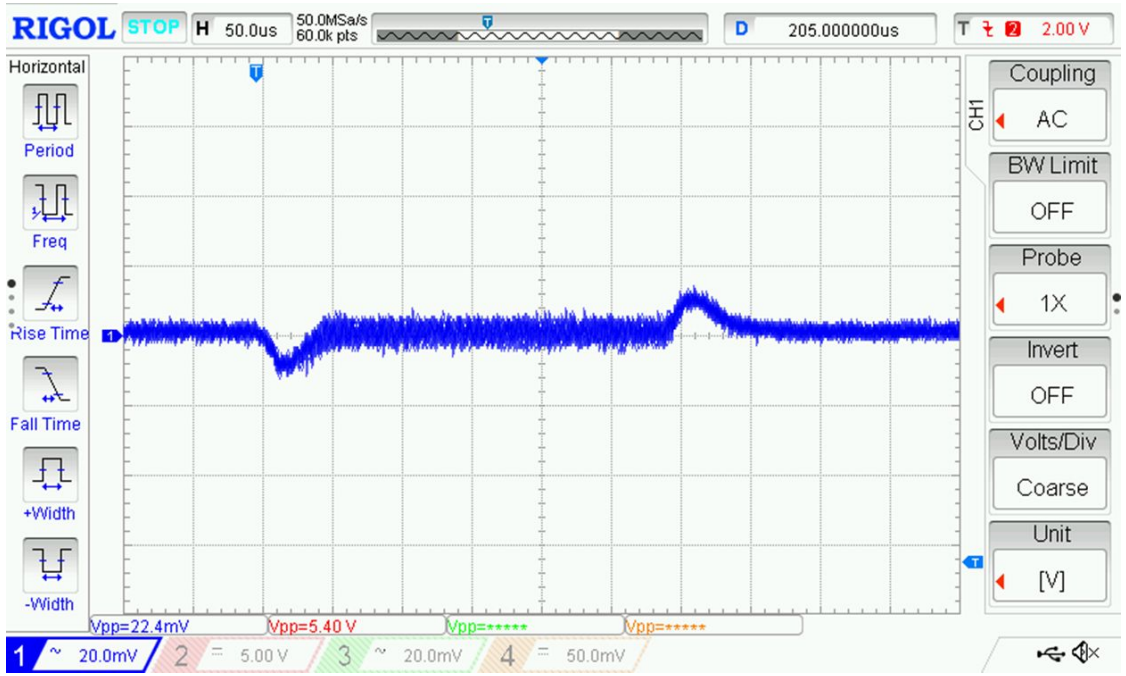
AnDAPT

DDR_VTT, DDR_VREF
0.6 V / 4 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.33 µH, P/N Wurth 744393440033
- C = 8x47 uF

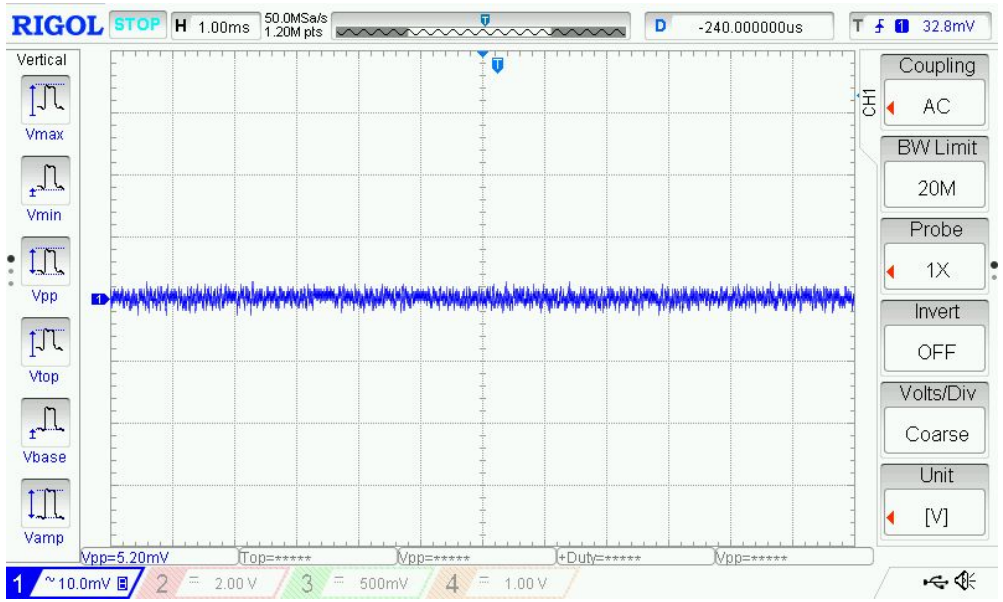
Efficiency & Transient





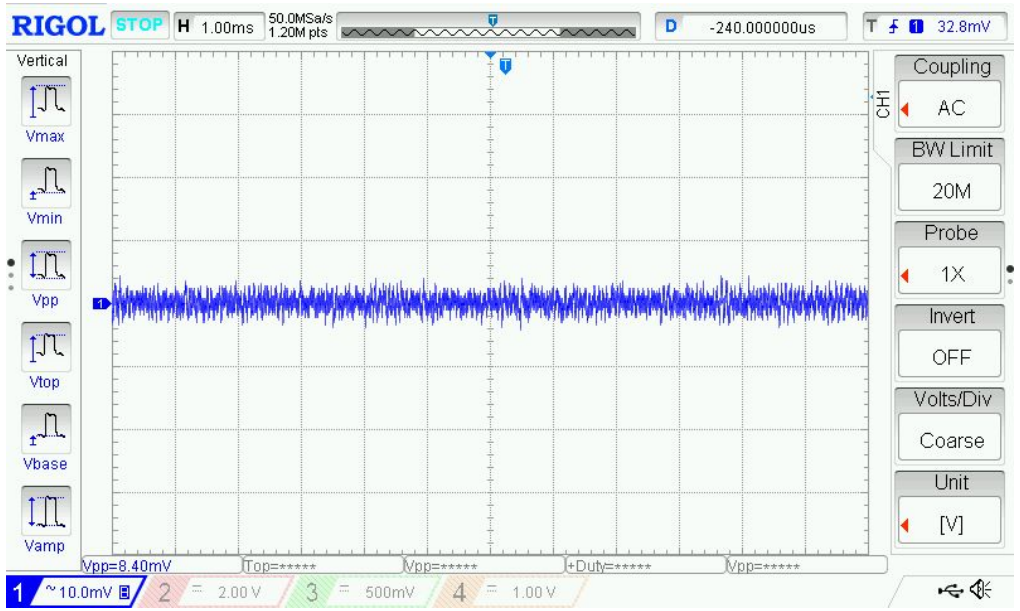
Vout = 0..6 V
Transient 3A – 4 A @ 10 A/µs
V_{PP} = 20.4 mV
Fsw = 1 MHz
Lout = 0.33 µH, Cout = 8 x 47 µF

Ripple



No Load
V_{PP} = 5.2 mV

Vout = 0.6 V



4 A Load
V_{PP} = 8.4 mV

Thank You

AnDAPT