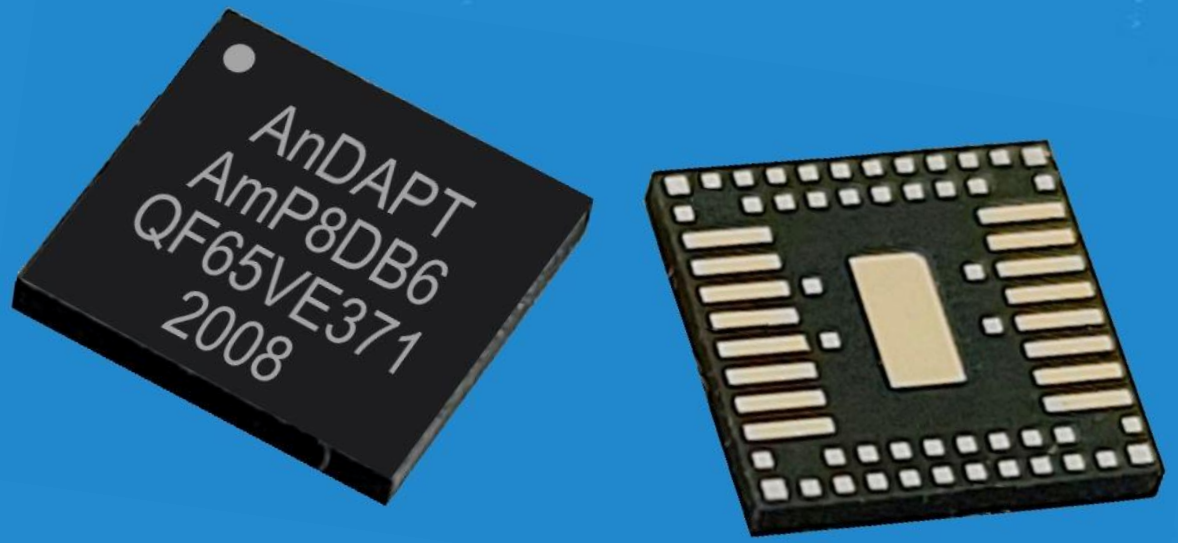


Virtex UltraScale+ (Full Power Management)

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

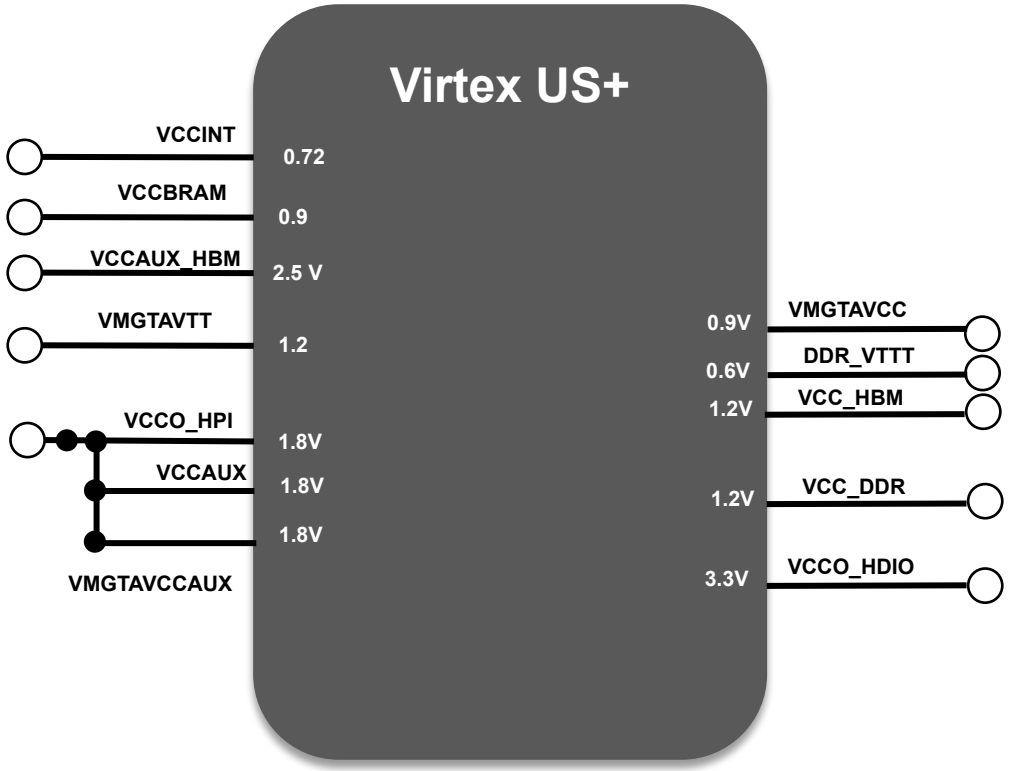
- Xilinx Virtex UltraScale+ (US+) family of devices SKUs (Full Power Management)
- Virtex US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for Virtex US+ family FPGAs

Virtex UltraScale+ Device SKUs Covered- Full Power Management

Supported SKUs
XCVU31P
XCVU33P
XCVU35P

Virtex UltraScale+ (Full Power Management)

Can be combined if voltage same



Power Tree: Virtex UltraScale+ (Full Power Management)

PVIN = 12V

#	Rail	Seq	Vout (V)	Iout (A)	Comment
1	VCCINT	1	0.72	60	
2	VCCINT_IO, VCCBRAM	1	0.9	6	
3	VCCAUX, VCCAUX_IO, VCCADC	2	1.8	3	
4	VMGTAVTT	3	1.2	6	
5	VMGTAVCCAUX	4	1.8	0.5	
6	VMGTAVCC	5	0.9	6	
7	VCC_HBM/VCC_IO_HBM	6	1.2	15	
8	VCCAUX_HBM	7	2.5	0.6	
9	VCCO_HDIO	6	3.3	3	
10	VCCO_HPIO	7	1.8	3	
11	VCC_DDR	6	1.2	4	
12	DDR_VTT, DDR_VREF	7	0.6	4	

Power Tree Mapping: Virtex UltraScale+ (Full Power Management)

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCINT	1	C870	2-ph DrMOS Ctrl	PVIN	12	0.72	60	ARD_X_VRX_A2_IC1
2	VCCBRAM (VCCINT_IO, VCCBRAM)	2	C200	Sync Buck	PVIN	12	0.9	6	
3	VCCAUX (VCCAUX, VCCAUX_IO, VCCADC)	3	C200	Sync Buck	PVIN	12	1.8	3	
4	VMGTAVTT	4	C200	Sync Buck	PVIN	12	1.2	6	
5	VMGTAVCCAUX	5	C200	Sync Buck	PVIN	12	1.8	0.5	ARD_X_VRX_A2_IC2
6	VMGTAVCC	6	C200	Sync Buck	PVIN	12	0.9	6	
7	VCC_HBM (VCC_HBM, VCC_IO_HBM)	7	C865	1-ph DrMOS Ctrl	PVIN	12	1.2	15	
8	VCCAUX_HBM	8	C200	Sync Buck	PVIN	12	2.5	0.6	
9	VCCO_HDIO	9	C200	Sync Buck	PVIN	12	3.3	3	ARD_X_VRX_A2_IC3
10	VCCO_HPIO	10	C200	Sync Buck	PVIN	12	1.8	3	
11	VCC_DDR	11	C200	Sync Buck	PVIN	12	1.2	4	
12	DDR_VTT (DDR_VTT, DDR_VREF)	12	C210	VTT Terminator	VCC_DDR	1.2	0.6	4	

Estimated total area estimated = 2034.38 mm^2

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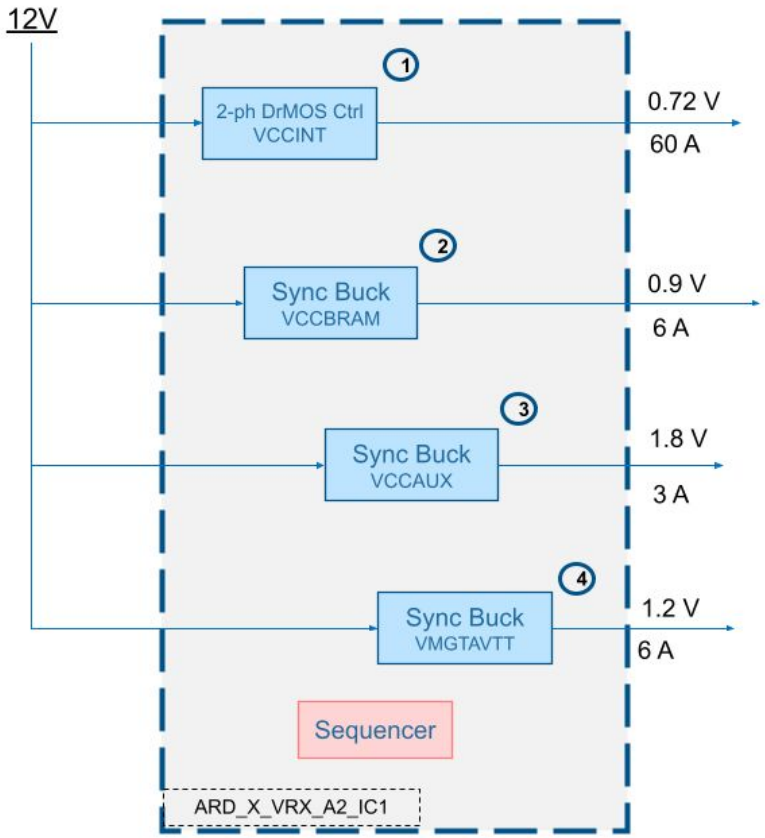
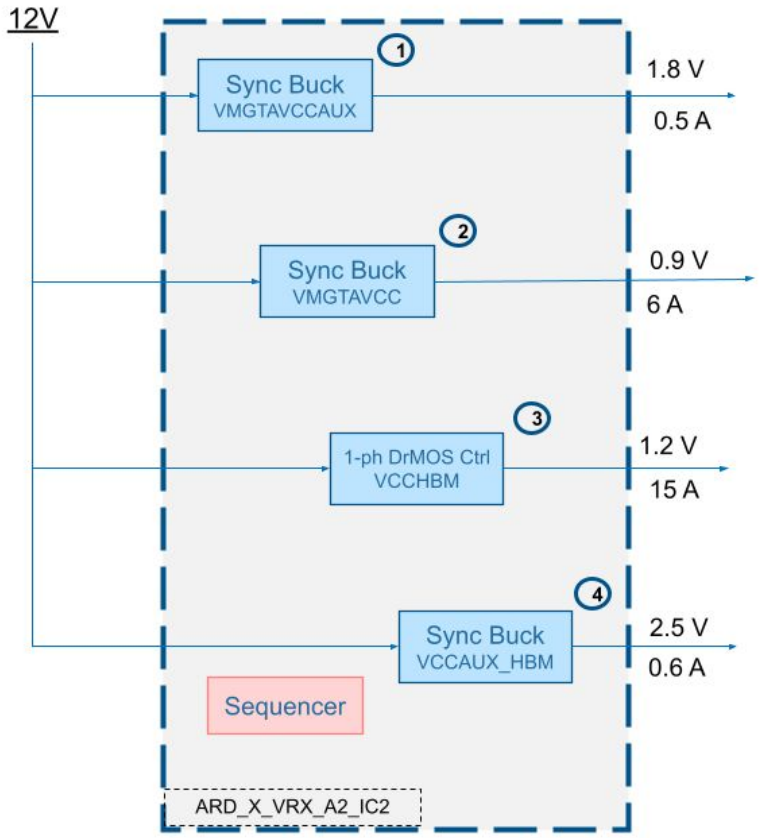
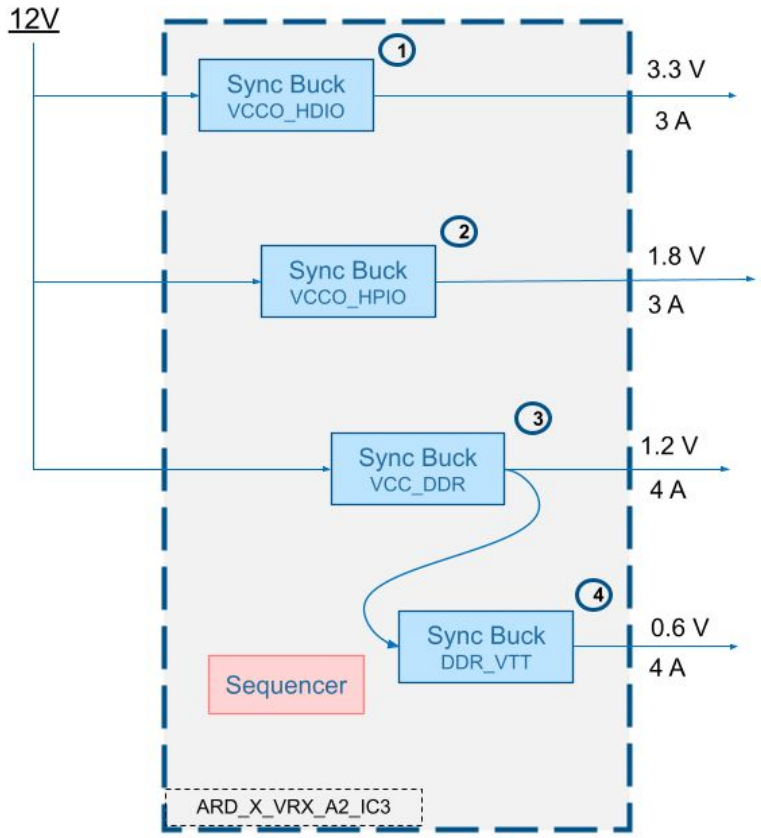
Power Tree Mapping- IC1, IC2, IC3



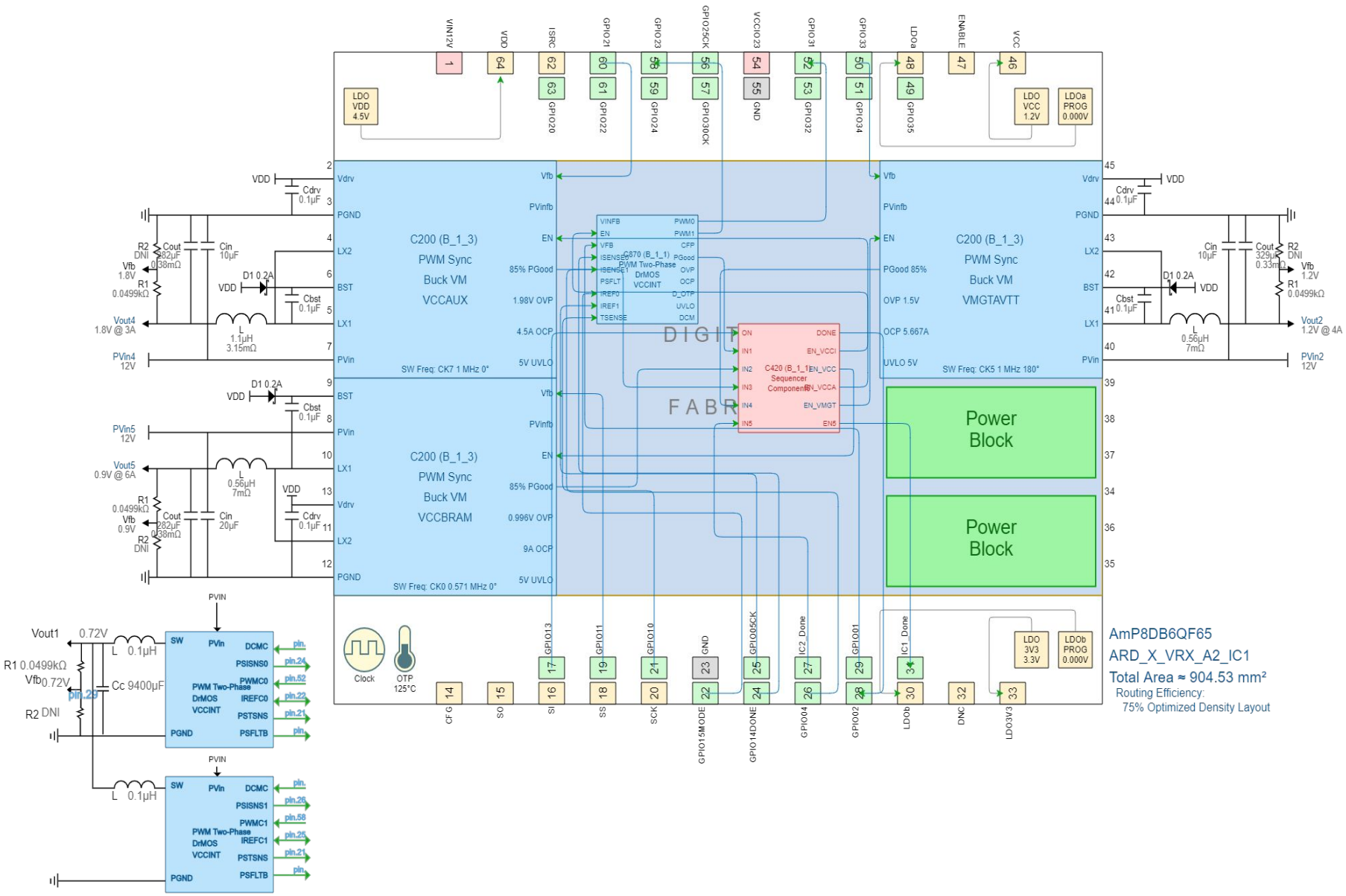




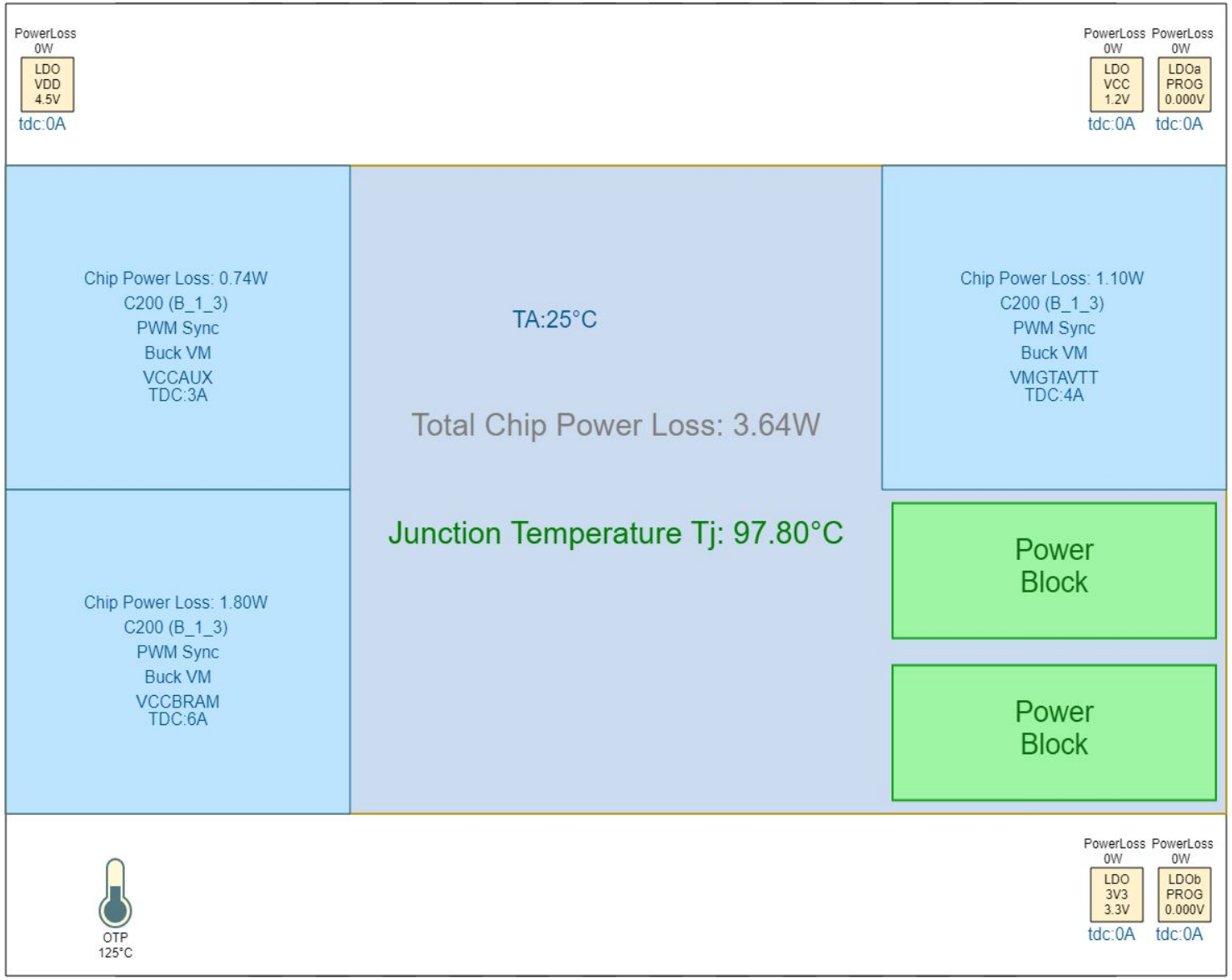
Estimated Total Area = 2034.38mm²

AnDAPT

Mapping (WebAmP View) –IC1

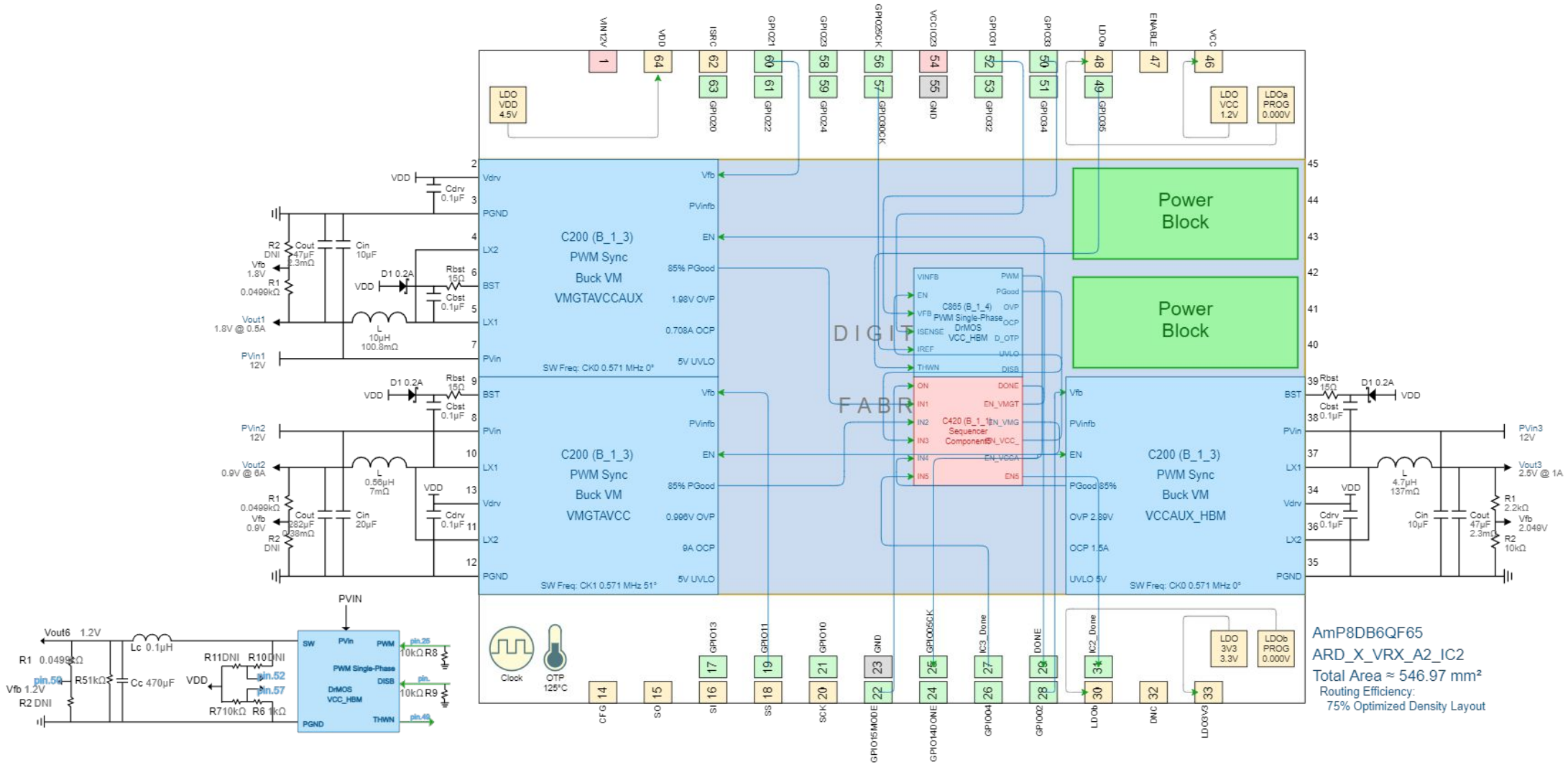


Mapping (Thermal View) –IC1

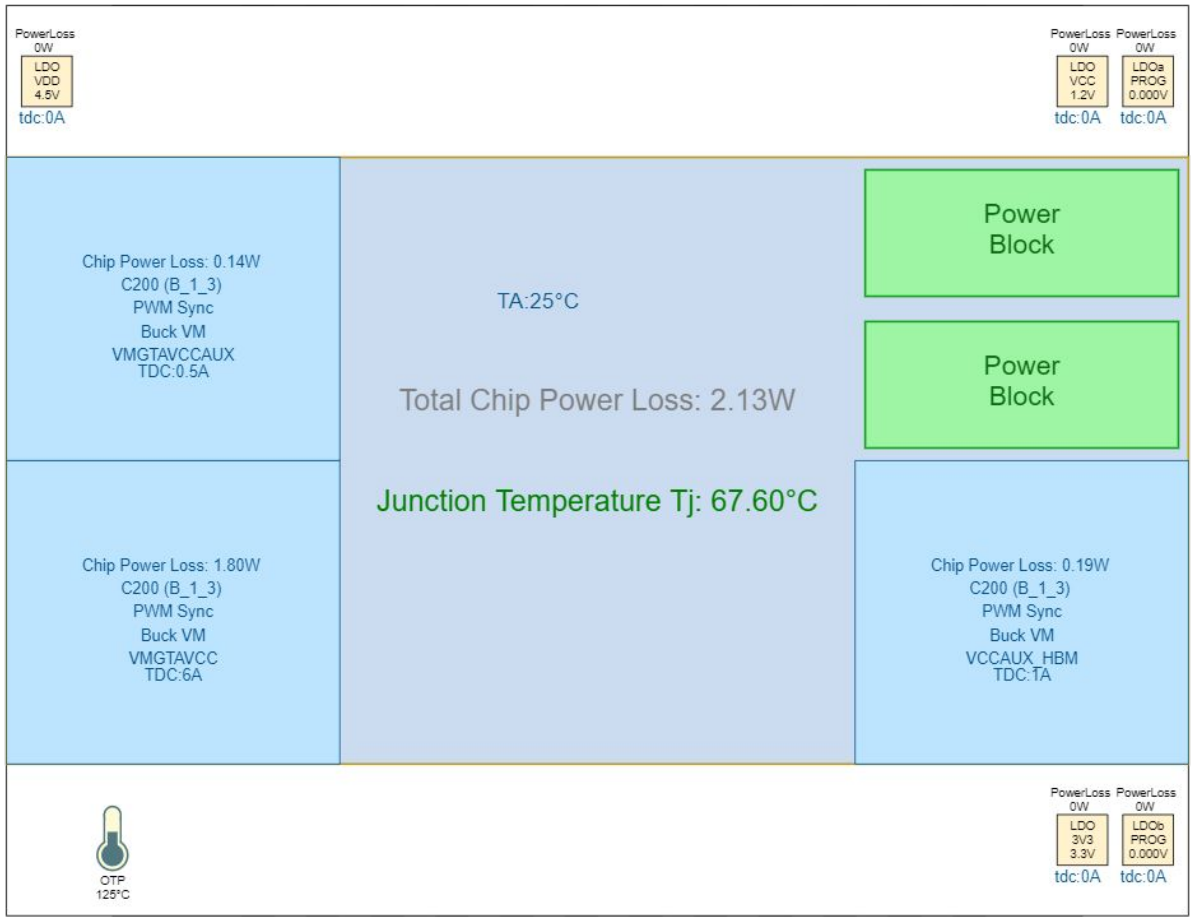


AmP8DB6QF65
ARD_X_VRX_A2_IC1
Total Area ≈ 904.53 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping (WebAmP View) –IC2



Mapping (Thermal View) –IC2



AmP8DB6QF65
ARD_X_VRX_A2_IC2
Total Area ≈ 546.97 mm²
Routing Efficiency:
75% Optimized Density Layout

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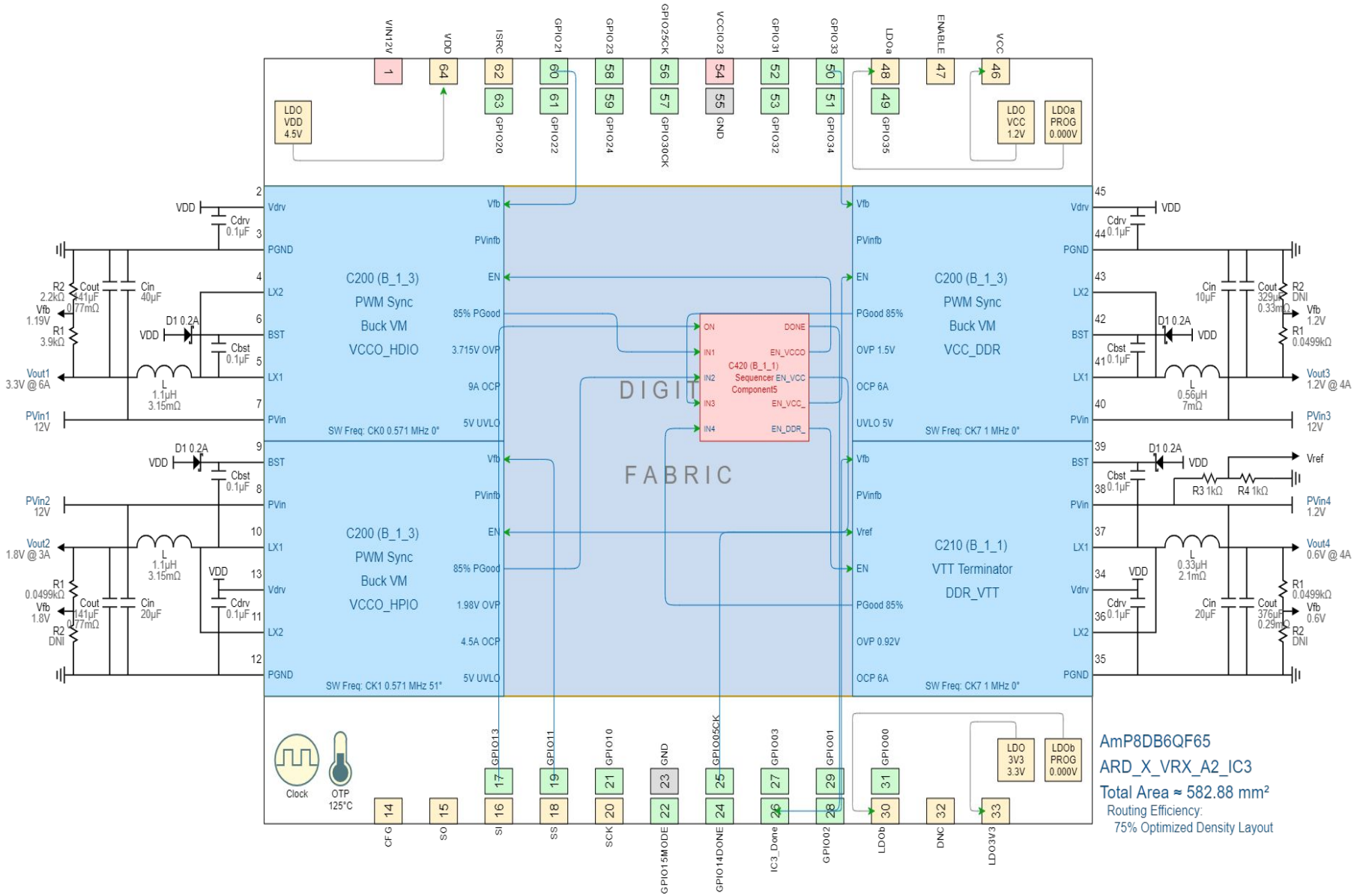
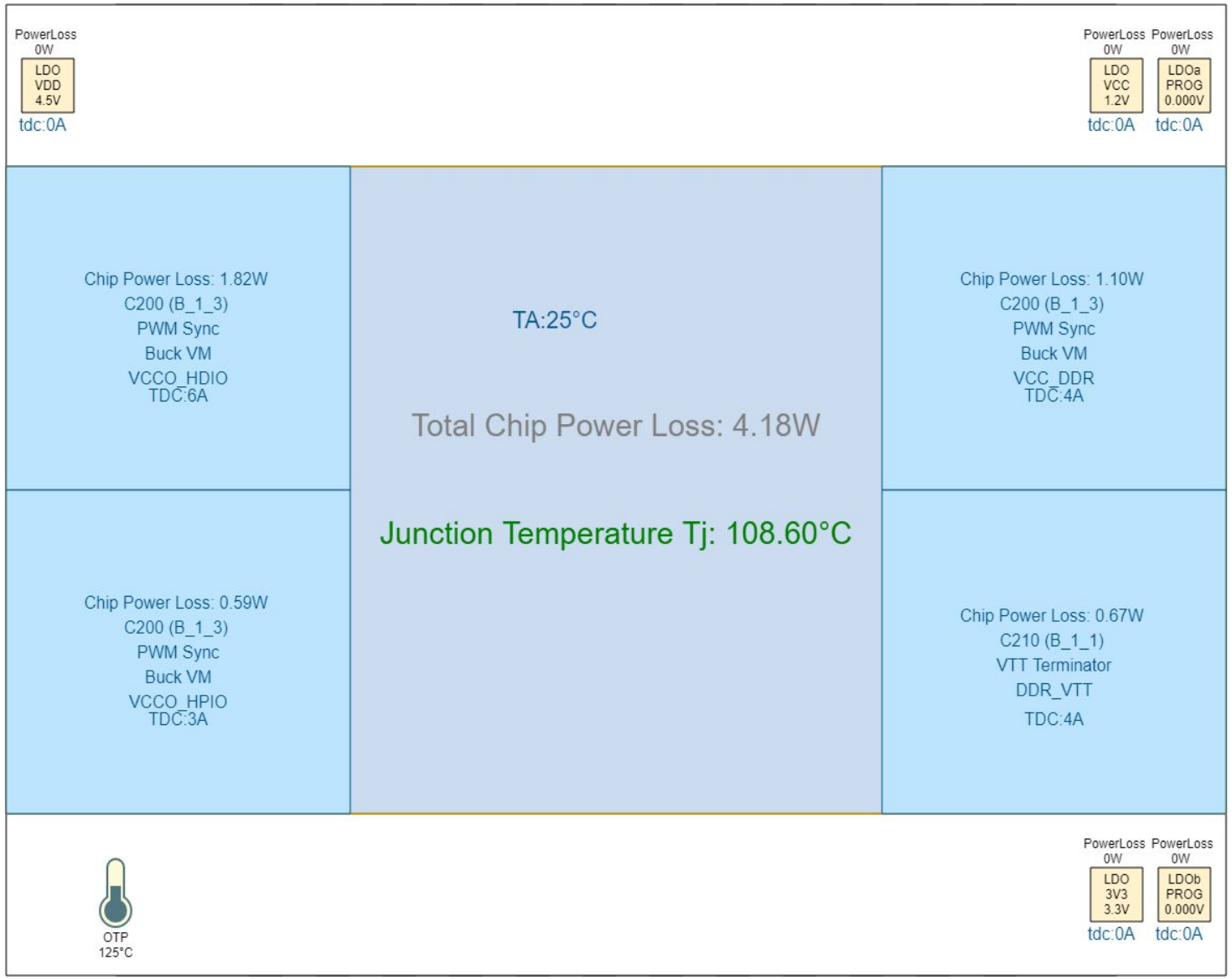
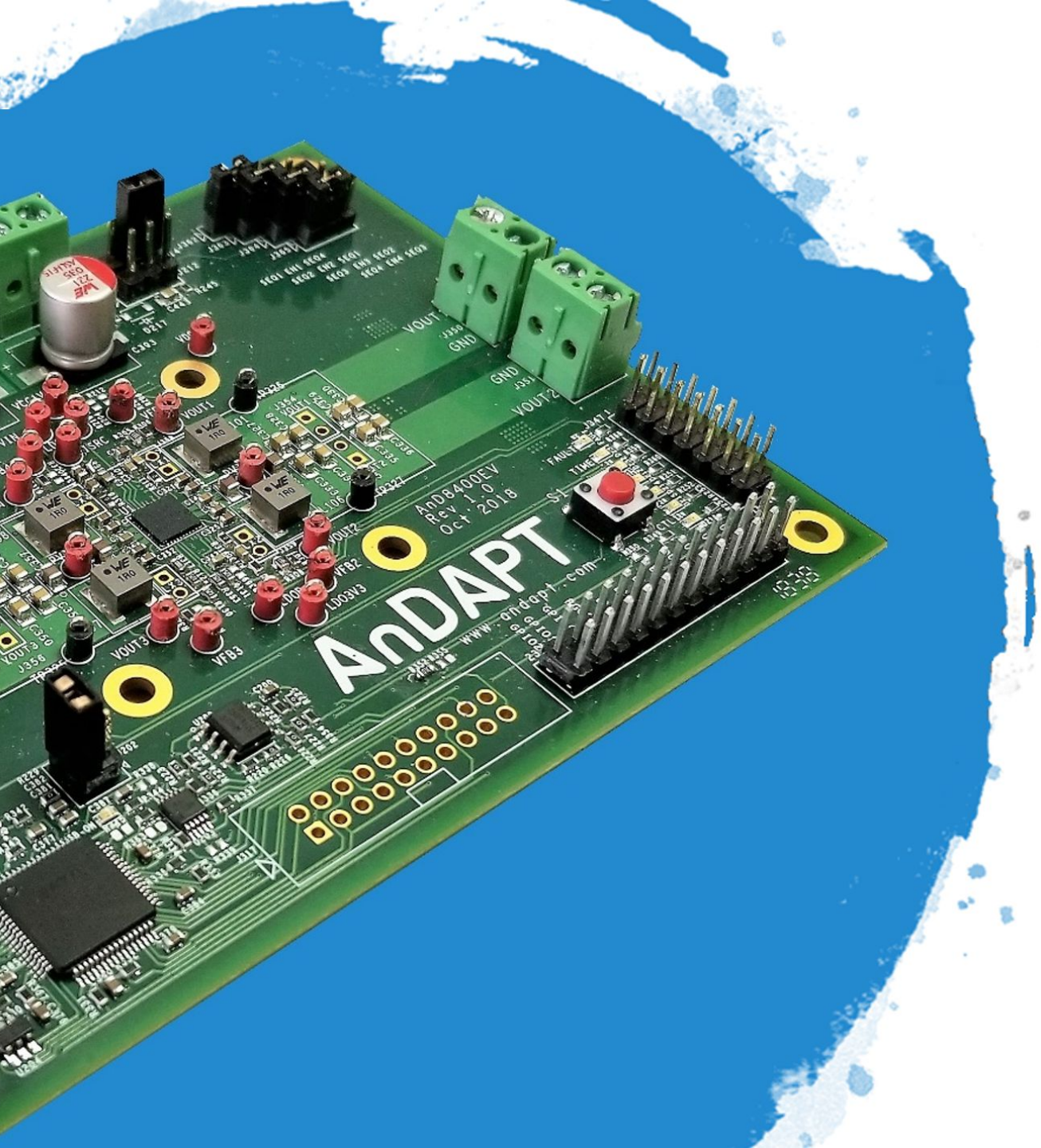
Mapping (WebAmP View) –IC3



Mapping (Thermal View) –IC3



AmP8DB6QF65
ARD_X_VRX_A2_IC3
Total Area ≈ 582.88 mm²
Routing Efficiency:
75% Optimized Density Layout



Test Data

Virtex UltraScale+ (Full Power Management)

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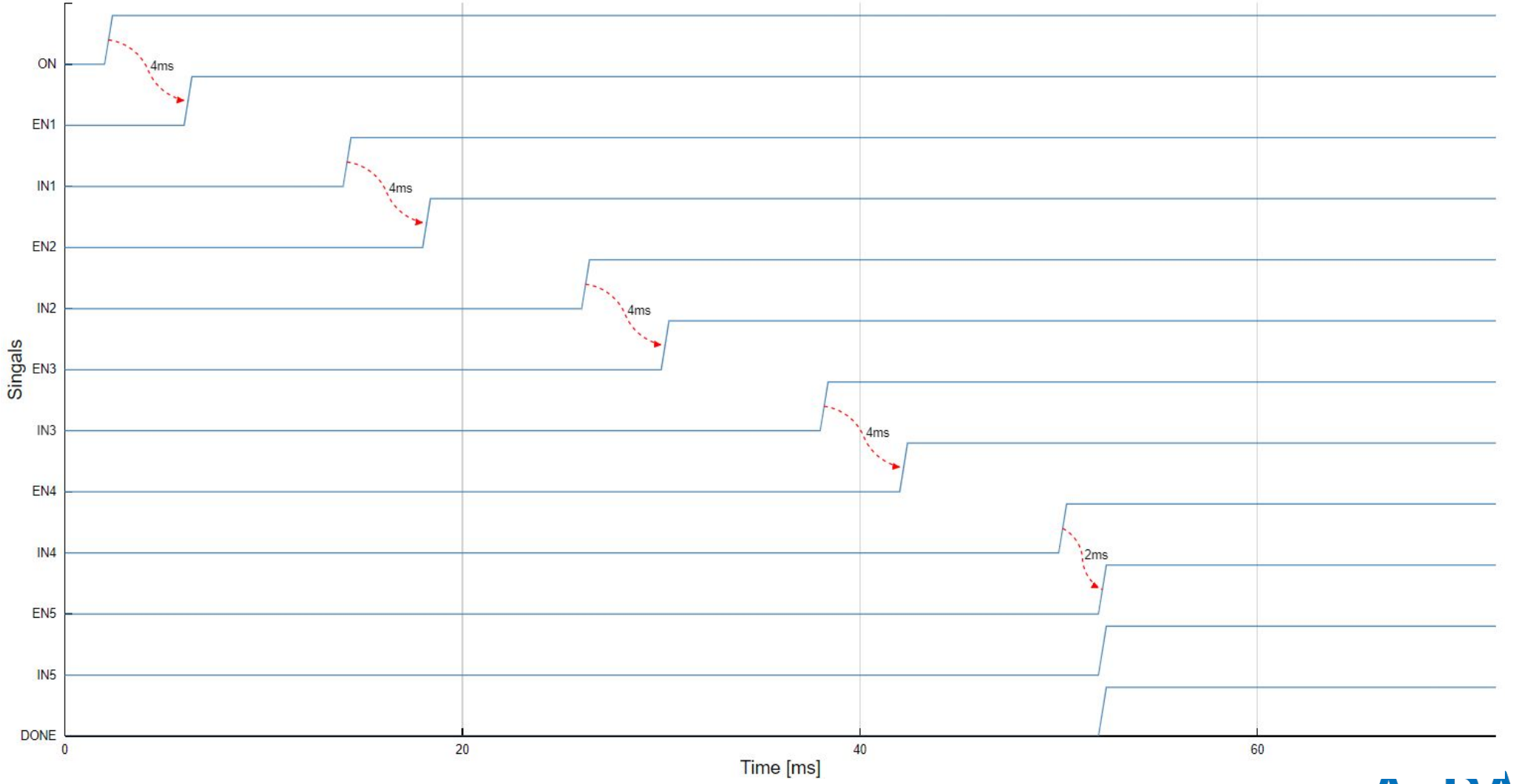
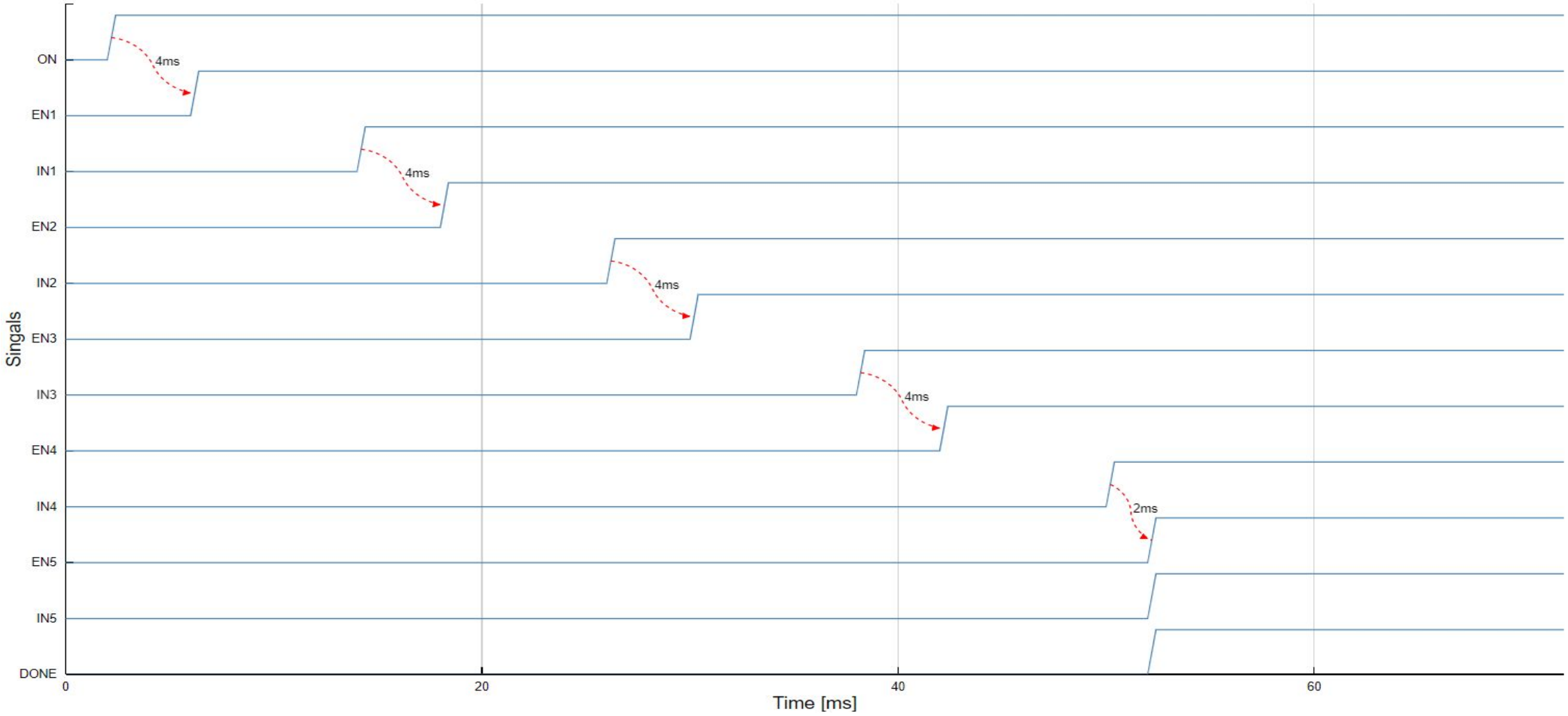
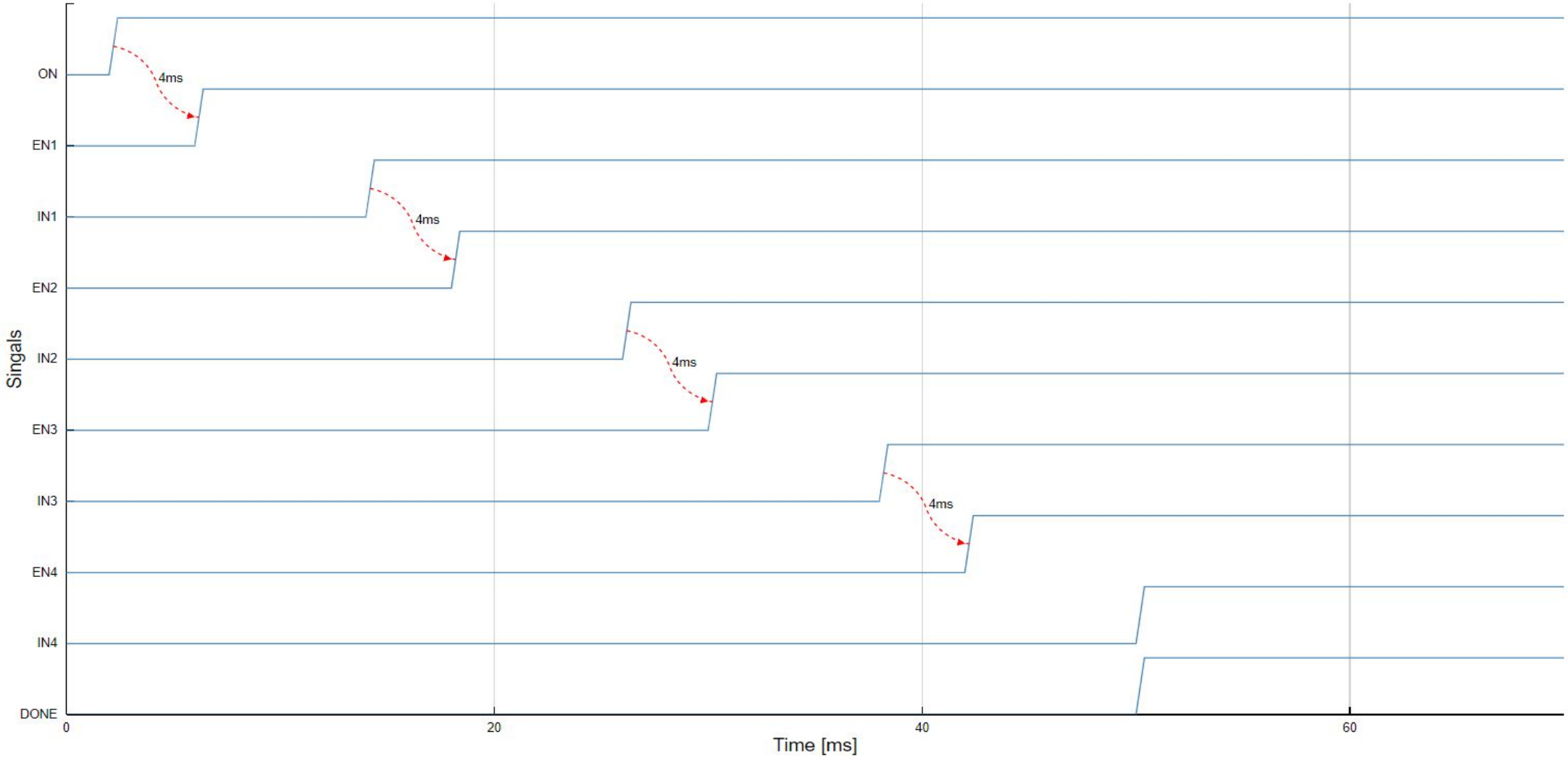
Integrated Sequencer Graphic IC1 (Turn ON)



Integrated Sequencer Graphic IC2 (Turn ON)



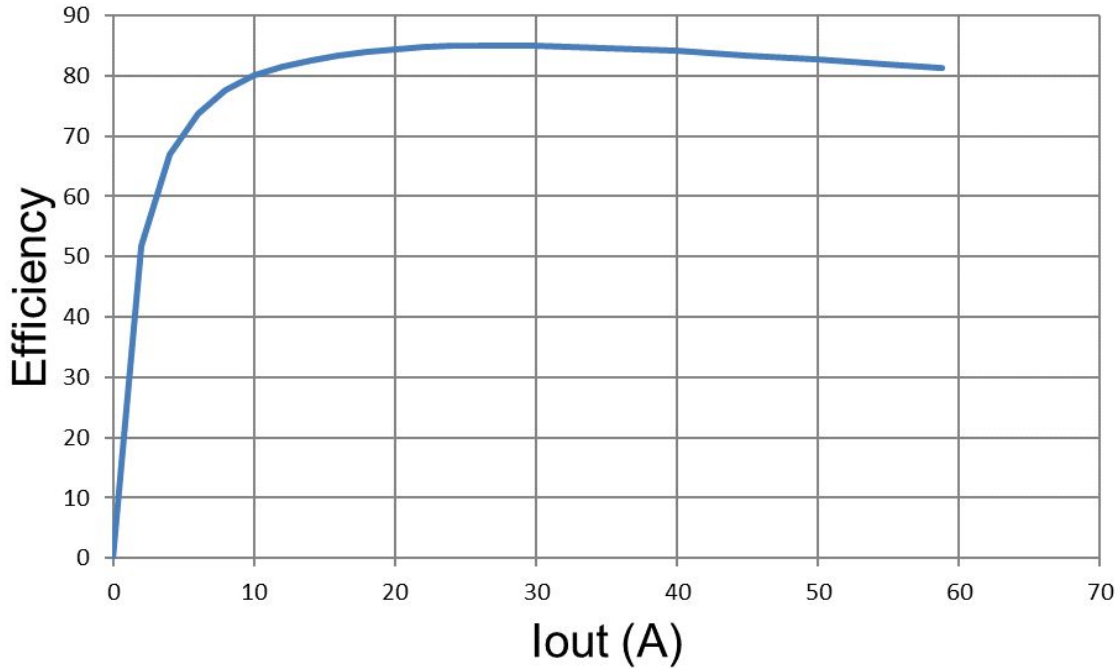
Integrated Sequencer Graphic IC3 (Turn ON)

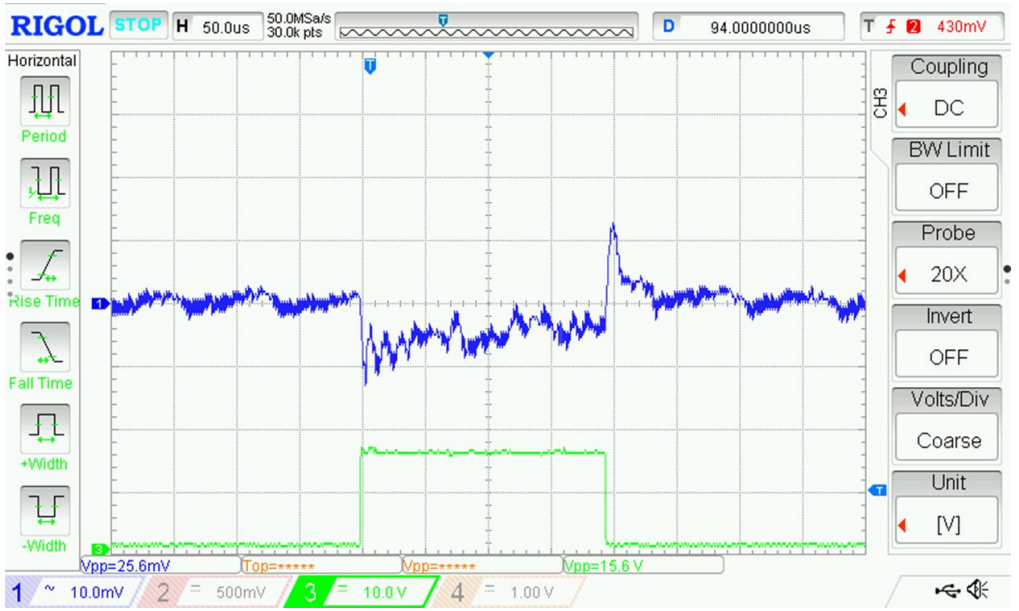


VCCINT
0.72 V / 60 A

- C870 2-ph DrMOS Ctrl
- Fsw = 1 MHz
- L = 0.1 µH, P/N Wurth 7443082010
- C = 9400 uF + 960 uF

Efficiency & Transient

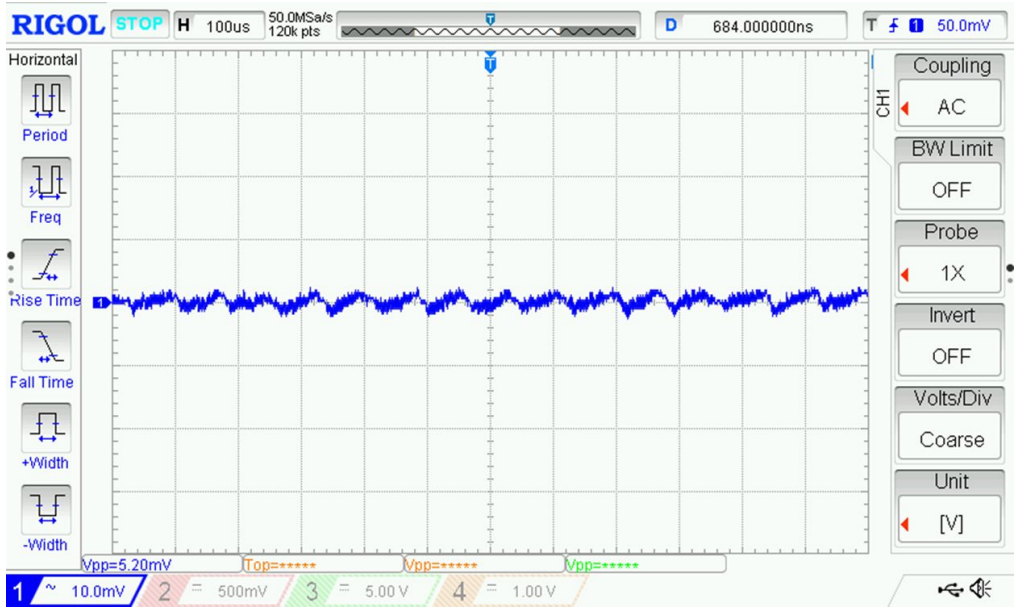




Vout = 0.72 V
Transient 45A – 60A @ 100 A/µs
V_{PP} = 25.6 mV
Fsw = 1 MHz
Lout = 0.1 µH, Cout = 20 x 220 µF

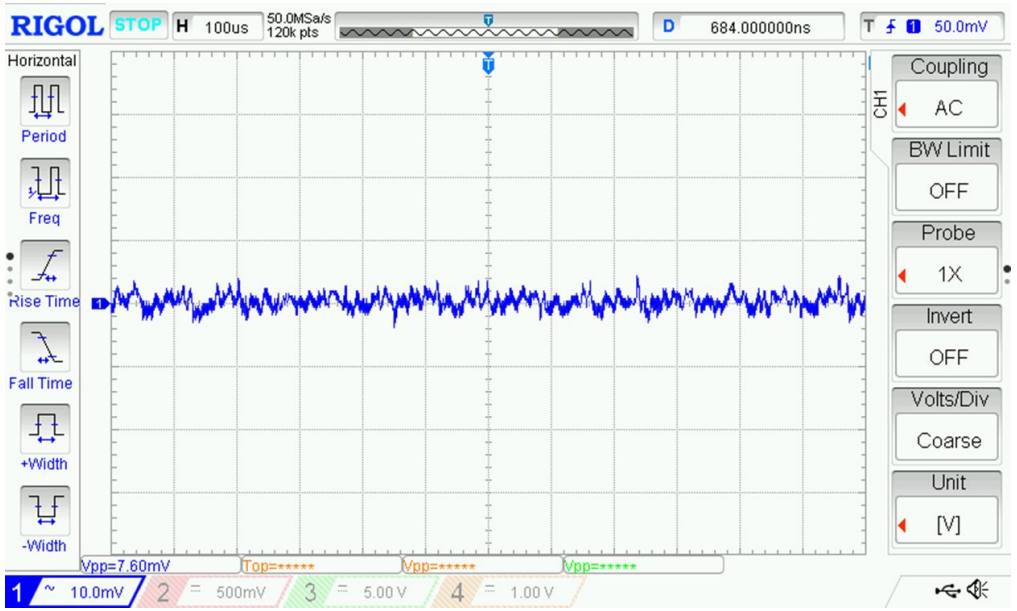
AnDAPT

Ripple



No Load
V_{PP} = 5.2 mV

Vout = 0.72 V



60 A Load
V_{PP} = 7.6 mV

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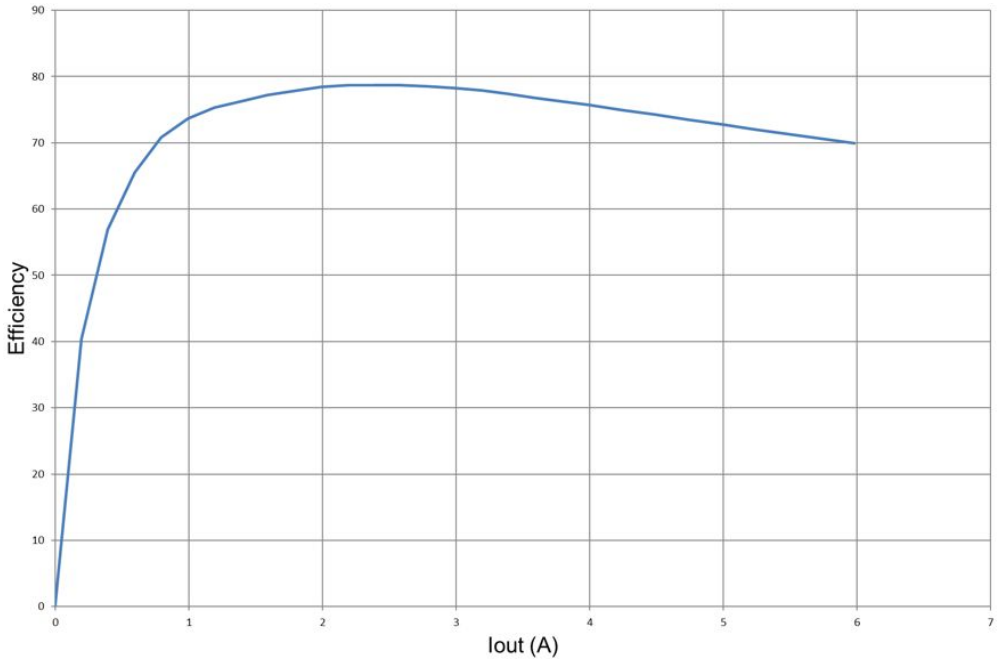
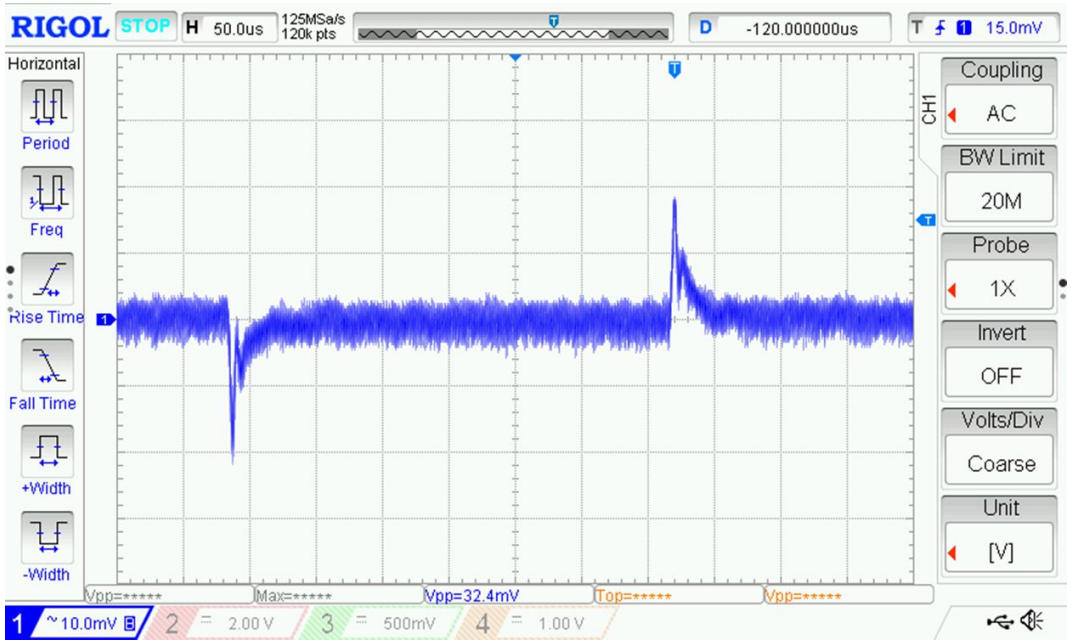
VCCBRAM (VCCINT_IO, VCCBRAM) 0.9 V / 6 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 6x47 uF

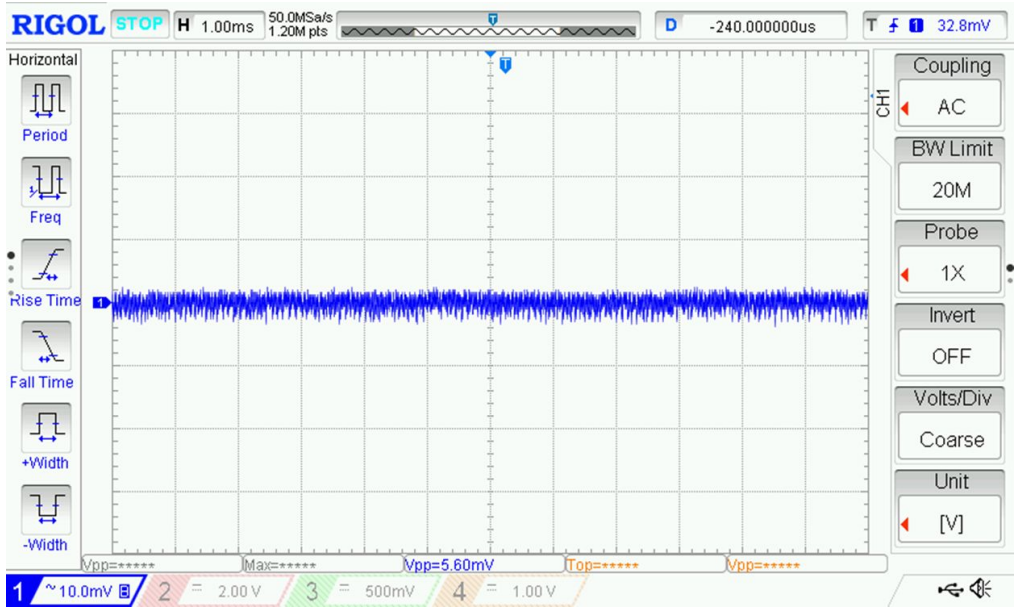
Efficiency & Transient





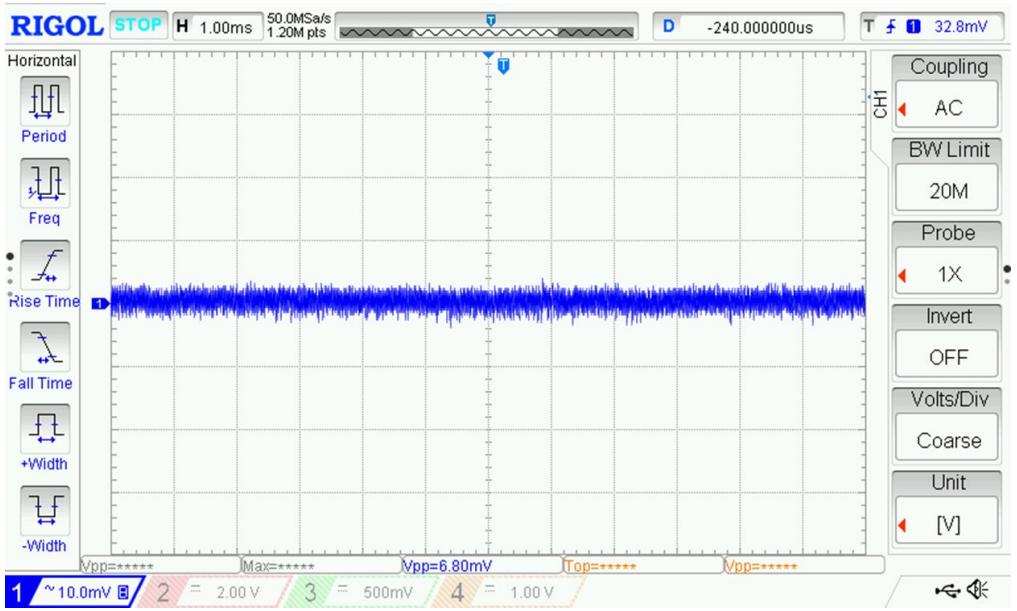
Vout = 0.9V
Transient 4.5 A – 6 A @ 10 A/µs
V_{PP} = 32.4 mV
Fsw = 571 kHz
Lout = 0.56 µH, Cout = 6 x 47 µF

Ripple



No Load
V_{PP} = 5.6 mV

Vout = 0.9 V



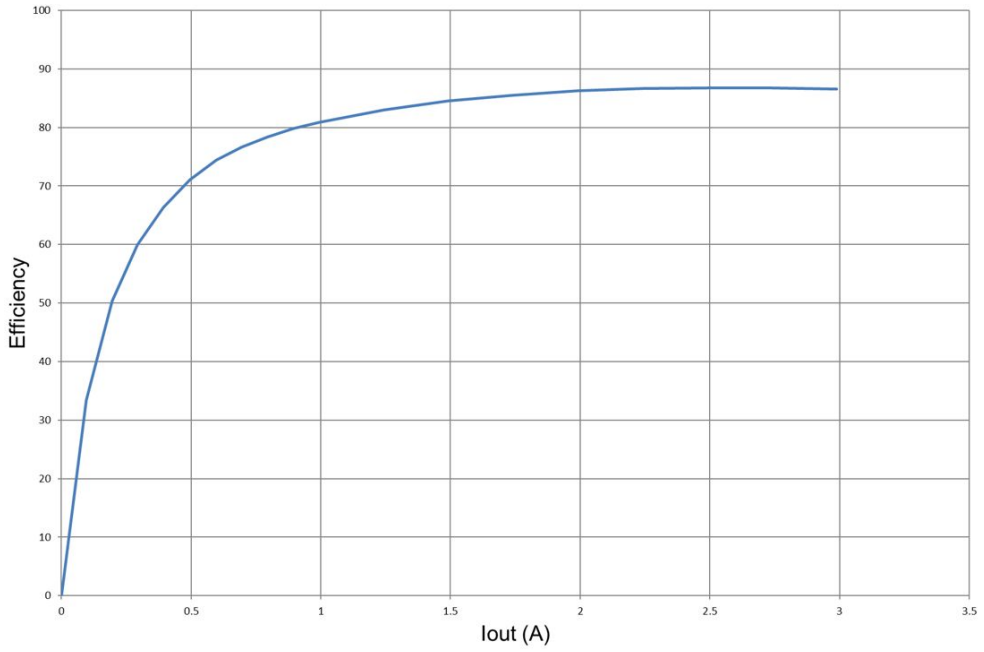
6 A Load
V_{PP} = 6.8 mV

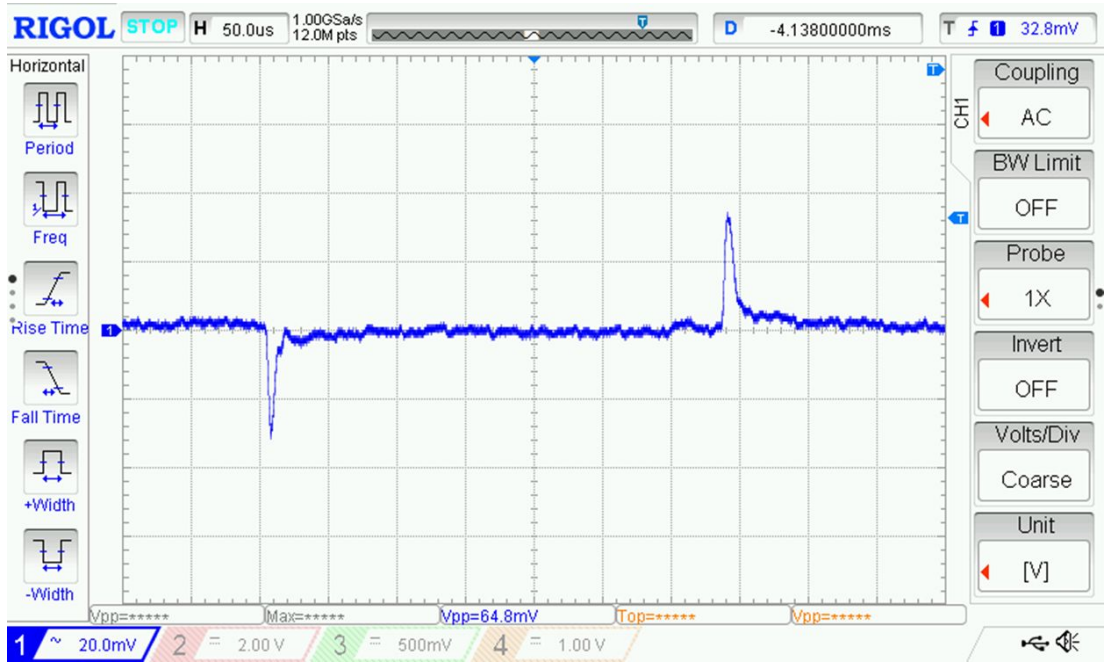
AnDAPT

VCCAUX (VCCAUX, VCCAUX_IO, VCCADC)
1.8 V / 3 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 6x47 uF

Efficiency & Transient

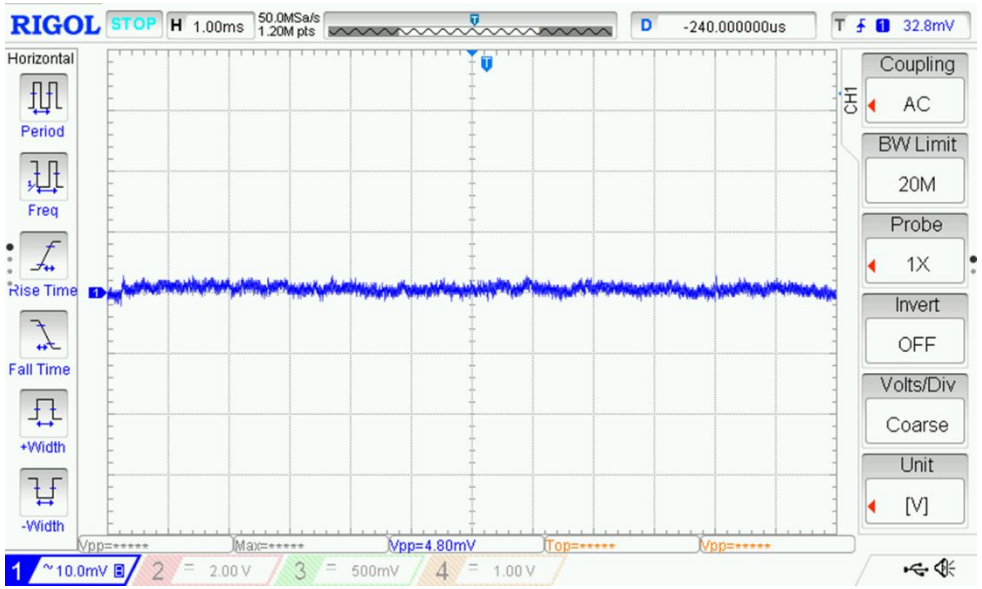




Vout = 1.8 V
Transient 0.3 A – 3 A @ 10 A/µs
V_{PP} = 64.8 mV
Fsw = 1 MHz
Lout = 1.1 µH, Cout = 6 x 47 µF

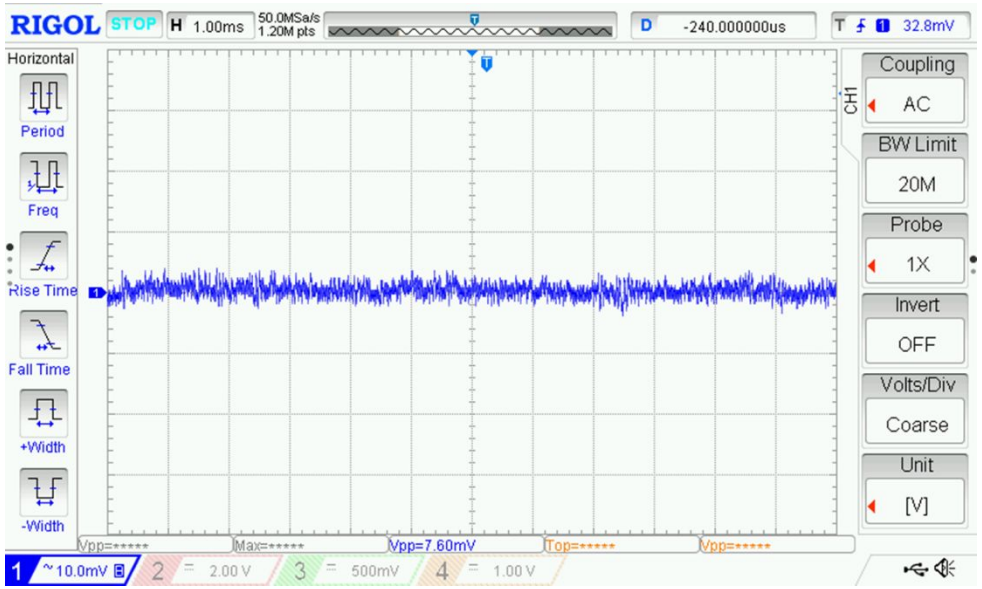
AnDAPT

Ripple



No Load
V_{PP} = 4.8 mV

Vout = 1.8 V



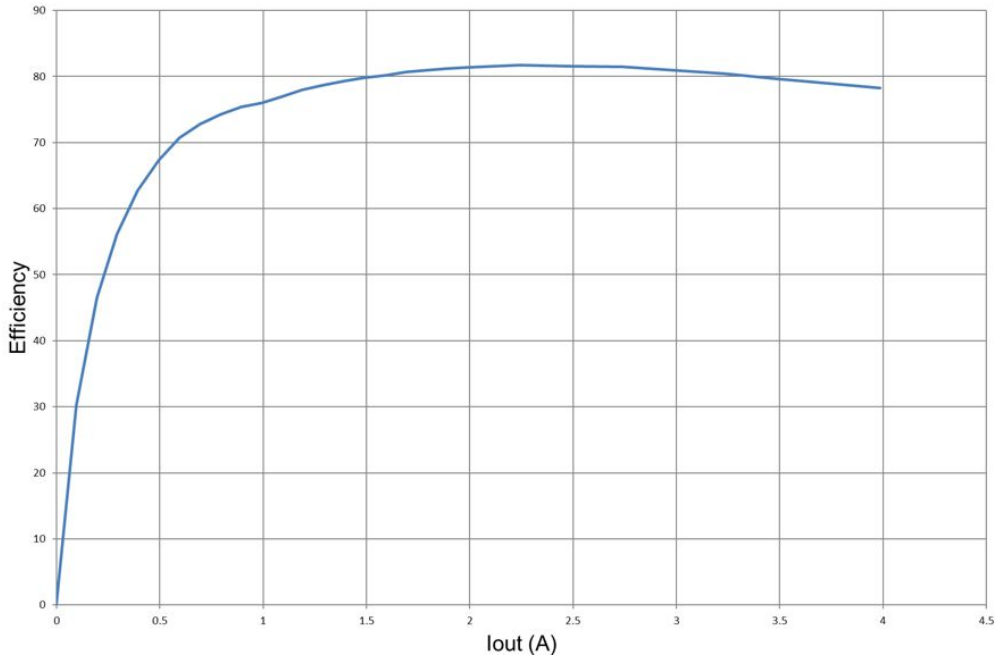
3 A Load
V_{PP} = 7.6 mV

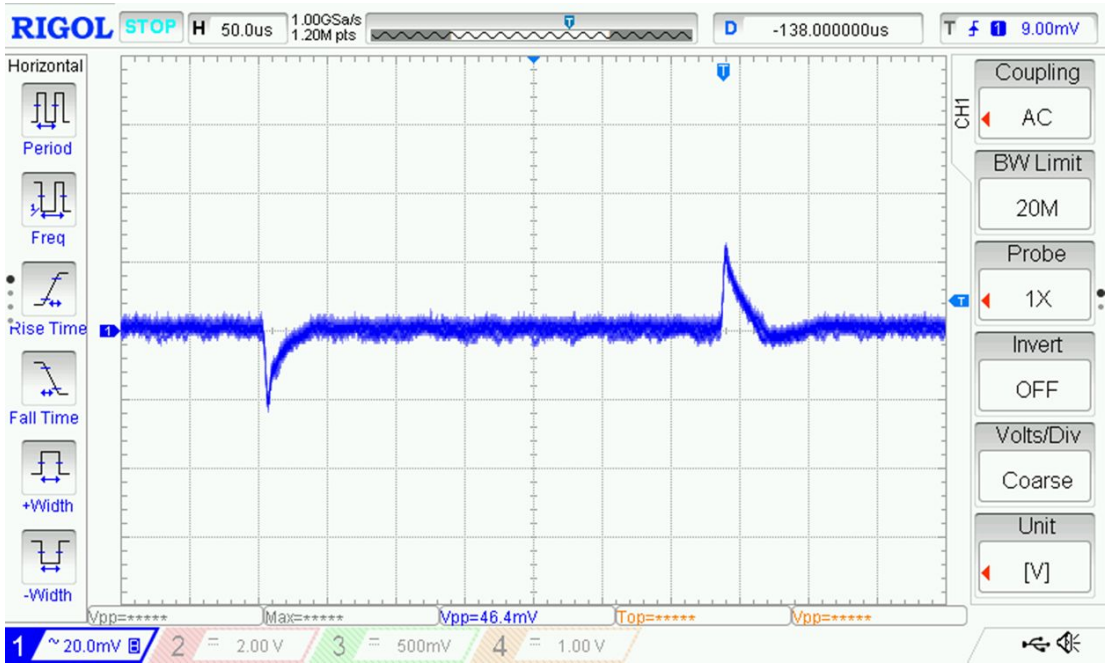
AnDAPT

VMGTAVTT
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

Efficiency & Transient

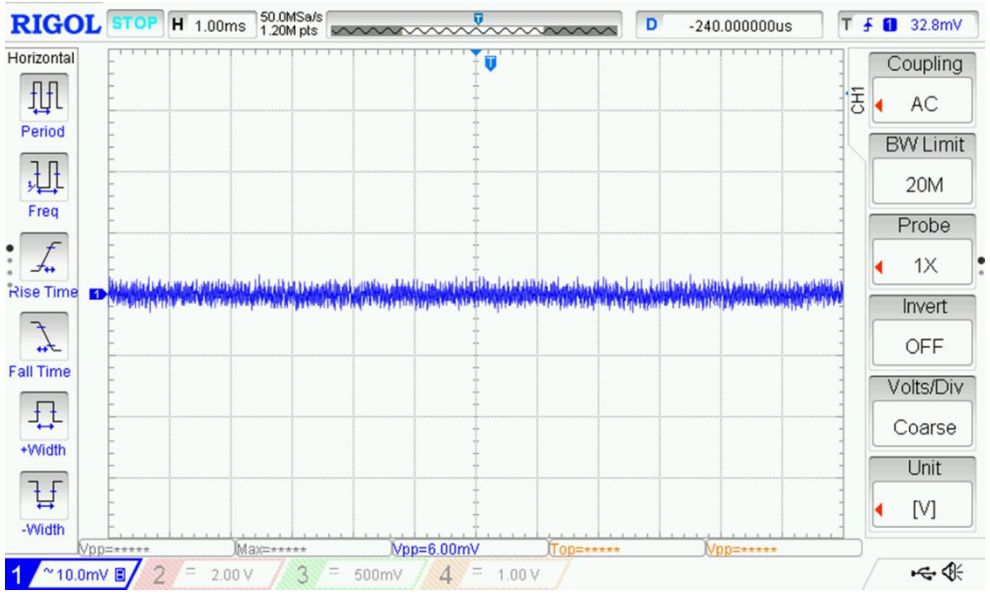




Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

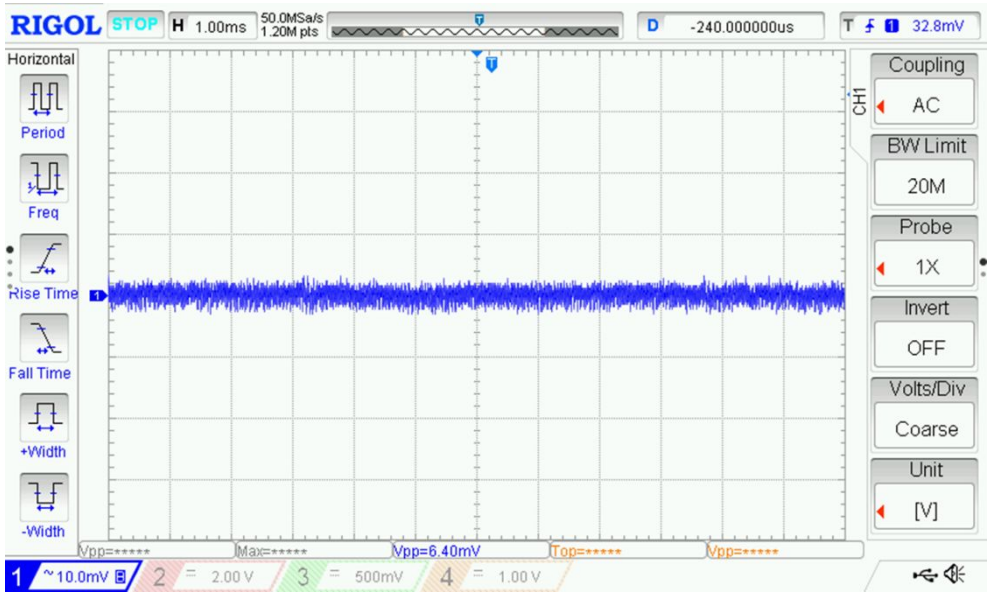
AnDAPT

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



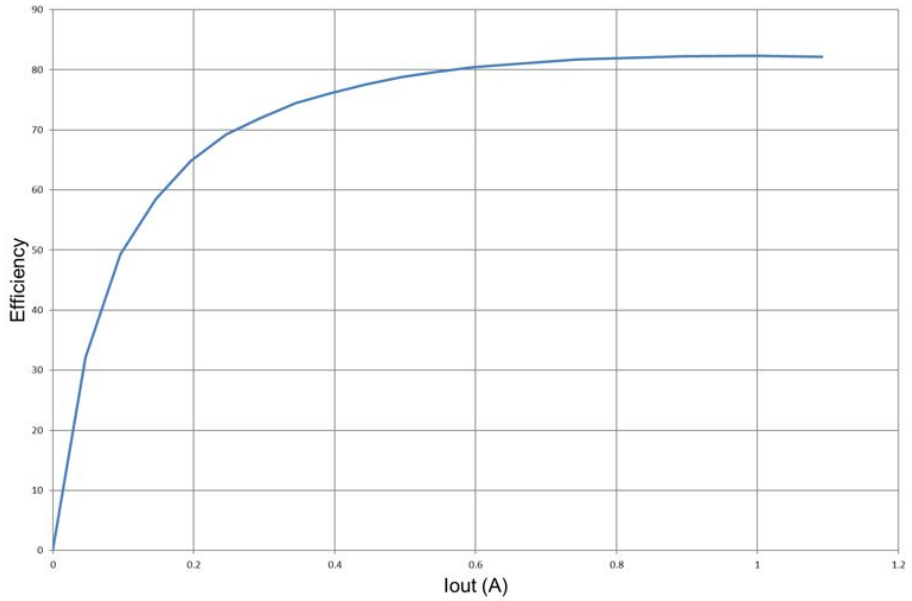
0.035 A Load
V_{PP} = 6.4 mV

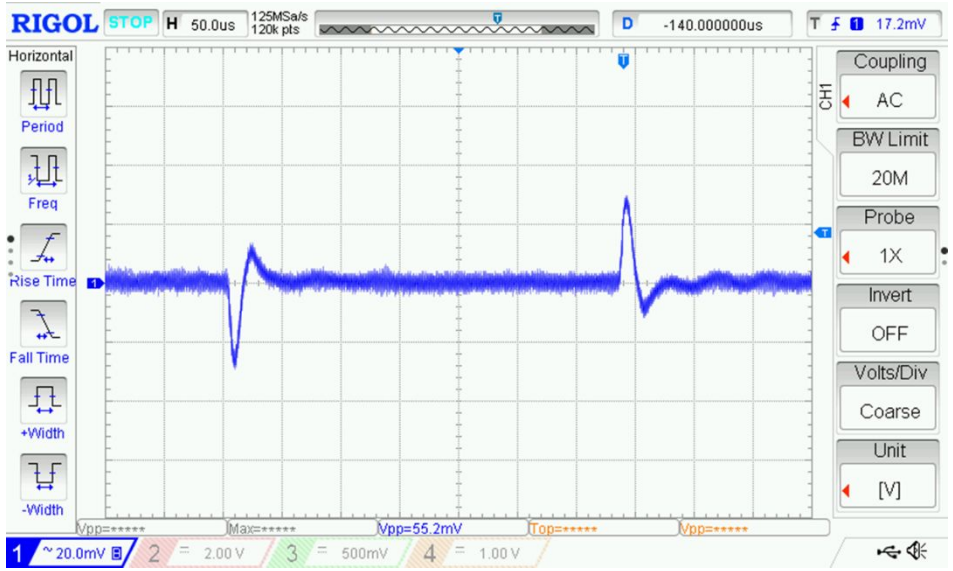
AnDAPT

VMGTAVCCAUX
1.8 V / 0.5 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74438357100
- C = 1x47 uF

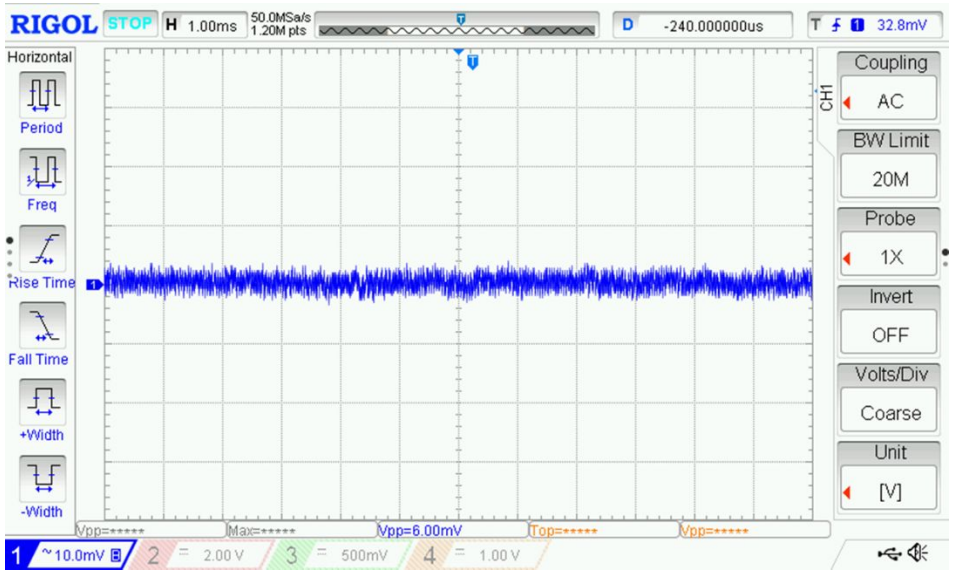
Efficiency & Transient

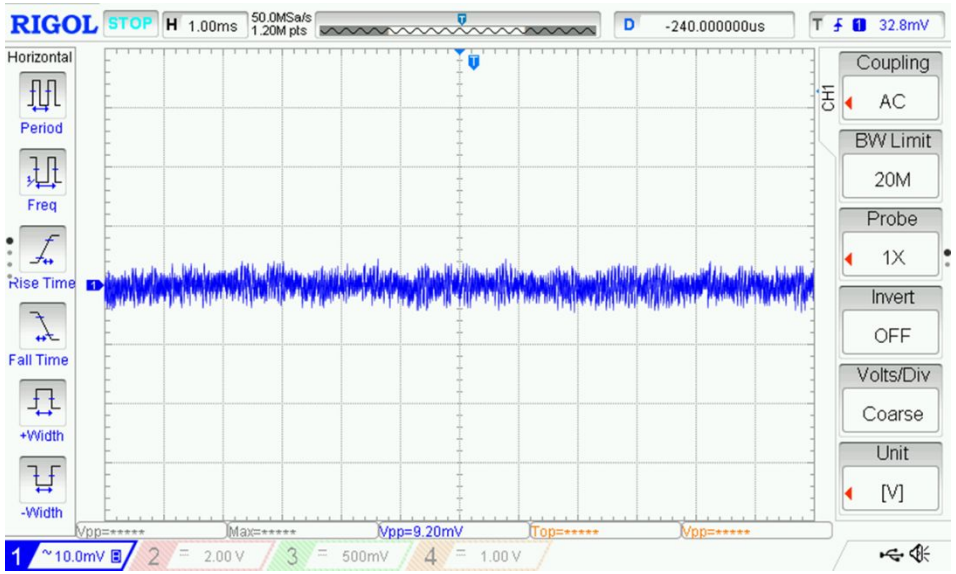




Vout = 1.8 V
Transient 0.75 A – 1 A @ 10 A/µs
V_{PP} = 55.2 mV
Fsw = 571 kHz
Lout = 4.7 µH, Cout = 1 x 47 µF

Ripple





No Load
V_{PP} = 6 mV

Vout = 1.8 V

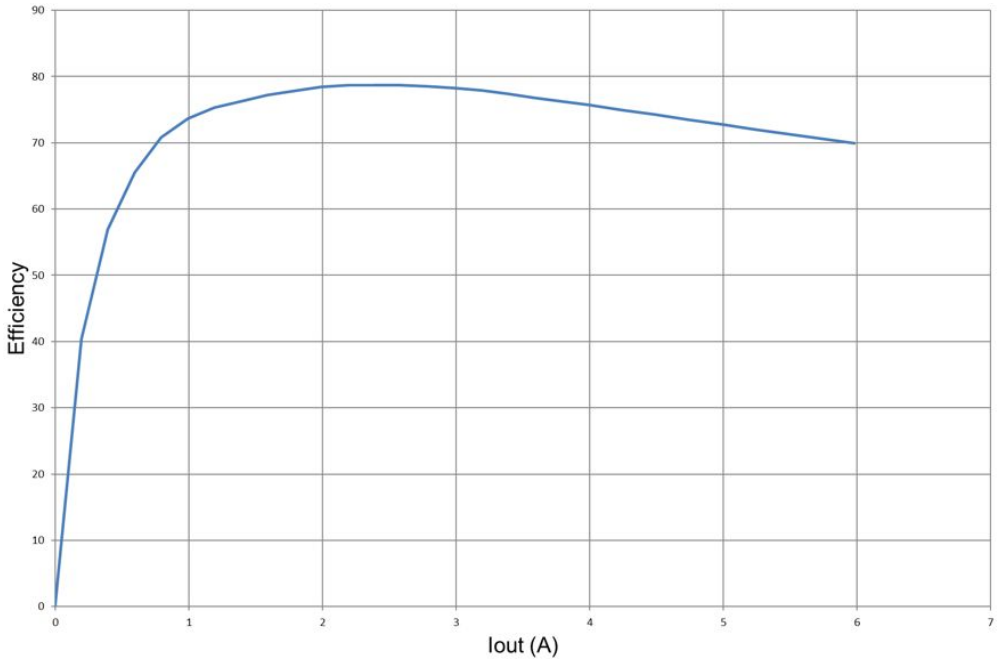
0.5 A Load
V_{PP} = 9.2 mV

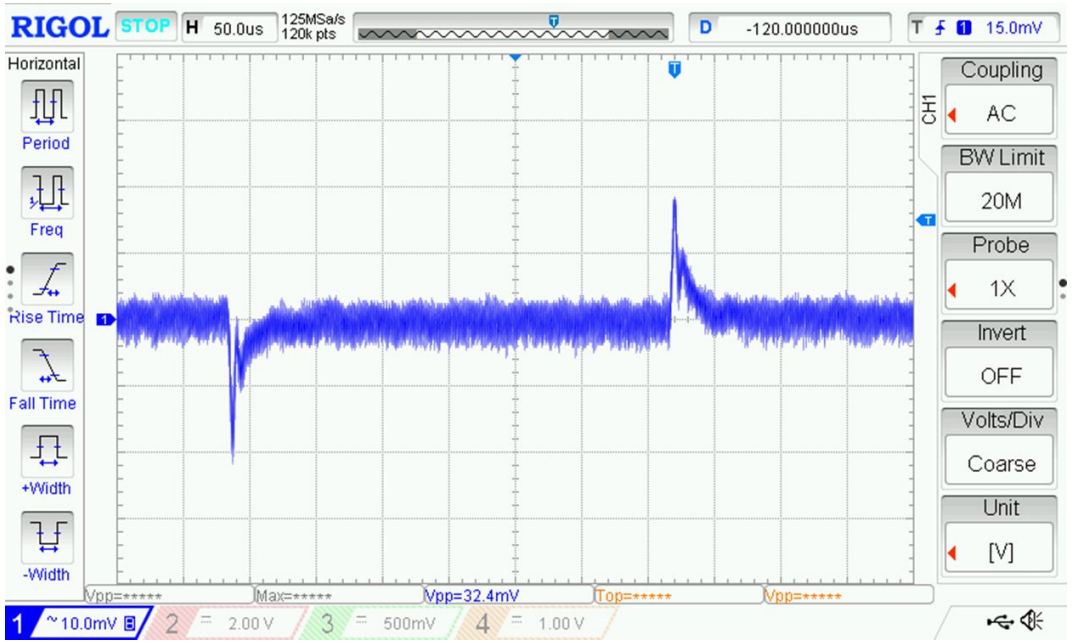
AnDAPT

VMGTAVCC
0.9 V / 6 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 6x47 uF

Efficiency & Transient

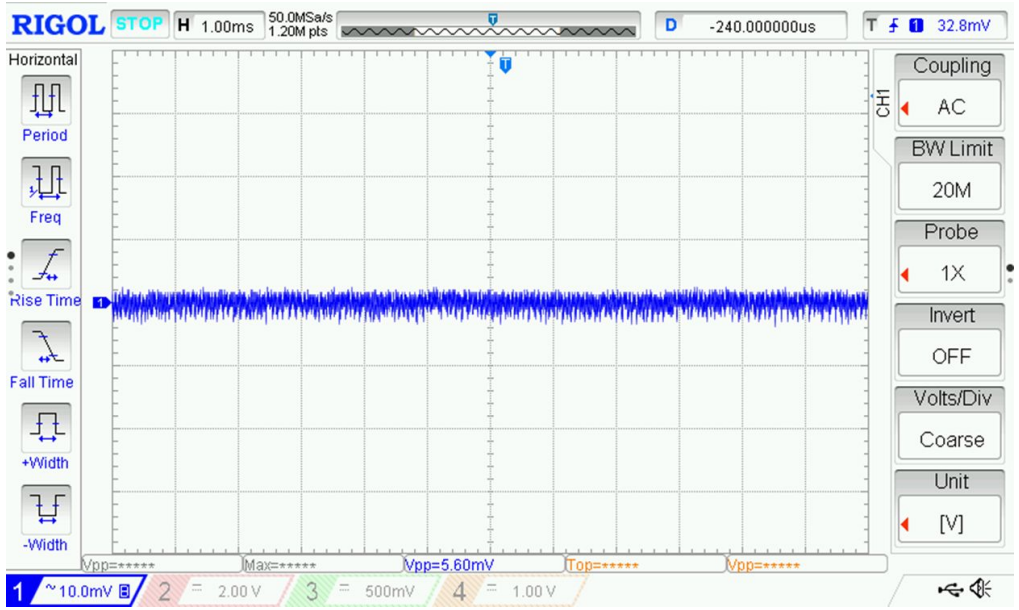


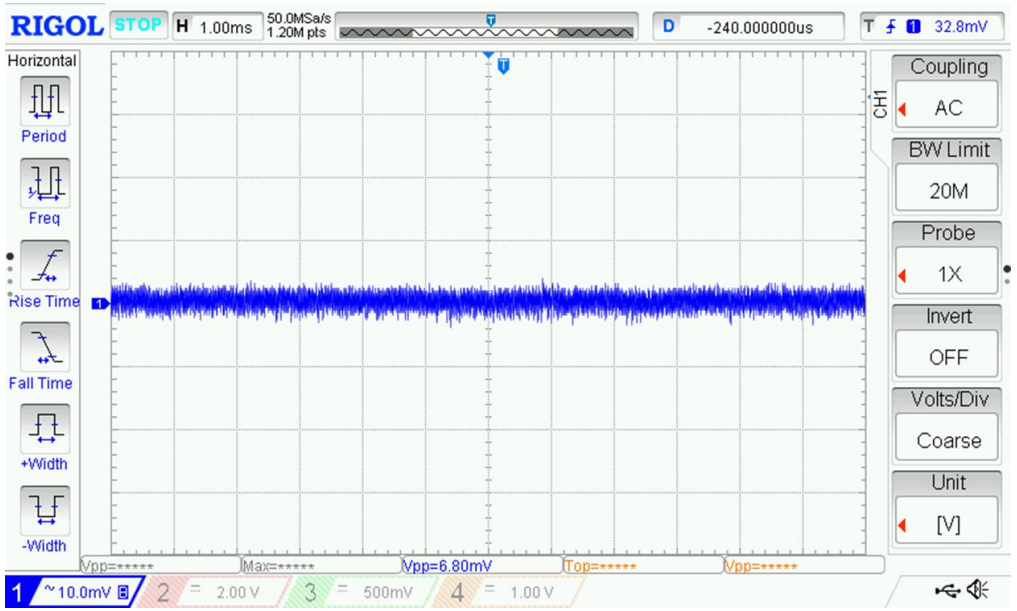


Vout = 0.9V
Transient 4.5 A – 6 A @ 10 A/µs
V_{PP} = 32.4 mV
Fsw = 571 kHz
Lout = 0.56 µH, Cout = 6 x 47 µF

AnDAPT

Ripple





No Load
V_{PP} = 5.6 mV

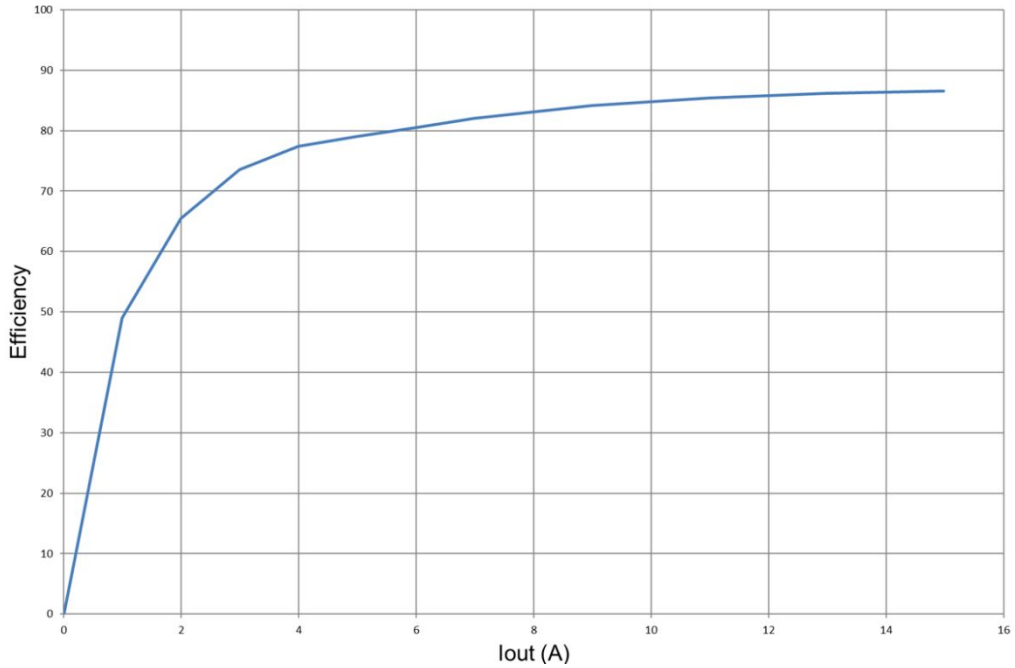
Vout = 0.9 V

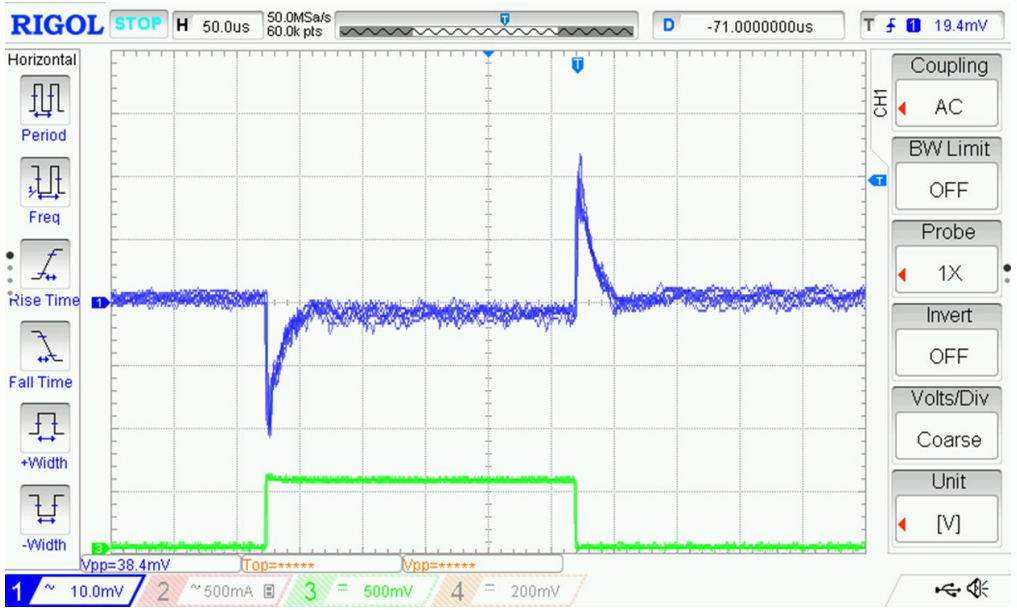
6 A Load
V_{PP} = 6.8 mV

VCC_HBM (VCC_HBM, VCC_IO_HBM) 1.2 V / 15 A

- C865 1-ph DrMOS Ctrl
- Fsw = 1 MHz
- L = 0.1 µH, P/N Wurth 7443082010
- C = 10x47 uF+4x220 uF

Efficiency & Transient

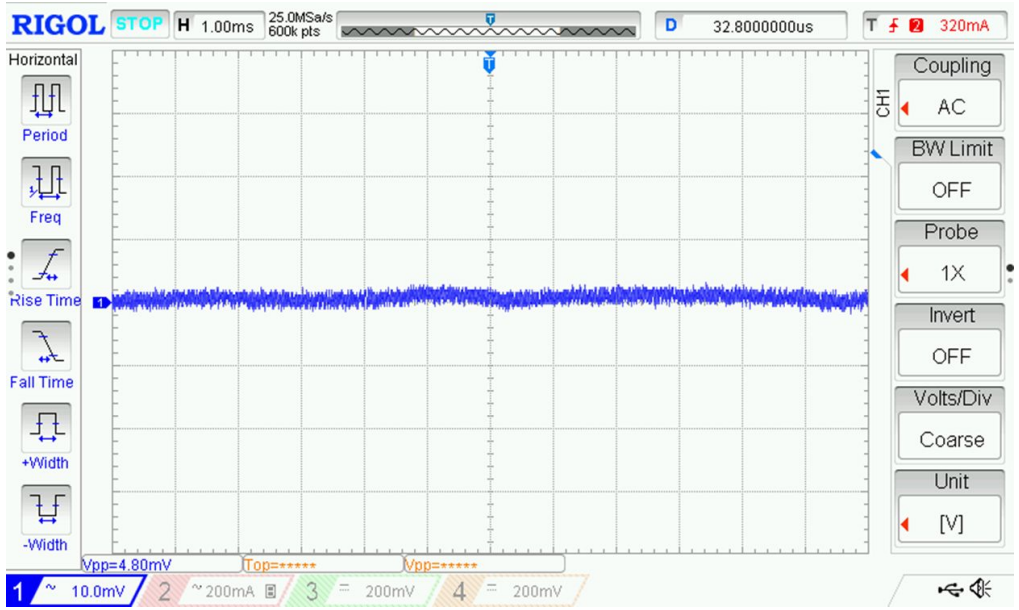




Vout = 1.2 V
Transient 3A – 15A @ 10 A/µs
V_{PP} = 38.4 mV
Fsw = 1 MHz
Lout = 0.1 µH, Cout = (10+4) x 47 µF

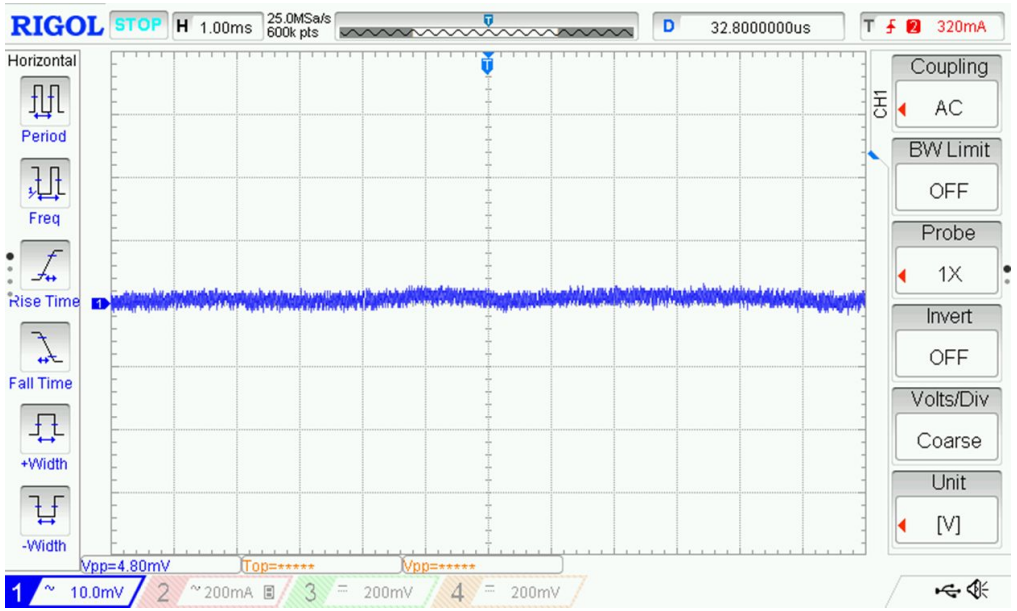
AnDAPT

Ripple



No Load
V_{PP} = 4.8 mV

Vout = 1.2 V



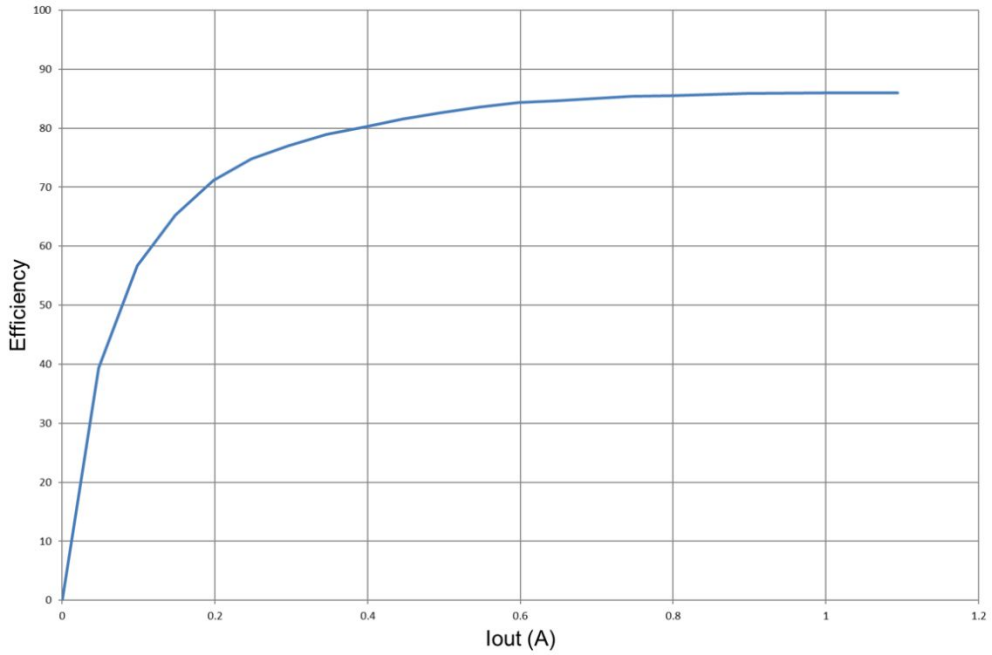
15 A Load
V_{PP} = 5.2 mV

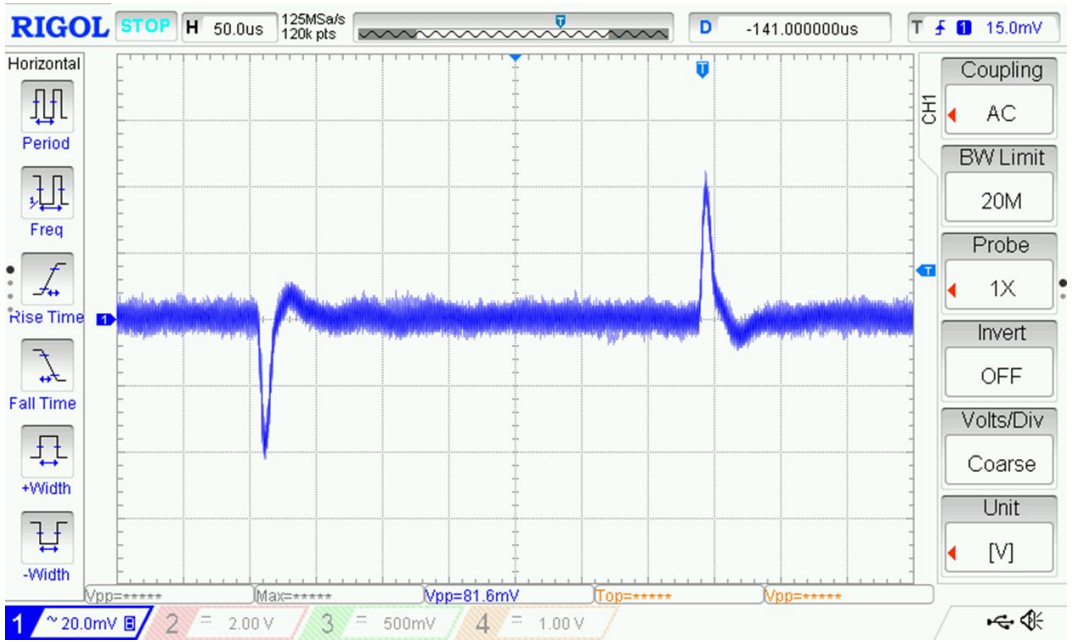
AnDAPT

VCCAUX_HBM
2.5 V / 1 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 4.7 µH, P/N Wurth 74438336047
- C = 1x47 uF

Efficiency & Transient

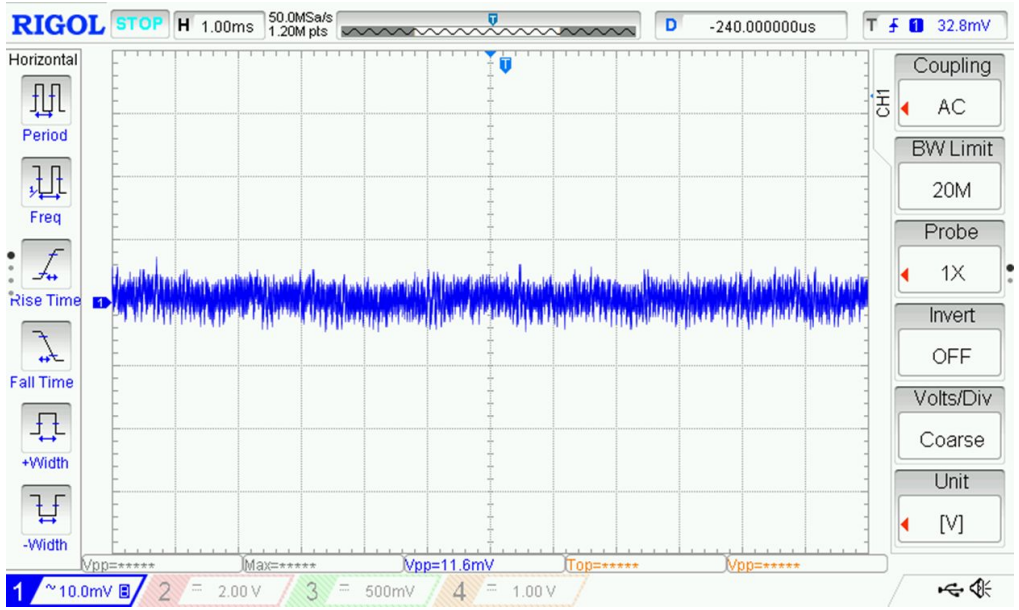




Vout = 2.5 V
Transient 0.2 A – 1 A @ 10 A/µs
V_{PP} = 81.6 mV
Fsw = 571 kHz
Lout = 4.7 µH, Cout = 1 x 47 µF

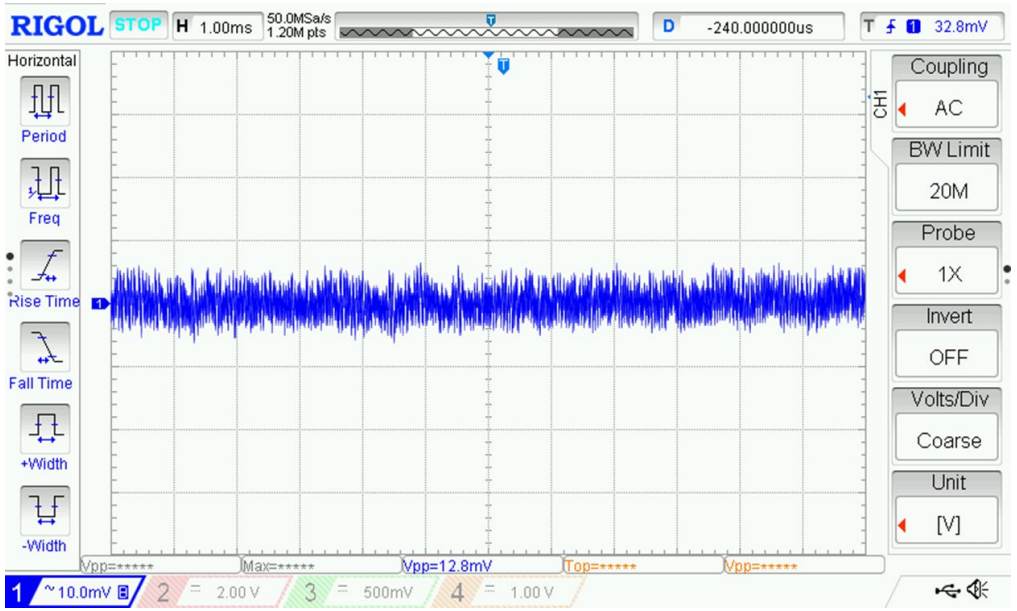
AnDAPT

Ripple



No Load
V_{PP} = 11.6 mV

Vout = 2.5 V



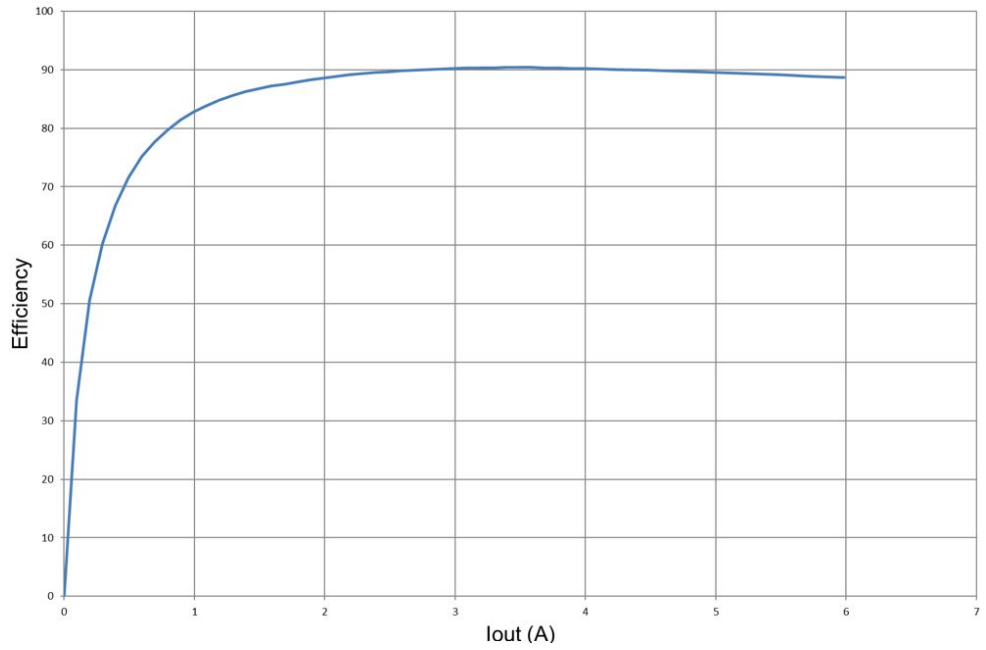
1 A Load
V_{PP} = 12.8 mV

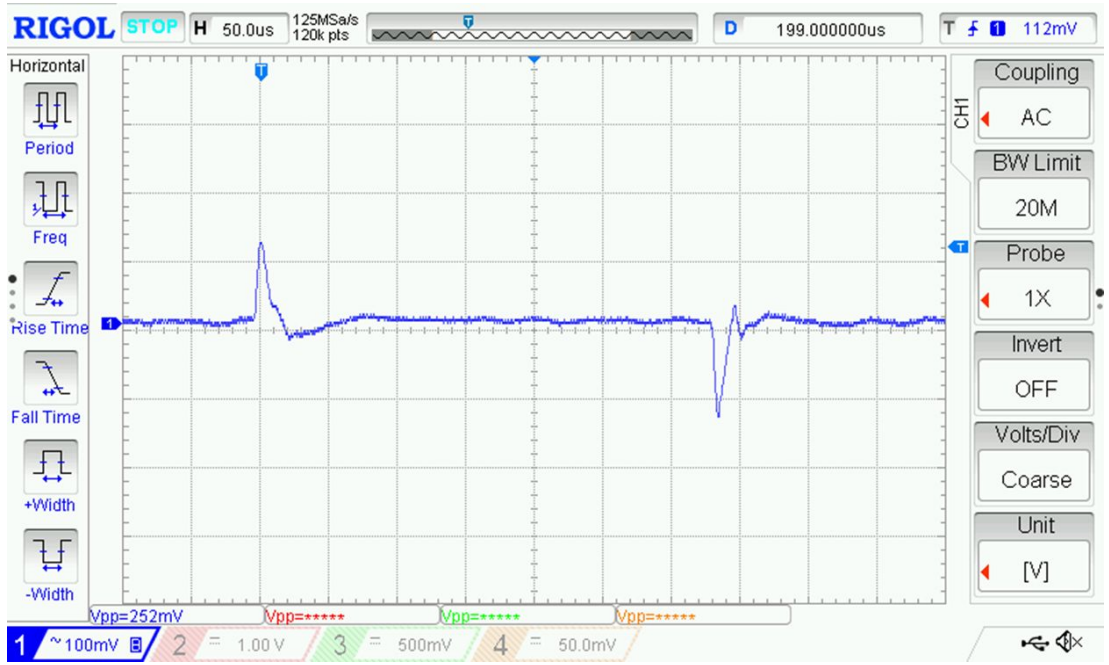
AnDAPT

VCCO_HDIO
3.3 V / 6 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

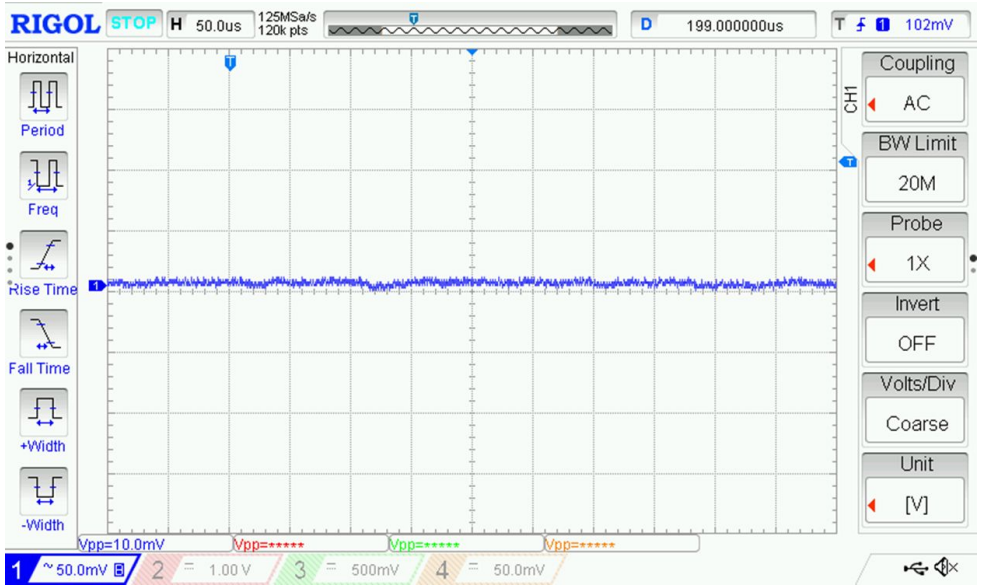
Efficiency & Transient

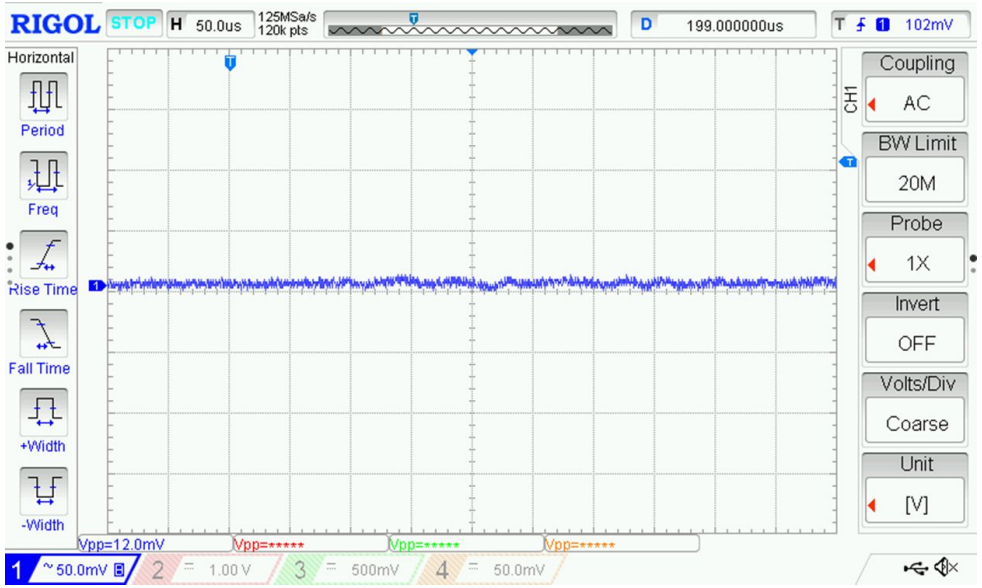




Vout = 3.3 V
Transient 0.6 A – 6 A @ 10 A/µs
V_{PP} = 252 mV
Fsw = 571 kHz
Lout = 1.1 µH, Cout = 3 x 47 µF

Ripple





No Load
V_{PP} = 10 mV

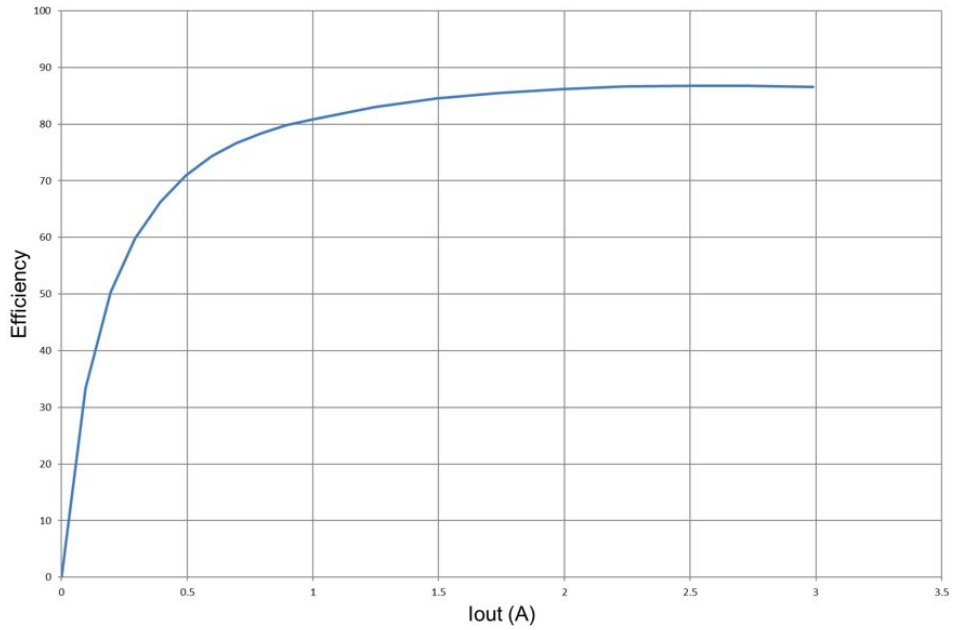
Vout = 3.3 V

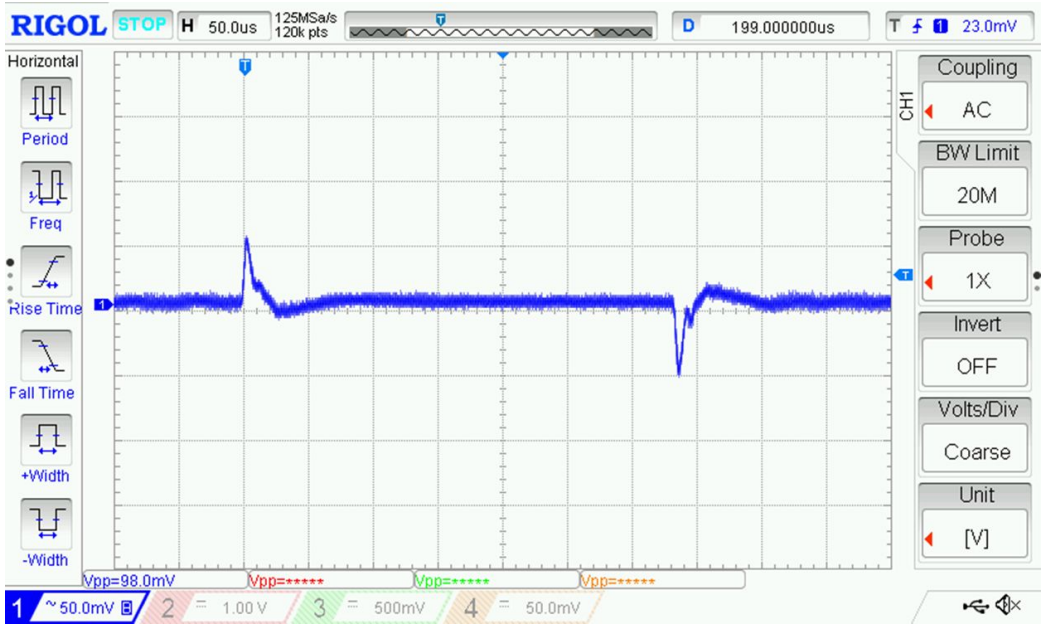
6 A Load
V_{PP} = 12 mV

VCCO_HPIO
1.8 V / 3 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

Efficiency & Transient

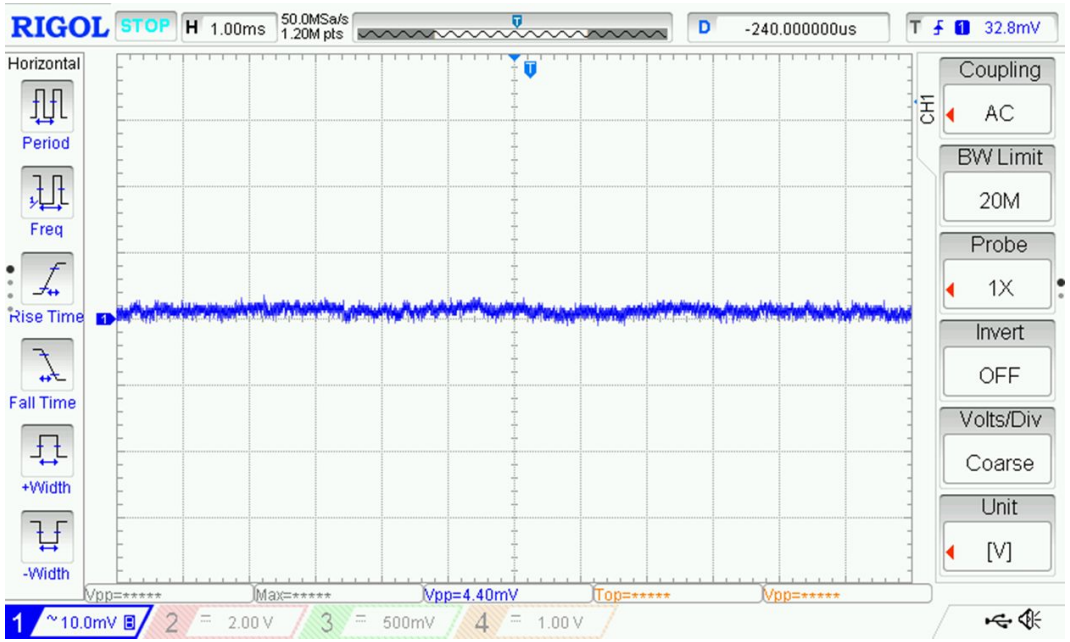




Vout = 1.8 V
Transient 0.3 A – 3A @ 10 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

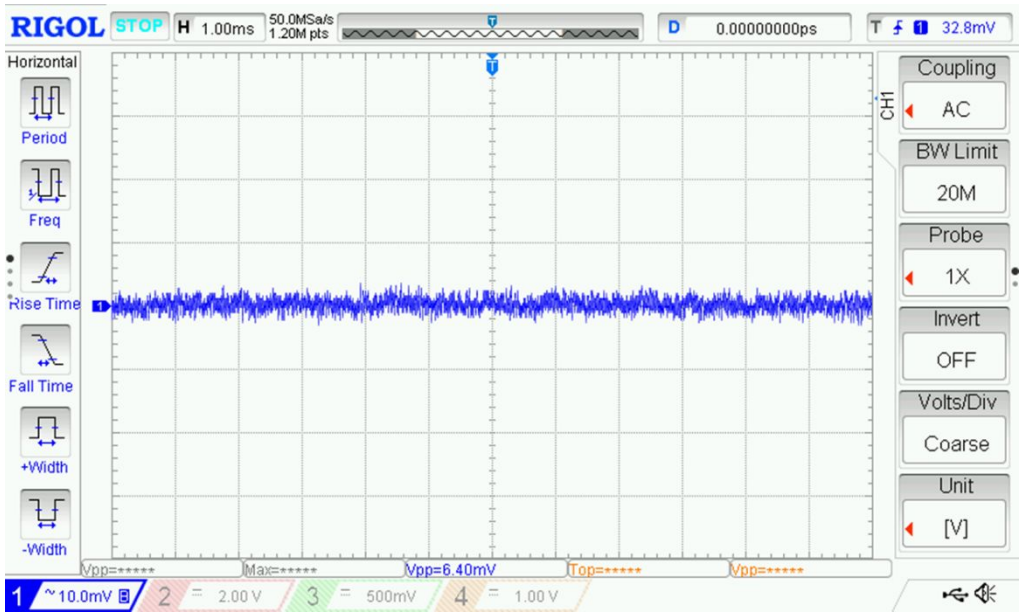
AnDAPT

Ripple



No Load
V_{PP} = 4.4 mV

Vout = 1.8 V



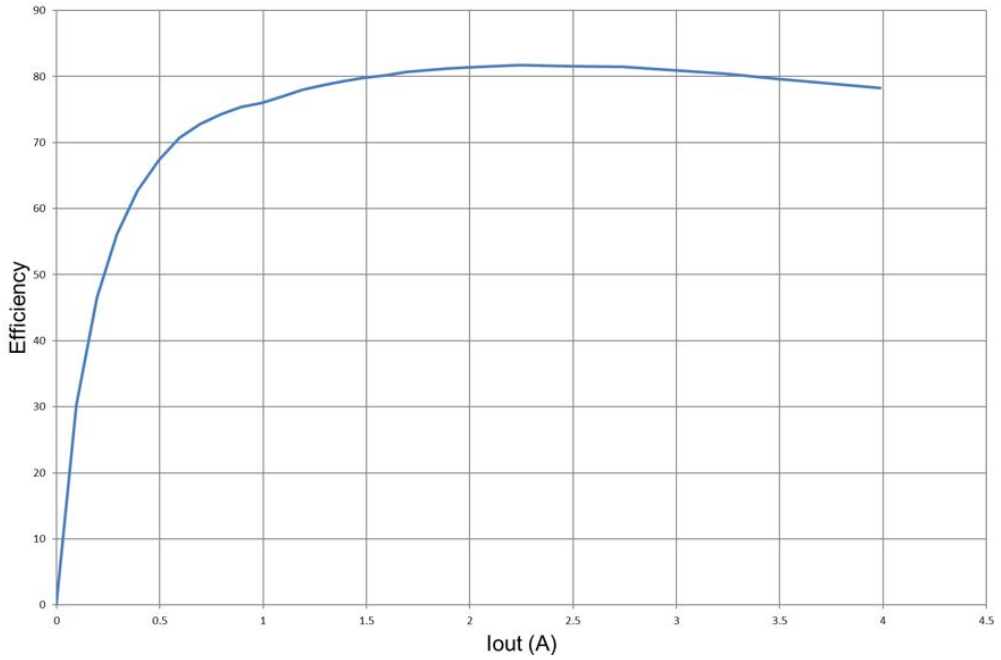
3 A Load
V_{PP} = 6.4 mV

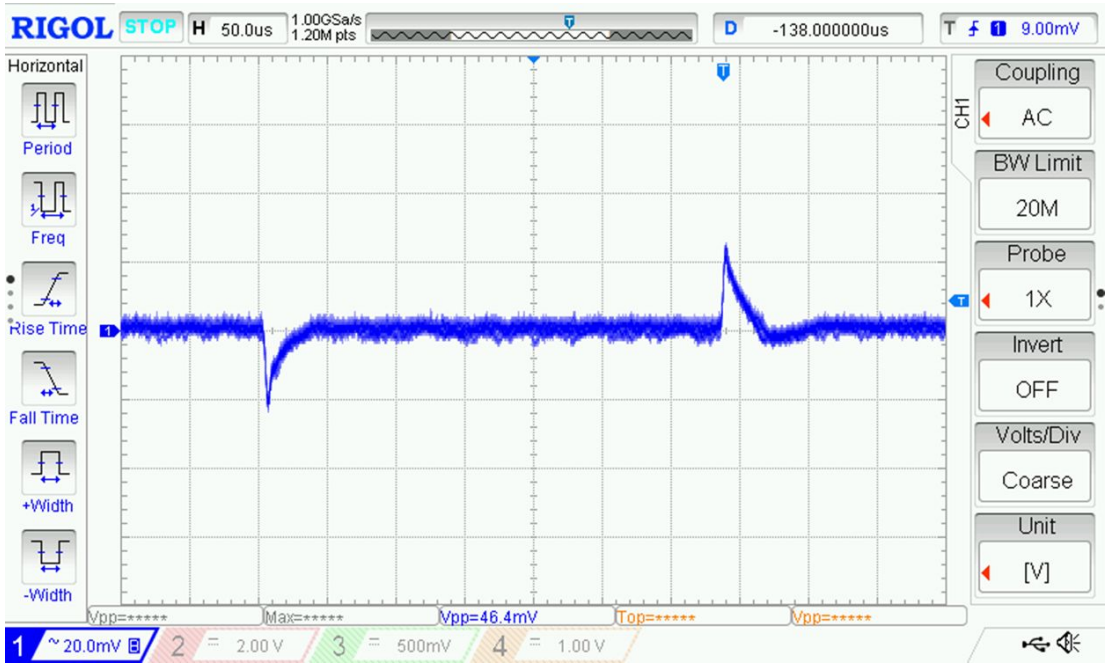
AnDAPT

VCC_DDR
1.2 V / 4 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 7x47 uF

Efficiency & Transient

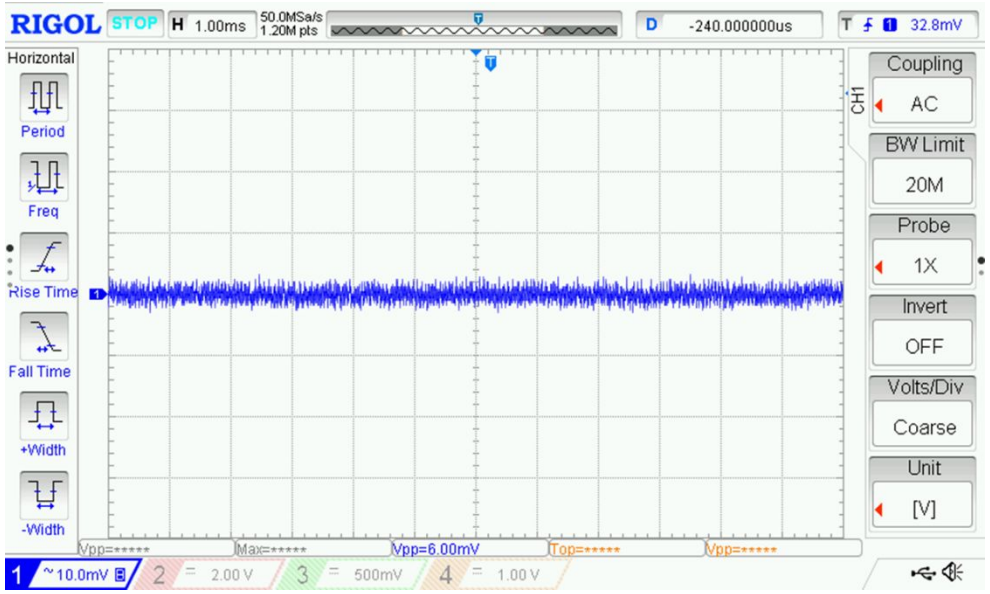




Vout = 1.2 V
Transient 0.8 A – 4 A @ 10 A/µs
V_{PP} = 46.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 7 x 47 µF

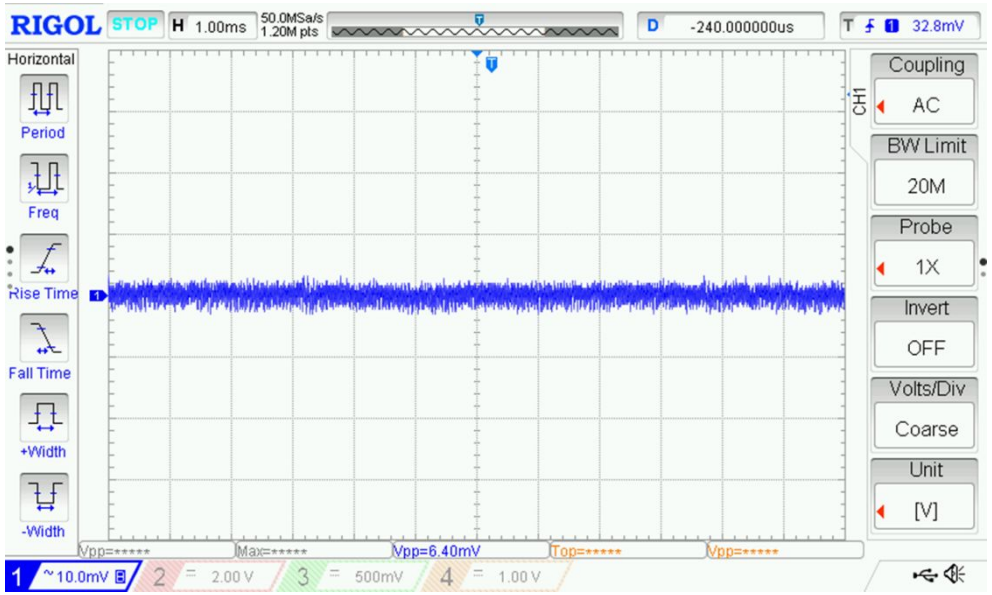
AnDAPT

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



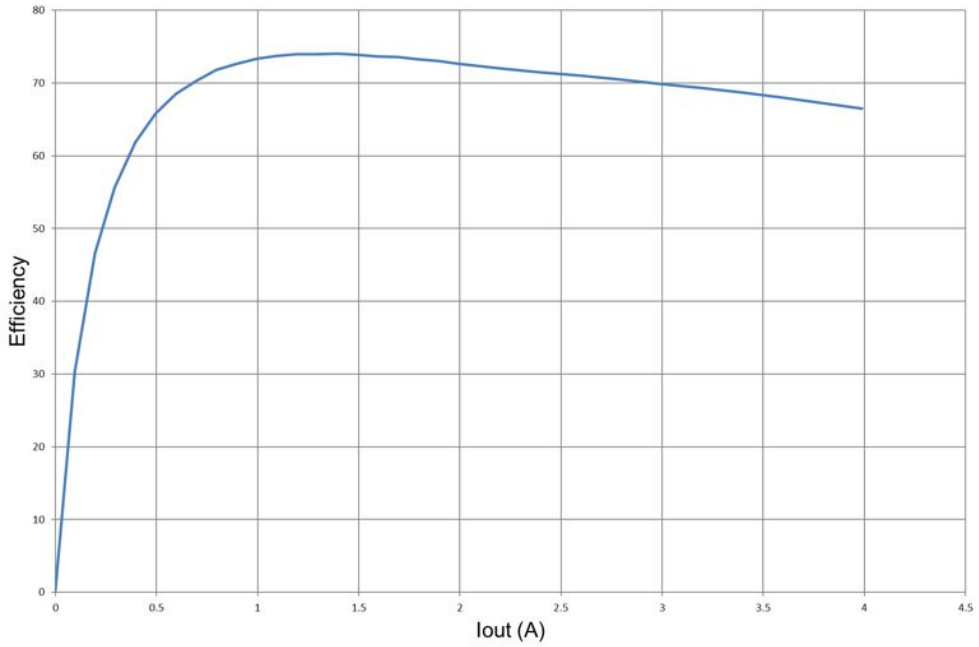
0.035 A Load
V_{PP} = 6.4 mV

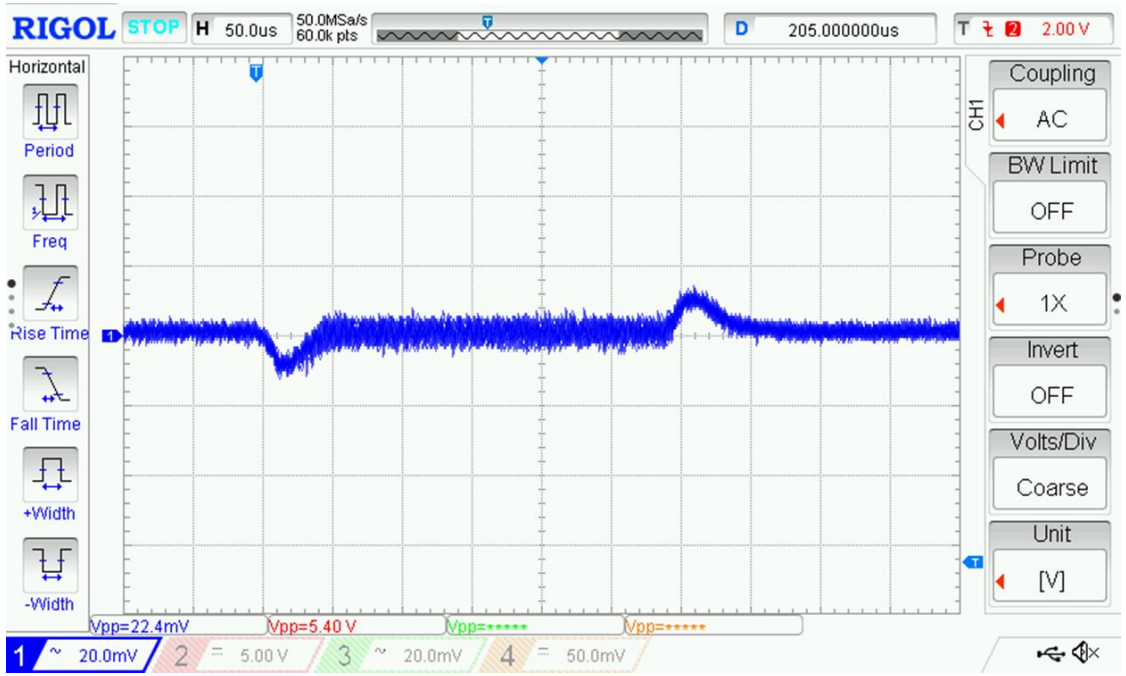
AnDAPT

DDR_VTT (DDR_VTT, DDR_VREF) 0.6 V / 4 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.33 µH, P/N Wurth 744383560056
- C = 8x47 uF

Efficiency & Transient

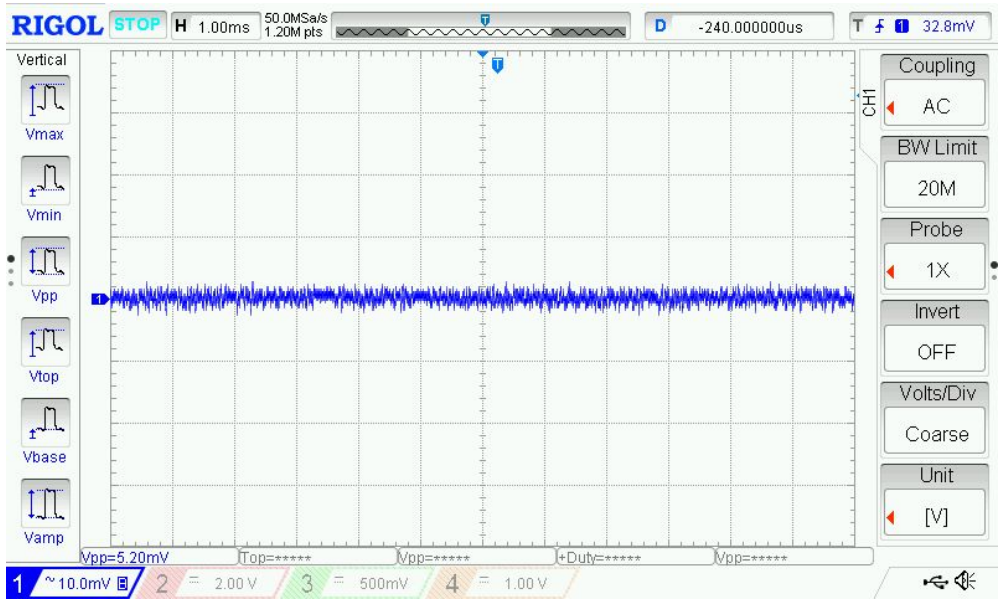




Vout = 0.6 V
Transient 3A – 4 A @ 10 A/µs
V_{PP} = 20.4 mV
Fsw = 1 MHz
Lout = 0.33 µH, Cout = 8 x 47 µF

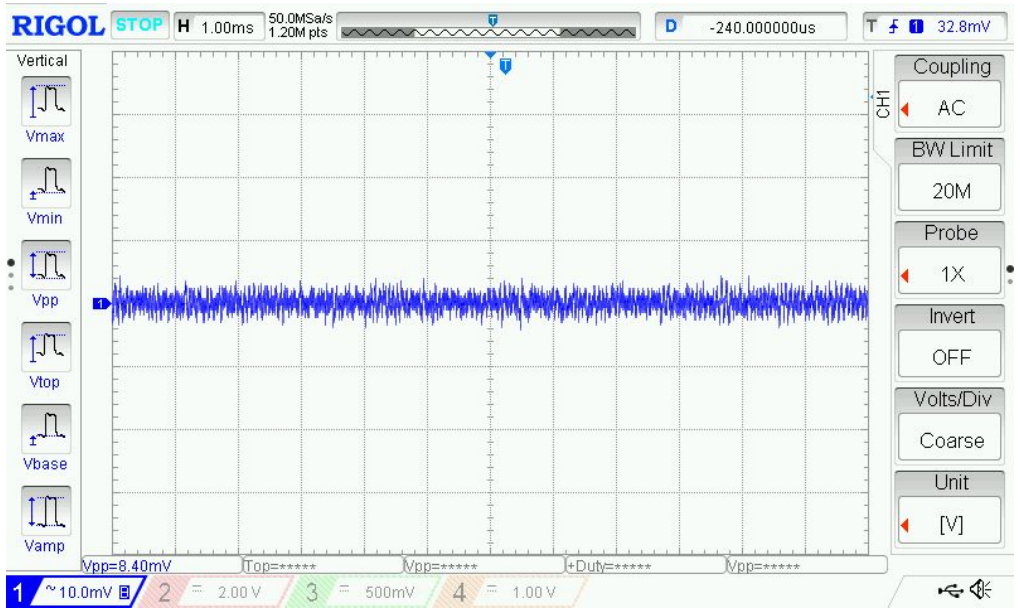
AnDAPT

Ripple



No Load
V_{PP} = 5.2 mV

Vout = 0.6 V



4 A Load
V_{PP} = 8.4 mV

AnDAPT

Thank You

AnDAPT