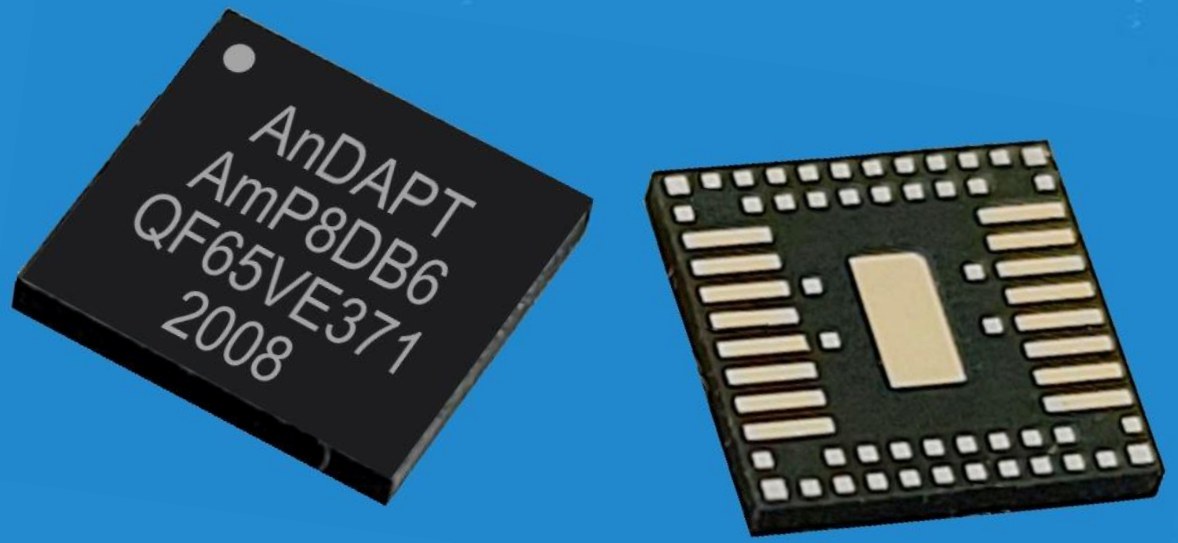


ZYNQ-7000 Cost-optimized Portfolio:

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

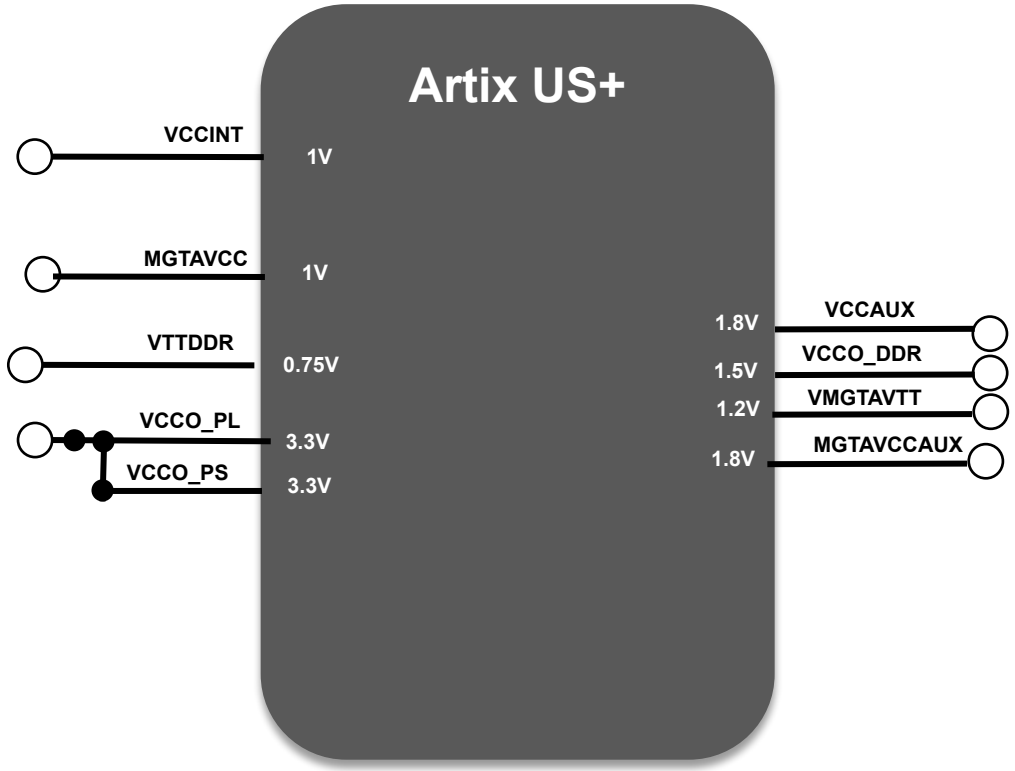
- Xilinx ZYNQ-7000+ family of devices SKUs in cost-optimized portfolio
- ZYNQ-7000+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for ZYNQ-7000+ family FPGAs

ZYNQ-7000 Device SKUs Covered (Cost-optimized)

Supported SKUs
XC7Z007S
XC7Z012S
XC7Z014S
XC7Z010
XC7Z015
XC7Z020

ZYNQ-7000 (Cost-optimized)

Can be combined if voltage same



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Power Tree: ZYNQ-7000 (Cost-optimized)

PVIN = 12V/1.8V

#	Rail	Seq	Vin (V)	Vout (V)	Iout (A)
1	VCCINT	1	12	1	7
2	MGTACCC	1	12	1	5
3	VCCAUX	2	12	1.8	2.5
4	MGTAVTT	2	12	1.2	2
5	VCCO_DDR	3	1.8	1.5	0.5
6	VCCO_PL	3	12	3.3	3
7	VCCO_PS	3	12	3.3	2
7	VTTDDR	4	12	0.75	3
8	MGTVCCAUX	4	1.8	1.8	0.12

Power Tree Mapping: ZYNQ-7000 (Cost-optimized)

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRM, VCCPINT	1	C220	Sync Buck HC	V_{IN}	12	1	7	ARD_X_Z70_A1_IC1
2	MGTAVCC	1	C200	Sync Buck	V_{IN}	12	1	5	ARD_X_Z70_A1_IC1
3	VCCAUX, VCCPAUX, VCCPLL	2	C200	Sync Buck	V_{IN}	12	1.8	2 + 0.5 + 0.12	ARD_X_Z70_A1_IC2
4	MGTAVTT	2	C200	Sync Buck	V_{IN}	12	1.2	2	ARD_X_Z70_A1_IC1
5	VCCO_DDR	3	C710	SIM LDO	VCCAUX	1.8	1.5	0.5	ARD_X_Z70_A1_IC2
6	VCCO_PL	3	C150	Async Buck	V_{IN}	12	3.3	3	ARD_X_Z70_A1_IC2
7	VCCO_PS	3	C150	Async Buck	V_{IN}	12	3.3	2	ARD_X_Z70_A1_IC2
8	VTTDDR	4	C200	Sync Buck	V_{IN}	12	0.75	3	ARD_X_Z70_A1_IC2
9	MGTVCCAUX, VCCADC	4	C750	Load Switch	VCCAUX	1.8	1.8	0.12	ARD_X_Z70_A1_IC2

Estimated total area estimated* = 535.84 + 634.05 = 1169.89 mm^2

*With 75% Layout optimization density

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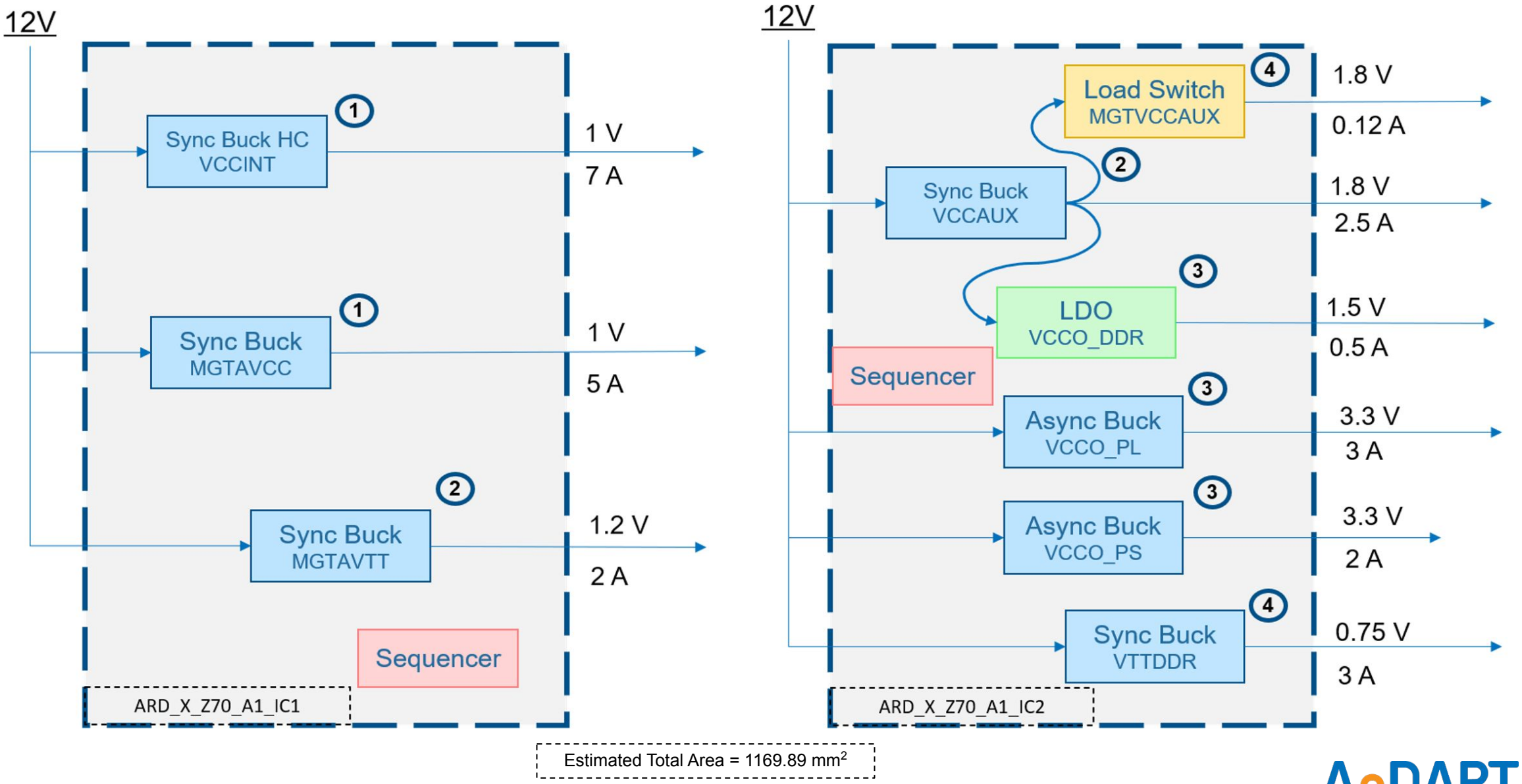
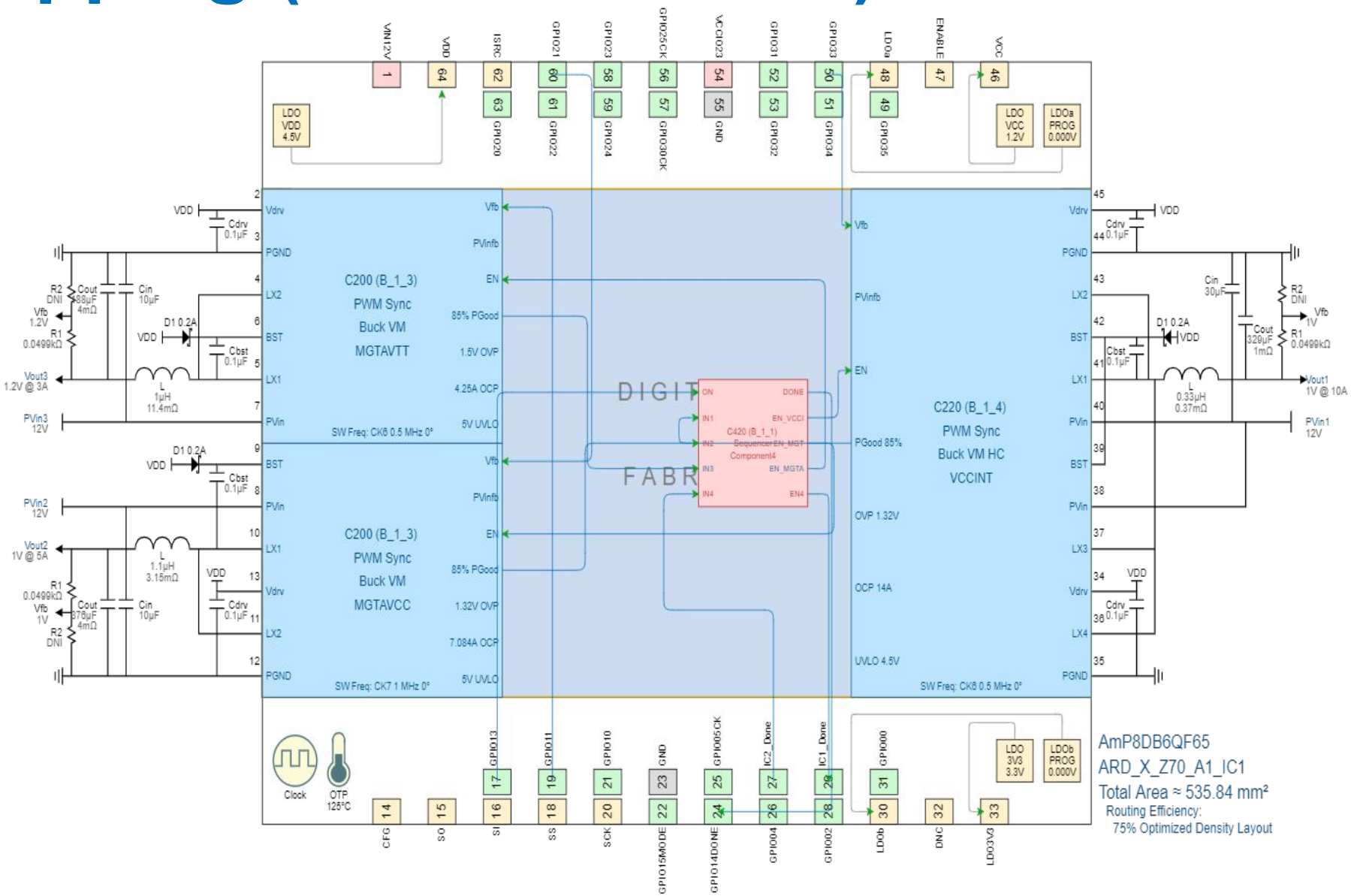
Power Tree Mapping



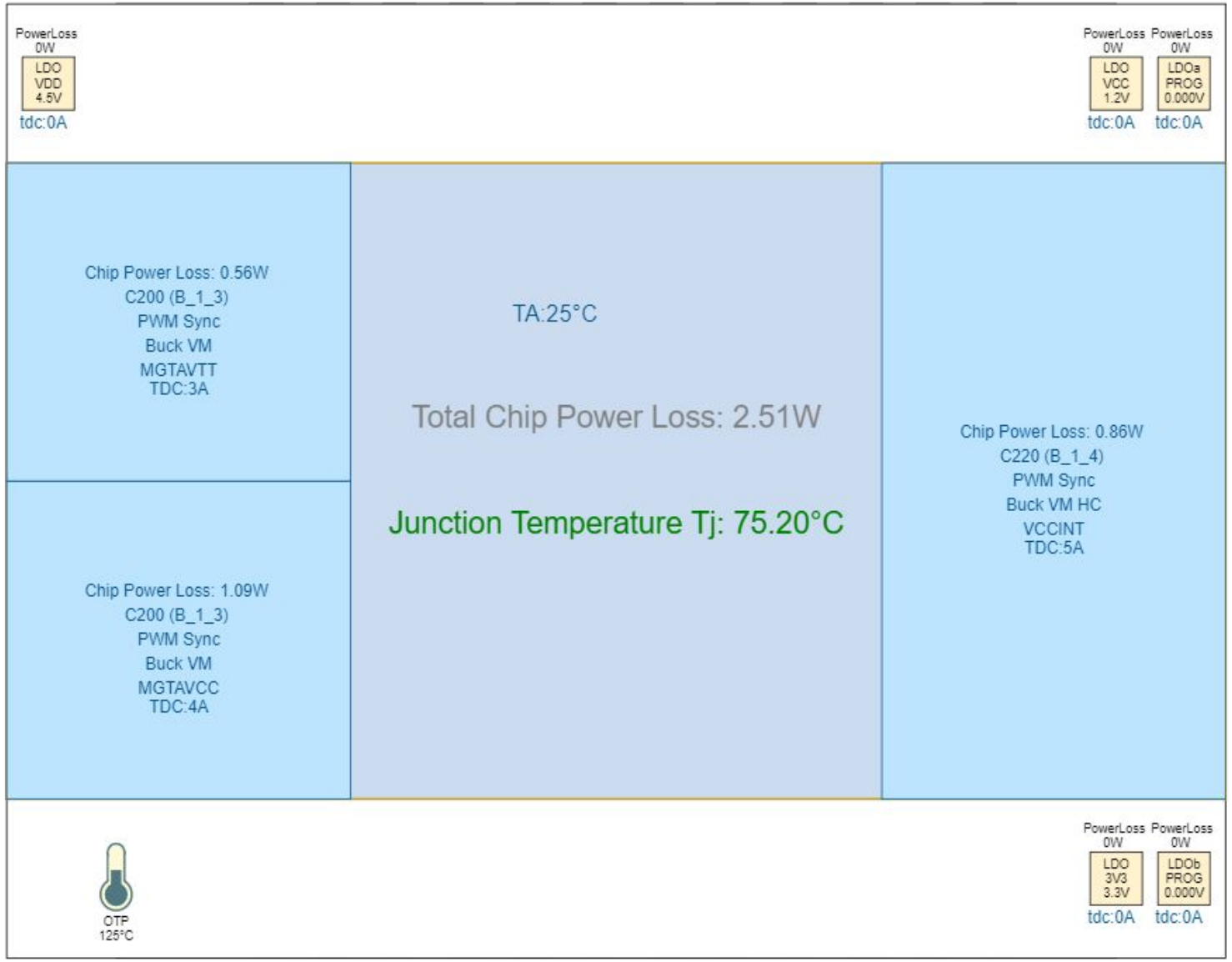
Estimated Total Area = 1169.89 mm^2

AnDAPT

Mapping (WebAmP View) IC1



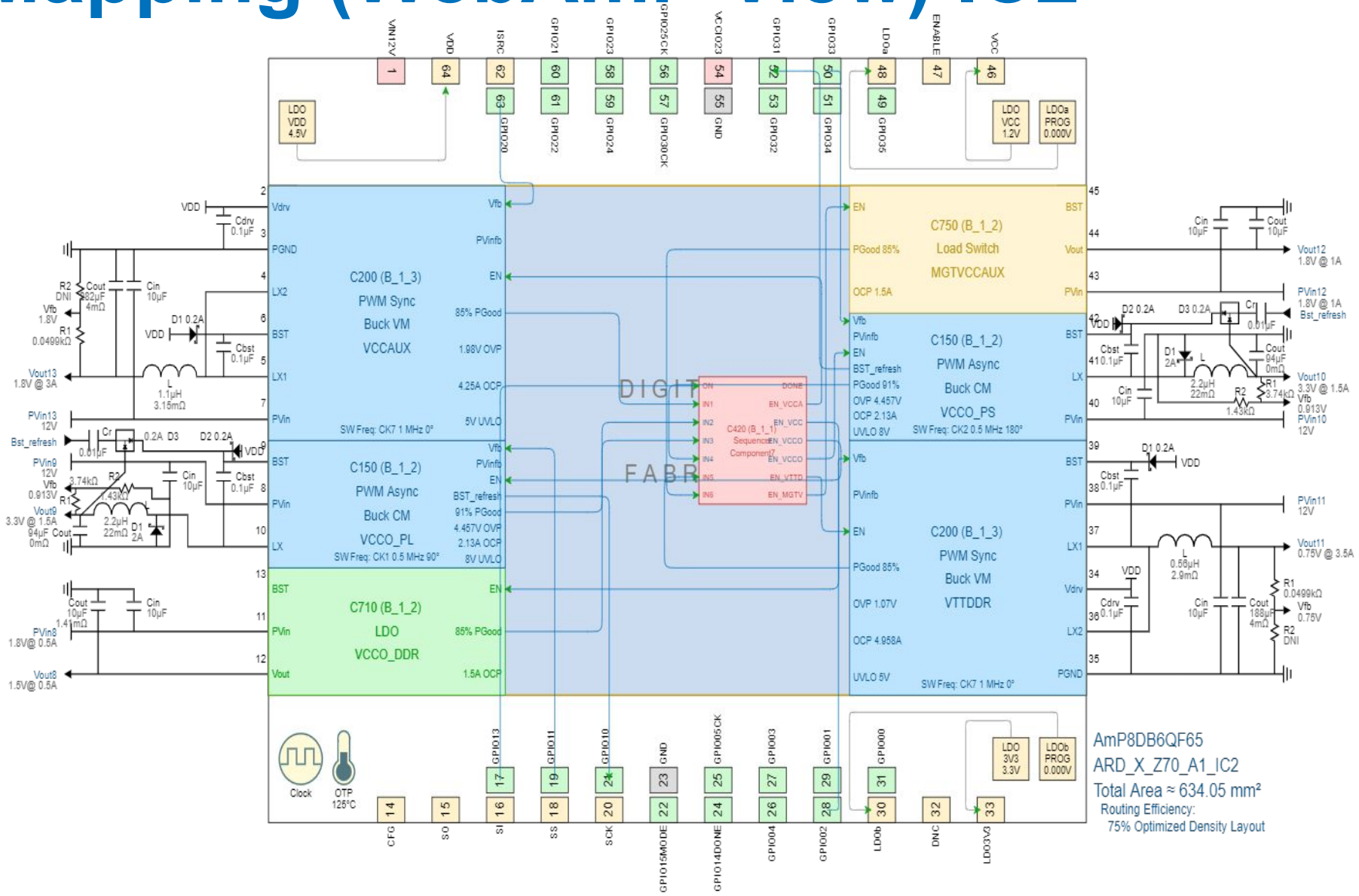
Mapping (Thermal View) IC1



AmP8DB6QF65
ARD_X_Z70_A1_IC1
Total Area ≈ 535.84 mm²
Routing Efficiency:
75% Optimized Density Layout

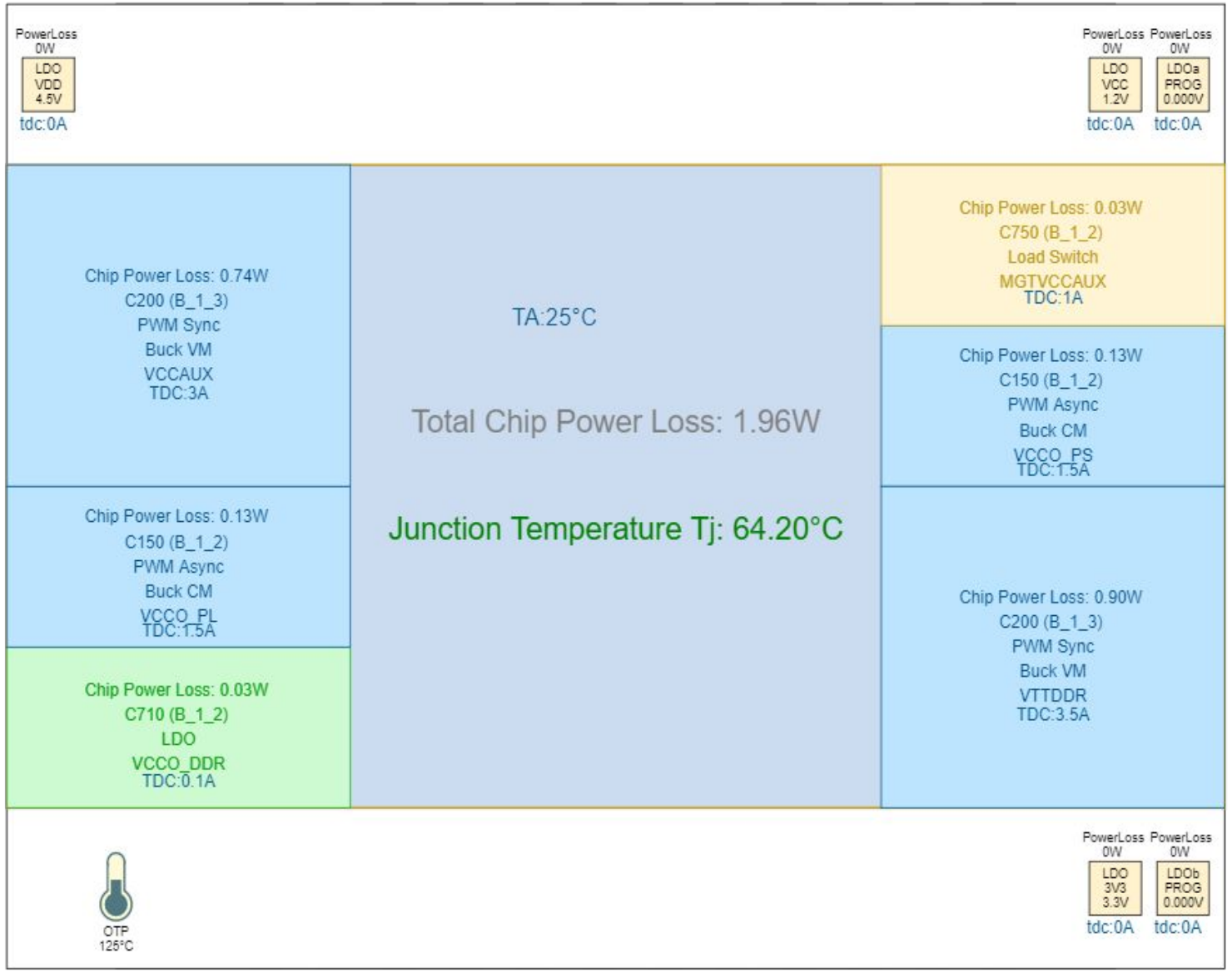
AnDAPT

Mapping (WebAmP View) IC2



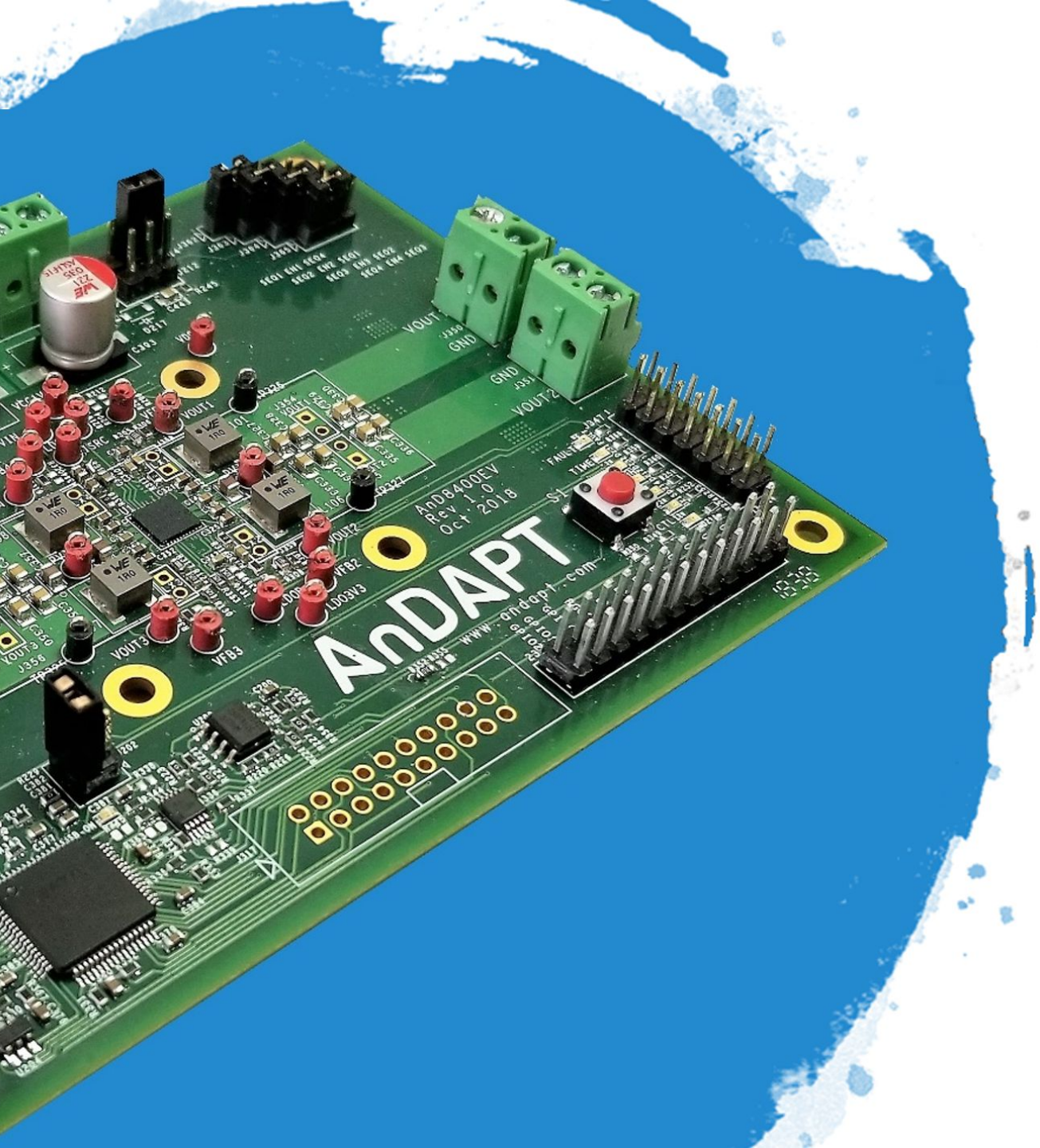
AnDAPT

Mapping (Thermal View) IC2



AmP8DB6QF65
ARD_X_Z70_A1_IC2
Total Area ≈ 634.05 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT

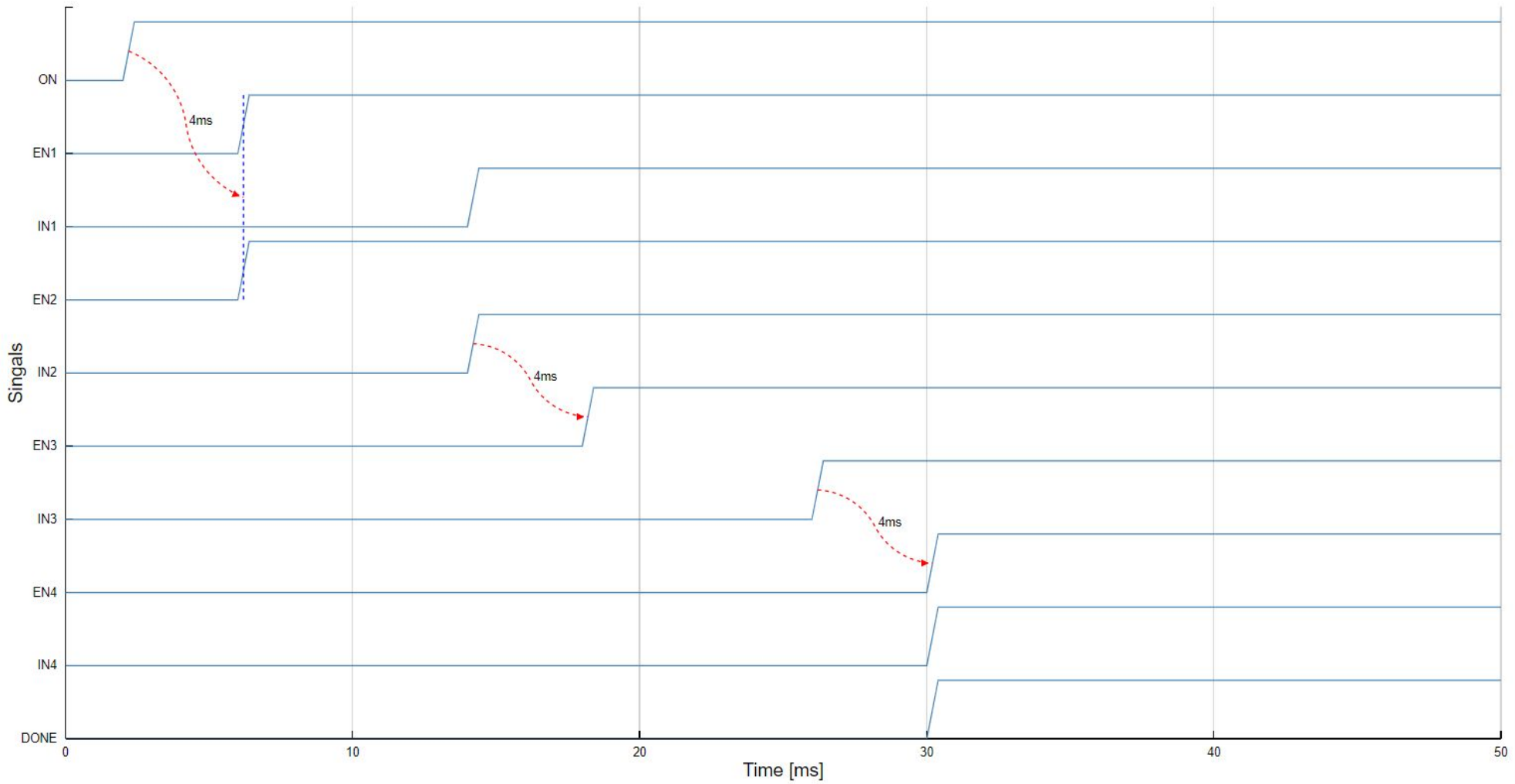


Test Data

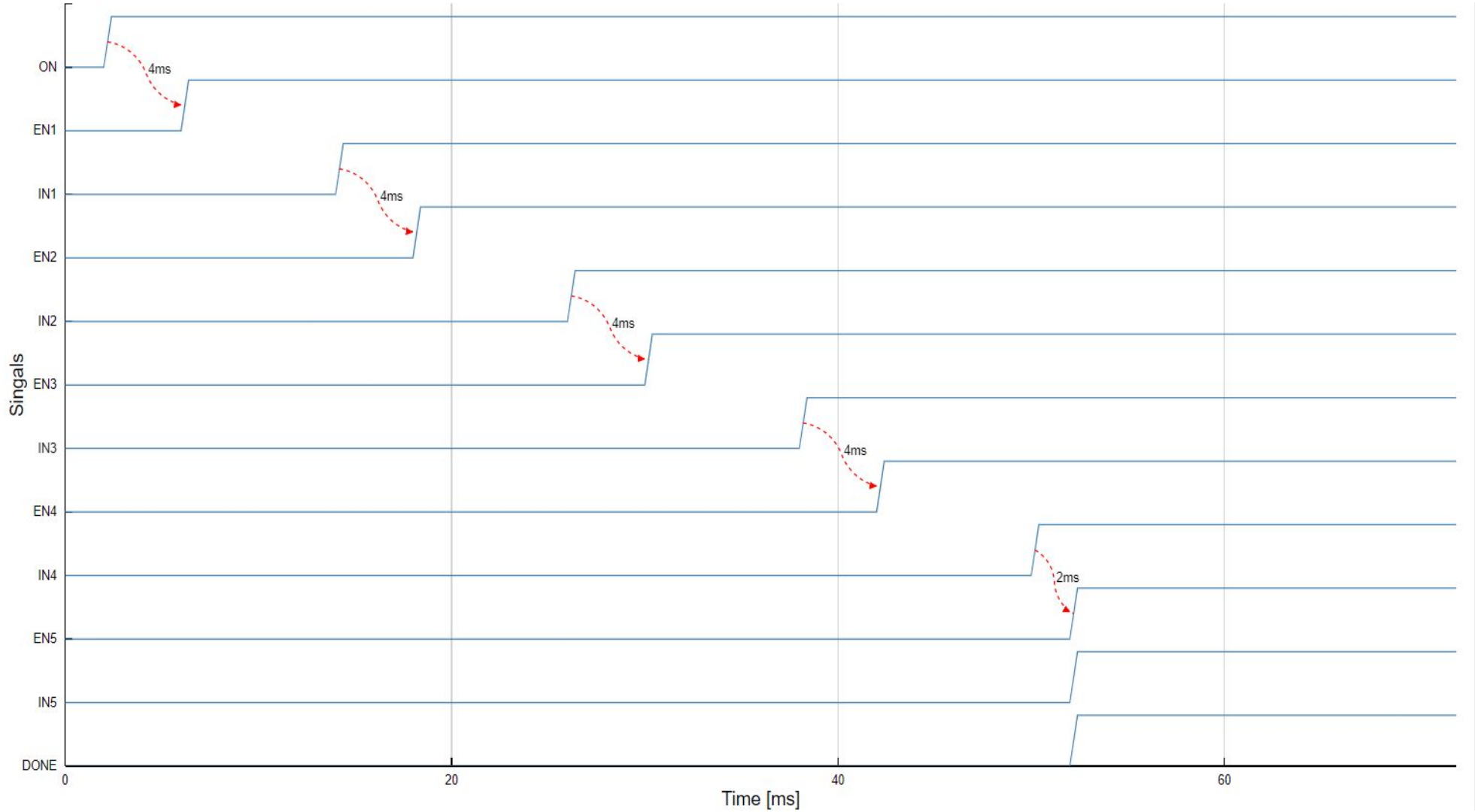
ZYNQ-7000
(Cost-optimized)

AnDAPT

Integrated Sequencer Graphic IC1 (Turn ON)



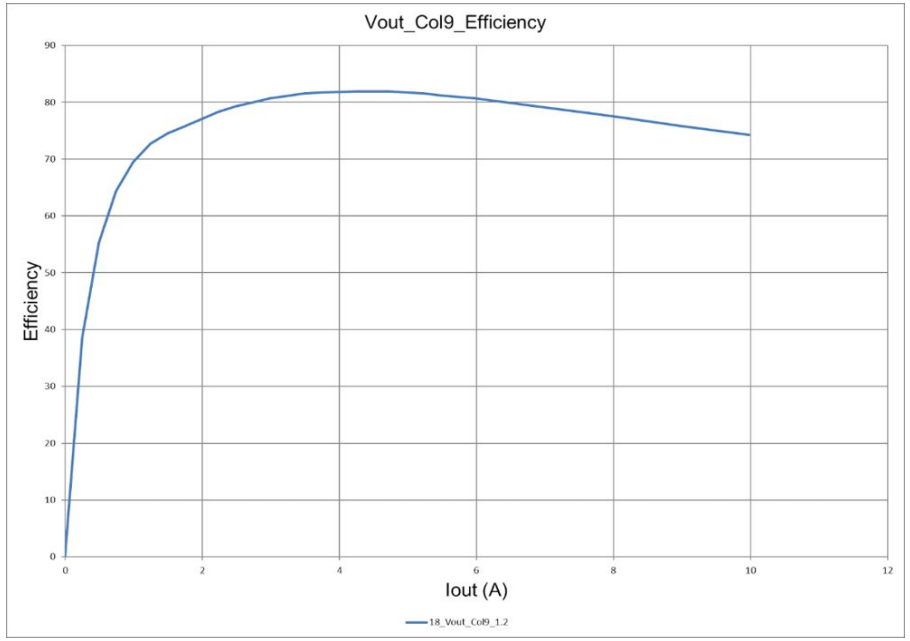
Integrated Sequencer Graphic IC2 (Turn ON)

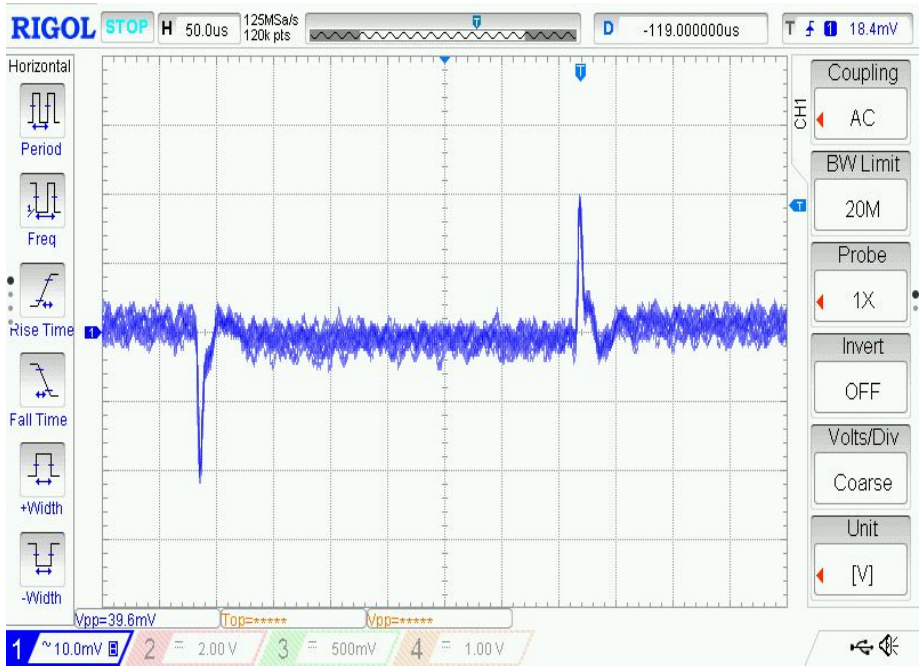


VCCINT
1 V / 7 A

- C220
- Fsw = 571 kHz
- L = 0.33 µH, P/N Wurth 744308033
- C = 329 uF

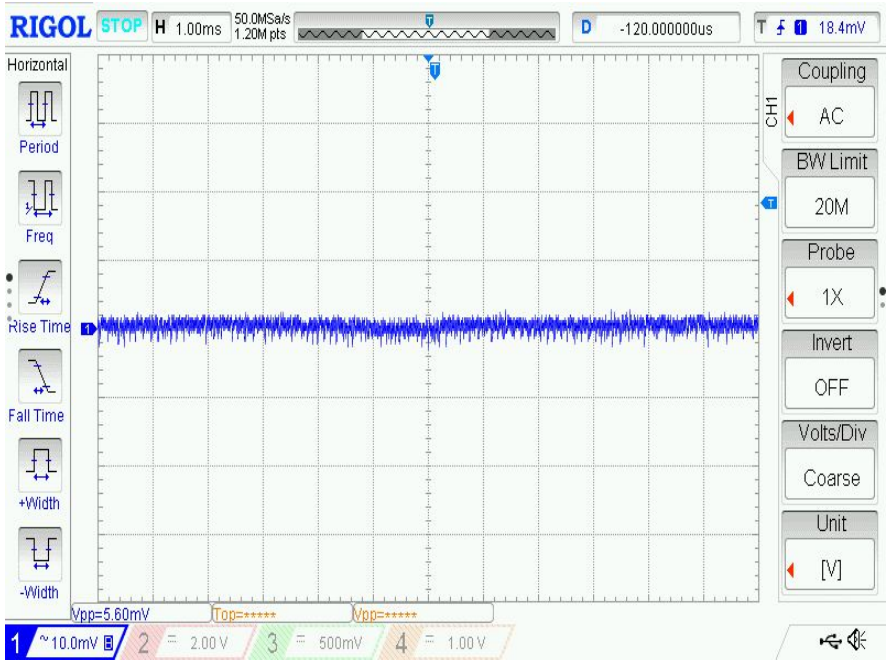
Efficiency & Transient





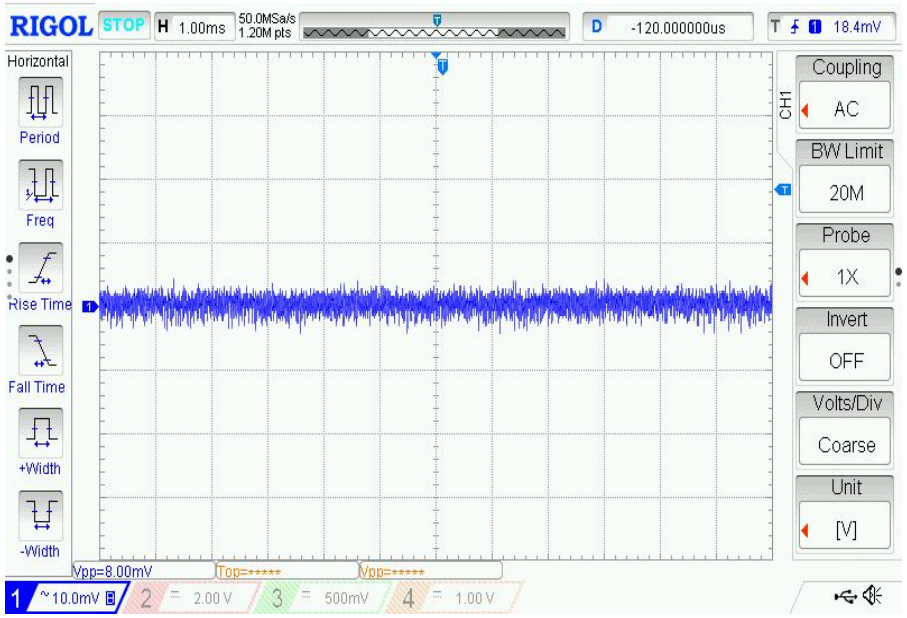
Vout = 1 V
Transient 7.5A – 10A @ 10 A/µs
V_{PP} = 39.6 mV
Fsw = 571 kHz
Lout = 0.33 µH, Cout = 329 µF

Ripple



No Load
V_{PP} = 5.6 mV

Vout = 1 V

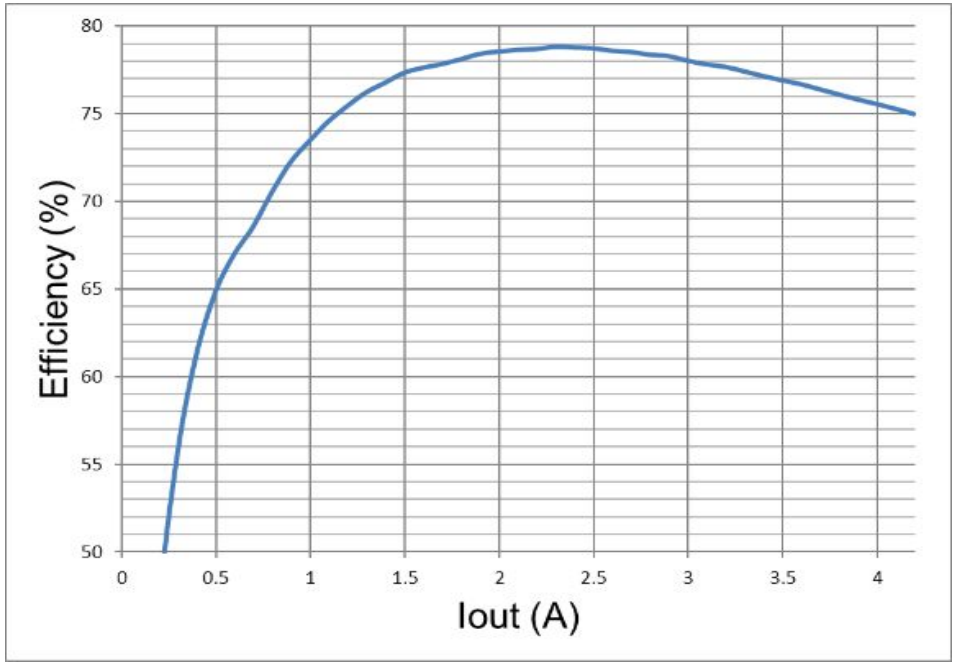


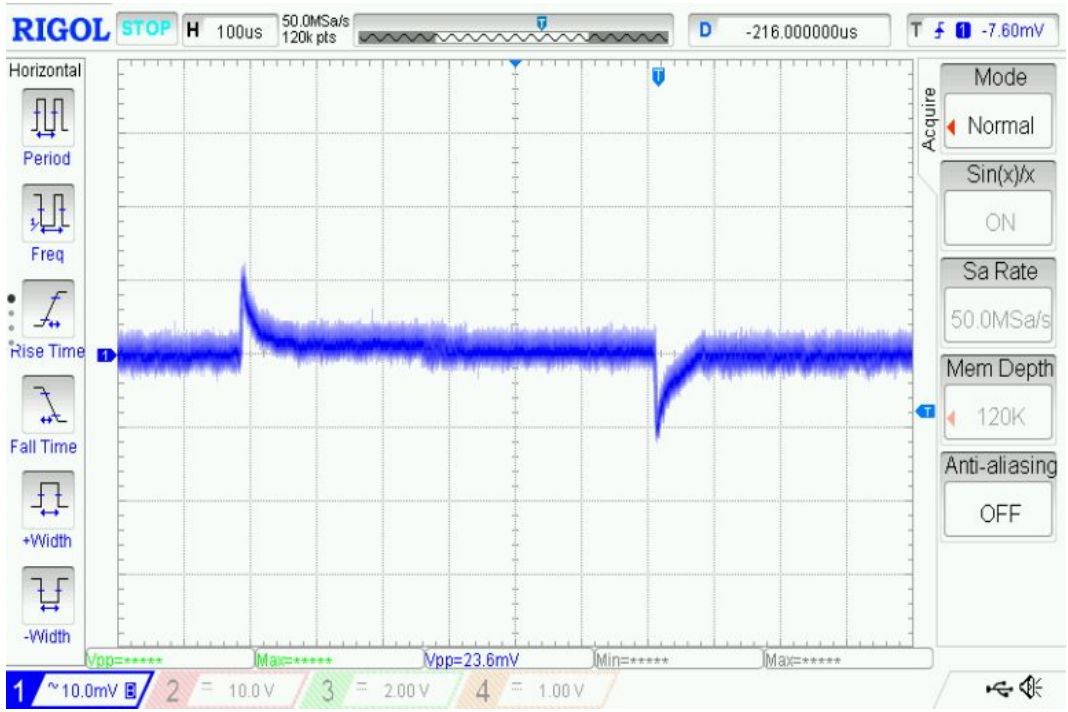
10 A Load
V_{PP} = 8 mV

MGTAVCC
1 V / 4.2 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 9x47 uF

Efficiency & Transient





Vout = 1 V
Transient 3.15 A – 4.2 A @ 100 A/µs
V_{PP} = 23.6 mV
Fsw = 1 MHz
Lout = 1.1 µH, Cout = 8 x 47 µF

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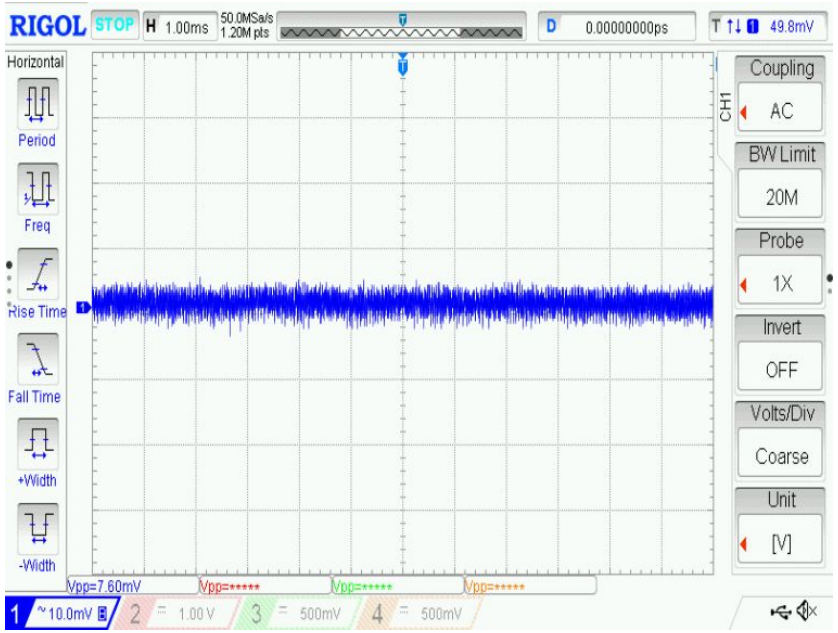
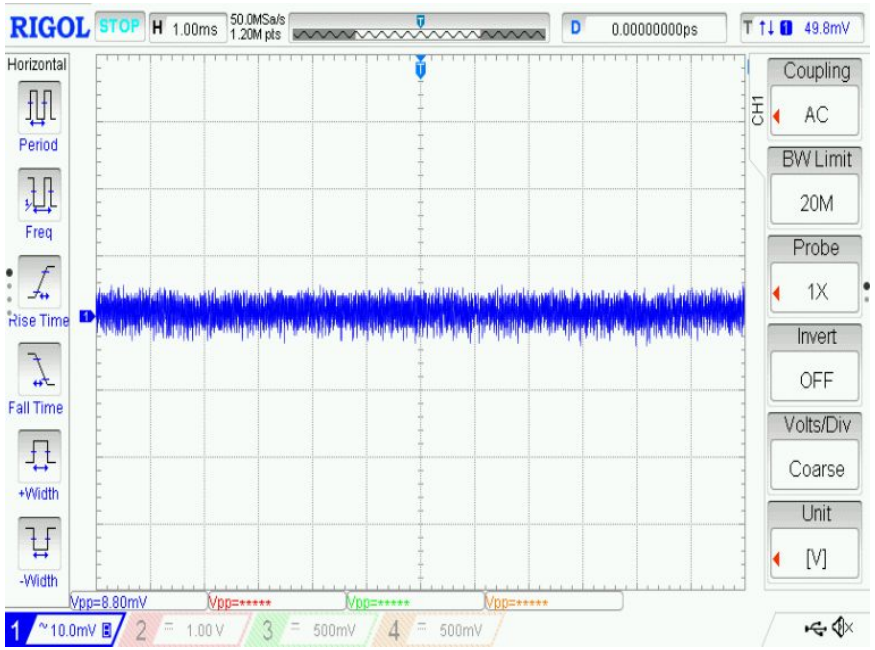
Ripple



No Load
V_{PP} = 7.6 mV

Vout = 1 V



4.2 A Load
V_{PP} = 8.80 mV

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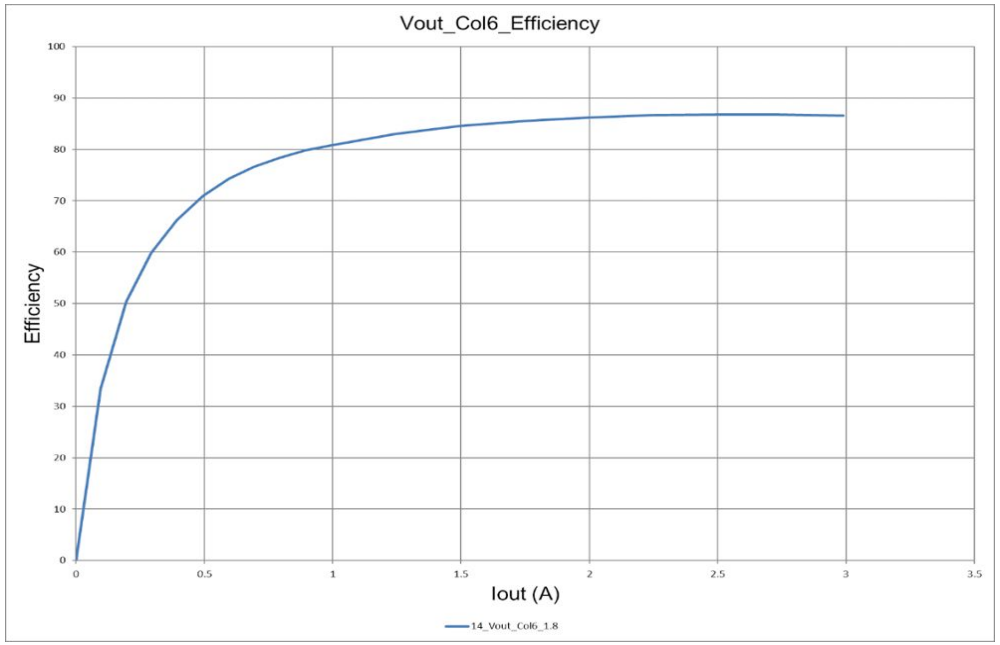
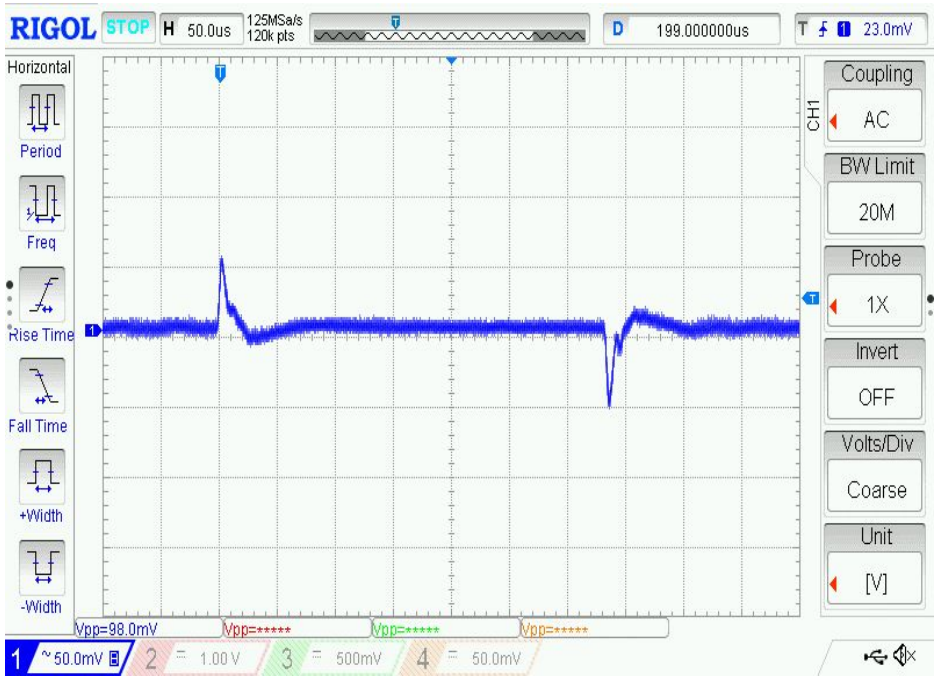
VCCAUX
1.8 V / 3 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 1.1 µH, P/N Wurth 744314110
- C = 3x47 uF

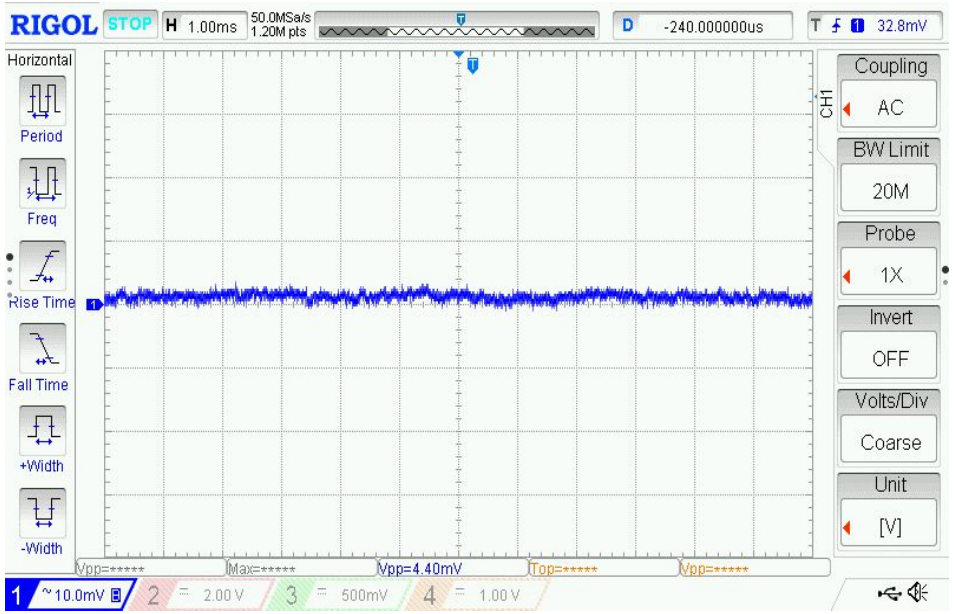
Efficiency & Transient





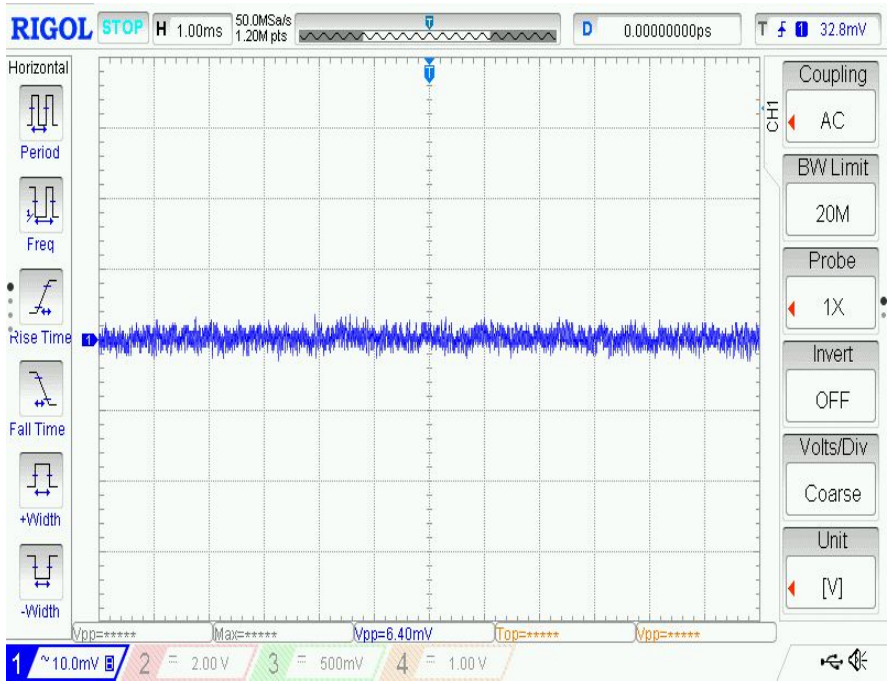
Vout = 1.8 V
Transient 0.3 A – 3 A @ 10 A/µs
V_{PP} = 98 mV
Fsw = 1 MHz
Lout = 1.1 µH, Cout = 3 x 47 µF

Ripple



No Load
V_{PP} = 4.4 mV

Vout = 1.8 V

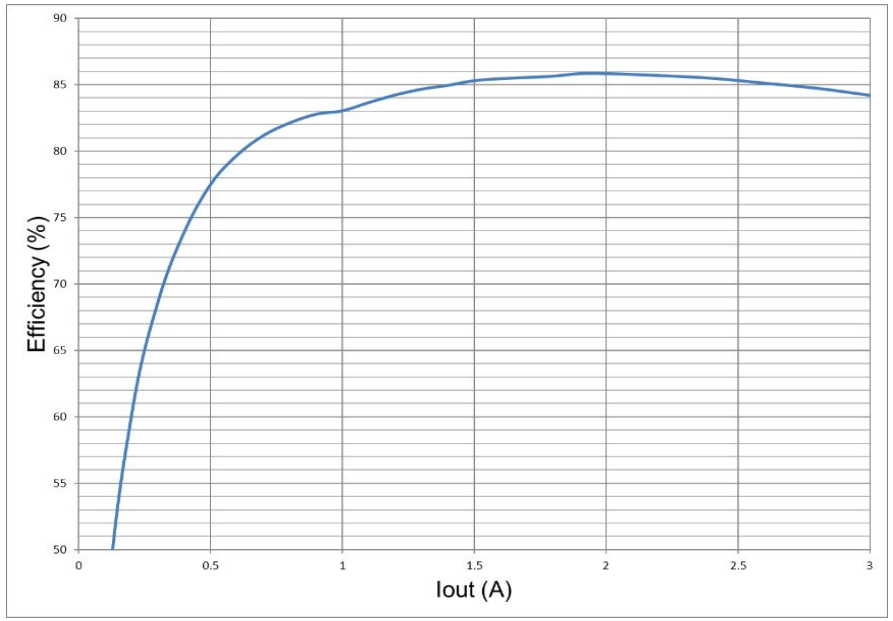


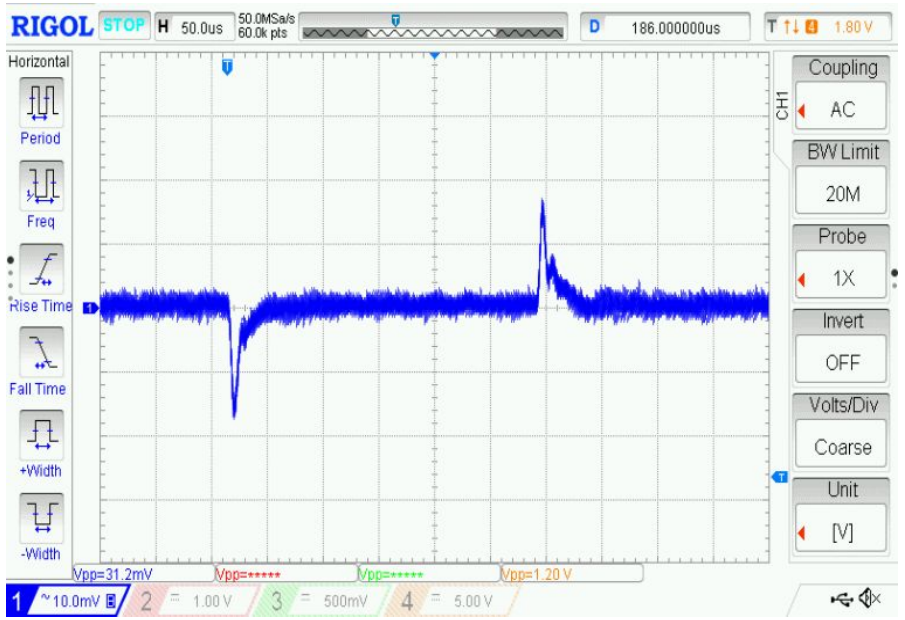
3 A Load
V_{PP} = 6.4 mV

MGTAVTT
1.2 V / 2 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1 µH, P/N Wurth 74438366010
- C = 4x47 uF

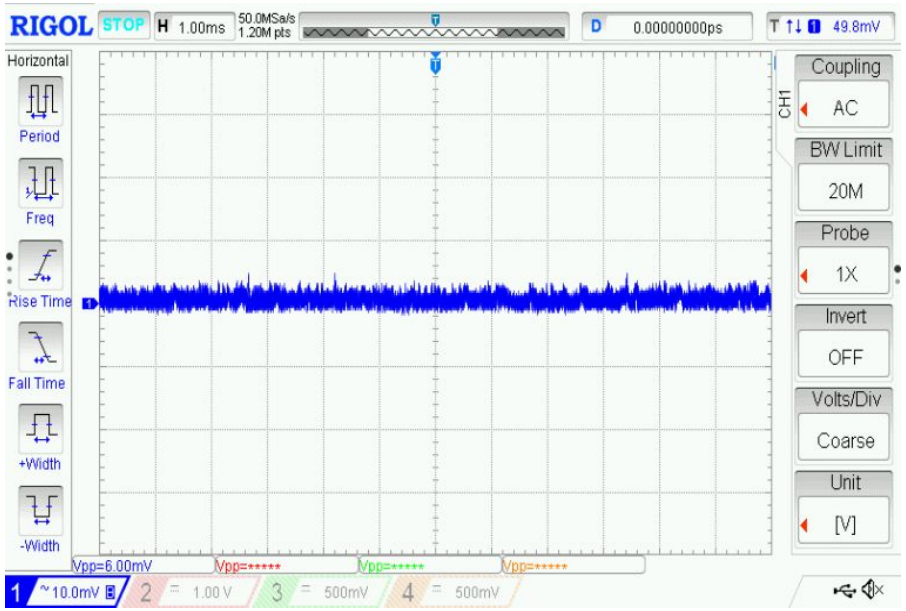
Efficiency & Transient





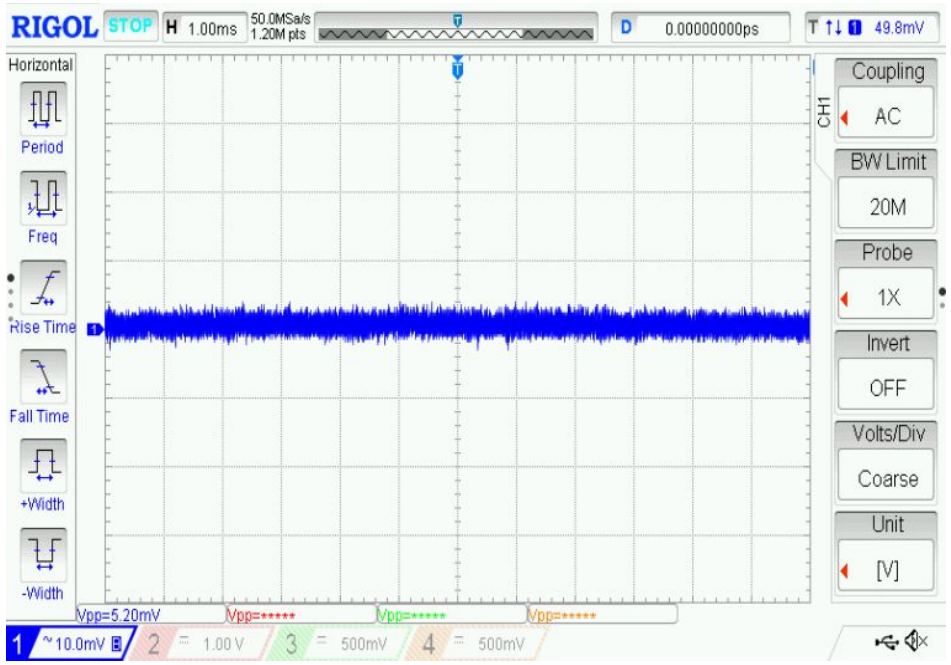
Vout = 1.2 V
Transient 2.25 A – 3 A @ 60 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

Ripple



No Load
V_{PP} = 6 mV

Vout = 1.2 V



3 A Load
V_{PP} = 5.2 mV

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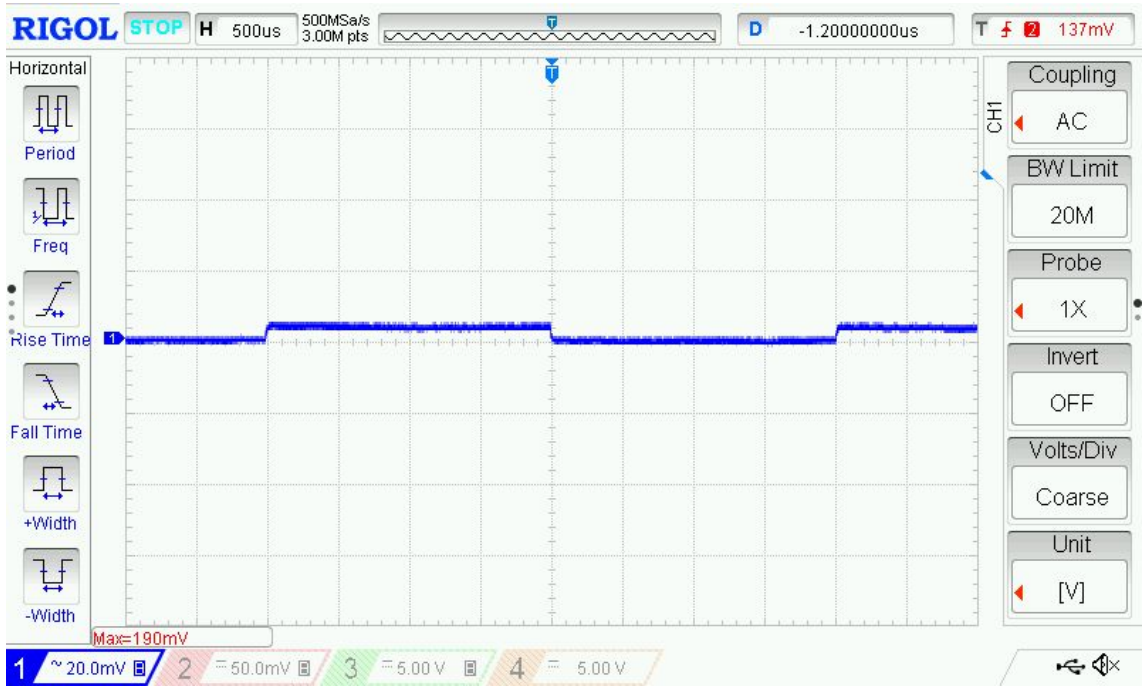
VCCO_DDR
1.5 V / 0.5 A

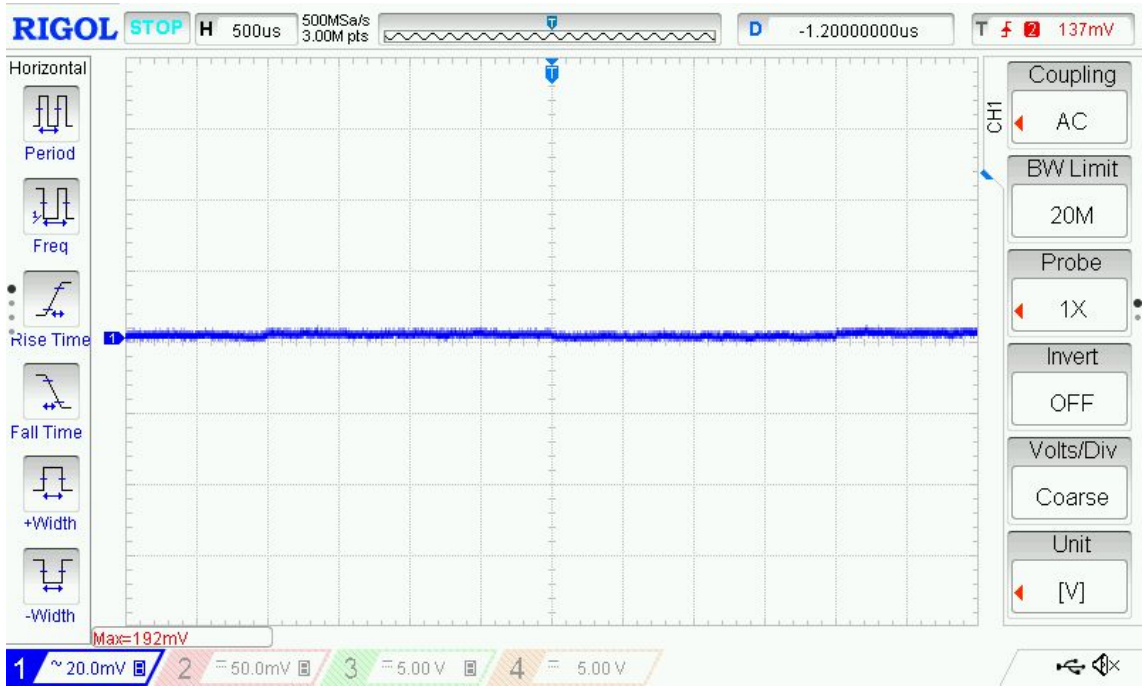
- C710 LDO

Transient



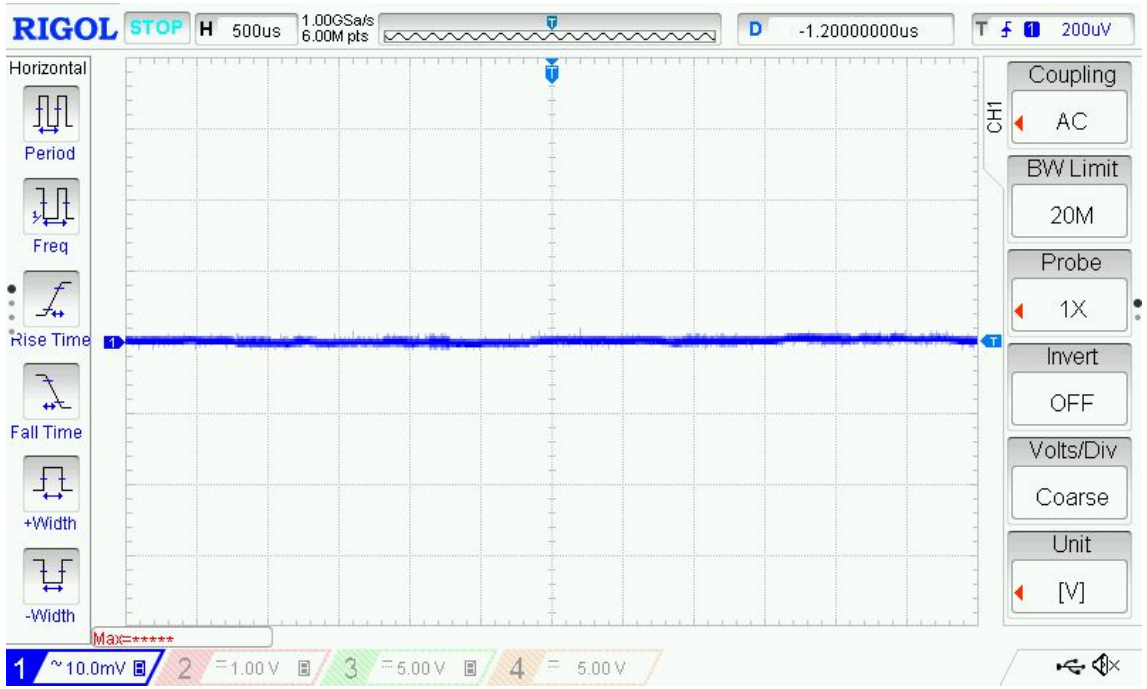
Internal

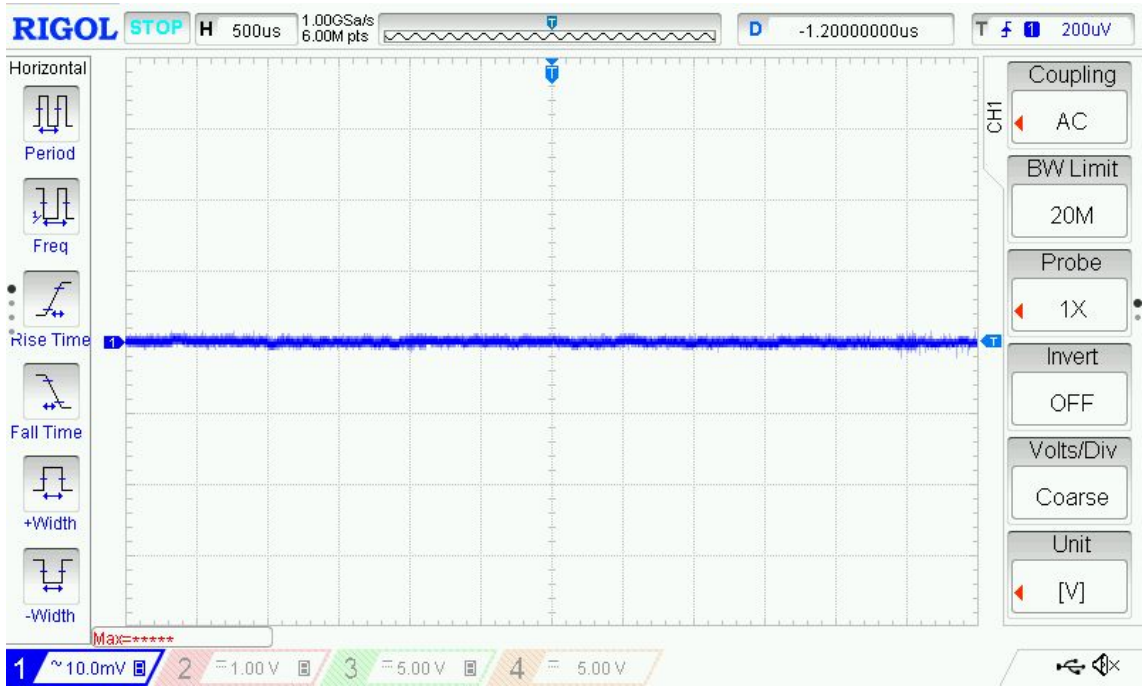
Vout = 1.5 V
Transient 0.25 A to 0.5 A
V_{PP} = 17.2 mV
Cout = 22uF



External

Ripple





No Load

Cout = 22uF

0.5 A Load

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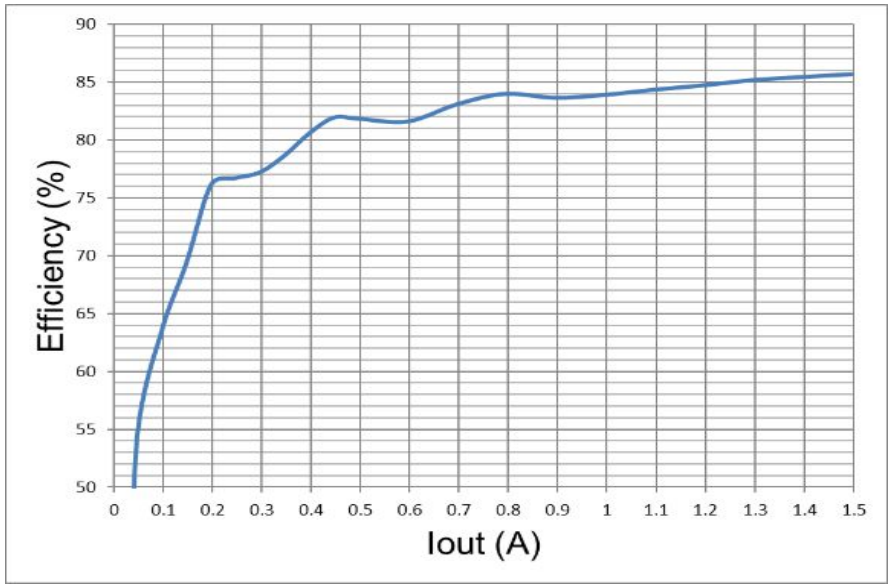
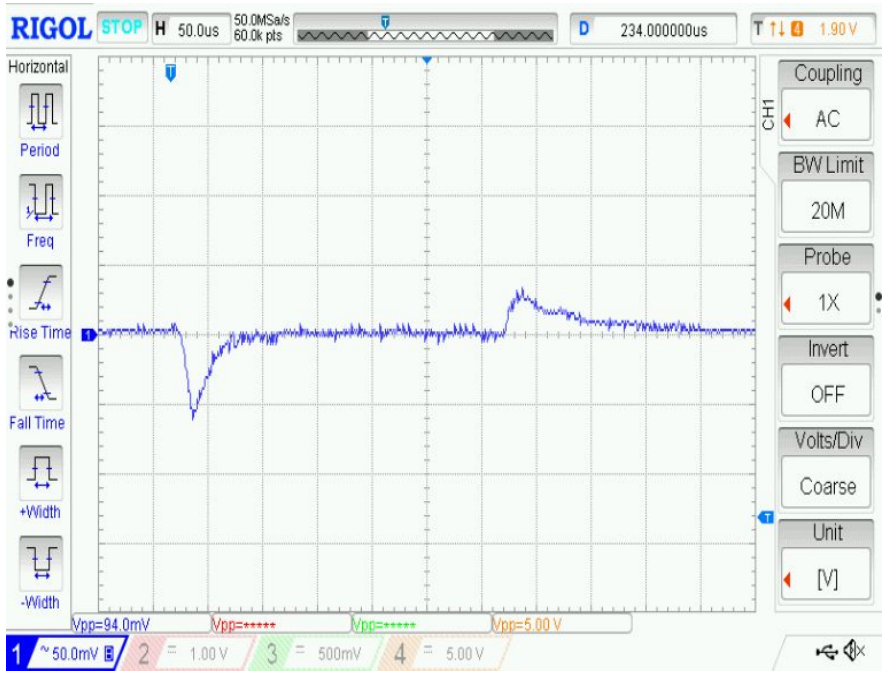
VCCO_PL
3.3 V / 3 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

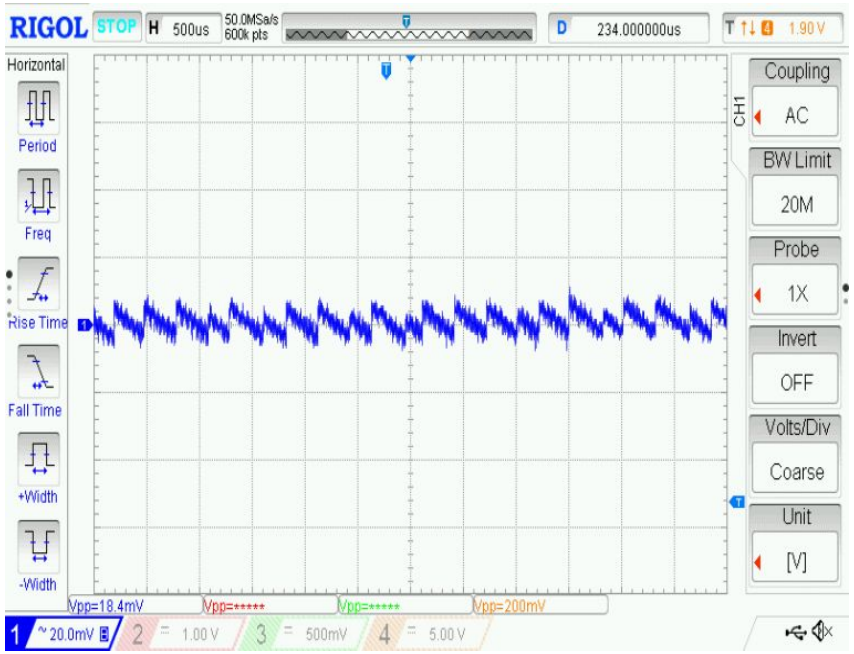
Efficiency & Transient





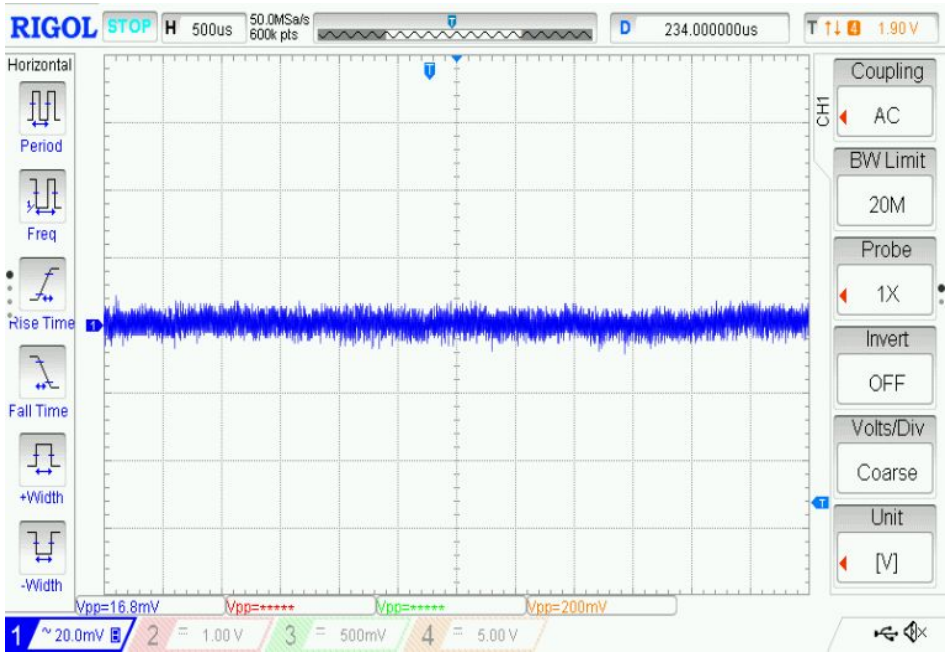
Vout = 3.3 V
Transient 0.15 A – 1.5A @ 2.5 A/µs
V_{PP} = 94 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

Ripple



No Load
V_{PP} = 18.4 mV

Vout = 3.3 V



1.5 A Load
V_{PP} = 16.8 mV

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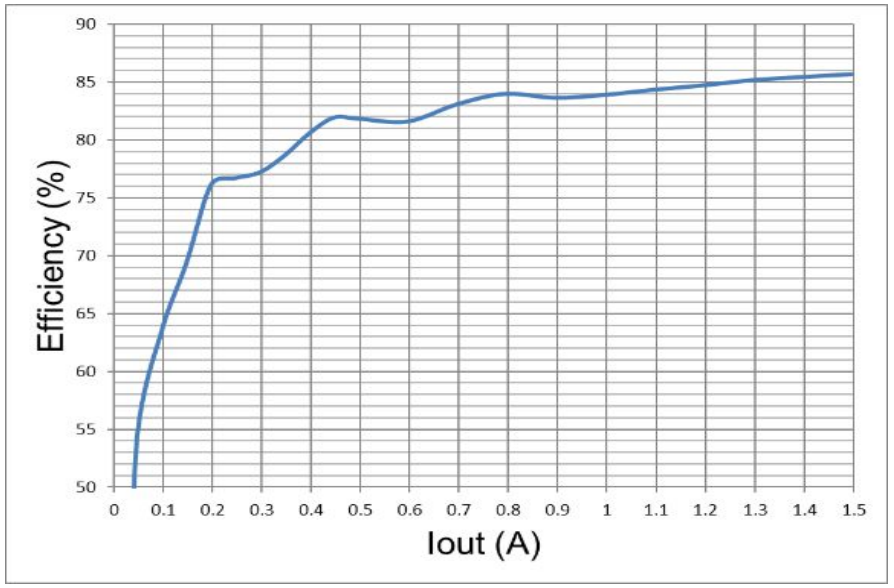
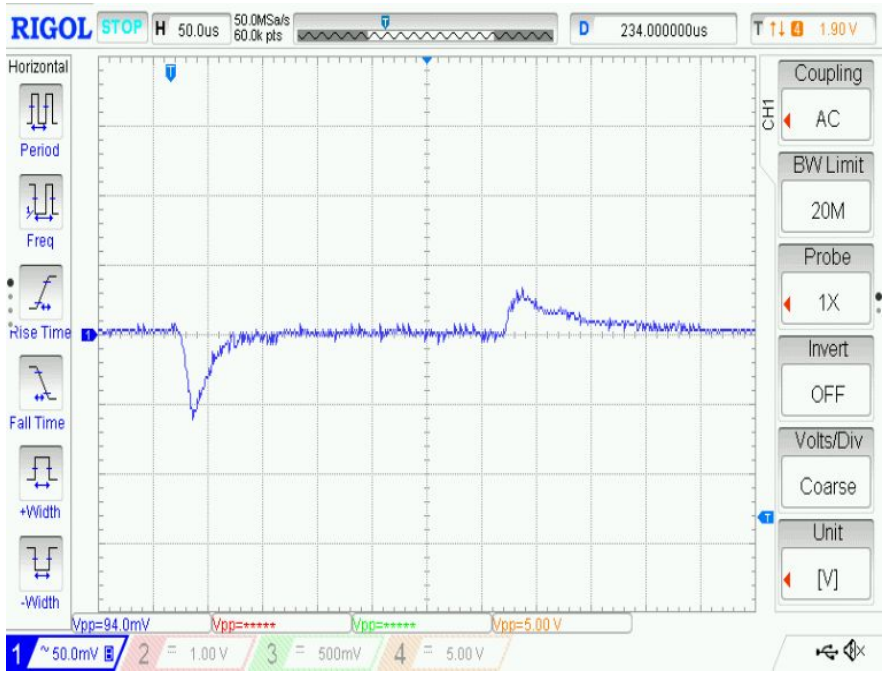
VCCO_PS
3.3 V / 2 A

- C150 Asynch Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient

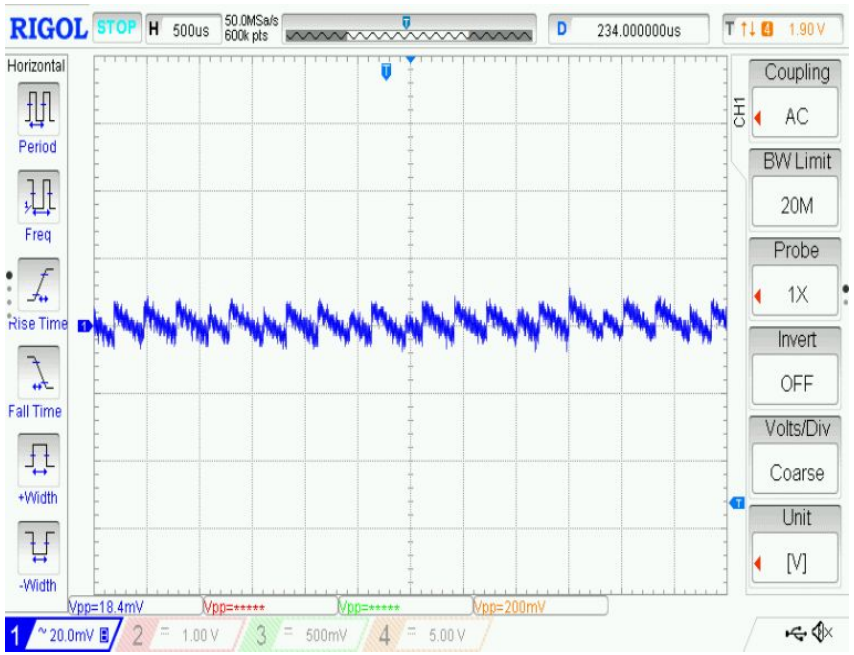


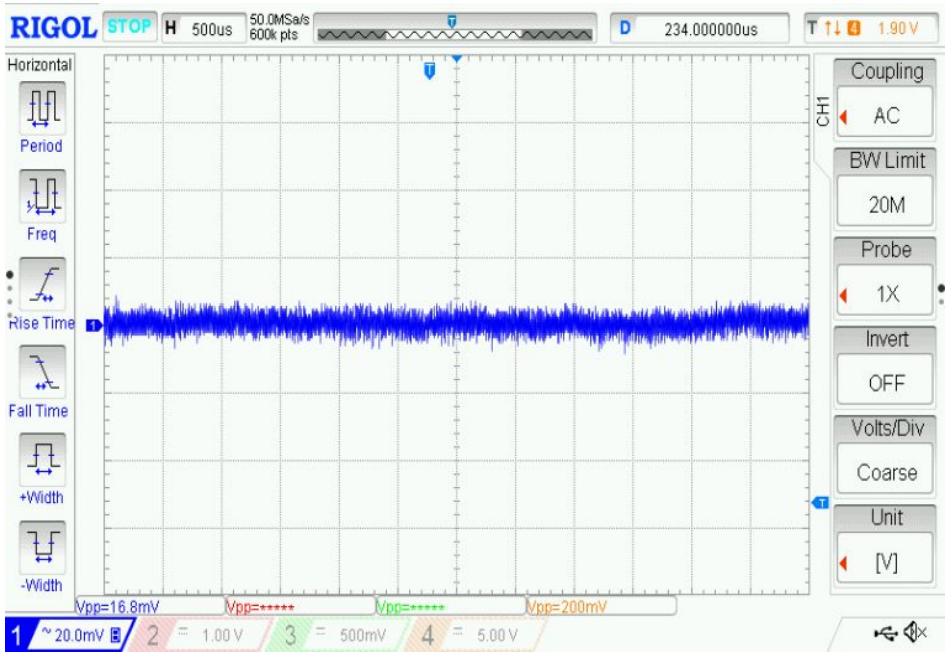


Vout = 3.3 V
Transient 0.15 A – 1.5A @ 2.5 A/µs
V_{PP} = 94 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

AnDAPT

Ripple





No Load
V_{PP} = 18.4 mV

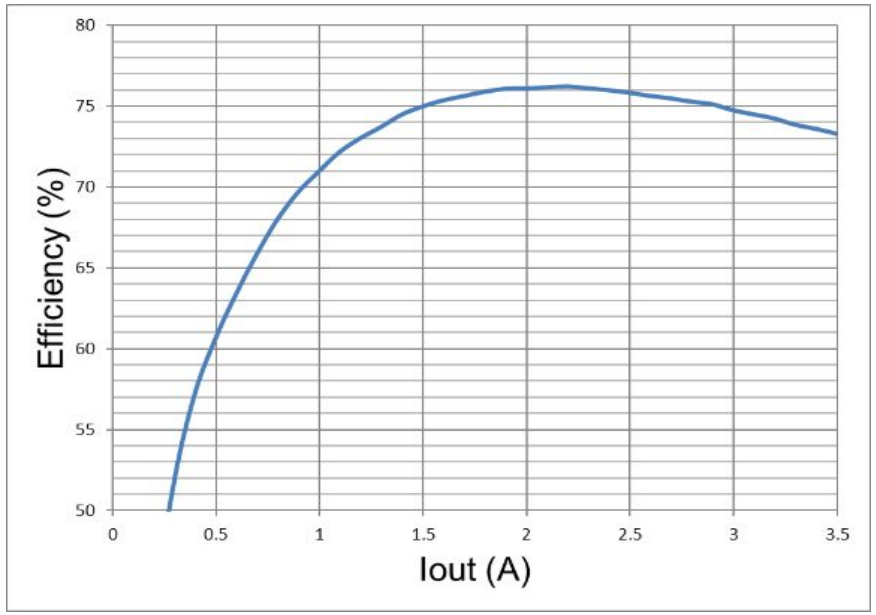
Vout = 3.3 V

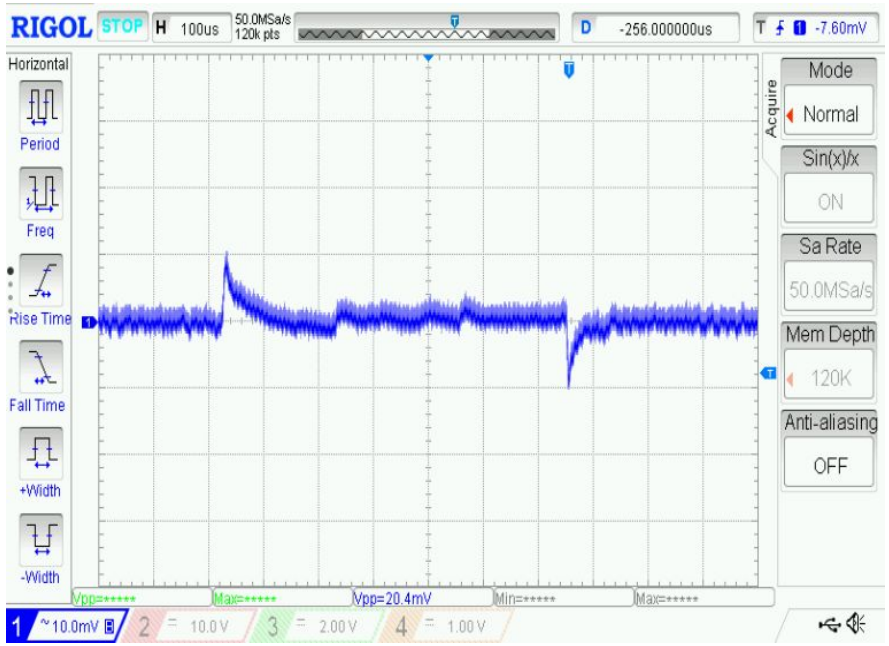
1.5 A Load
V_{PP} = 16.8 mV

VTTDDR
0.75 V / 3 A

- C200 Synch Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

Efficiency & Transient

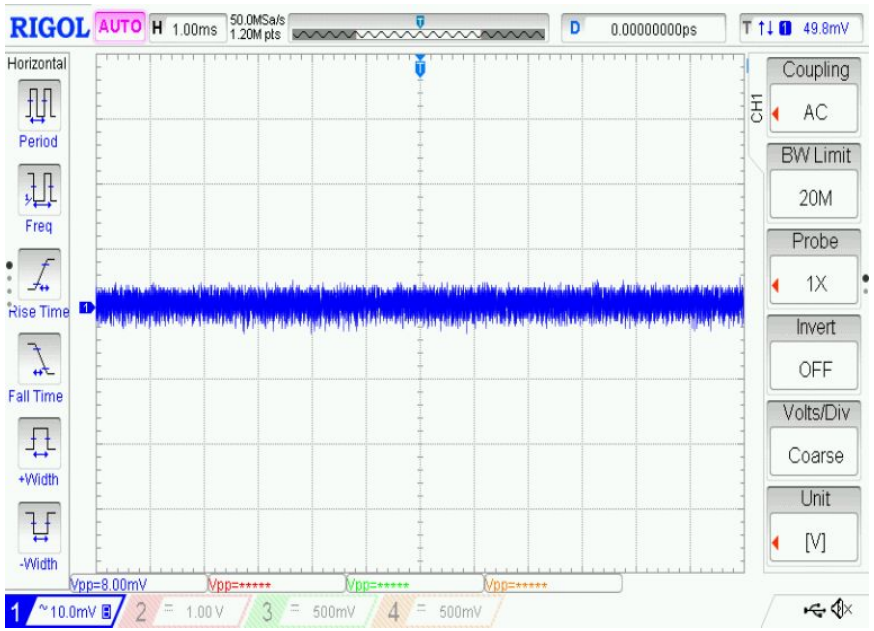




Vout = 0.75 V
Transient 2.625 A – 3.5A @ 100 A/µs
V_{PP} = 20.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

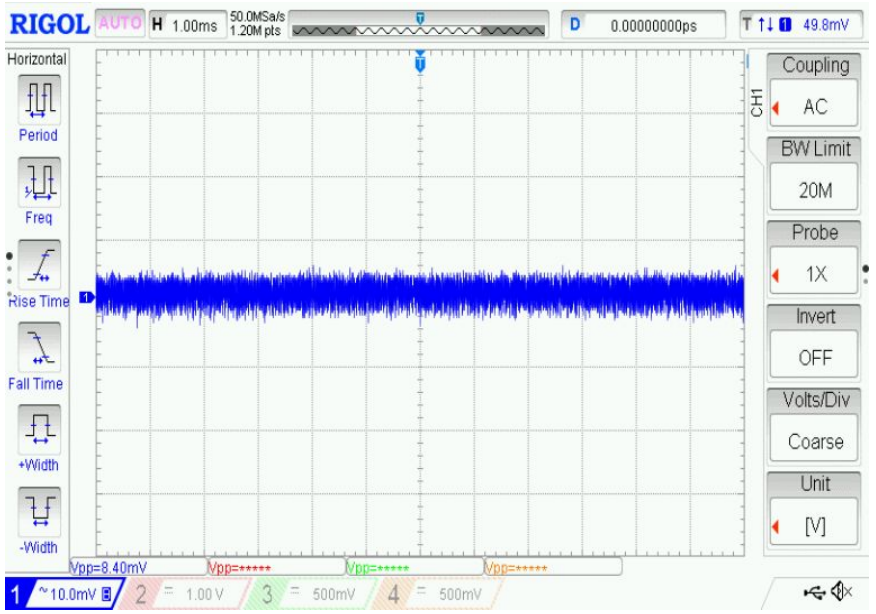
AnDAPT

Ripple



No Load
V_{PP} = 8 mV

Vout = 0.75 V



3 A Load
V_{PP} = 8.40 mV

AnDAPT

MGTVCCAUX
1.8 V / 0.12 A

- C750 Load Switch

Thank You

AnDAPT