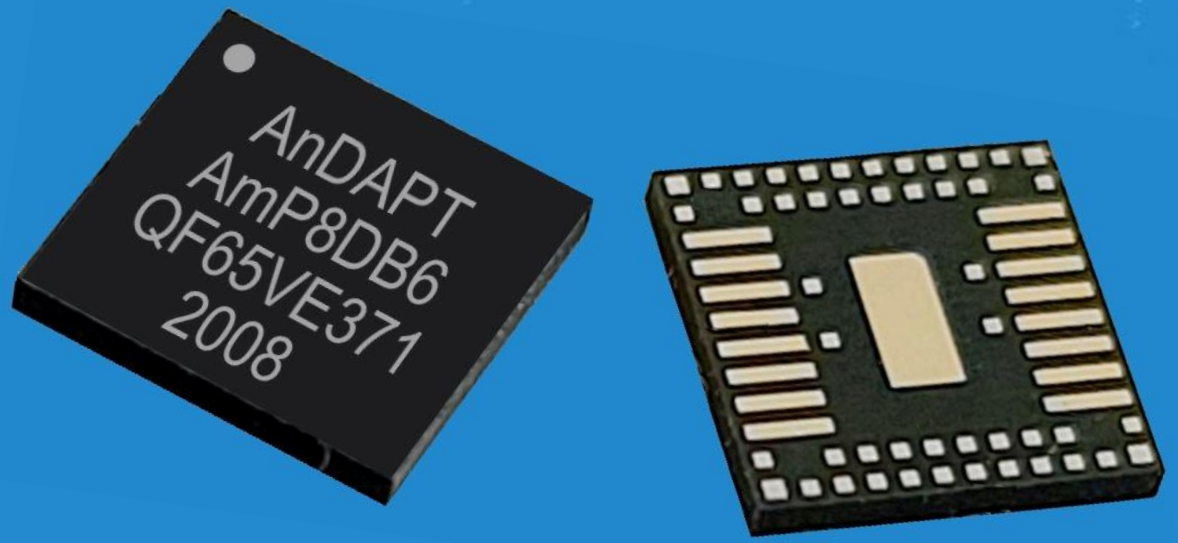

AnDAPT Power Solutions for Xilinx

Zynq 7000 (No MGT)

Mapping & Test Data

AnDAPT Marketing Team

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Contents

- Xilinx ZYNQ-7000(No MGT)+ family of devices SKUs in cost-optimized portfolio
- ZYNQ-7000(No MGT)+ power maps
- Bench data including efficiency, transients, ripple (no load and full-load) for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for ZYNQ-7000 (No MGT)+ family FPGAs
- Total solution area is 710.25 mm^2
- Presentation contains thermal view of the IC.

Zynq 7000 (No MGT)Device SKUs Covered

Supported SKUs
XC7Z007S
XC7Z014S
XC7Z010
XC7Z020

Power Tree: ZYNQ-7000 (No MGT Devices)

PVIN = 12 V

#	Rail	Seq	Vout (V)	Iout (A)
1	VCCINT, VCCBRAM, VCCPINT	1	0.95/1	6
2	VCCAUX, VCCPAUX, VCCPLL, VCCADC	2	1.8	0.8
3	VCC_IO	3	1.8	1.5
4	VCC_DDR	4	1.35/1.5	3+2
5	DDR_VTT	5	VCC_DDR/2	2

Power Tree Mapping

PVIN = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRAM, VCCPINT	1	C150	Async Buck	PVIN	12	0.95/1	6	ARD_X_Z70_A3_IC1
2	VBUS	1	C150	Async Buck	PVIN	12	2.5	0.8 + 1.5	
3	VCCAUX, VCCPAUX, VCCPLL, VCCADC	2	C710	LDO	VBUS	2.5	1.8	0.8	
4	VCC_IO	3	C710	LDO	VBUS	2.5	1.8	1.5	
5	VCC_DDR	4	C200	Sync Buck	PVIN	12	1.35/1.5	3	
6	DDR_VTT	5	C210	Terminator	VCC_DDR	1.5	0.75	2	

Estimated solution area = 710.25mm^2

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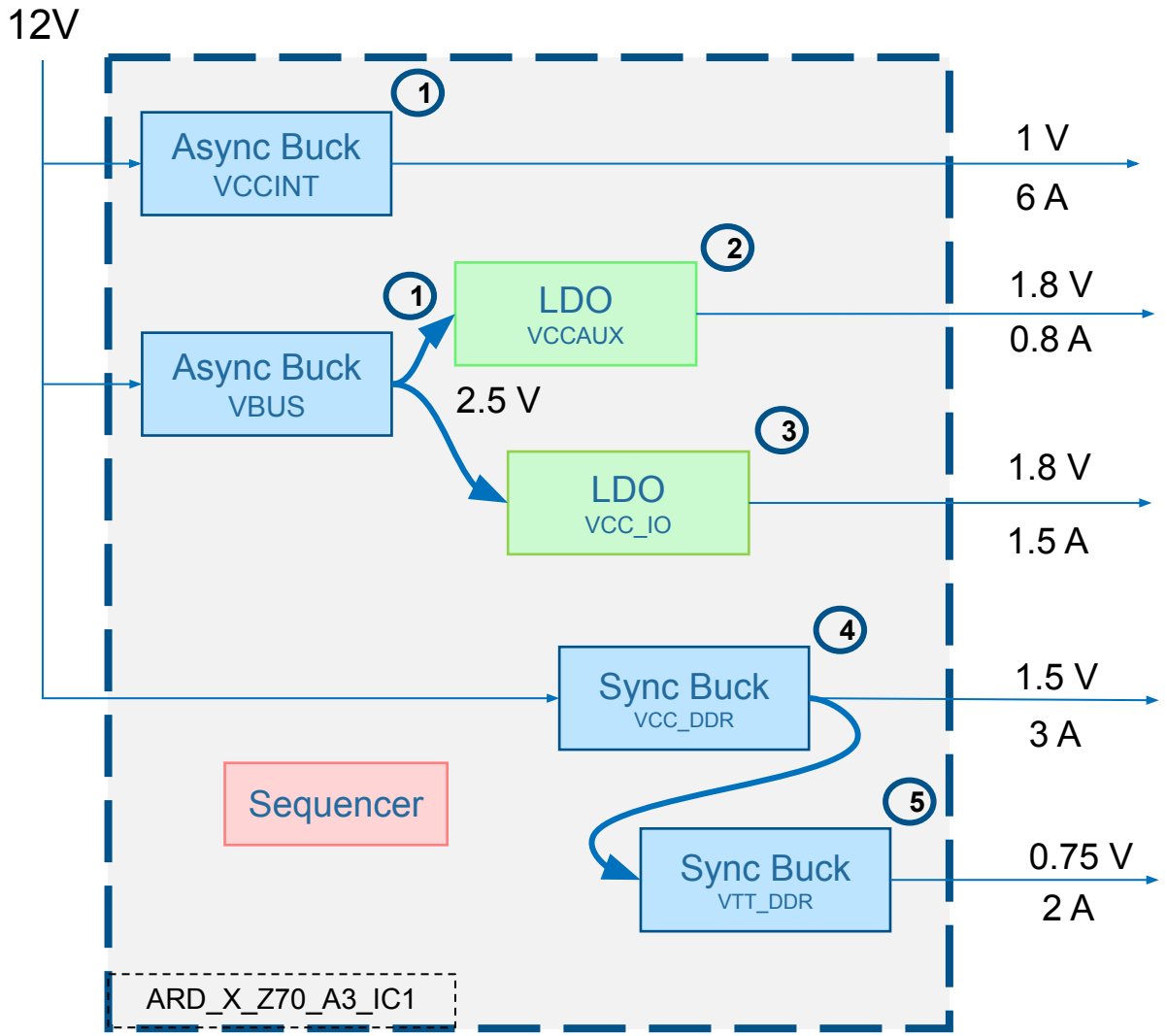
Proposed Solution (1xPMIC)



Estimated solution area = 710.25 mm^2

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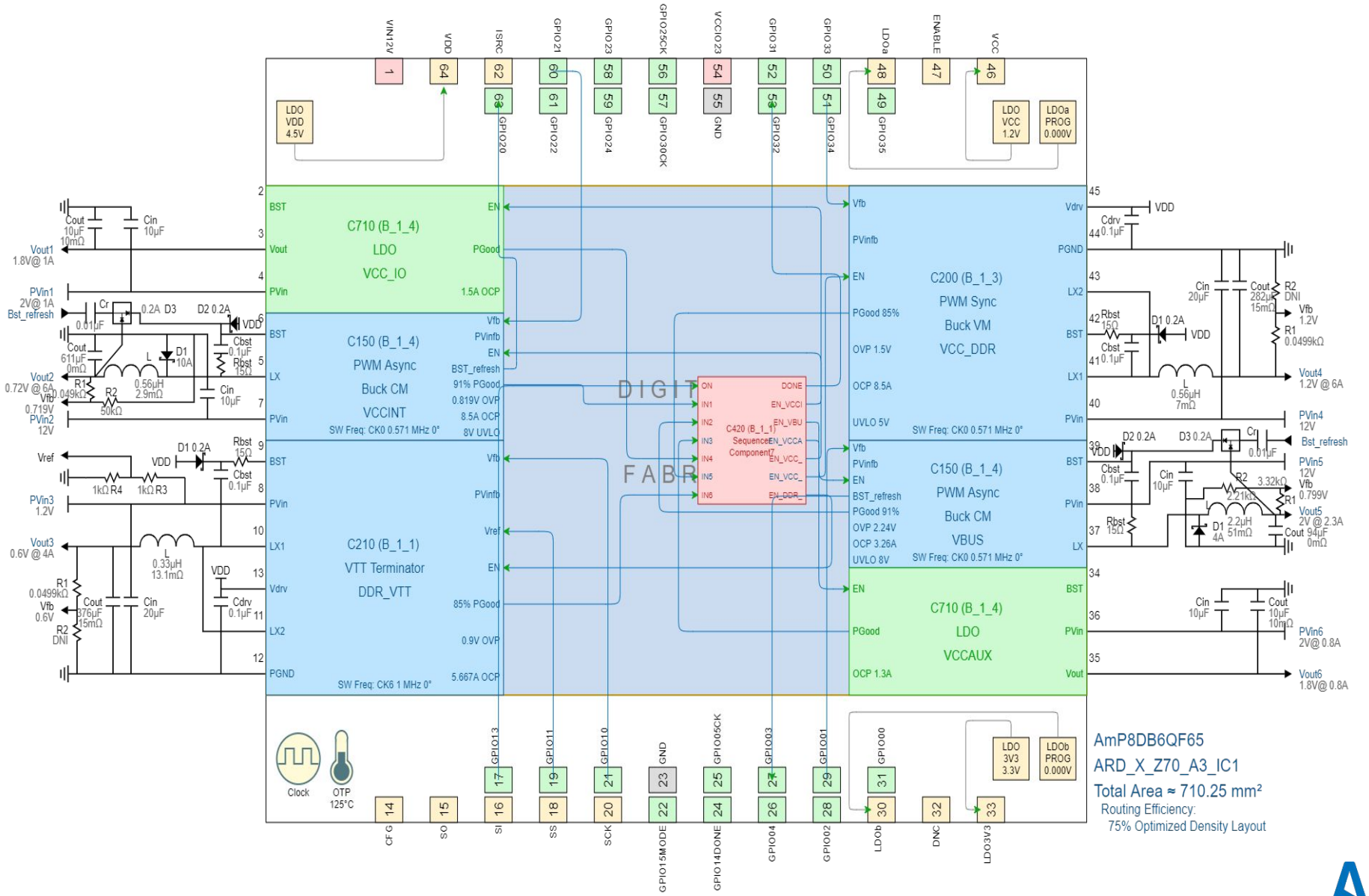
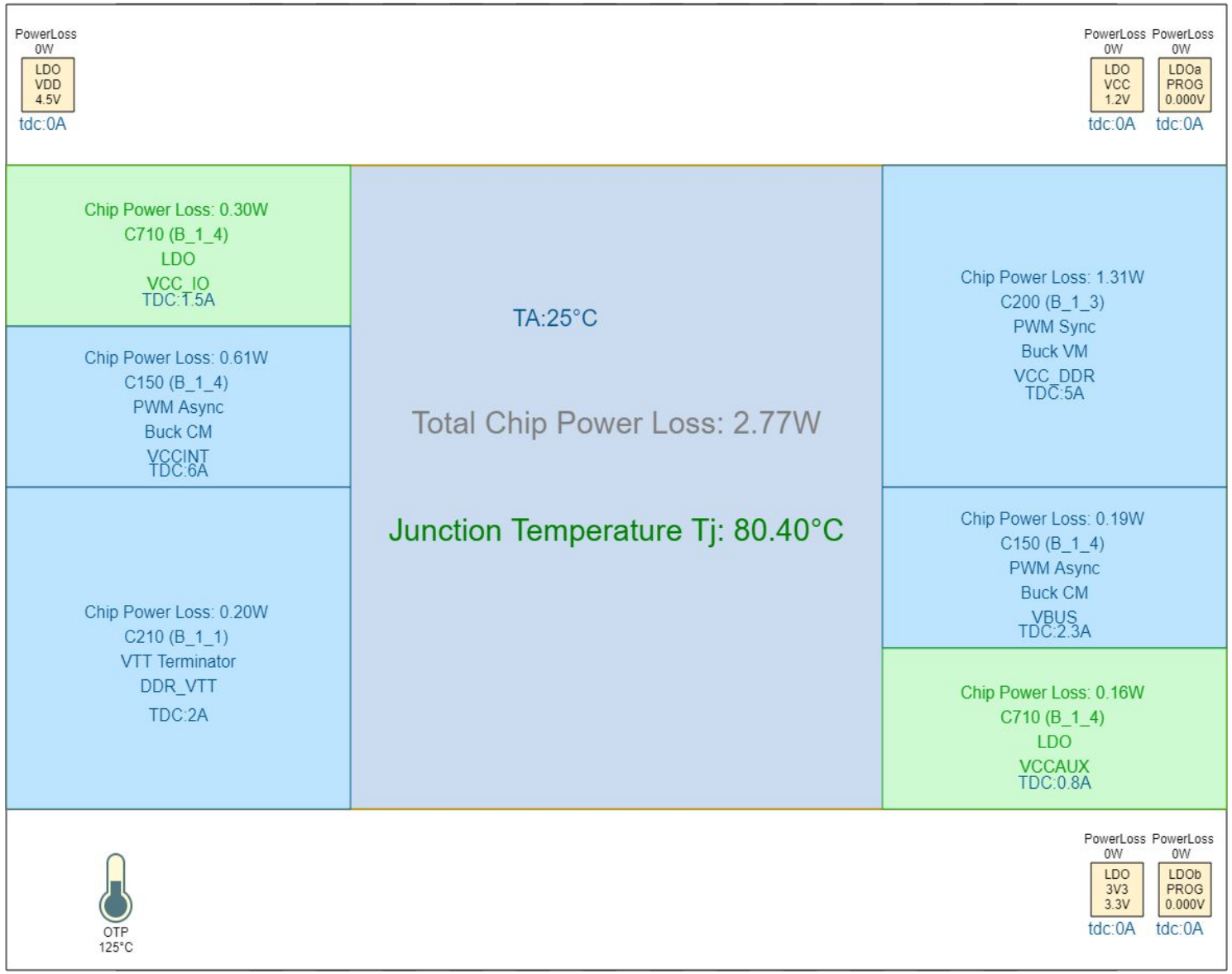
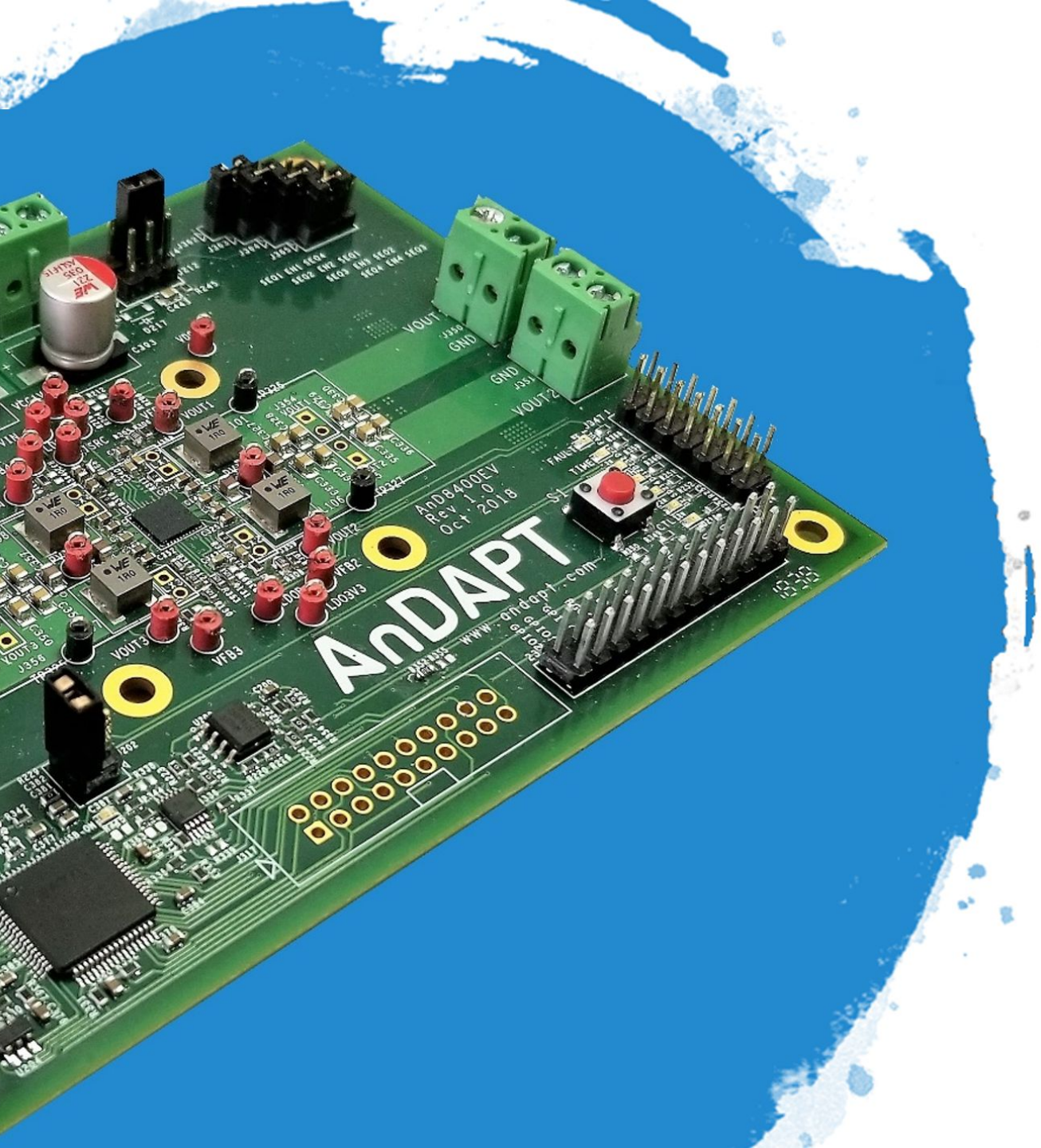
Mapping (WebAmP View)



Thermal Design View



AmP8DB6QF65
ARD_X_Z70_A3_IC1
Total Area ≈ 710.25 mm²
Routing Efficiency:
75% Optimized Density Layout



Test Data

ZYNQ-7000 (No MGT)

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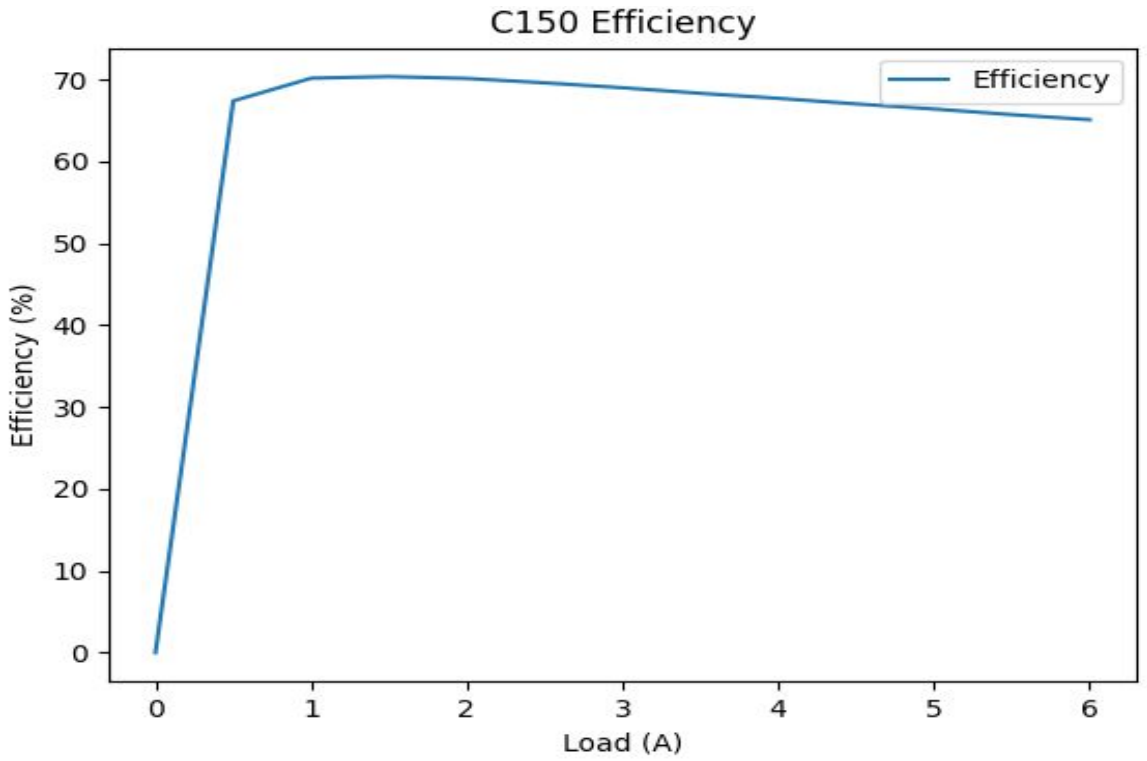
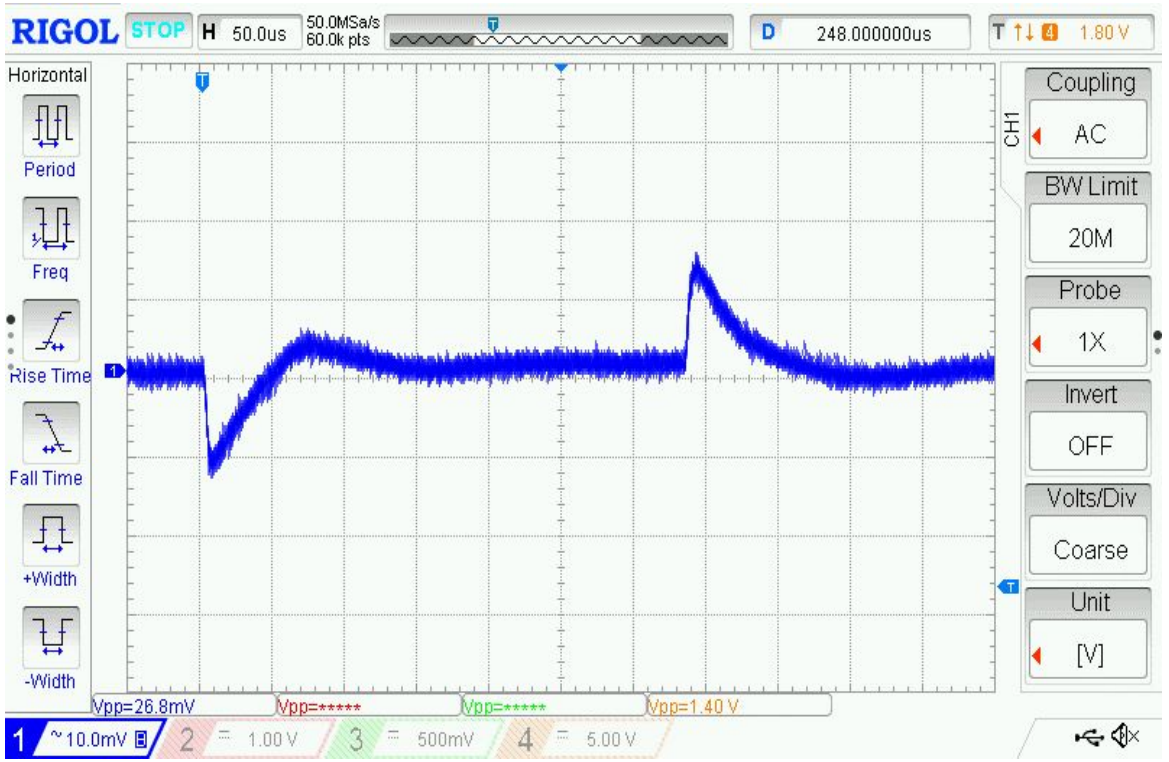
VCCINT
0.95 V / 6 A

- C150 (Async Buck)
- Fsw = 571 kHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 611 uF

Efficiency & Transient





Vout = 0.95 V
Transient 4.5A – 6A @ 100 A/µs
V_{PP} = 26.8 mV
Fsw = 571 kHz
Lout = 0.56 µH, Cout = 13 x 47 µF

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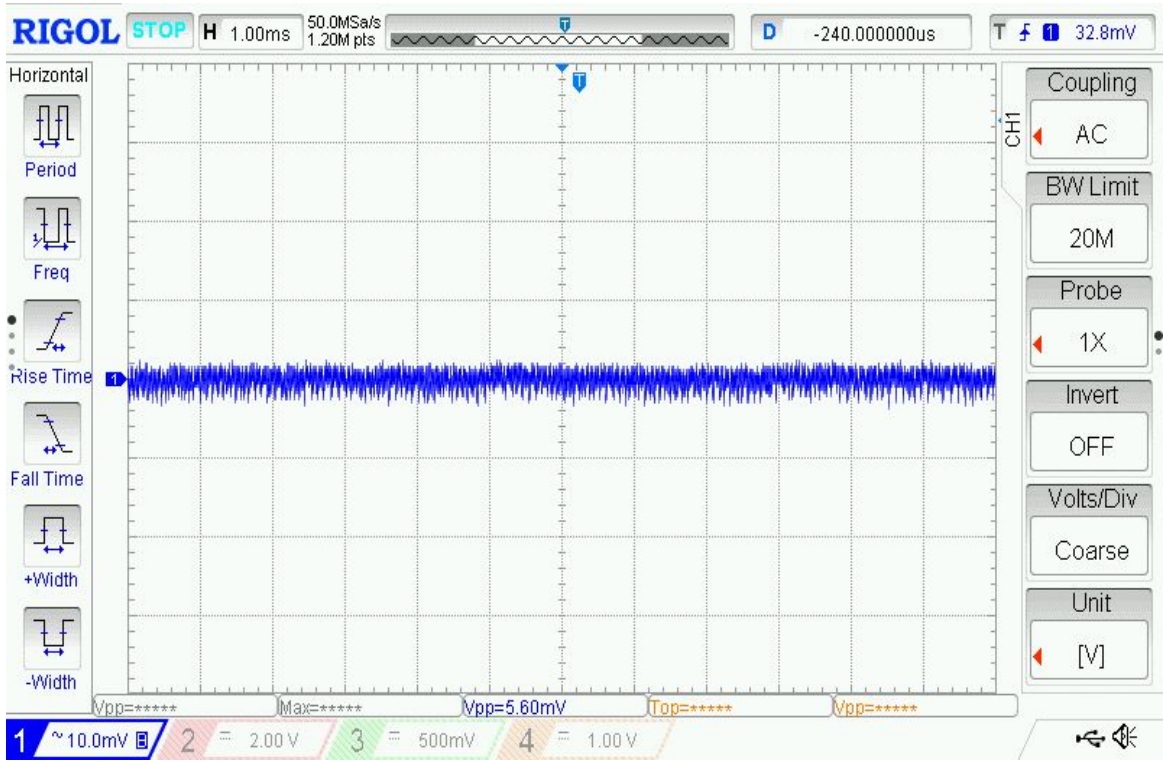
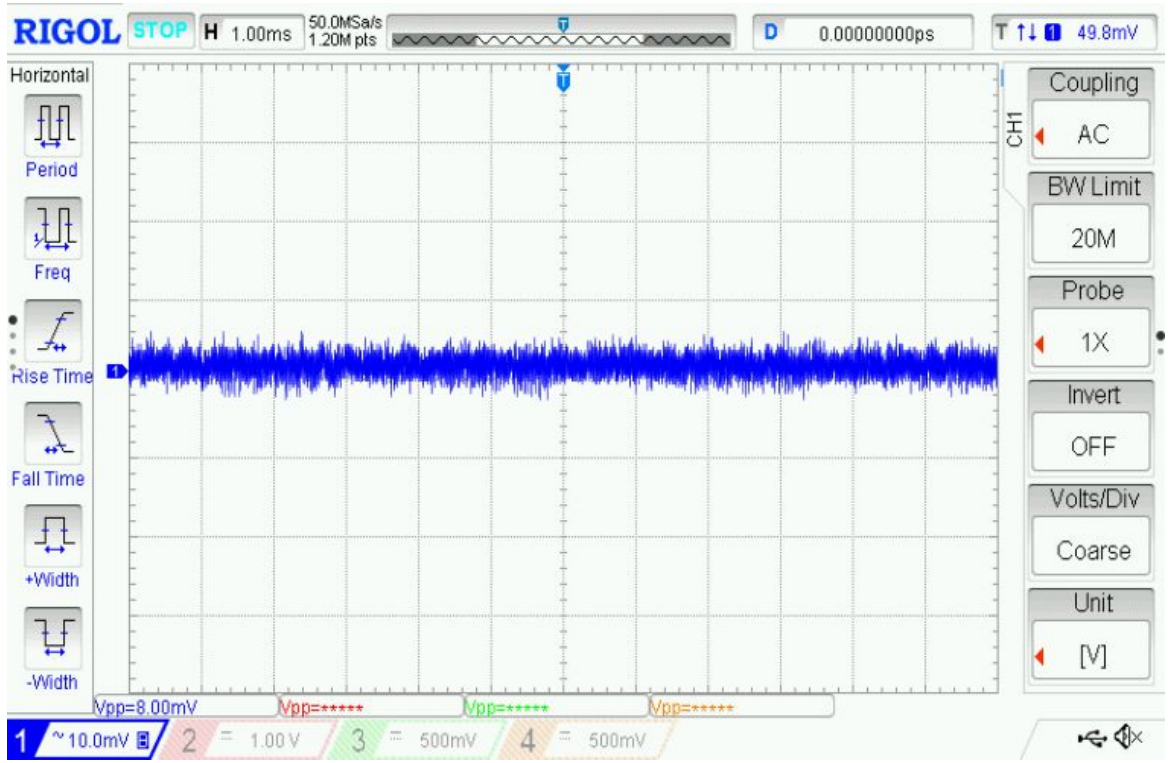
Ripple





No Load
V_{PP} = 5.6 mV

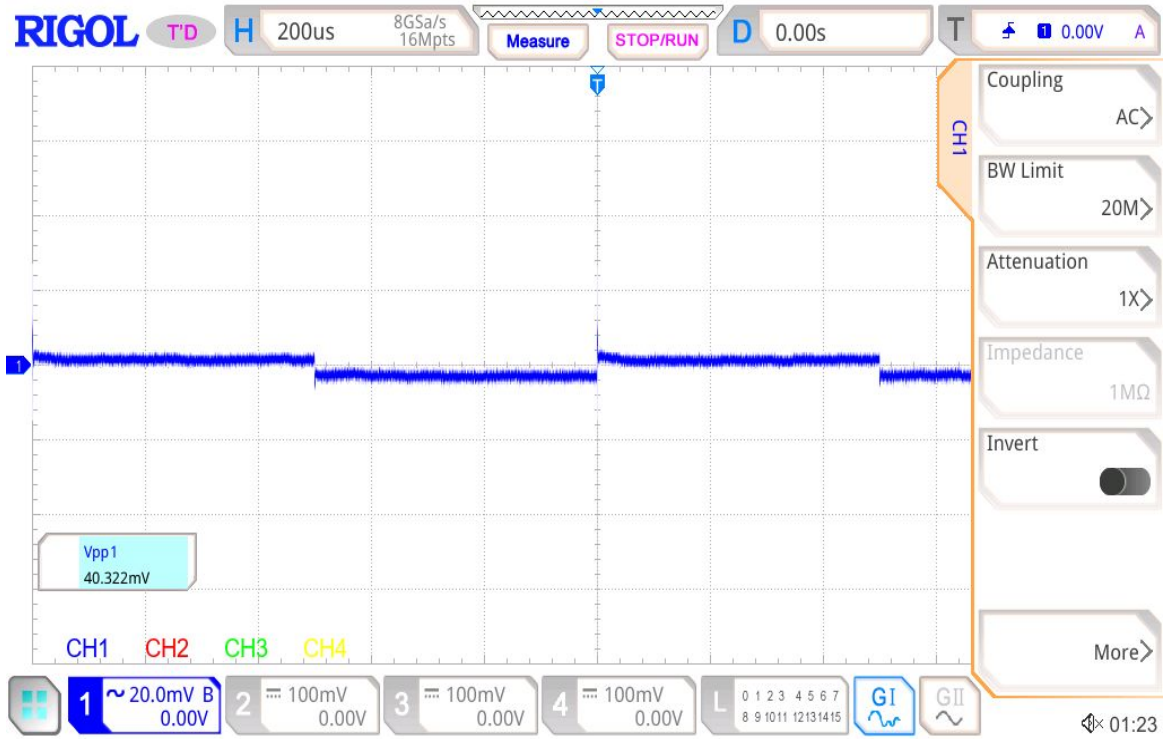
Vout = 0.95 V

6 A Load
V_{PP} = 8 mV

VCCAUX
1.8 V / 0.8 A

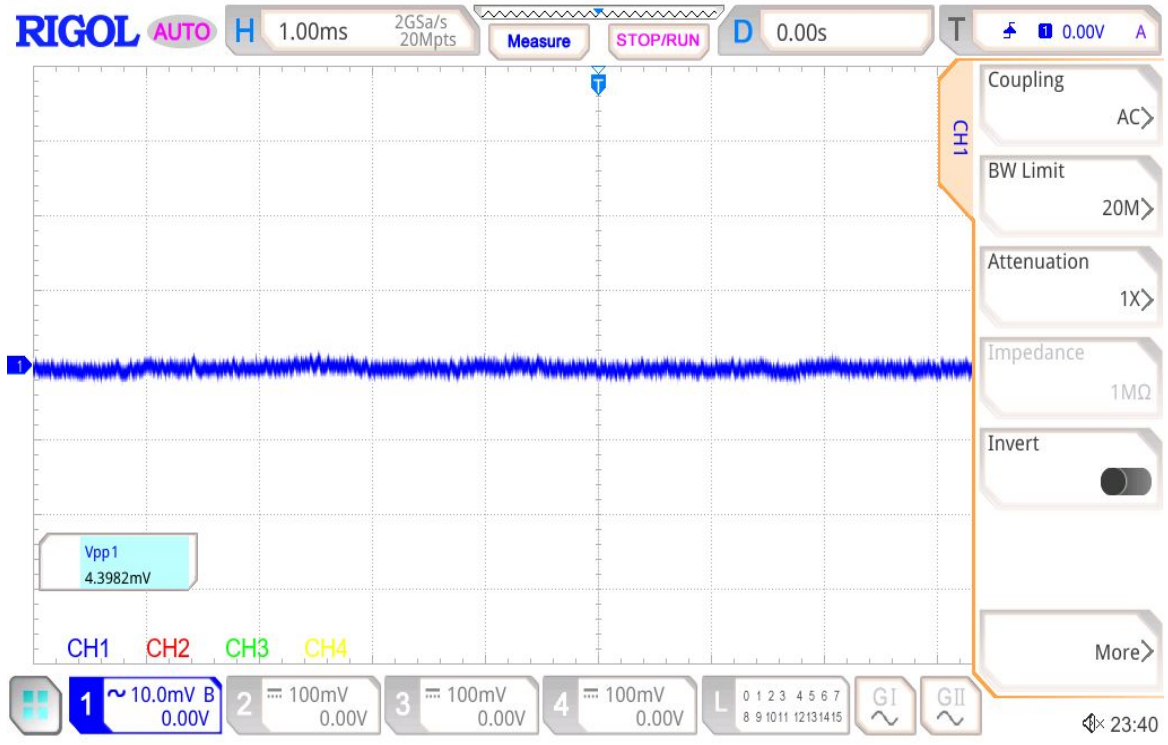
- C710 (LDO)

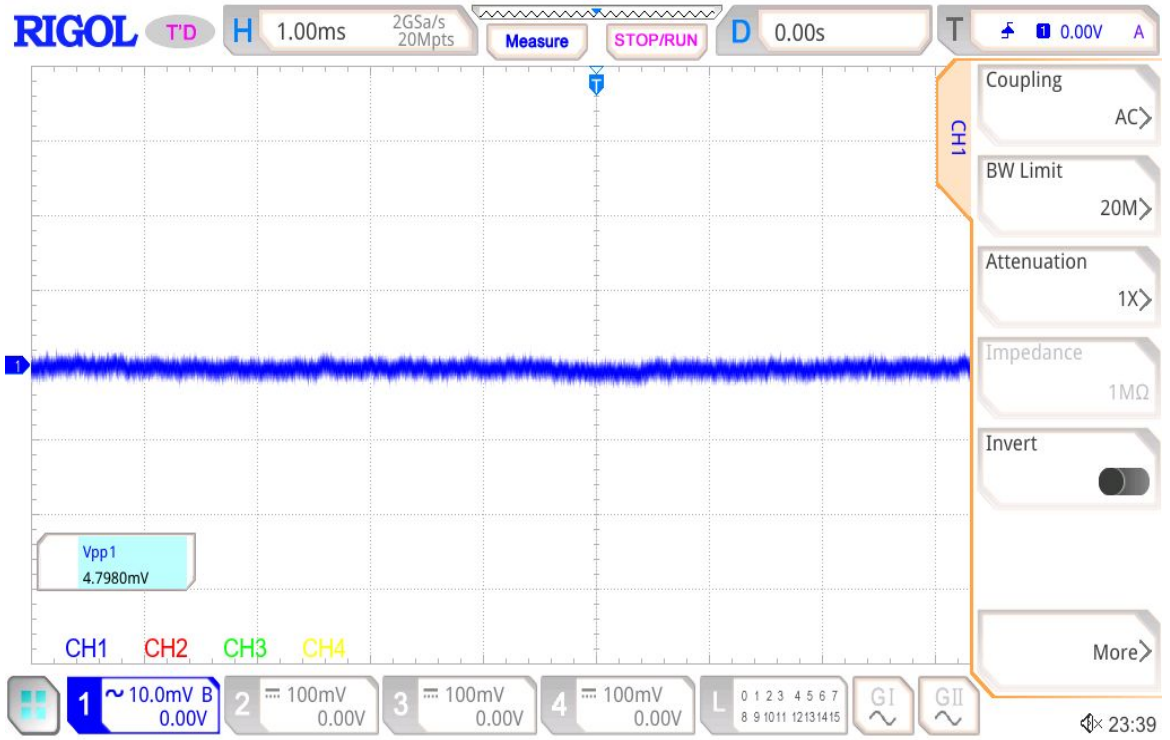
Transient



Vout = 1.8 V
Transient 0.6A – 0.8A @ 10 A/µs
V_{PP} = 40.32 mV

Ripple





No Load
V_{PP} = 4.39 mV

Vout = 1.8 V

0.8 A Load
V_{PP} = 4.79 mV

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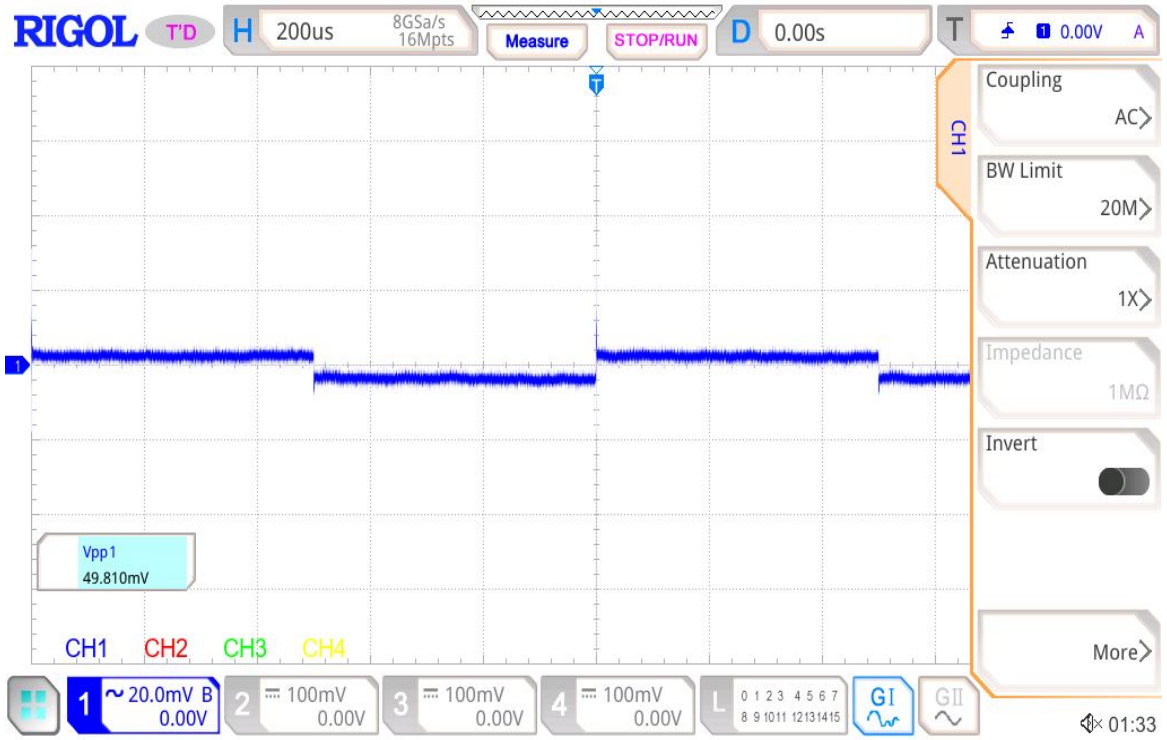
VCC_IO
1.8 V / 1.5 A

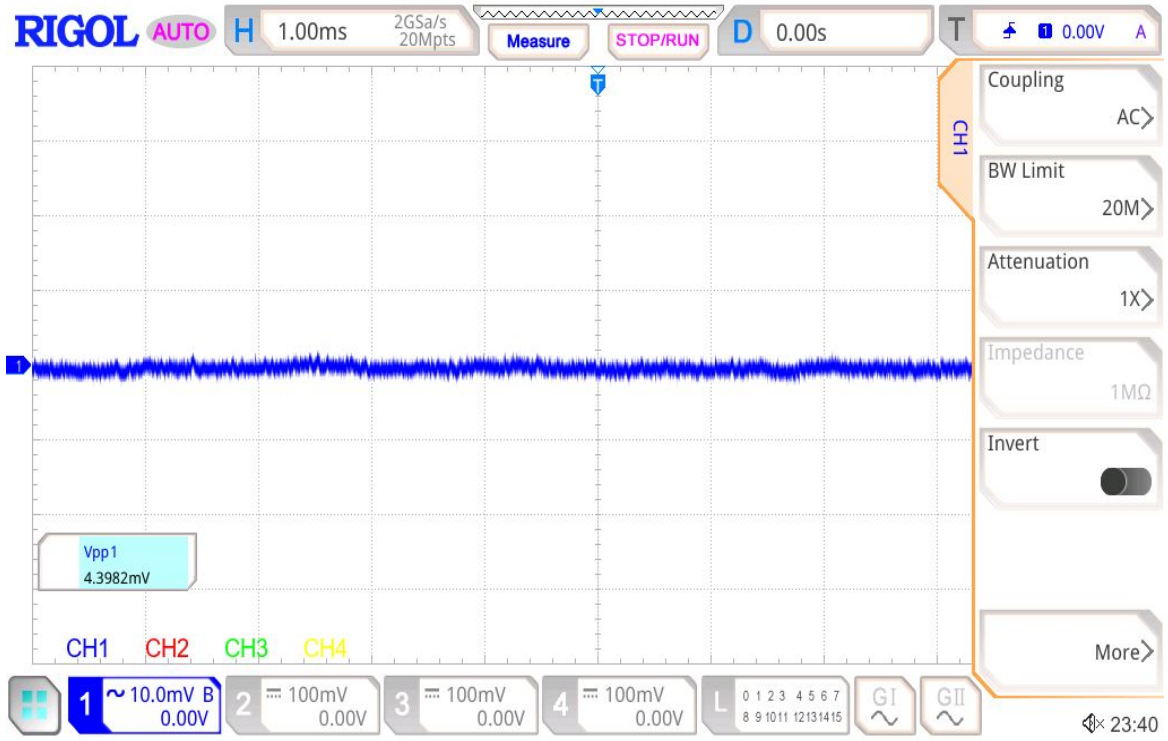
- C710 (LDO)

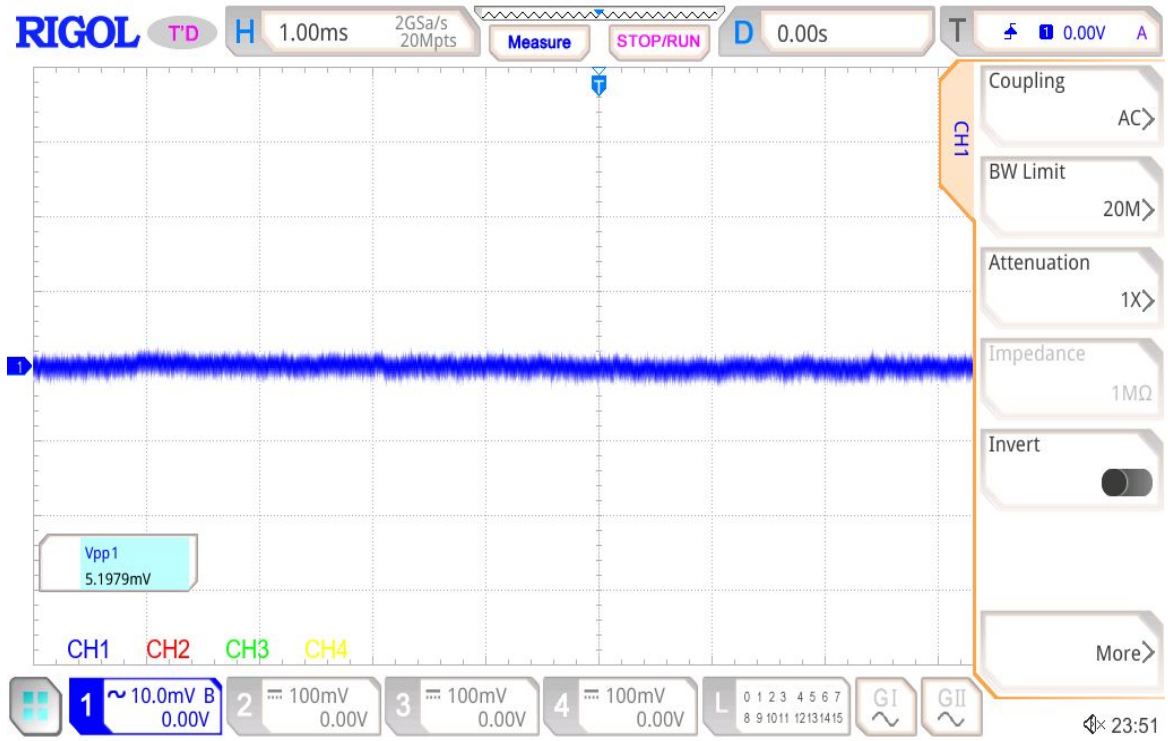
Transient



Vout = 1.8 V
Transient 1.125A – 1.5A @ 10 A/µs
V_{PP} = 49.81 mV

Ripple





No Load
V_{PP} = 4.39 mV

Vout = 1.8 V

1.5 A Load
V_{PP} = 5.19 mV

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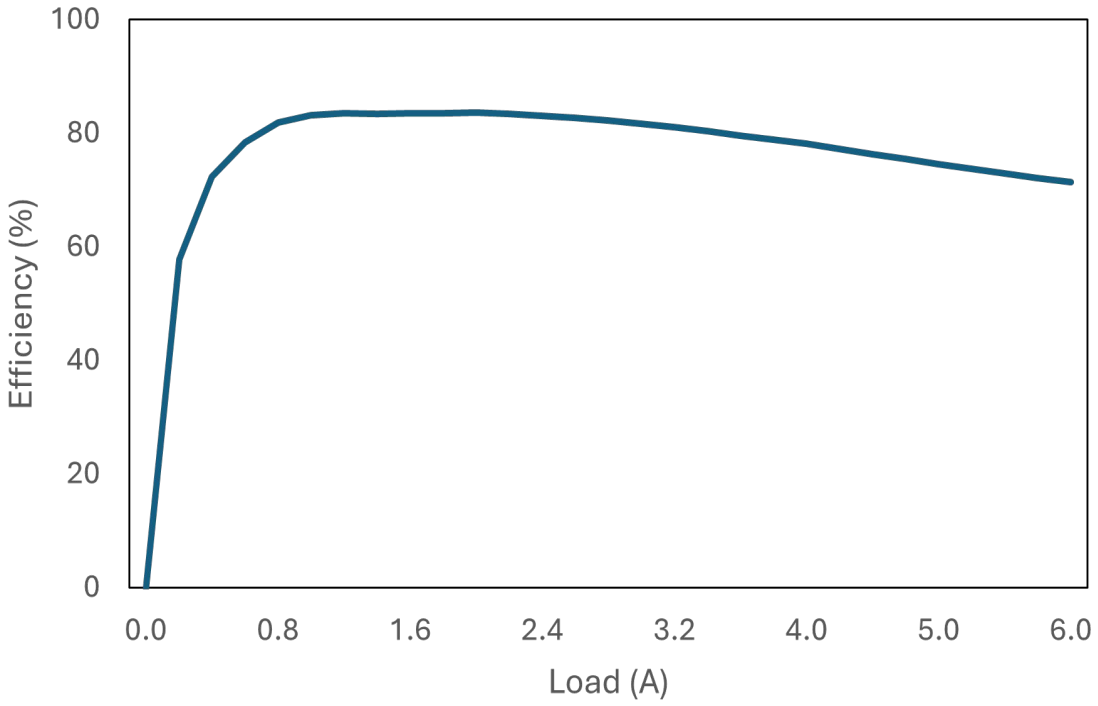
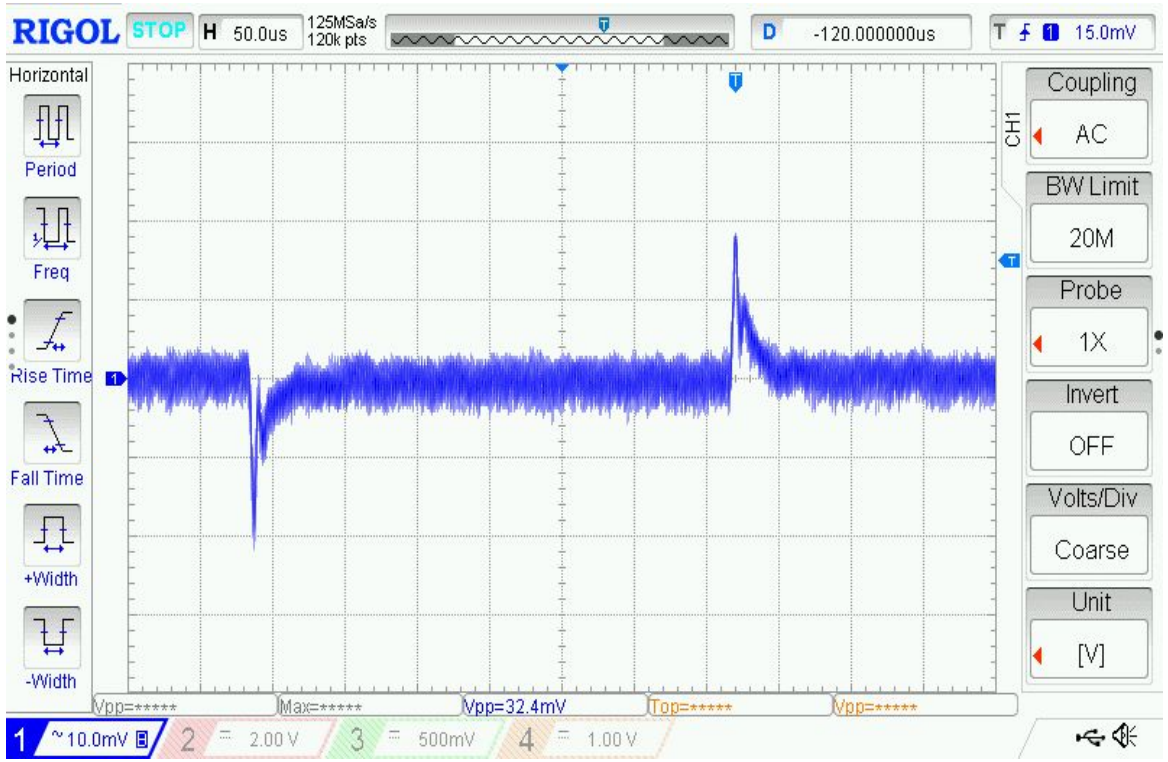
VCC_DDR
1.2 V / 6 A

- C200 (Sync Buck)
- Fsw = 571 kHz
- L = 0.56 µH, P/N Wurth 744383560056
- C = 282 uF

Efficiency & Transient





Vout = 1.2 V
Transient 4.5A – 6A @ 10 A/µs
V_{PP} = 32.4 mV
Fsw = 571 kHz
Lout = 0.56 µH, Cout = 6 x 47 µF

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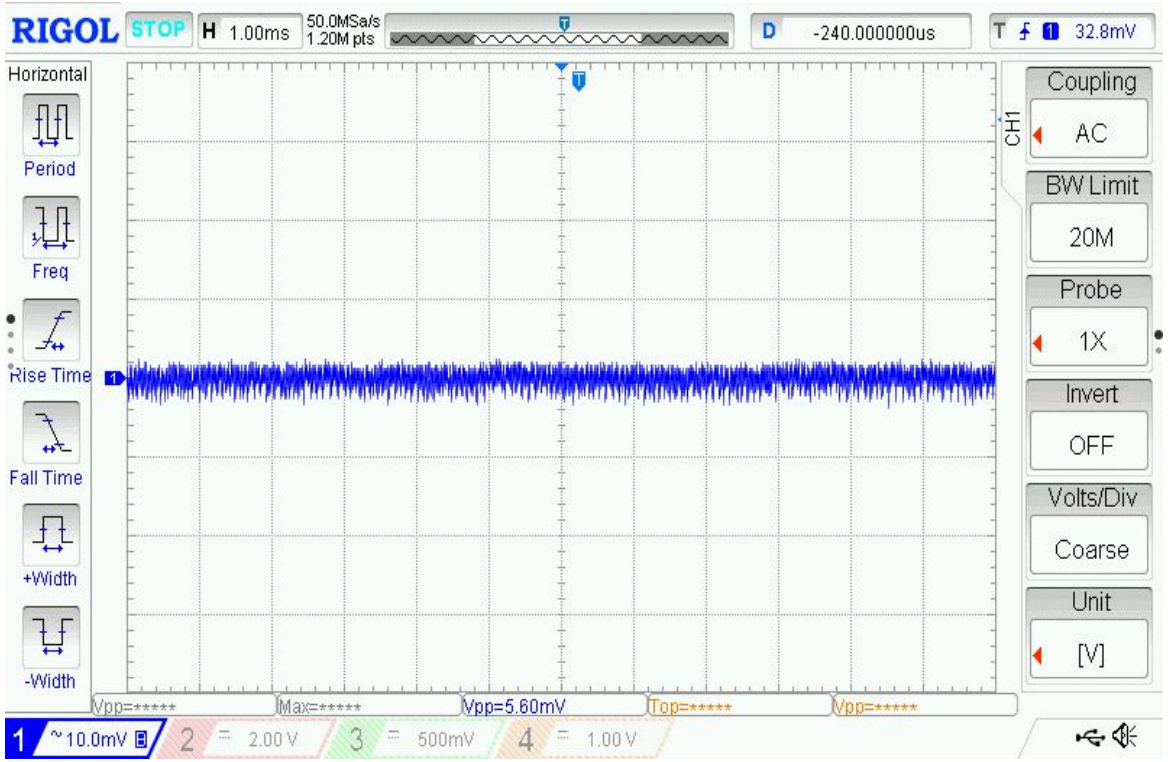
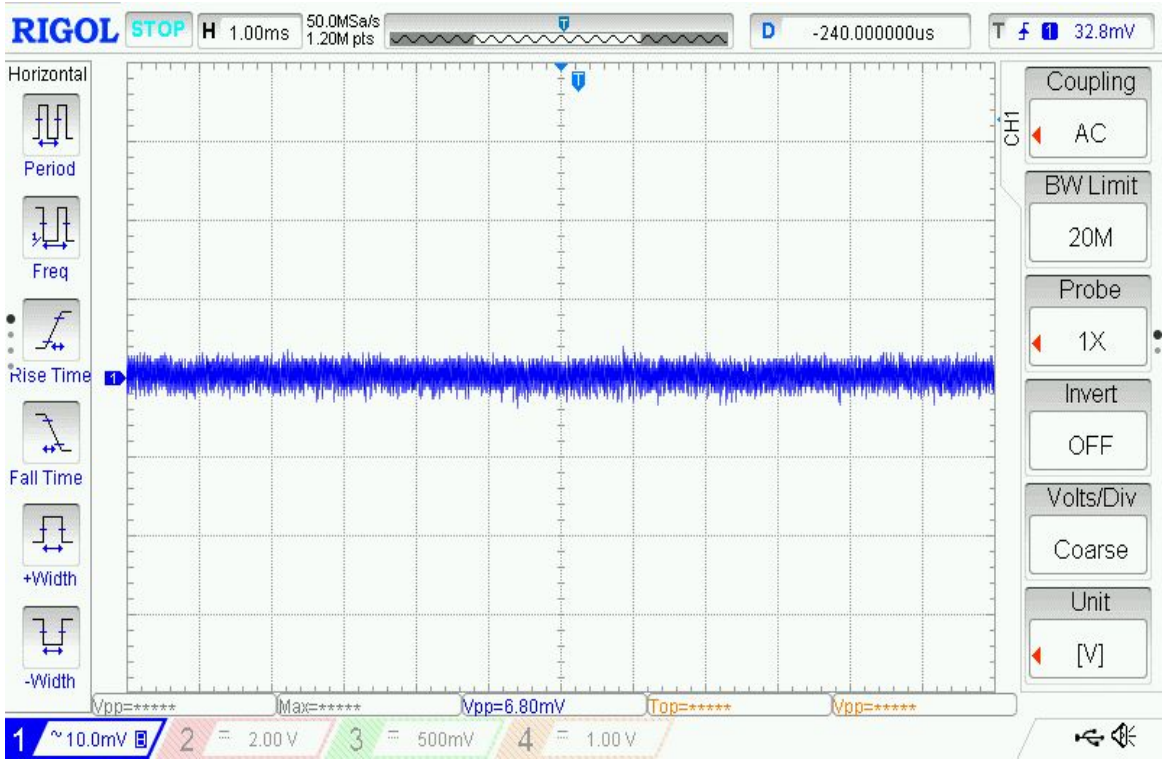
Ripple





No Load
V_{PP} = 5.60 mV

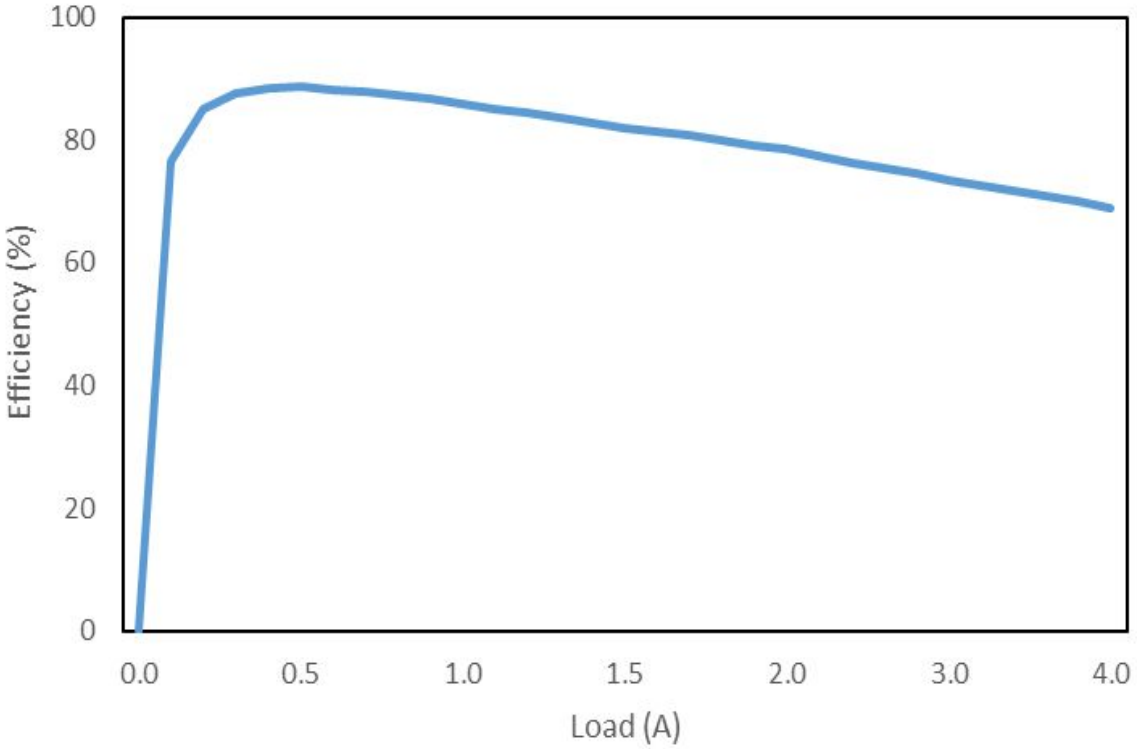
Vout = 1.2 V

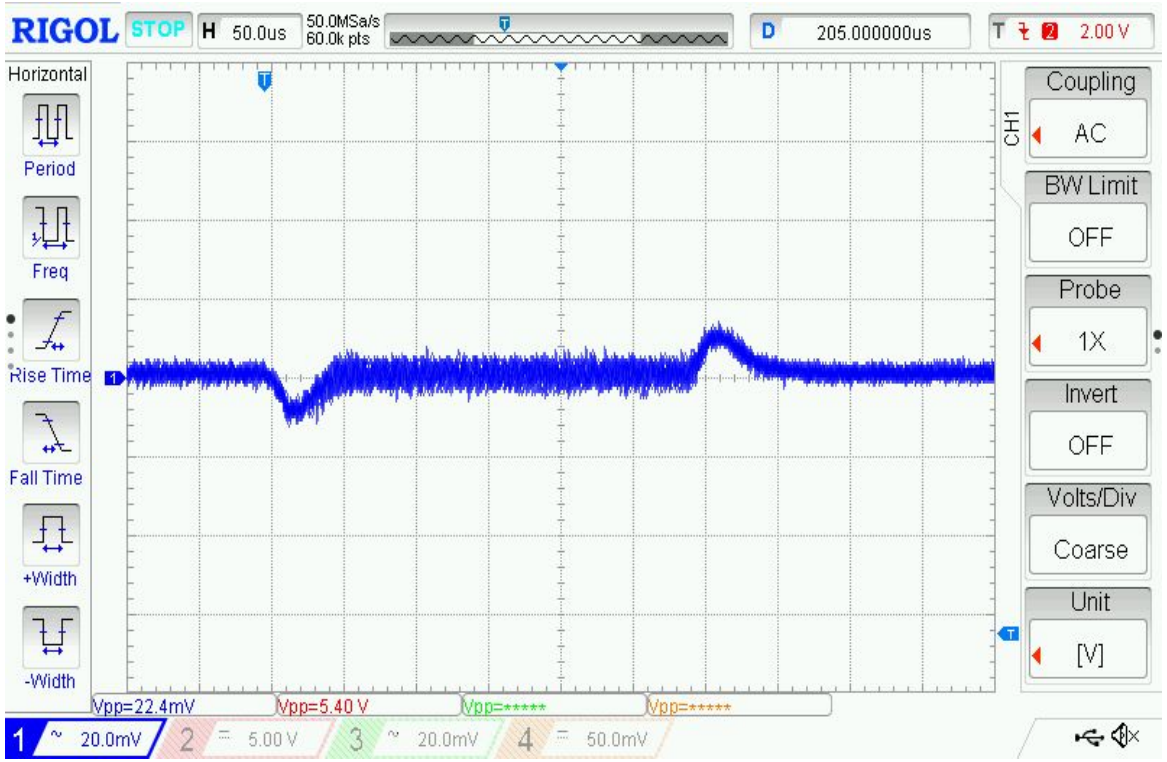
6 A Load
V_{PP} = 6.80 mV

DDR_VTT
0.6 V / 4 A

- C210 (VTT Terminator)
- Fsw = 1 MHz
- L = 0.33 µH, P/N Wurth 744393440033
- C = 8x47 uF

Efficiency & Transient





Vout = 0.6V
Transient 3 – 4A @ 10 A/µs
V_{PP} = 22.4 mV
Fsw = 1 MHz
L = 0.33 µH, C = 8x47 uF

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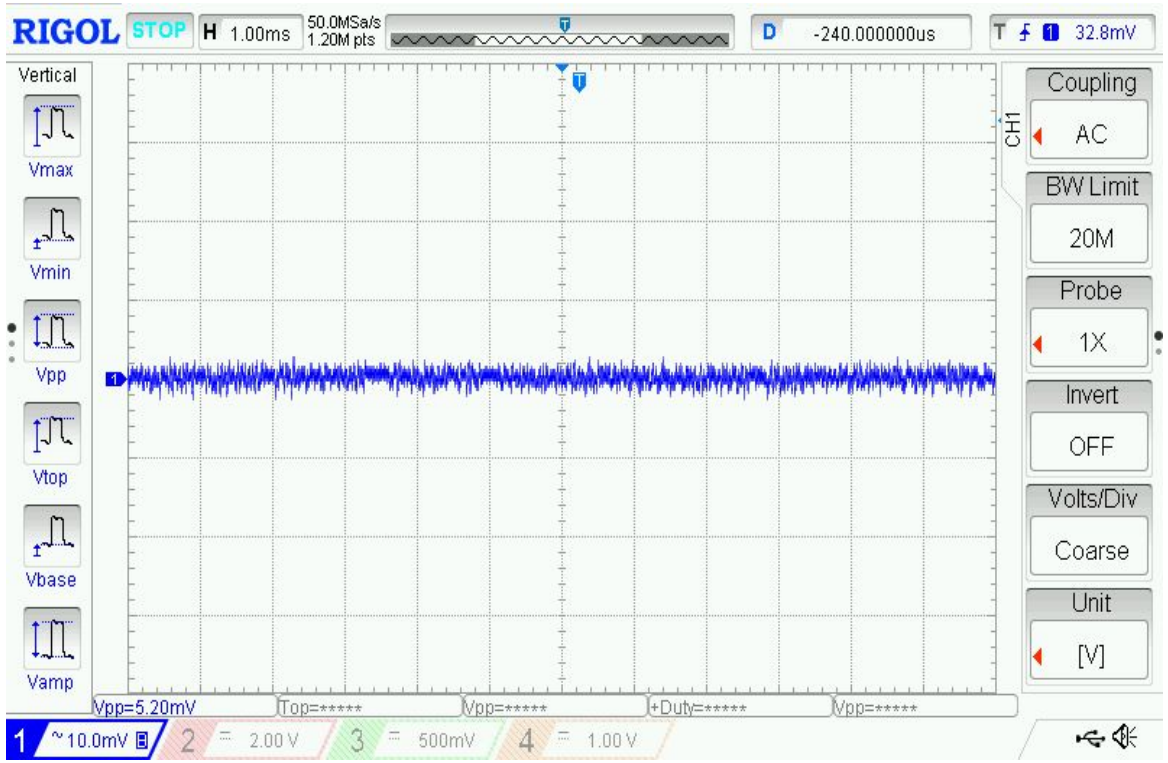
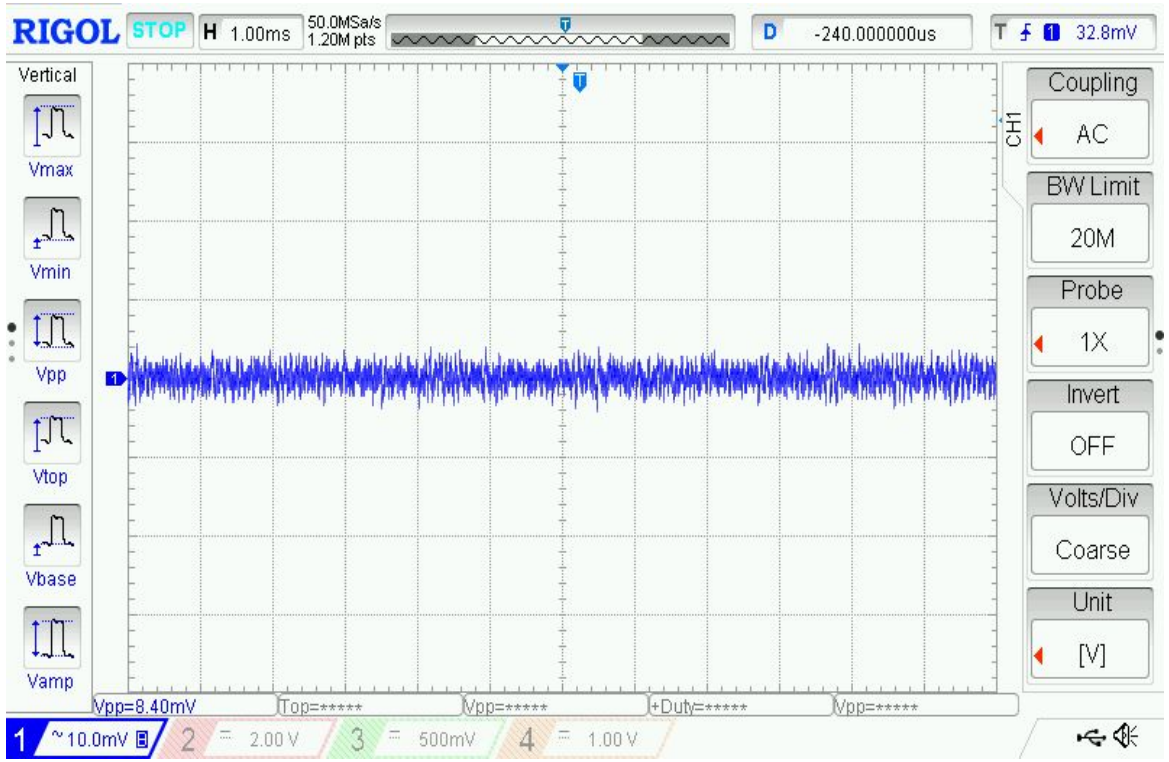
Ripple





No Load
V_{PP} = 5.20 mV

Vout = 0.6 V

4 A Load
V_{PP} = 8.40 mV

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Thank You

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