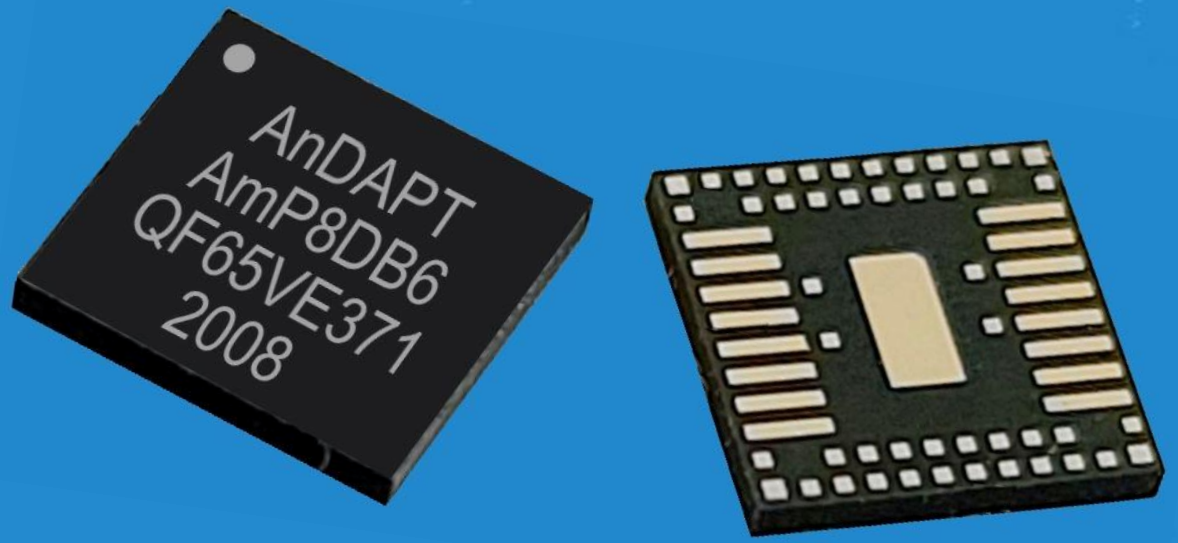


Zynq UltraScale+ (Minimum Rails) Cost-optimized Portfolio

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Zynq UltraScale+ (ZU+) family of devices SKUs (minimum rails/rail consolidation) in cost-optimized portfolio
- Zynq US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for ZU+ family FPGAs

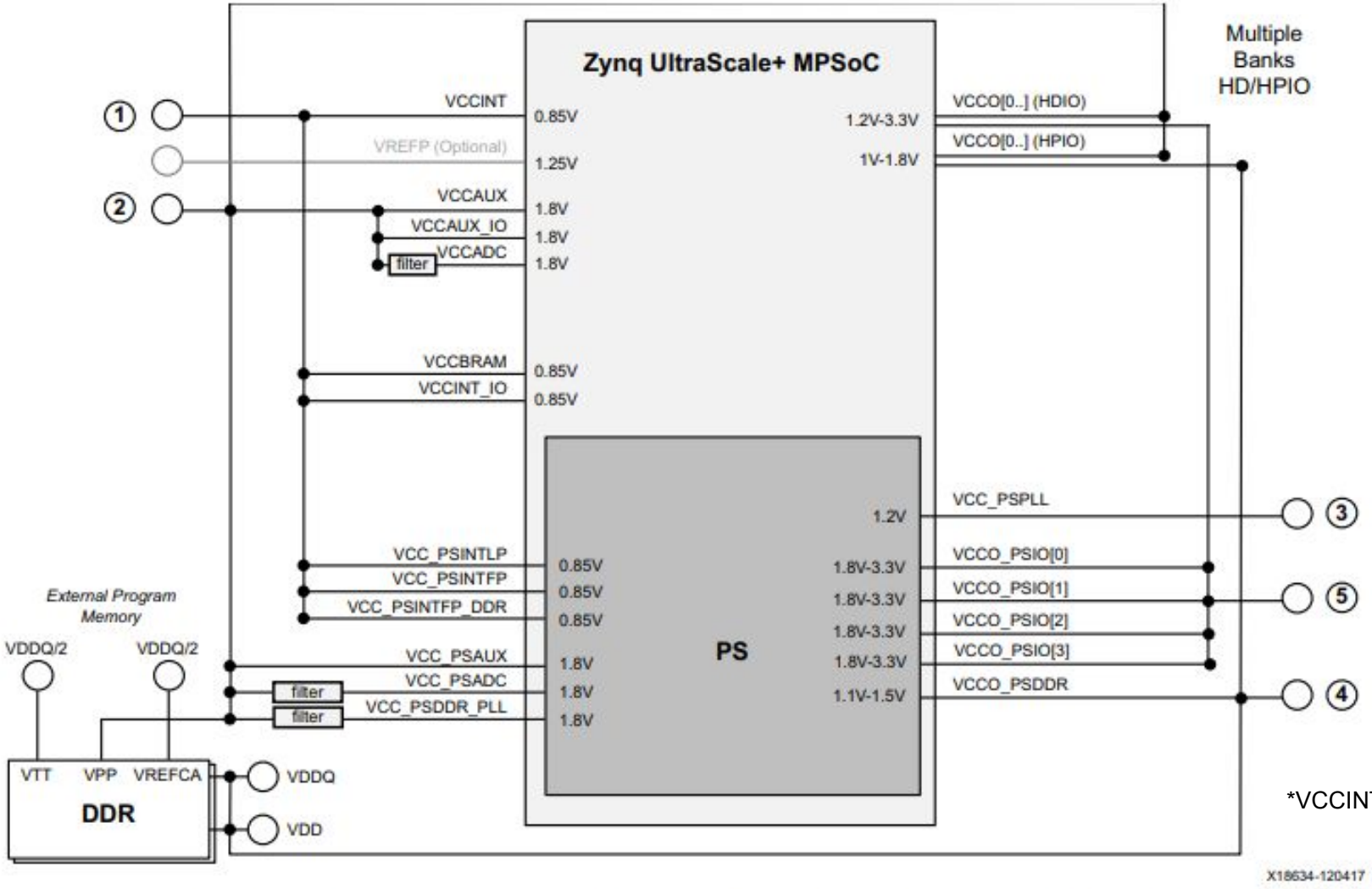
*Xilinx document: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Zynq UltraScale+ (ZU+) Device SKUs Covered- Minimum Rails

Supported SKUs
XCZU1
XCZU2
XCZU3

List may not be exhaustive. Please contact AnDAPT for further details

Zynq UltraScale+ (Minimum Rails)



*VCCINT separated out for 0.72V Devices

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree: Zynq UltraScale+ (Minimum Rails)

PVIN = 12V

#	Rail	Seq	Vout (V)	Iout (A)	Comment
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR	1	0.72/0.85	2-4.2	
2	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL	2	1.8	0.5-1	
3	VCC_PSPLL	3	1.2	0.1	
4	VCCO_PSDDR, DDR_VDDQ/VDD	4	1.1-1.5	3	
5	VCCO_PSIO	5	1.8-3.3	0.5	
6	VTT	6	VCCO_PSDDR/2	2	

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Power Tree Mapping: Zynq UltraScale+ (Minimum Rails)

PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCINT (VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR)	1	C200	Sync Buck	PVIN	12	0.72	4.2	ARD_X_ZUM_A1_IC1
2	VCCAUX (VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL)	2	C150	Async Buck	PVIN	12	1.8	1 + 0.5 + 0.1	ARD_X_ZUM_A1_IC1
3	VCC_PSPLL	3	C710	LDO	VCCAUX	1.8	1.2	0.1	ARD_X_ZUM_A1_IC1
4	VCCO_PSDDR (VCCO_PSDDR, DDR_VDDQ/VDD)	4	C150	Async Buck	PVIN	12	1.2	3	ARD_X_ZUM_A1_IC1
5	VCCO_PSIO	5	C750	Load Switch	VCCAUX	1.8	1.8	0.5	ARD_X_ZUM_A1_IC1
6	VTT	6	C210	VTT Term.	VCCO_PSDDR	1.2	0.6	1.5	ARD_X_ZUM_A1_IC1

Estimated total area estimated = 355 mm^2

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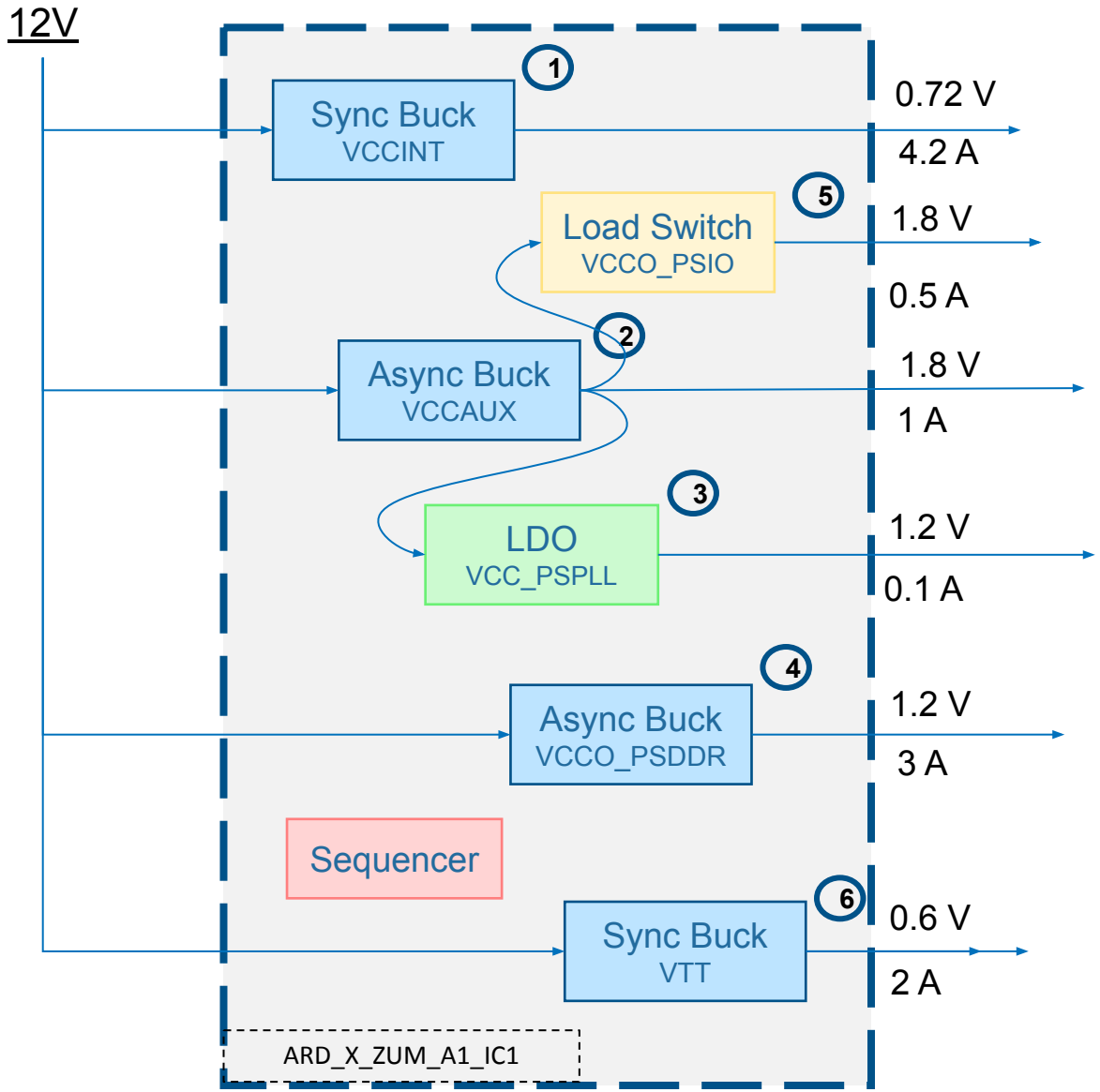
Power Tree Mapping



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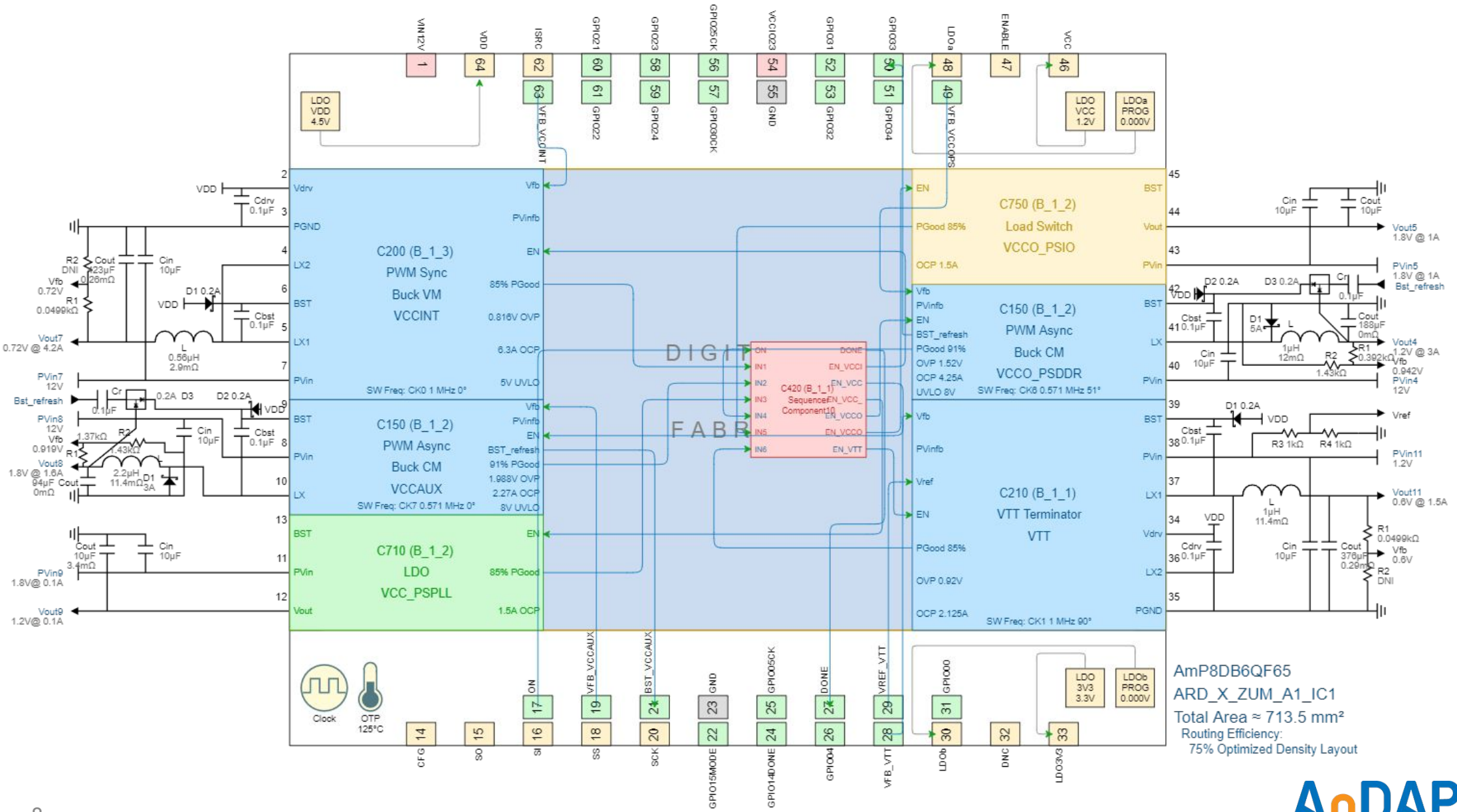
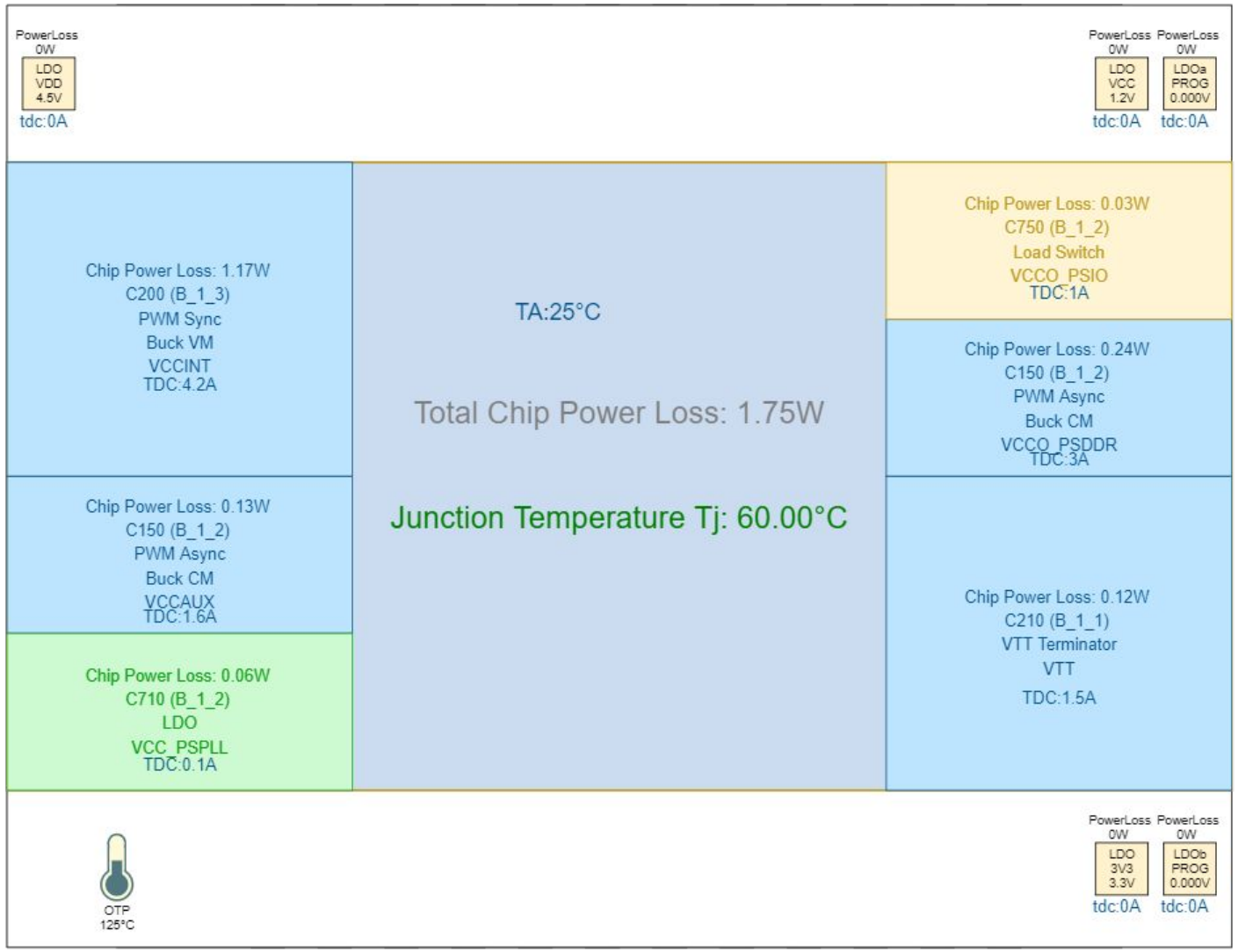
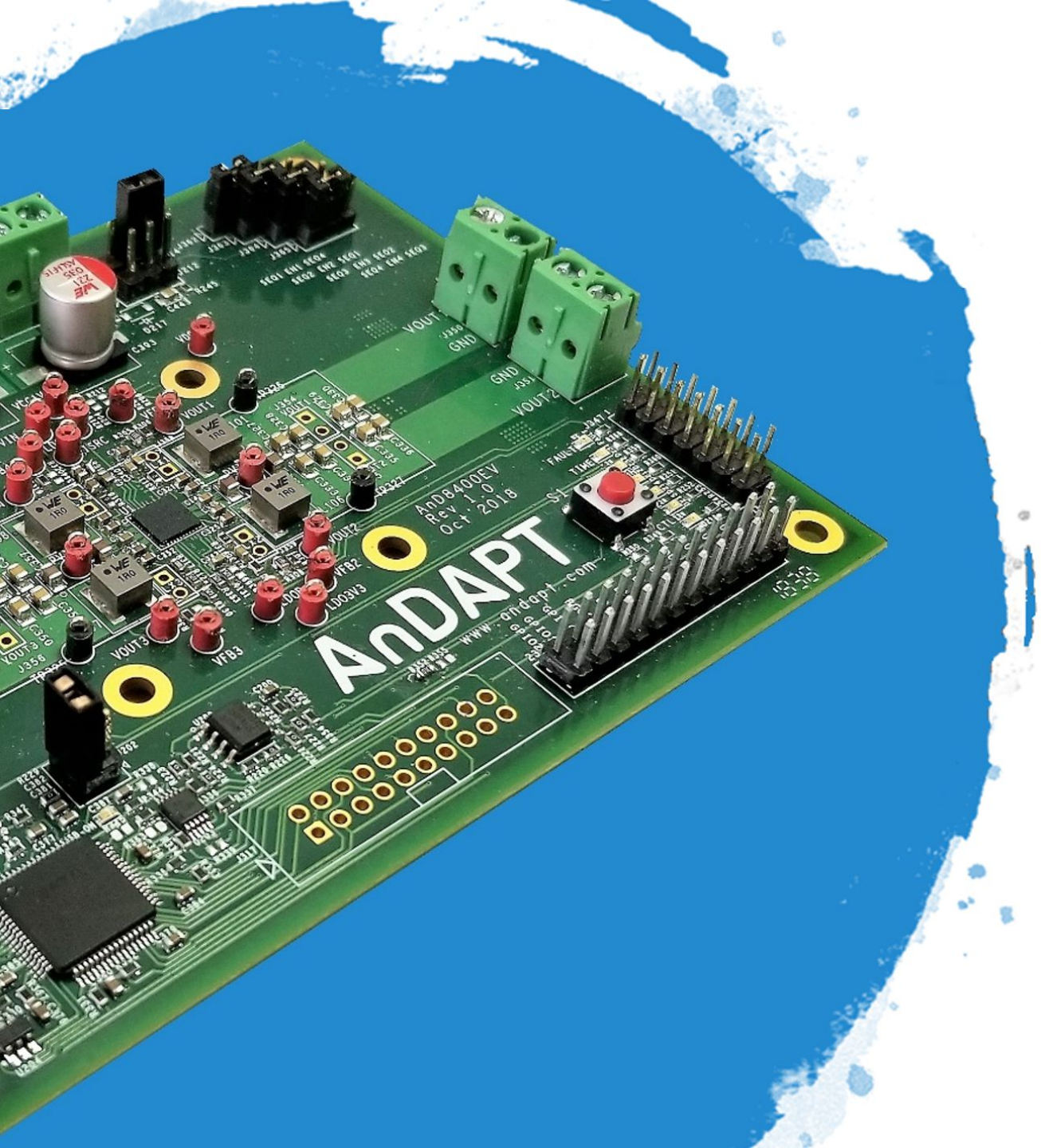
Mapping (WebAmP View)



Mapping (Thermal View)



AmP8DB6QF65
ARD_X_ZUM_A1_IC1
Total Area ≈ 713.5 mm²
Routing Efficiency:
75% Optimized Density Layout



Bench Data

Zynq UltraScale+ (Minimum Rails)

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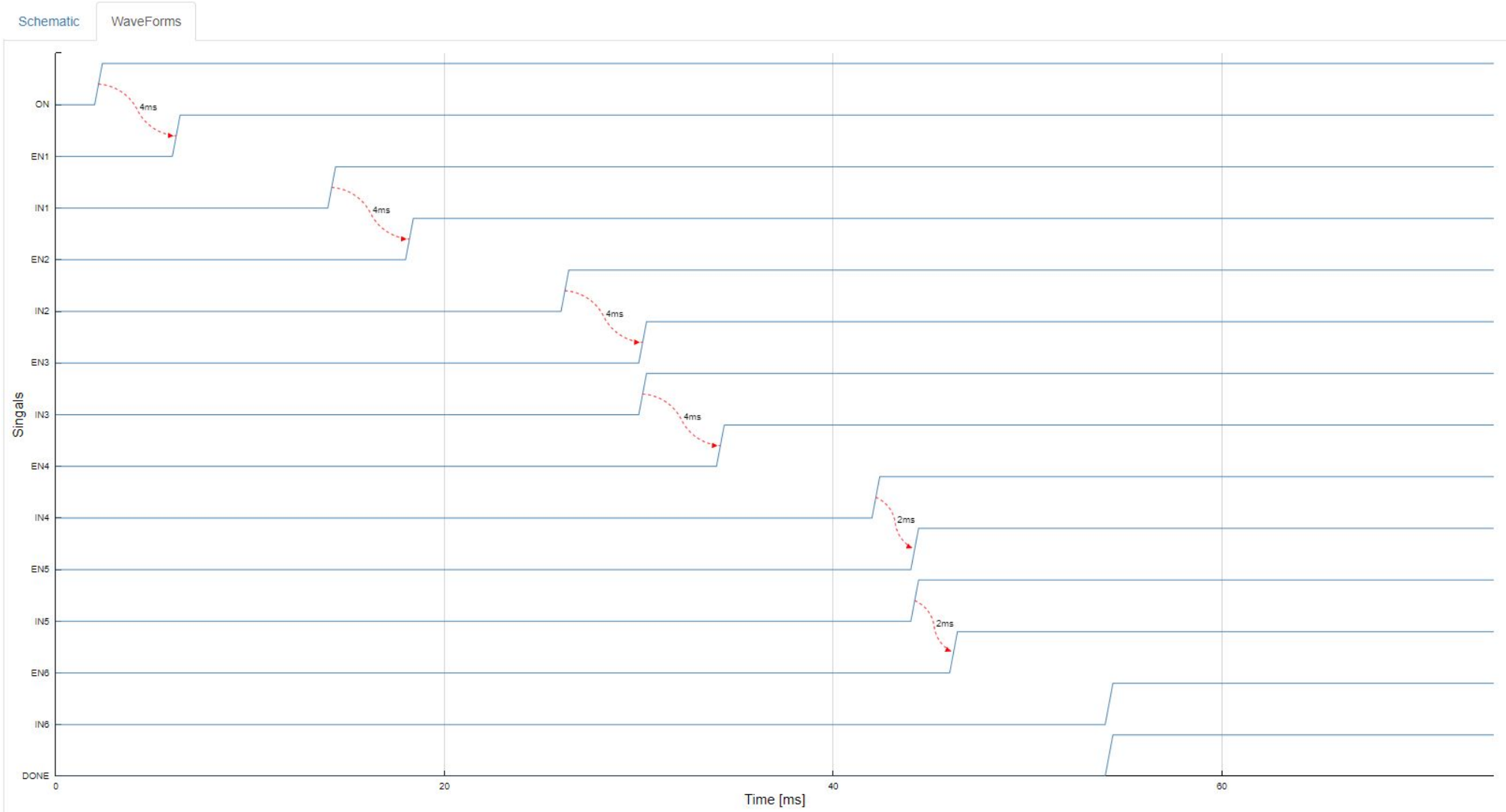
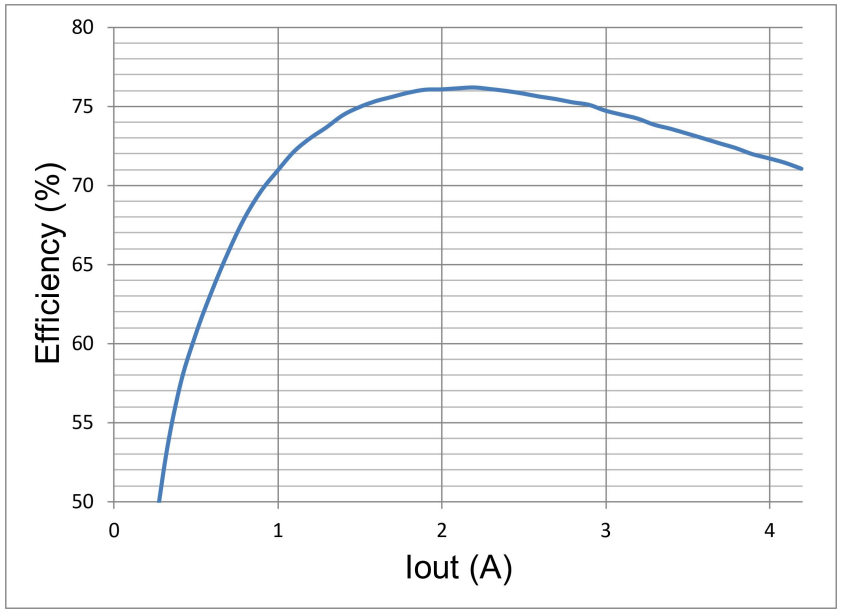
Integrated Sequencer Graphic (Turn ON)

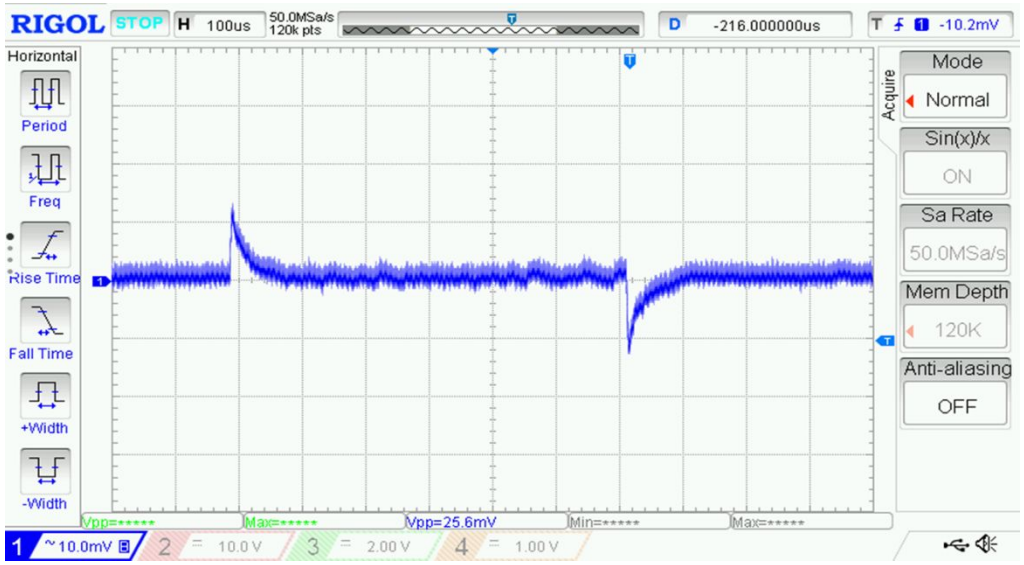


VCCINT (VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR) 0.72 V / 4.2 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

Efficiency & Transient





Vout = 0.72 V
Transient 3.15A – 4.2A @ 100 A/µs
V_{PP} = 25.6 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

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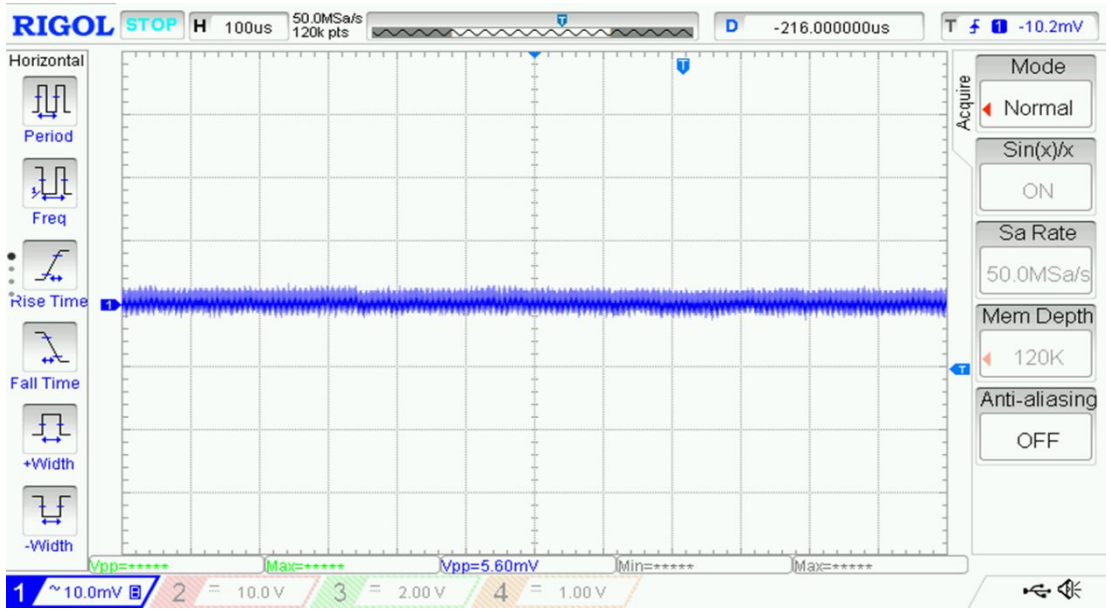
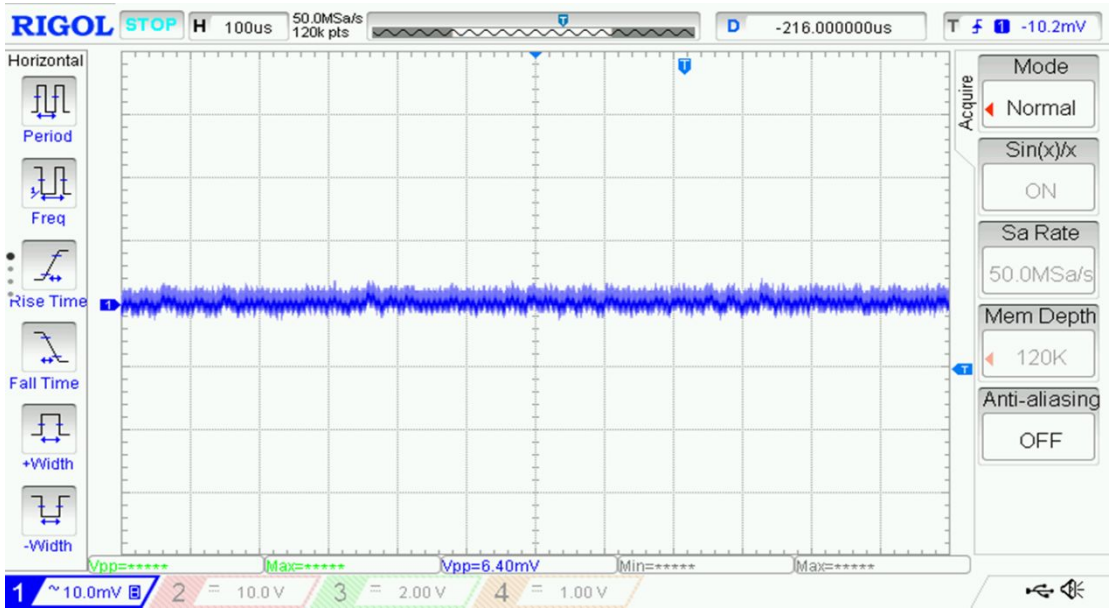
Ripple



No Load
V_{PP} = 5.6 mV

Vout = 0.72 V



4.2A Load
V_{PP} = 6.4 mV

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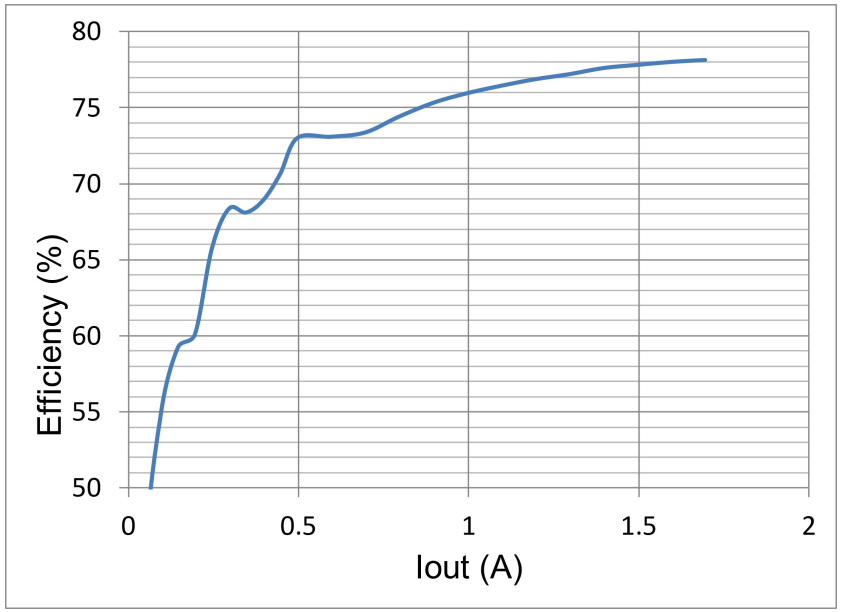
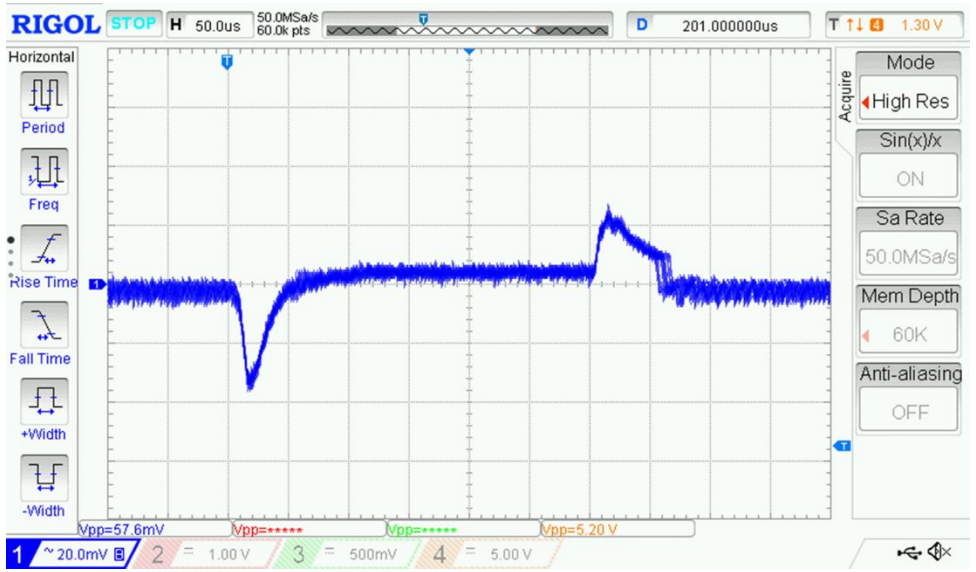
VCCAUX (VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL) 1.8 V / 1.6 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 744311220
- C = 2x47 uF

Efficiency & Transient

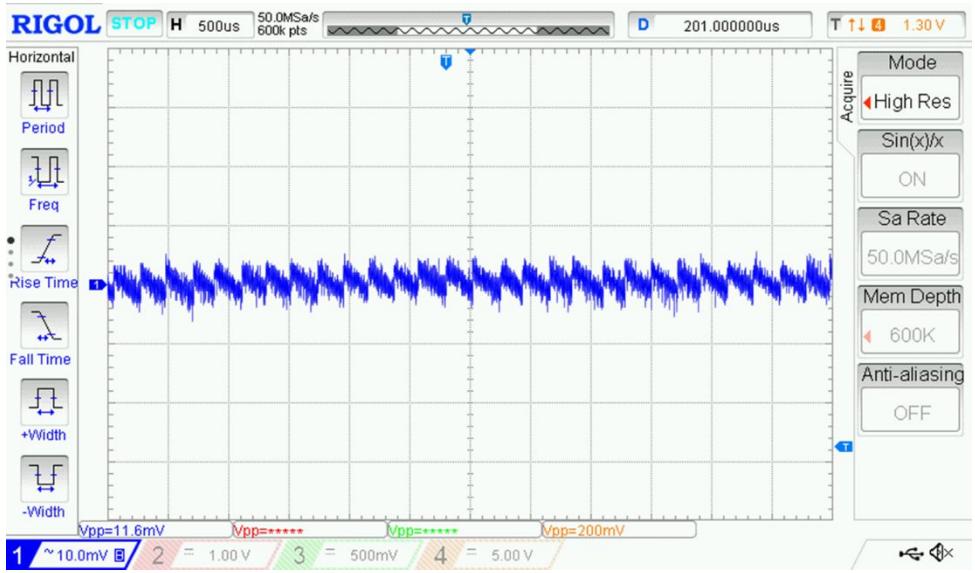




Vout = 1.8 V
Transient 0.16 A – 1.6 A @ 2.5 A/µs
V_{PP} = 57.6 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 2 x 47 µF

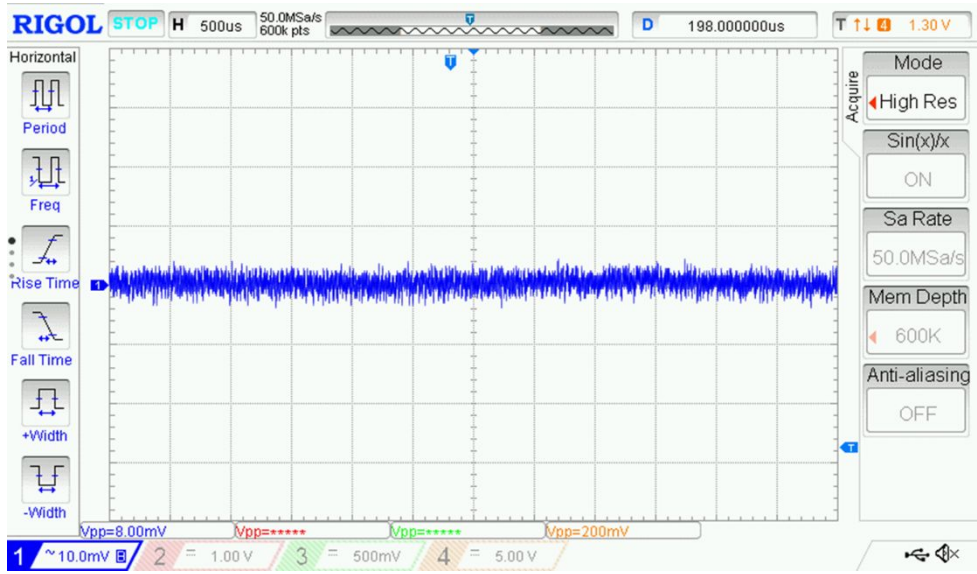
AnDAPT

Ripple



No Load
V_{PP} = 11.6 mV

Vout = 1.8 V



1.6A Load
V_{PP} = 8.0 mV

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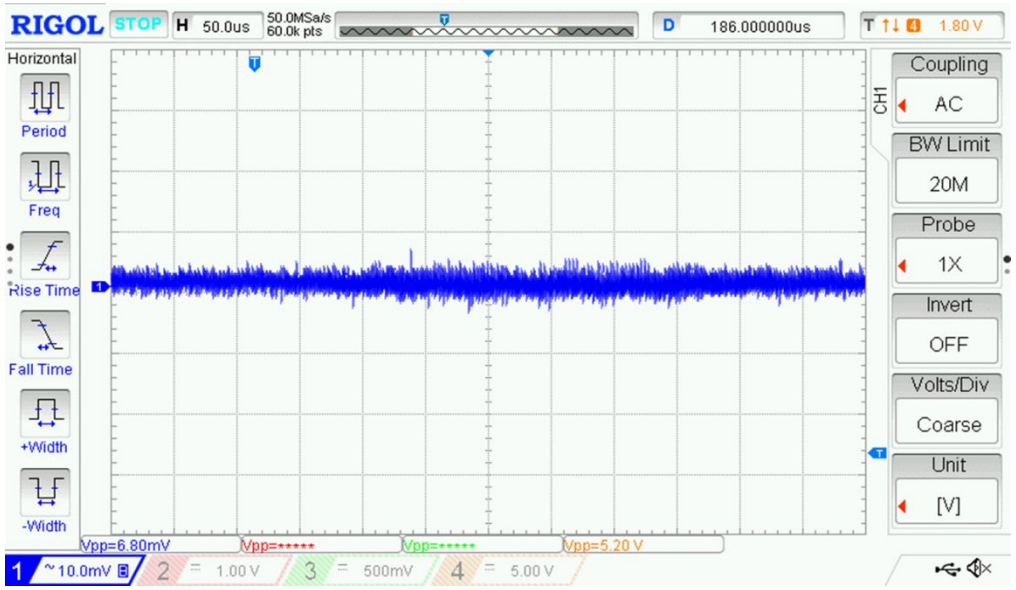
VCC_PSPLL
1.2 V / 0.1 A

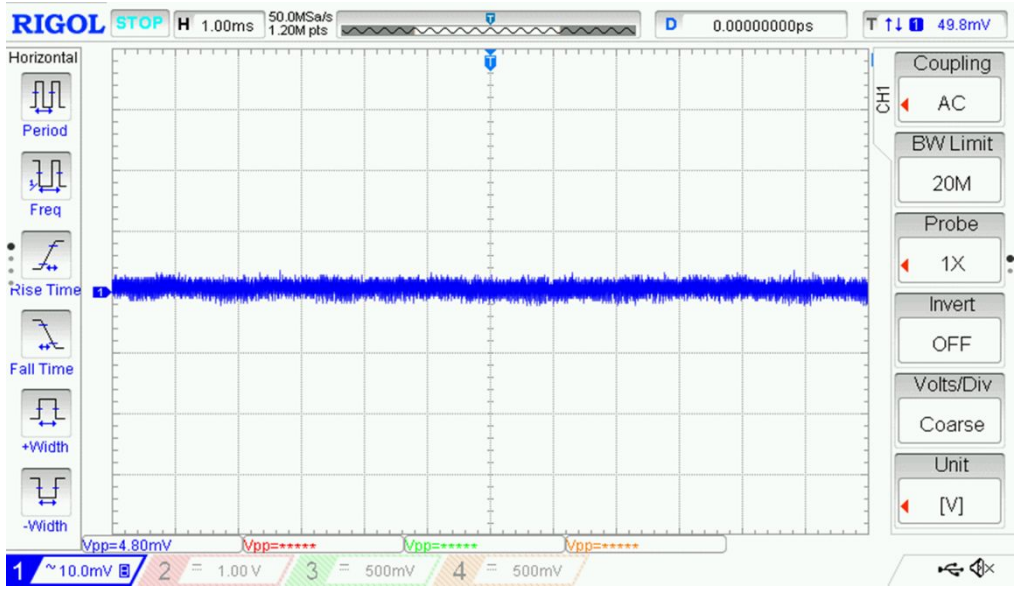
- C710 LDO
- C = 10 µF

Transient



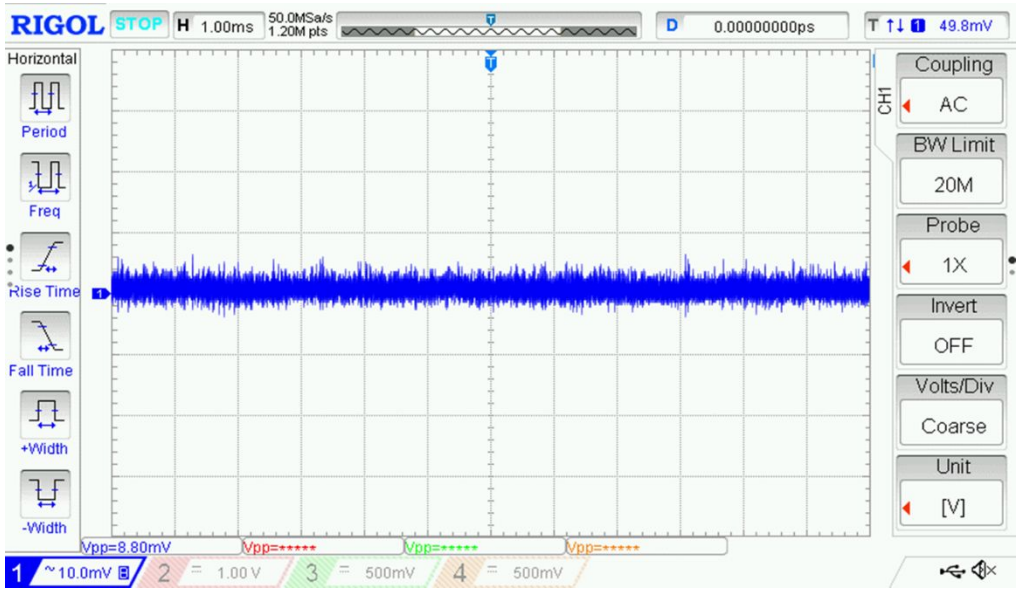
Vout = 1.2 V
Transient 0 A – 0.1 A @ 2.5 A/µs
V_{PP} = 6.8 mV
C = 10 µF

Ripple



No Load
V_{PP} = 4.8 mV

Vout = 1.2 V



0.1 A Load
V_{PP} = 8.8 mV

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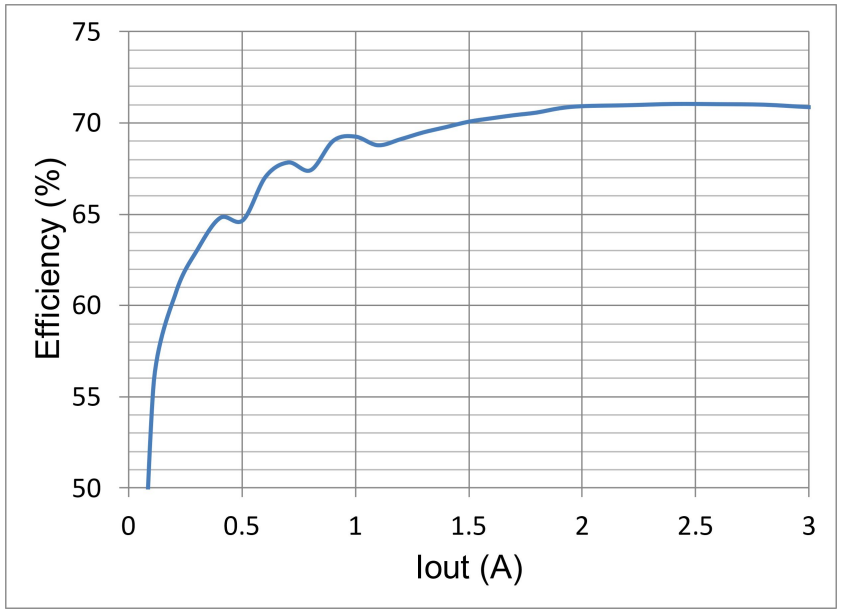
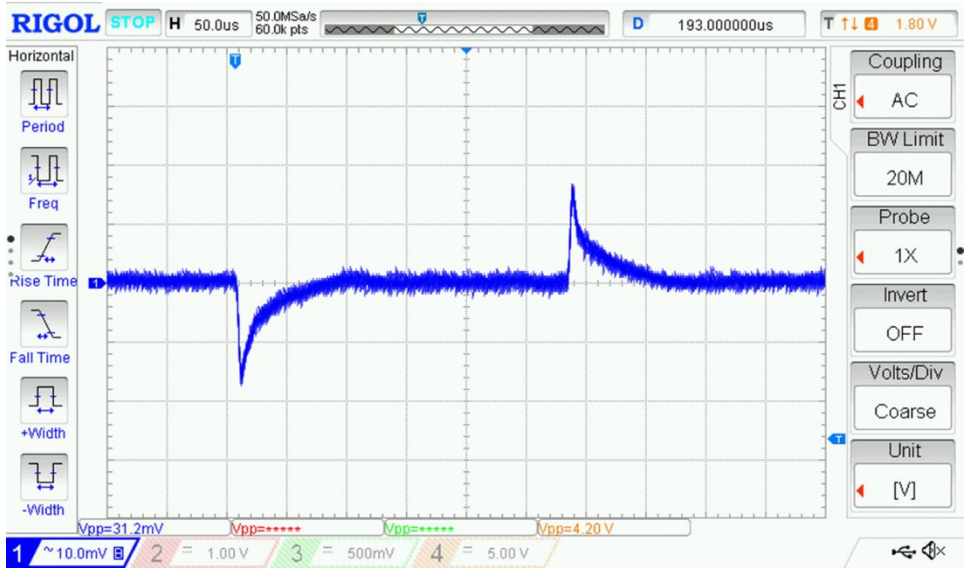
VCCO_PSDDR (VCCO_PSDDR, DDR_VDDQ/VDD) 1.2 V / 3 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 1 µH, P/N Wurth 74438356010
- C = 4x47 uF

Efficiency & Transient

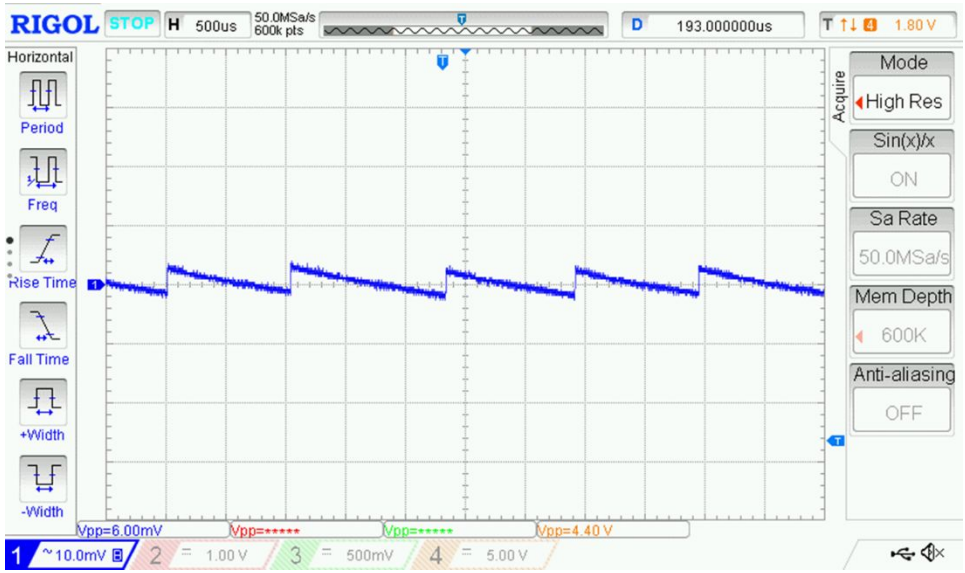




Vout = 1.2 V
Transient 2.25 A – 3 A @ 2.5 A/µs
V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1µH, Cout = 4 x 47 µF

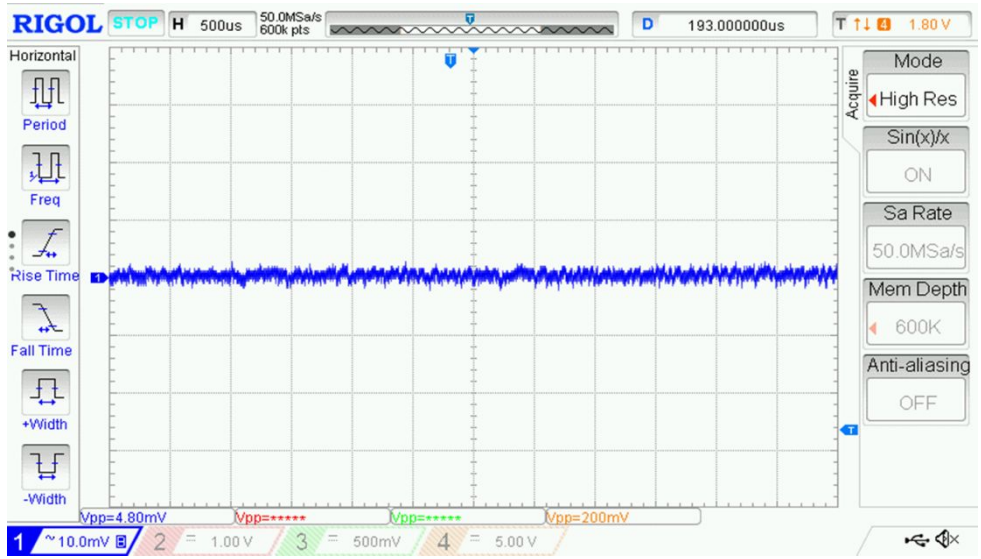
AnDAPT

Ripple



No Load
V_{PP} = 6.0 mV

Vout = 1.2 V



3 A Load
V_{PP} = 4.8 mV

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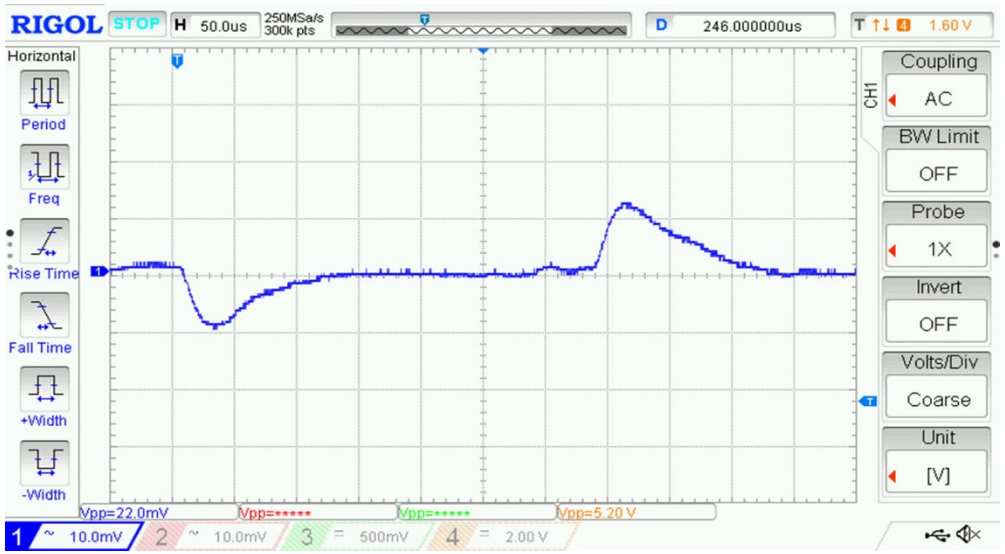
VTT
0.6 V / 1.5 A

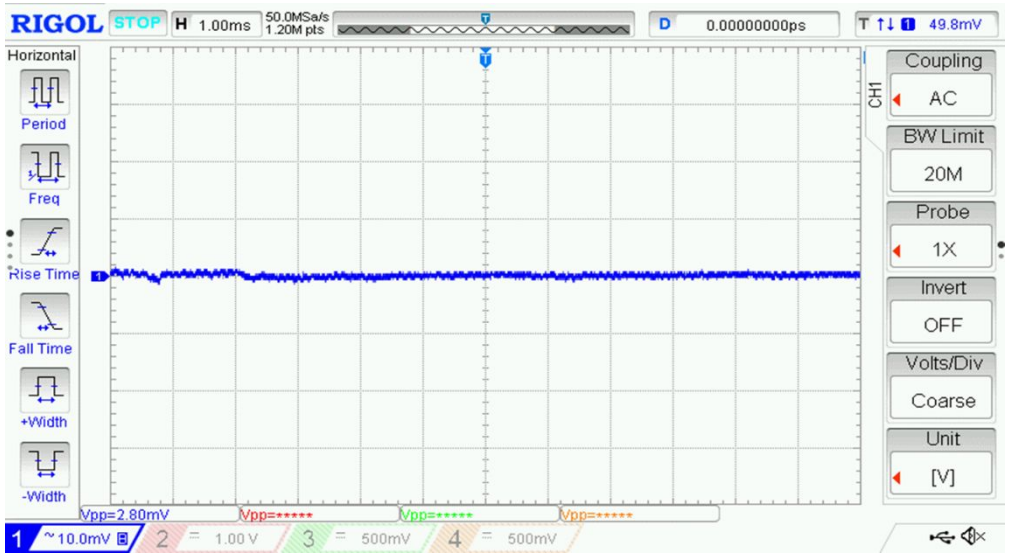
- C210 VTT_Terminator
- Fsw = 1 MHz
- L = 1 µH, P/N Wurth 74438366010
- C = 8x47 uF

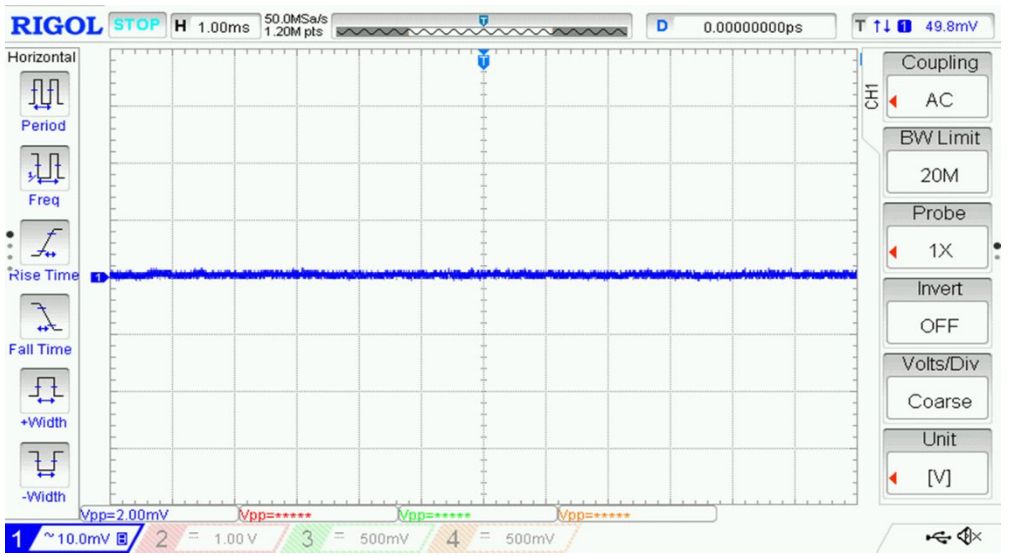
Transient



Vout = 0.6 V
Transient 1.125A – 1.5A @ 2.5 A/µs
V_{PP} = 22.0 mV
Fsw = 1 MHz
Lout = 1 µH, Cout = 8 x 47 µF

Ripple





No Load
V_{PP} = 2.8 mV

Vout = 0.6 V

1.5A Load
V_{PP} = 2.0 mV

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Thank You

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