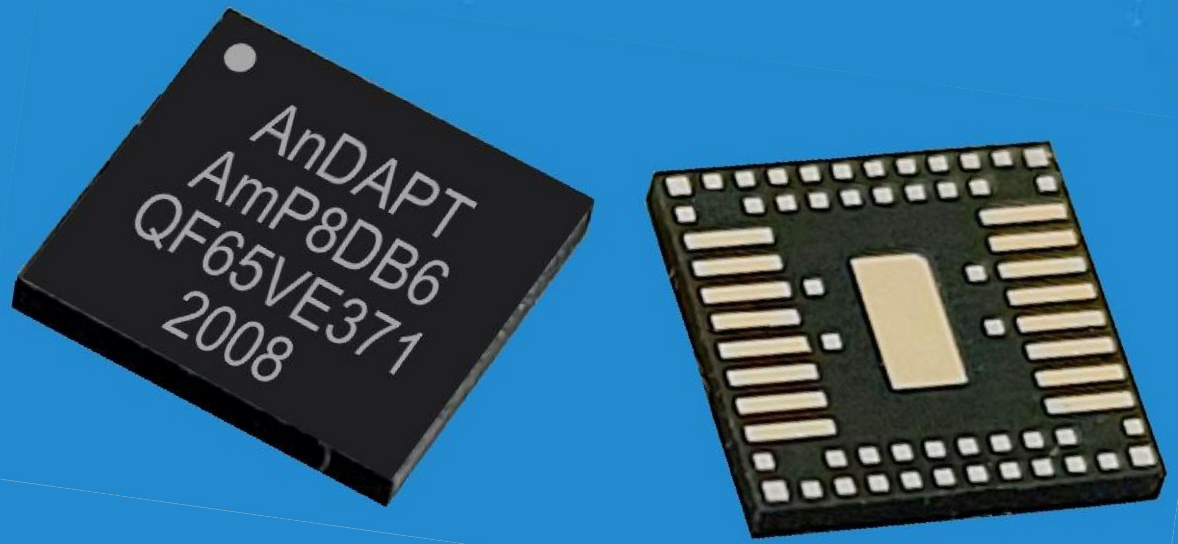

AnDAPT Power Solutions for Xilinx

Zynq Ultrascale+ MPSoC Mapping & Lab Data

Use-Case A2

AnDAPT Marketing Team

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Contents

- Xilinx Zynq Ultrascale+ (ZU+) family of MPSoC devices' use-cases
- AnDAPT integrated power supply reference design availability for ZU+ MPSOC SKUs
- Lab data for each power rail for Cost-optimized with MGT rails (A2) use-case using AnDAPT PMICs

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Use-Cases (MPSoC Devices)

<table>
<tr><th rowspan="2">Devices
(CG+EG+EV)</th><th colspan="2">Cost-Optimized</th><th rowspan="2">Power
Optimized</th><th rowspan="2">Performance
Optimized</th><th rowspan="2">Full Power
Management</th></tr>
<tr><th>W/o MGT</th><th>With MGTs</th></tr>
<tr><td>ZU2-ZU3</td><td rowspan="3">A1
(1x
AnDAPT
PMIC)</td><td rowspan="3">A2
(2x
AnDAPT
PMICs)</td><td rowspan="3">B
(2x
AnDAPT
PMICs)</td><td rowspan="3">C
(2x
AnDAPT
PMICs)</td><td>D1
(2x AnDAPT PMICs)</td></tr>
<tr><td>ZU4-ZU5</td><td rowspan="2">D2
(3x AnDAPT PMICs)</td></tr>
<tr><td>ZU6-ZU9</td></tr>
<tr><td>ZU11-ZU19</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

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ZU+ MPSoC Rail Coverage with AmP Power Components

Use Case	SKU	VCCINT	VCCBRAM	VCCINT_IO	VCCINT_VCU	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	VCCAUX	VCCAUX_IO	VCCADC	VCC_PSAUX	VCC_PSDDR_PLL	VCC_PSADC	VMGTAVTT (GTH)	VMGTYATT (GTY)	VCC_PSPLL	VCCO_PSDDR	VCCO_PSIO	VPS_MGTRAVCC	VMGTVCCAUX (GTH)	VMGTYVCCAUX (GTY)	VPS_MGTRAVTT	VMGTAVCC (GTH)	VMGTYAVCC (GTY)	HDIOVCCO	HPIOVCCO
Cost-optimized	ZU2-ZU19 (w/o MGTs)	Rail 1			Rail 6	Rail 1			Rail 4						-	-	Rail 3	Rail 2	Rail 5	-	-	-	-	-	-	-	-
	ZU2-ZU19 (w MGTs)	Rail 1			Rail 5	Rail 1			Rail 3						Rail 6			Rail 2	Rail 4	Rail 7	Rail 8			Rail 9		-	-
Power-Optimized	ZU2-ZU19	Rail 1	Rail 2						Rail 4						Rail 3			Rail 8	Rail 5	Rail 9	Rail 6			Rail 7		-	-
Performance-Optimized	ZU2-ZU19	Rail 1			Rail 2	Rail 1			Rail 4						Rail 3			Rail 8	Rail 5	Rail 7	Rail 6			Rail 7		Rail 9	Rail 10
Full-Power Management	ZU2-ZU3	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	-	-	Rail 3	Rail 7	Rail 4	Rail 11	-	-	Rail 12	-	-	Rail 13	Rail 14
	ZU4-ZU19	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	Rail 13		Rail 3	Rail 7	Rail 4	Rail 11	Rail 15		Rail 12	Rail 14		Rail 16	Rail 17

C860 (DrMOS Ctrl)	
C220 (Sync Buck HC)	
C200 (Sync Buck)	
C150 (Async Buck)	
C710 (SIM LDO)	
C750 (Load Switch)	
Corner LDO	

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Zynq Ultrascale+ (ZU+) MPSoC Device SKUs Covered

CG Devices (Dual Application Processor)	**EG Devices** (Quad Application Processor & GPU)	**EV Devices** (Video Codec)
XCZU2CG	XCZU2EG	XCZU4EV
XCZU3CG	XCZU3EG	XCZU5EV
XCZU4CG	XCZU4EG	
XCZU5CG	XCZU5EG	
XCZU6CG	XCZU6EG	
XCZU7CG	XCZU9EG	
XCZU9CG	XCZU11EG	
	XCZU15EG	
	XCZU17EG	
	XCZU19EG	

List may not be exhaustive. Please contact AnDAPT for further details

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Zynq Ultrascale+ MPSoC (Always On, Cost-Optimized (With MGTs)) Use Case: A2

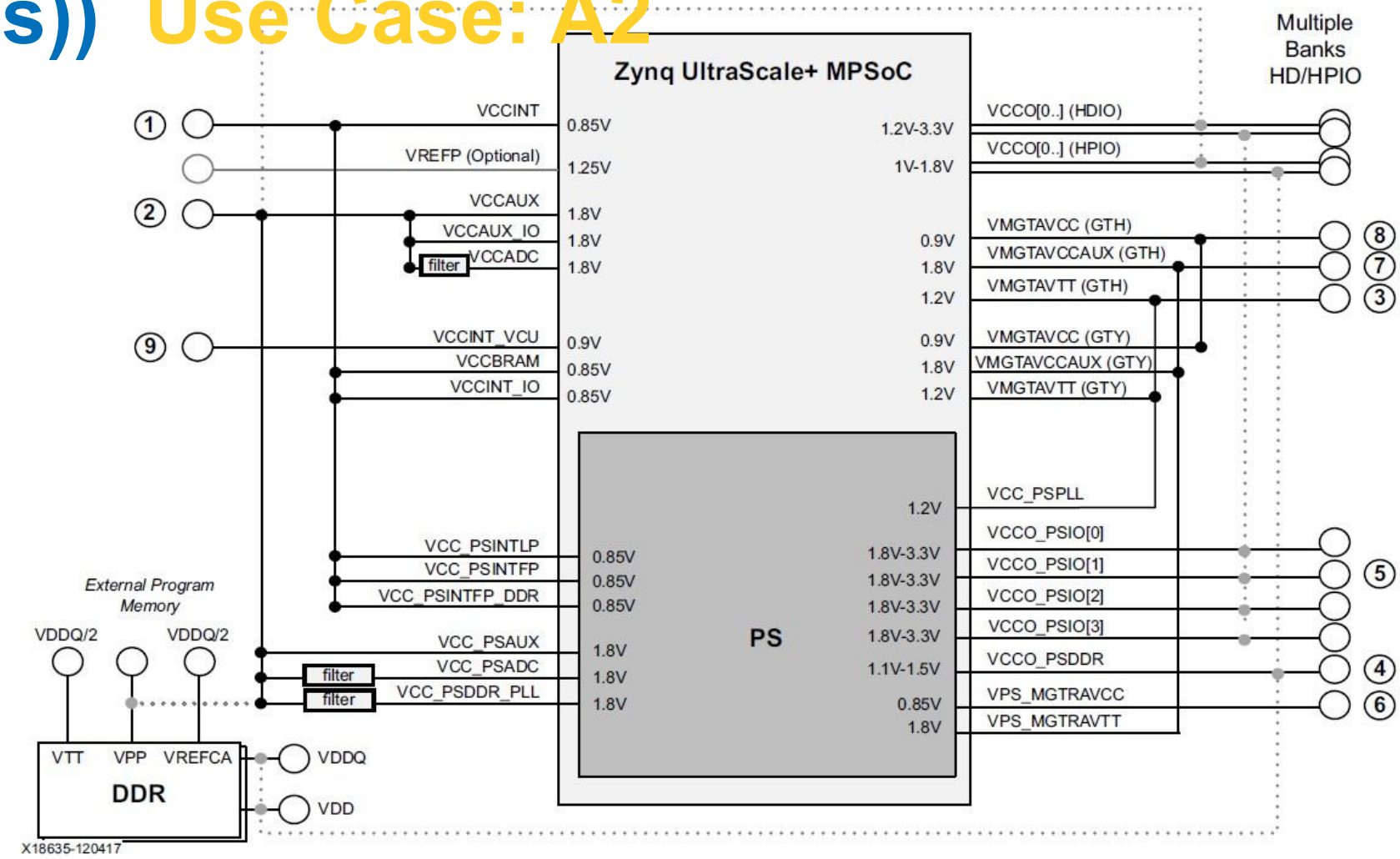


Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree Mapping- Use Case: A2

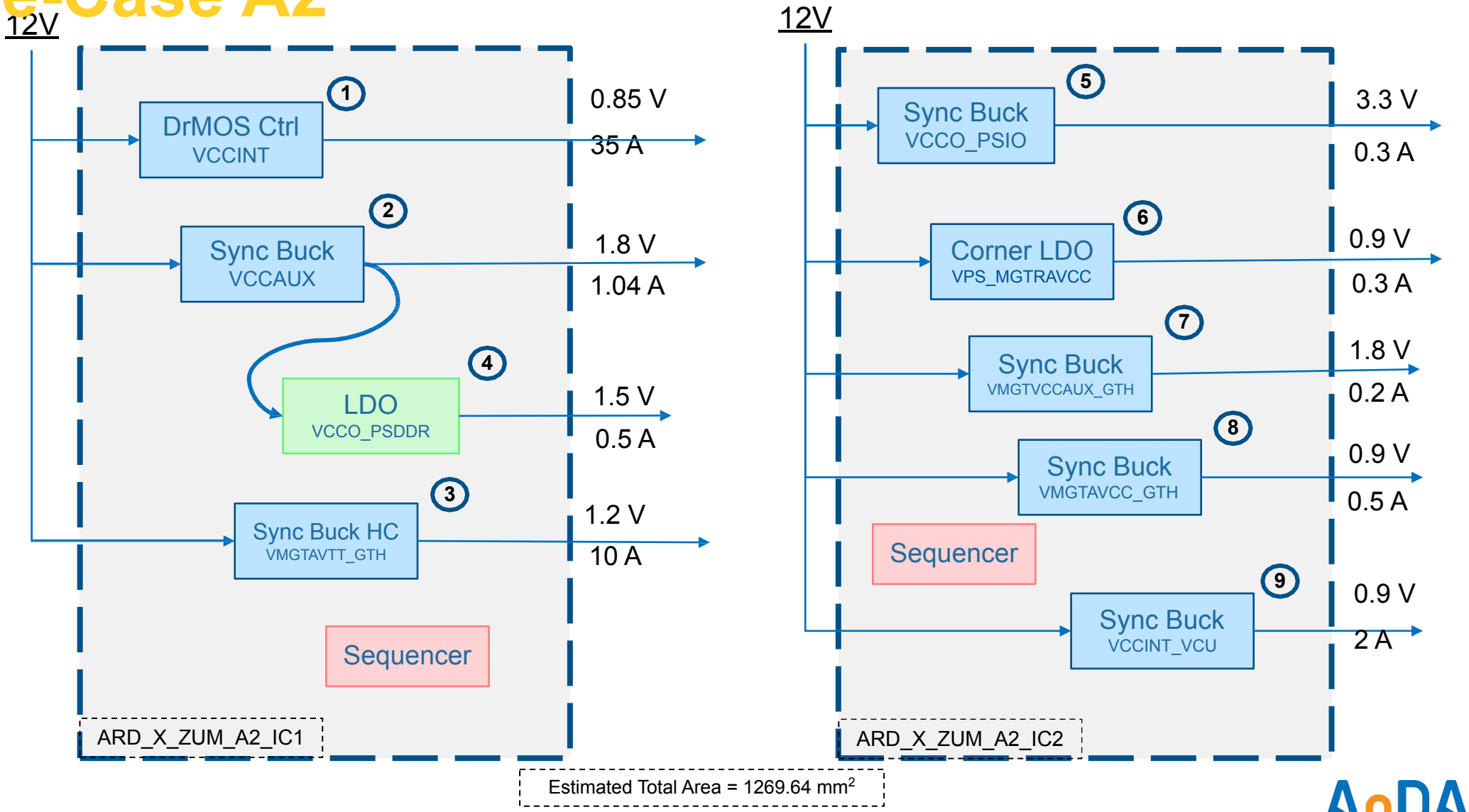
V_{IN} = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR	1	C860	DrMOS Ctrl	V_{IN}	12	0.85	35	ARD_X_ZUM_A2_IC1
2	VCCO_PSDDR	4	C710	SIM LDO	VCCAUX	1.8	1.1 – 1.5	0.5	ARD_X_ZUM_A2_IC1
3	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VCCO_HDIO, VCCO_HPIO	2	C200	Sync Buck	V_{IN}	12	1.8	1.04 + 0.5	ARD_X_ZUM_A2_IC1
4	VCCO_PSIO[0:3]	5	C200	Sync Buck	V_{IN}	12	1.8 – 3.3	0.300	ARD_X_ZUM_A2_IC2
5	VCCINT_VCU*	9	C200	Sync Buck	V_{IN}	12	0.9	2	ARD_X_ZUM_A2_IC2
6	VMGTAVTT(GTH), VMGTYAVTT(GTY), VCC_PSPLL	3	C220	Sync Buck HC	V_{IN}	12	1.2	2.6-10.6	ARD_X_ZUM_A2_IC1
7	VPS_MGTRAVCC	6	CLDO	Corner LDO	V_{IN}	12	0.85/0.9	0.3	ARD_X_ZUM_A2_IC2
8	VMGTVCCAUX(GTH), VMGTYVCCAUX(GTY), VPS_MGTRAVTT	7	C200	Sync Buck	V_{IN}	12	1.8	0.2	ARD_X_ZUM_A2_IC2
9	VMGTAVCC(GTH), VMGTYAVCC(GTY)	8	C200	Sync Buck	V_{IN}	12	0.9	0.5	ARD_X_ZUM_A2_IC2

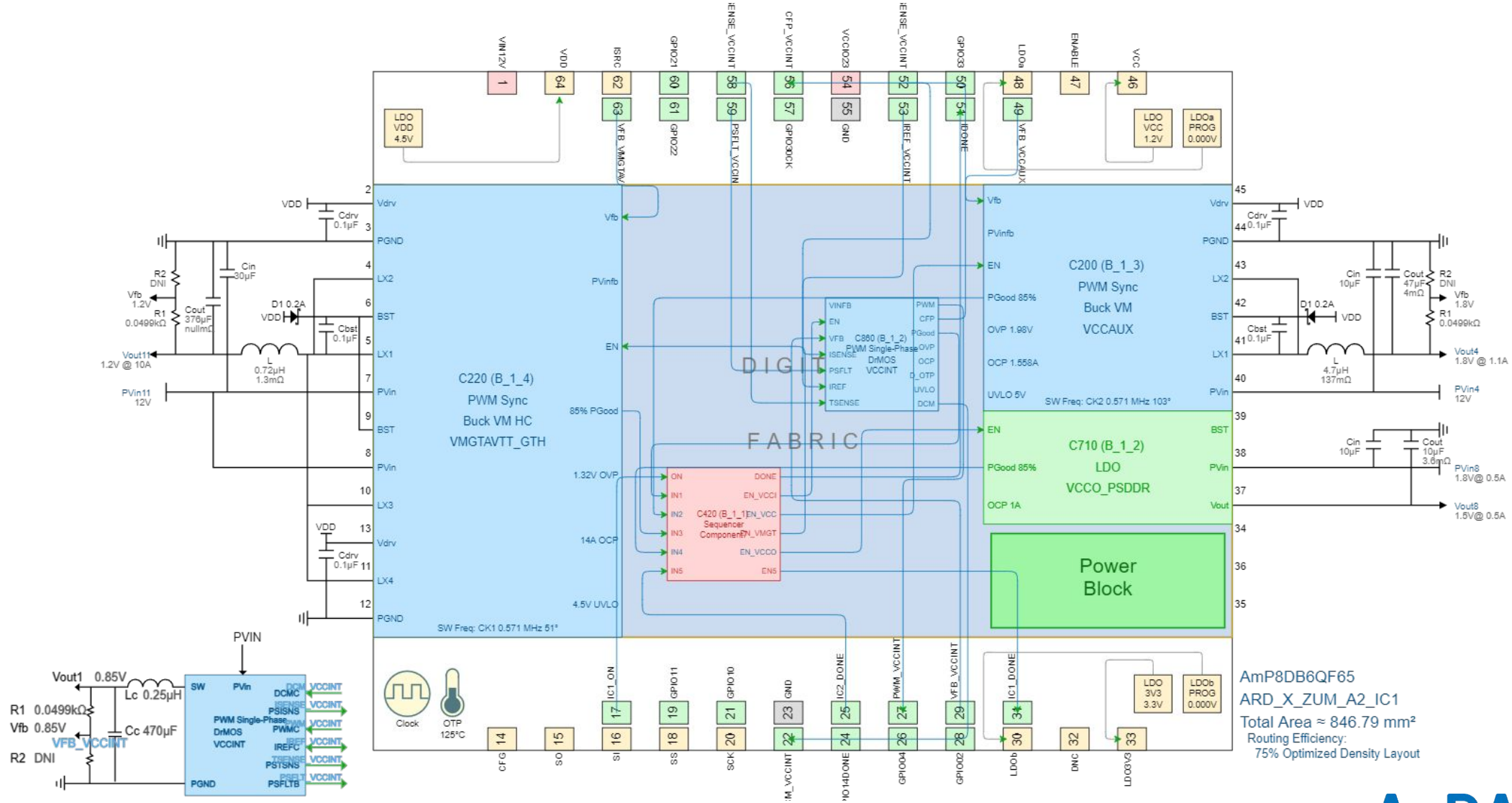
*Only required for EV devices

Proposed Solution (2xPMICs)

Use-Case A2

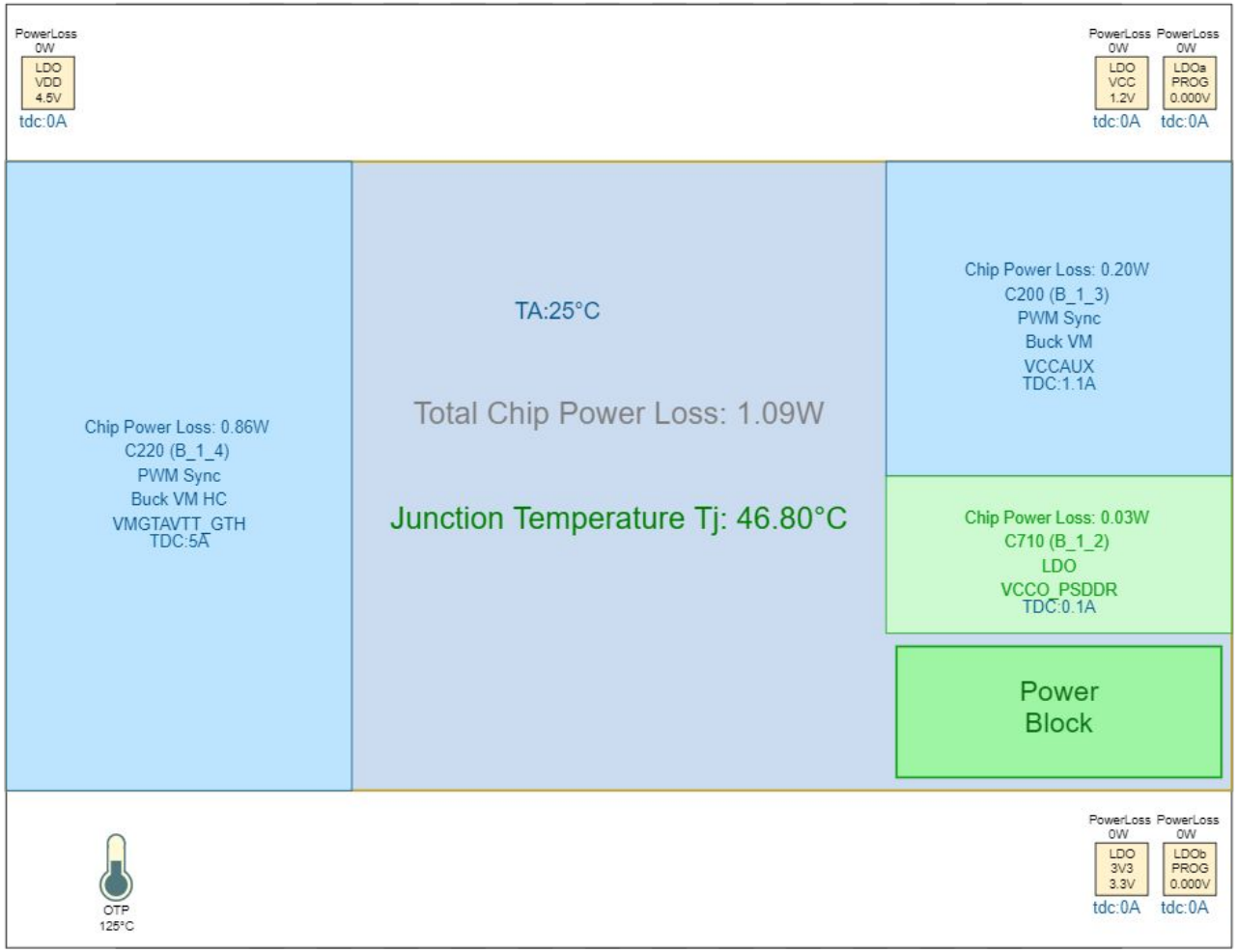


Mapping IC1 (WebAmP View) Use-Case A2



Thermal Design View (IC1)

Use-Case A2



AmP8DB6QF65
ARD_X_ZUM_A2_IC1
Total Area ≈ 846.79 mm²
Routing Efficiency:
75% Optimized Density Layout

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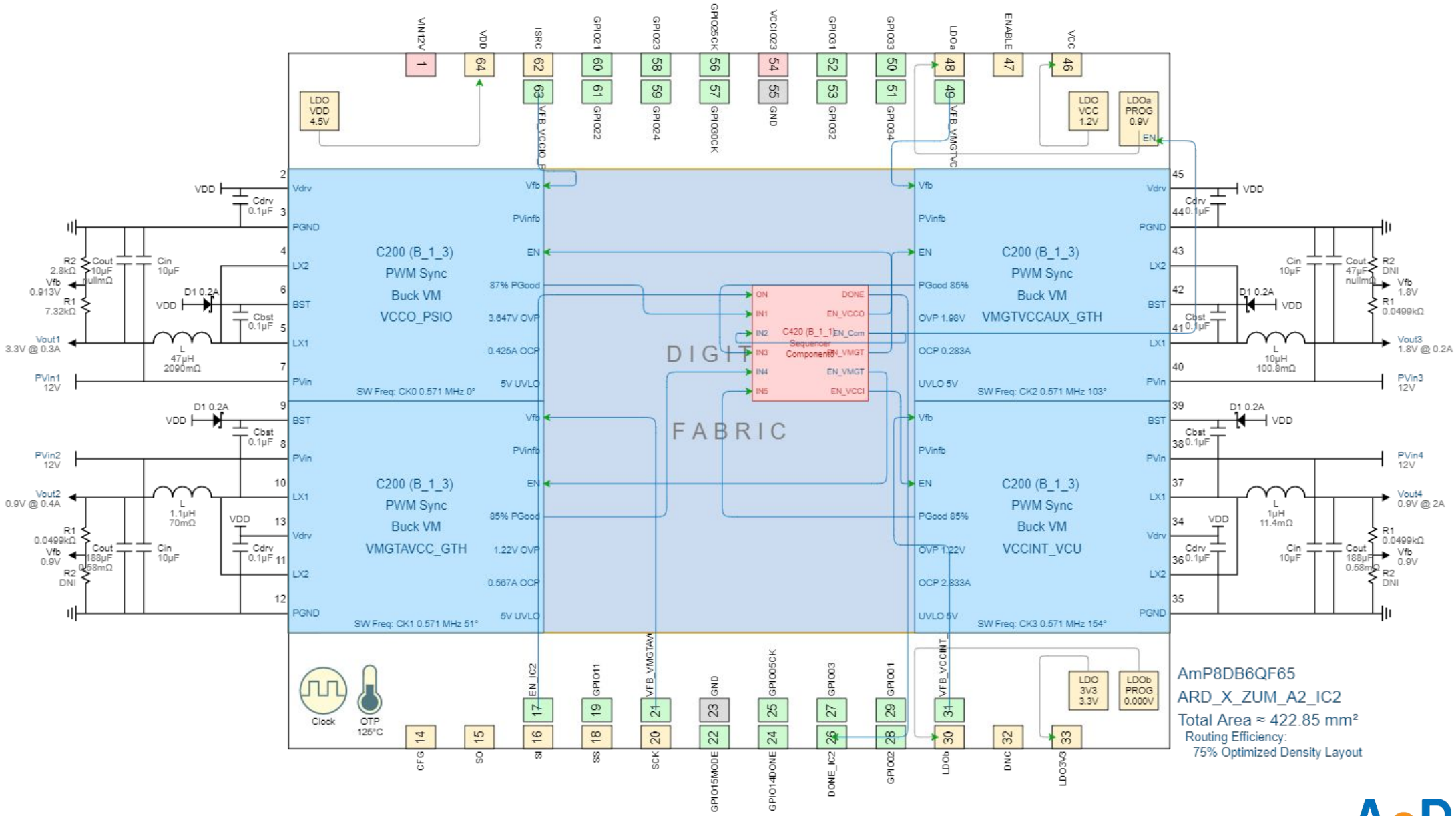
Mapping IC2 (WebAmP View) Use-Case A2



AmP8DB6QF65
ARD_X_ZUM_A2_IC2
Total Area ≈ 422.85 mm²
Routing Efficiency:
75% Optimized Density Layout

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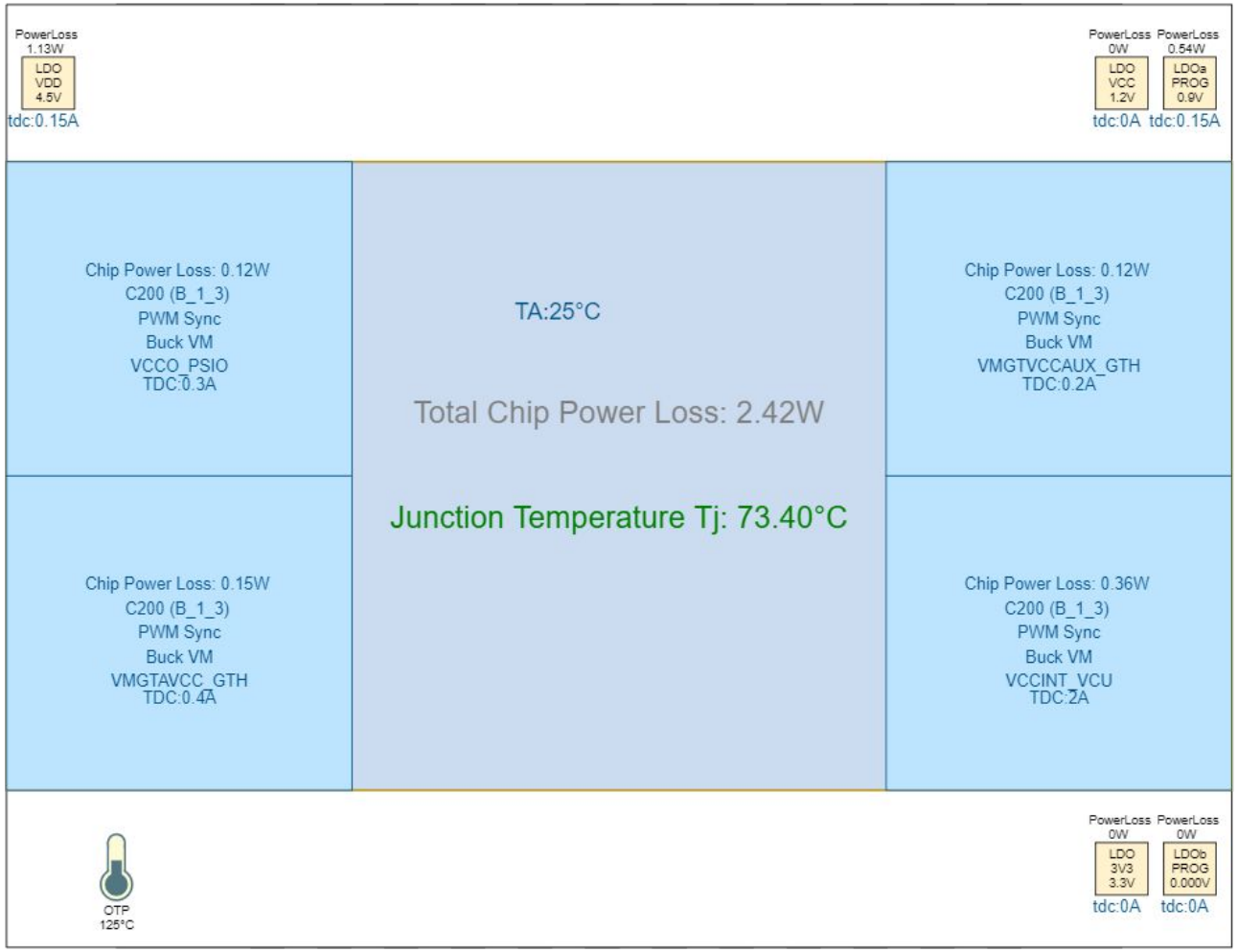
Thermal Design View (IC2)

Use-Case A2



AmP8DB6QF65
ARD_X_ZUM_A2_IC2
Total Area ≈ 422.85 mm²
Routing Efficiency:
75% Optimized Density Layout

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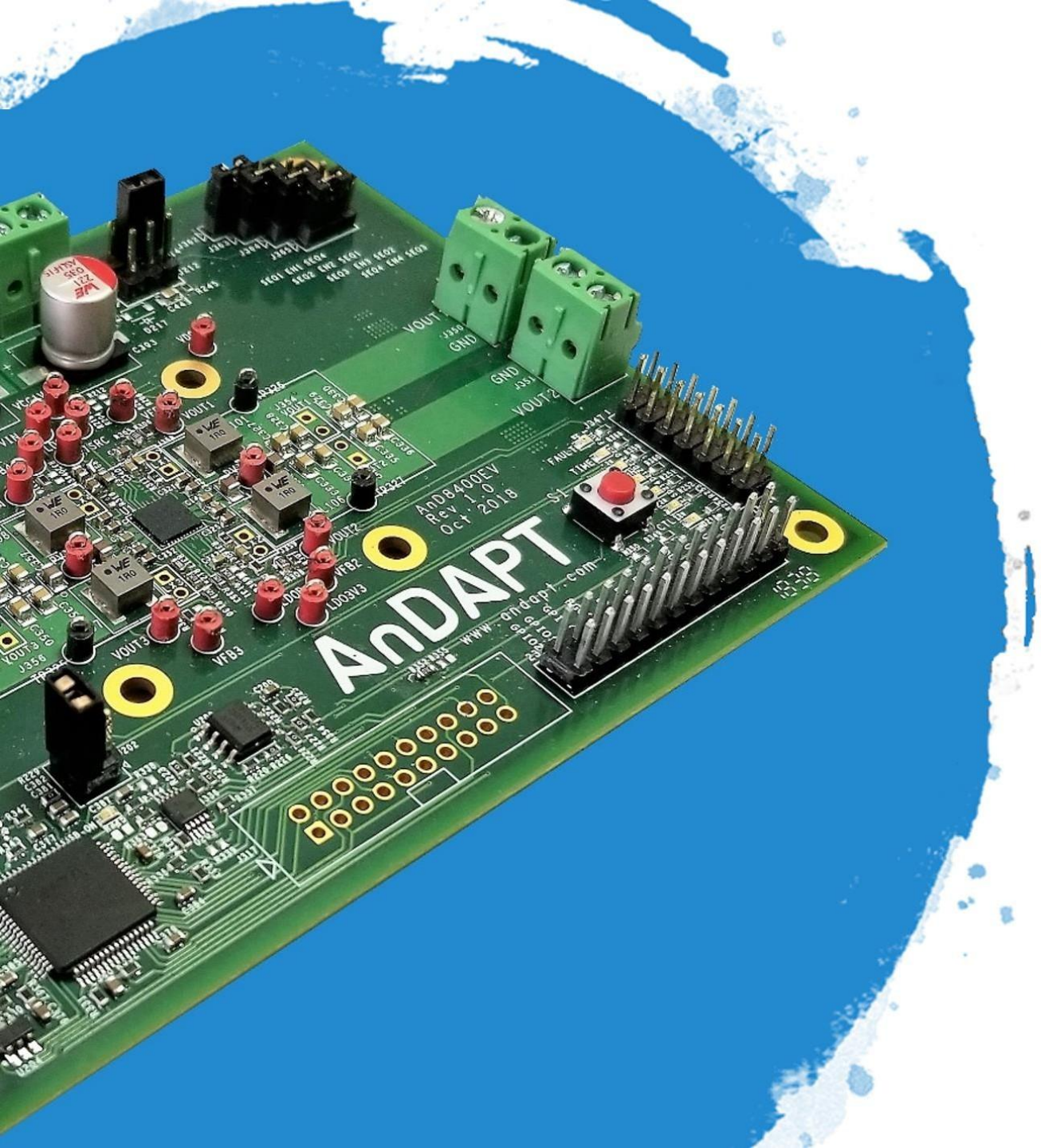

Bench Data

Use-Case
A2

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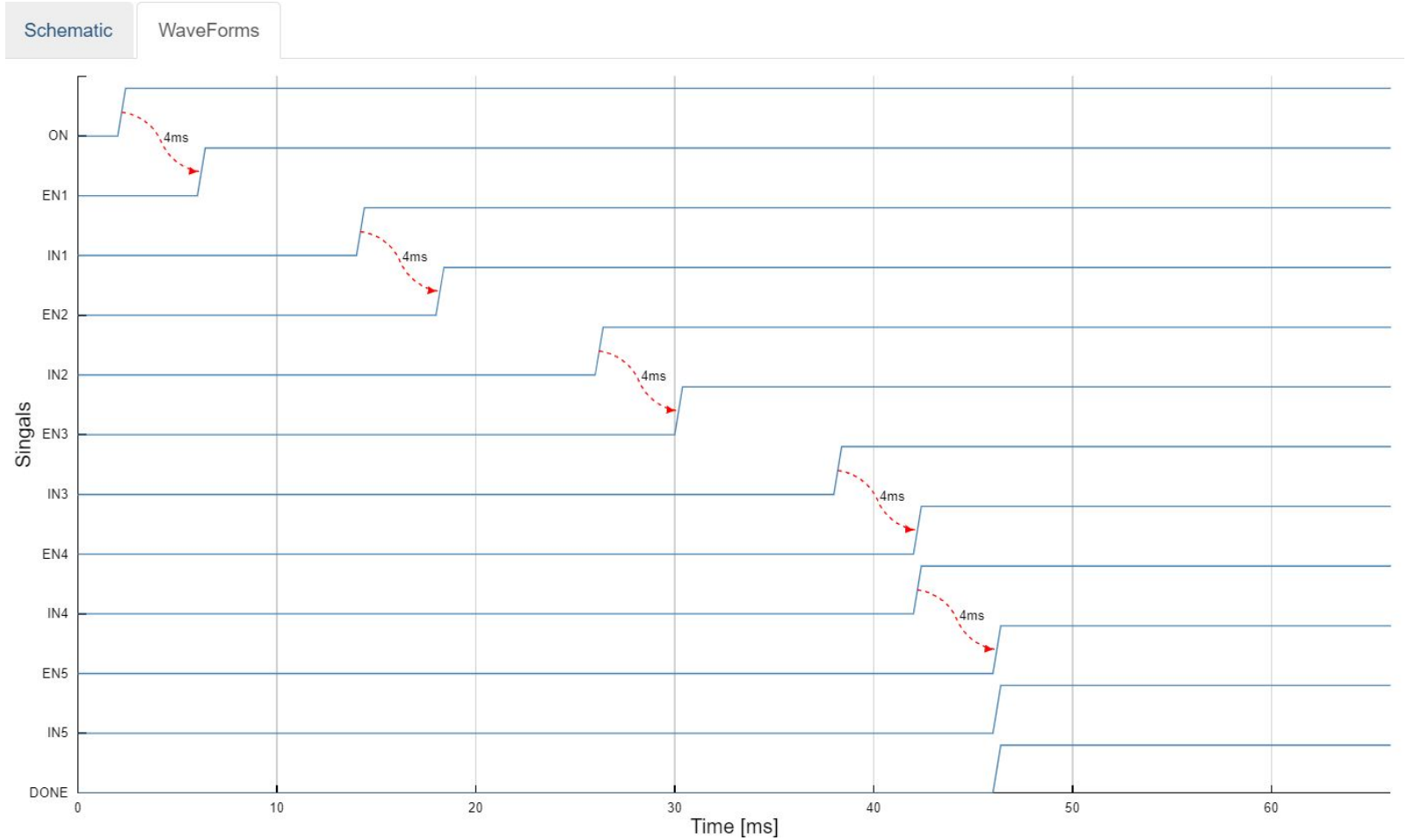
WebAmP Sequencer Graphic (IC1)



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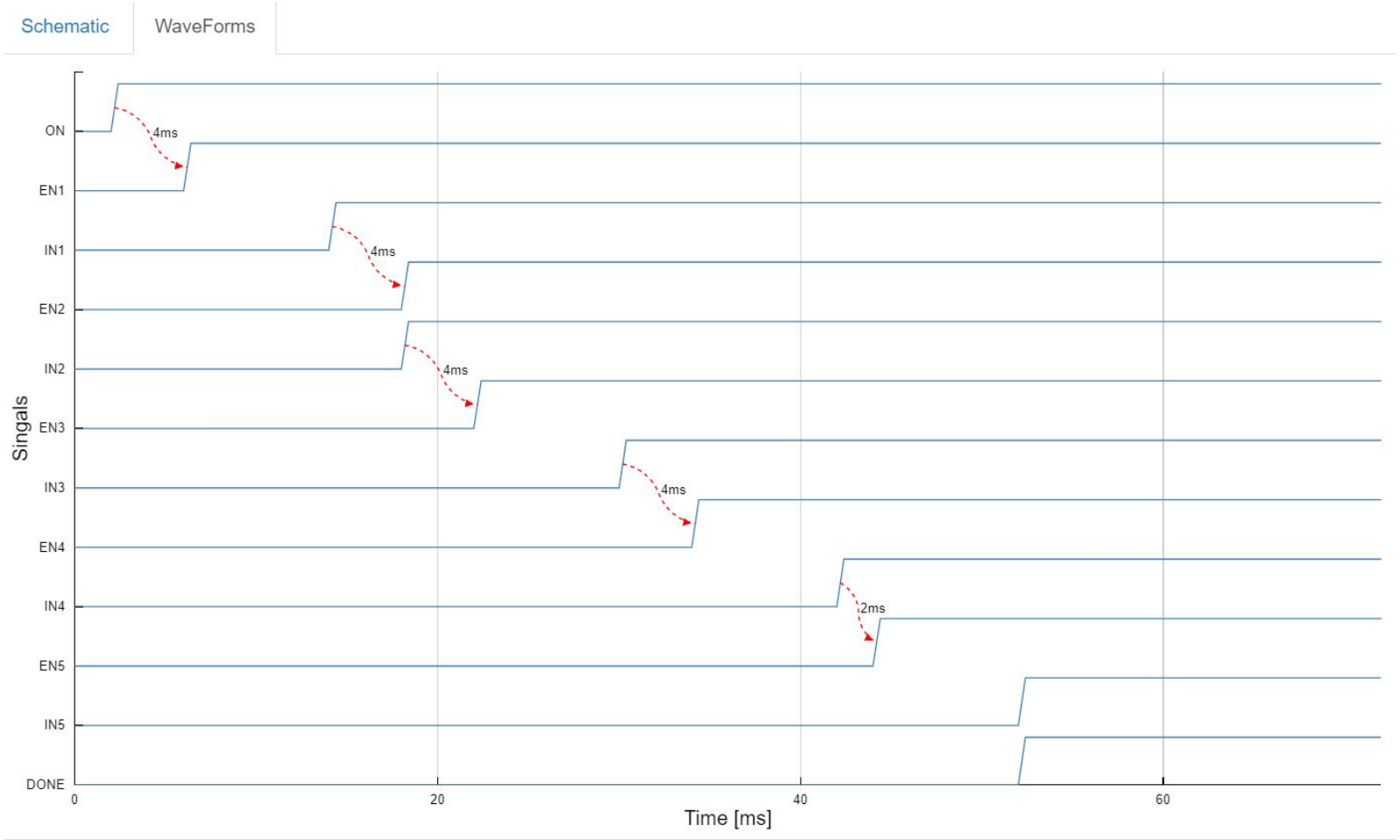
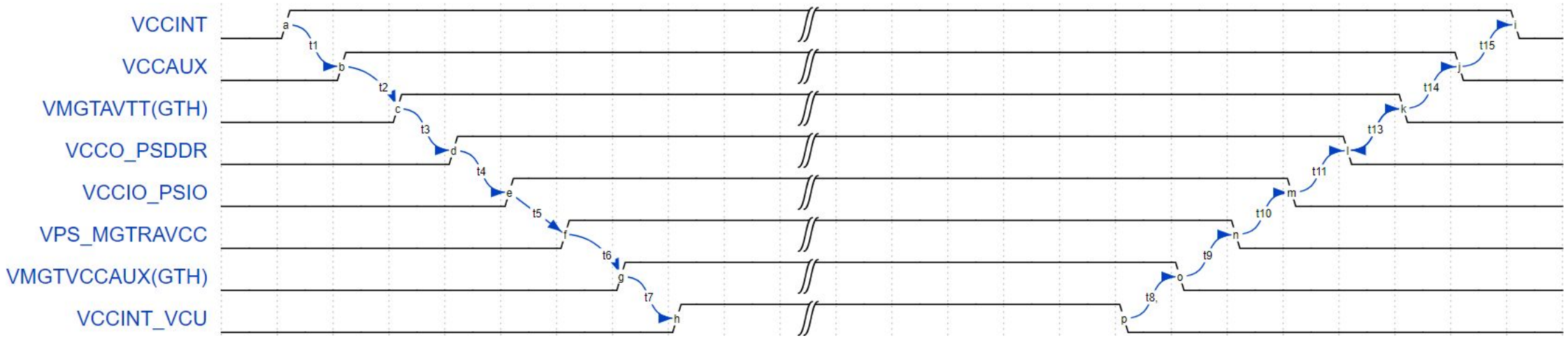
WebAmP Sequencer Graphic (IC2)



Integrated Sequencer Graphic (Turn ON/OFF)



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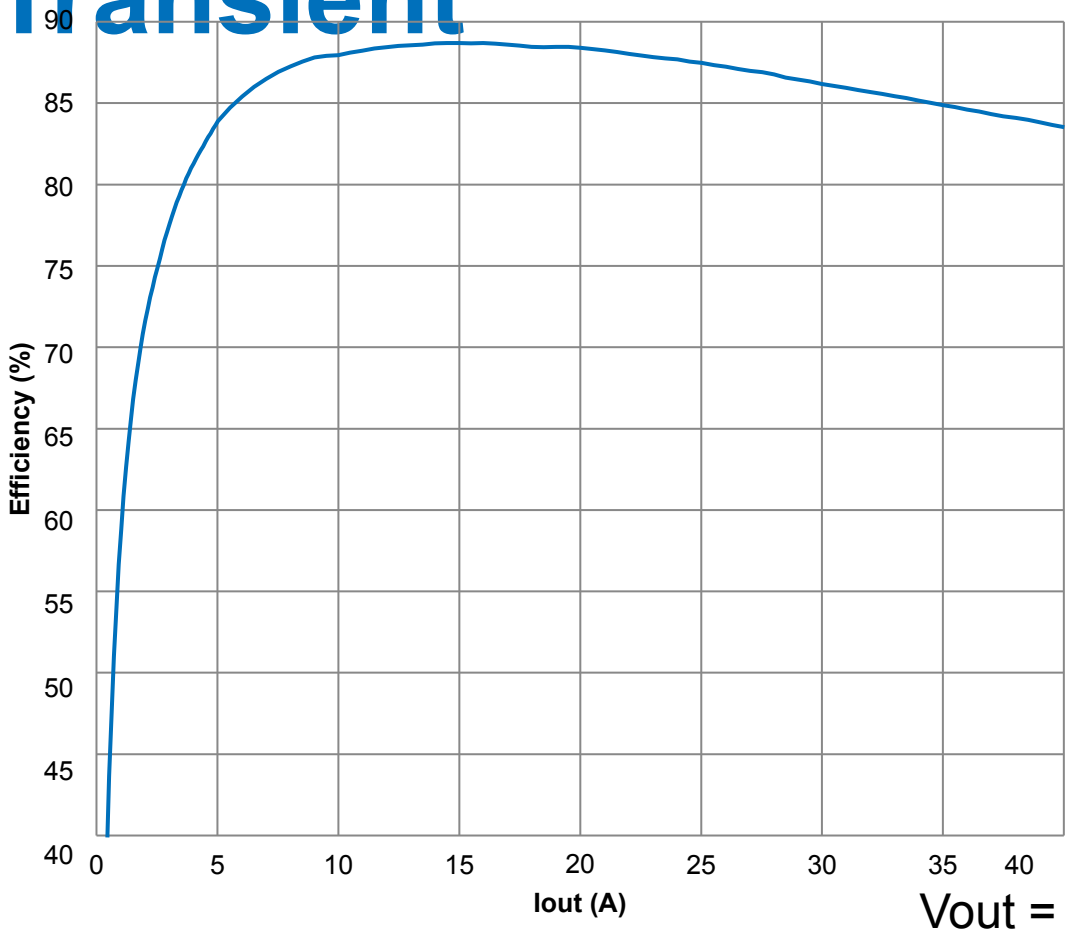
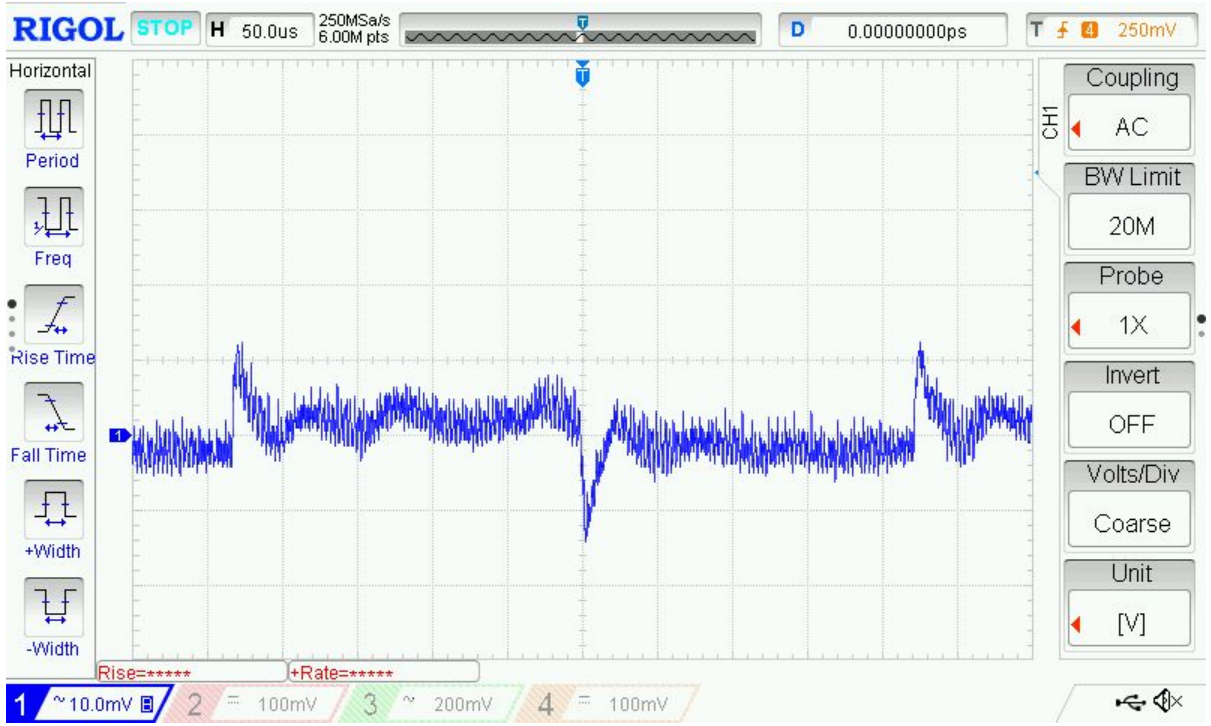
VCCINT: Efficiency & Transient





Vout = 0.85 V

Transient 26 A – 35.35 A @ 100 A/us V_{PP} = 26 mV

Lout = 250 nH, Cout = 20 x 47 µF

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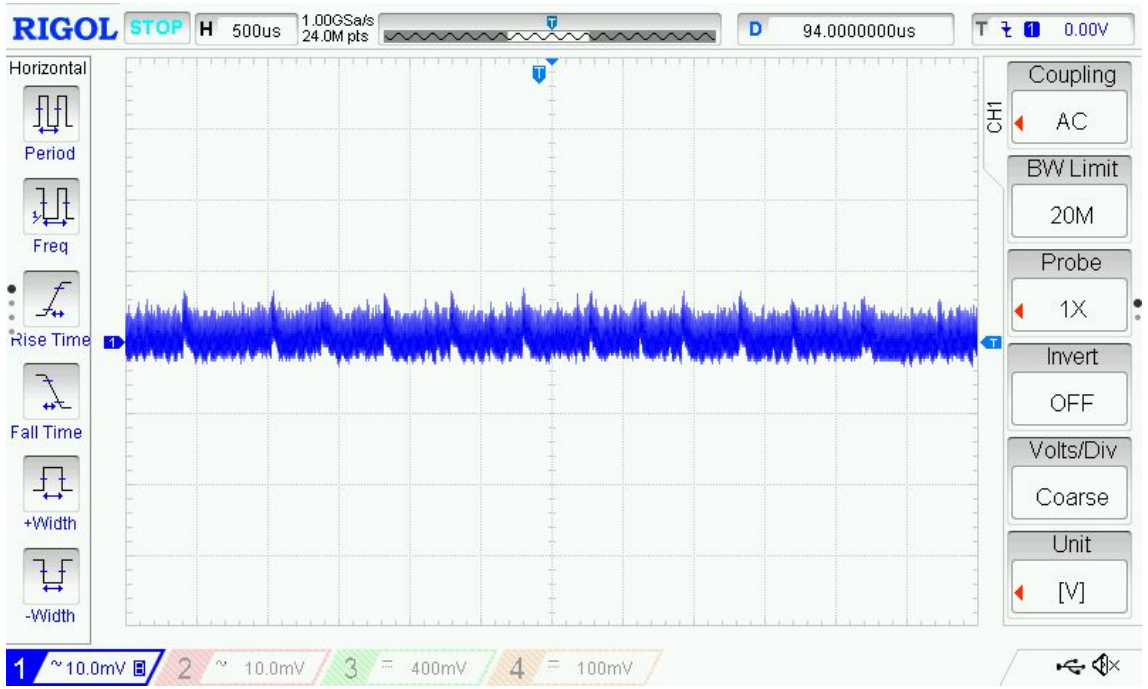
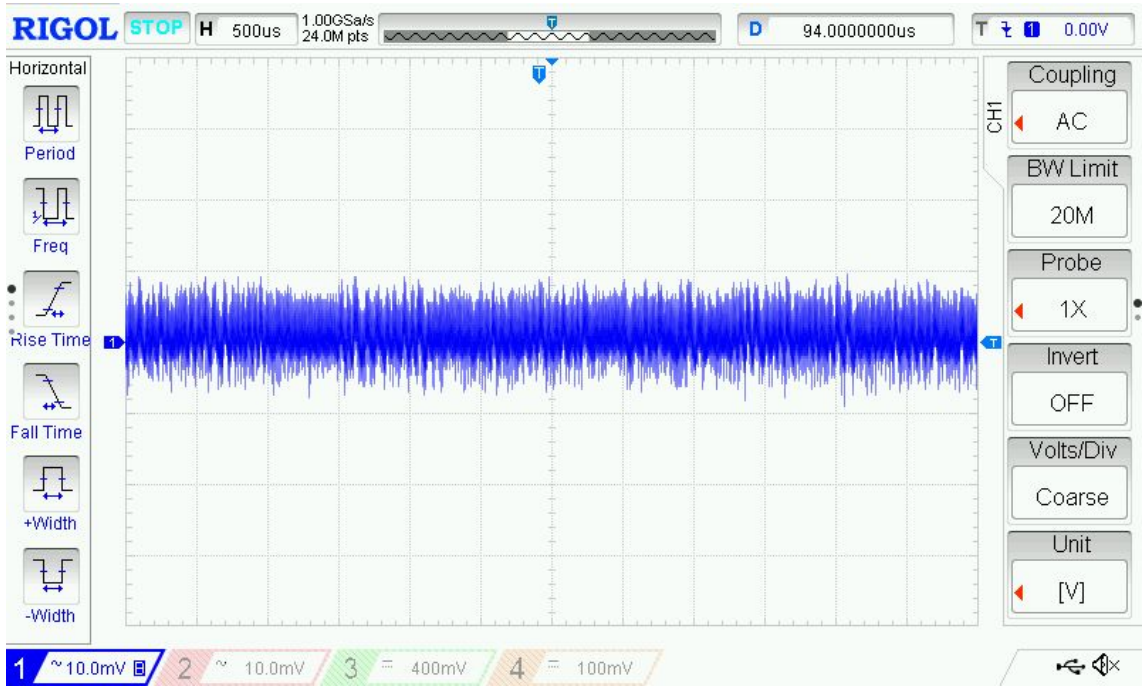
VCCINT: Ripple



No Load Ripple
V_{PP} = 10 mV



Ripple 40A Load
V_{PP} = 16.4 mV

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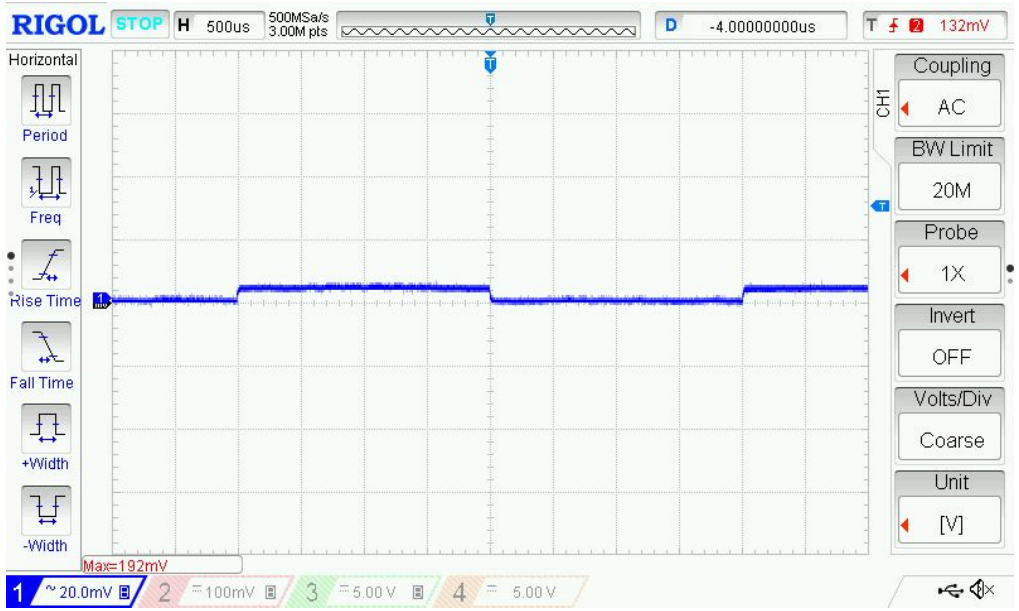
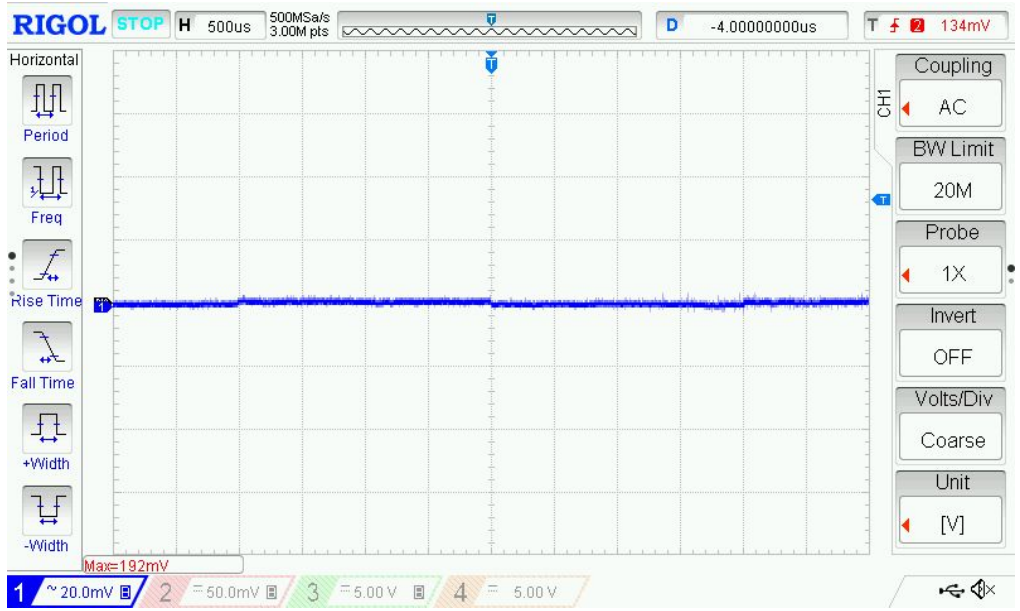
VCCO_PSDDR: Transient



Internal Feedback



External Feedback

Vout = 1.2 V
Transient 0.25 A to 0.5 A @ 10 A/us Cout = 22 µF

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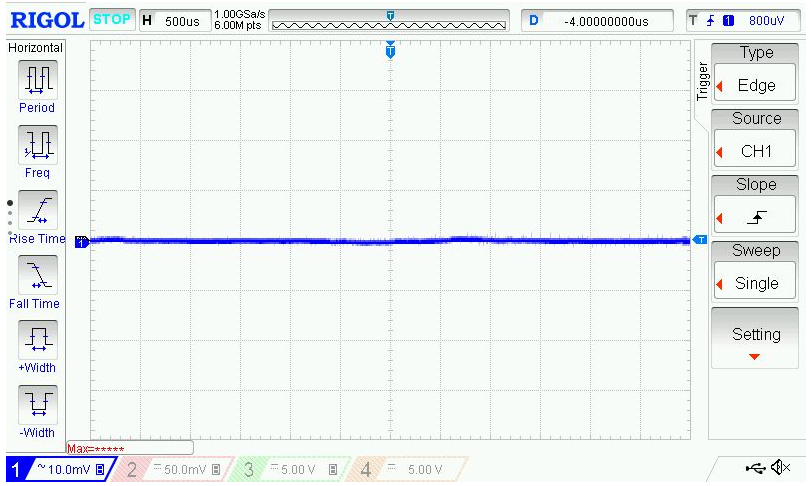
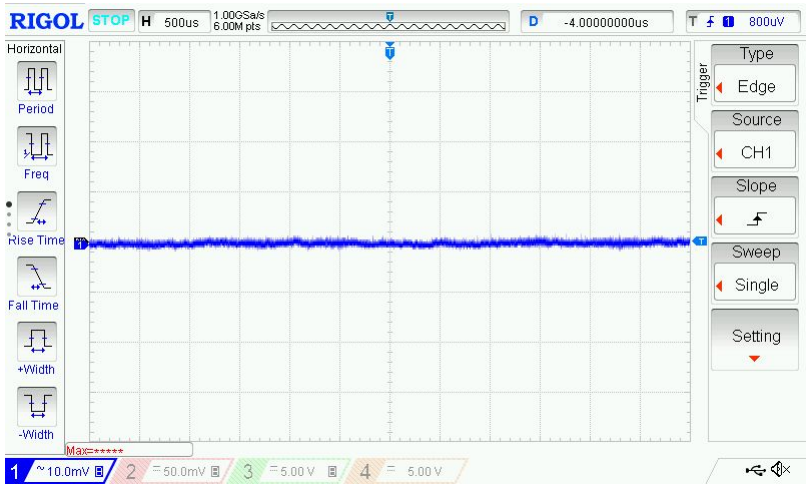
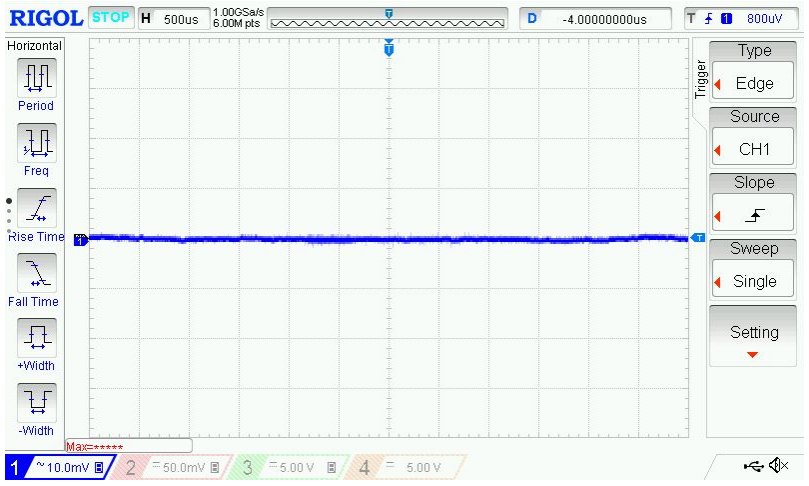
VCCO_PSDDR: Ripple



No Load Ripple



Ripple 100 mA Load



Ripple 500 mA Load

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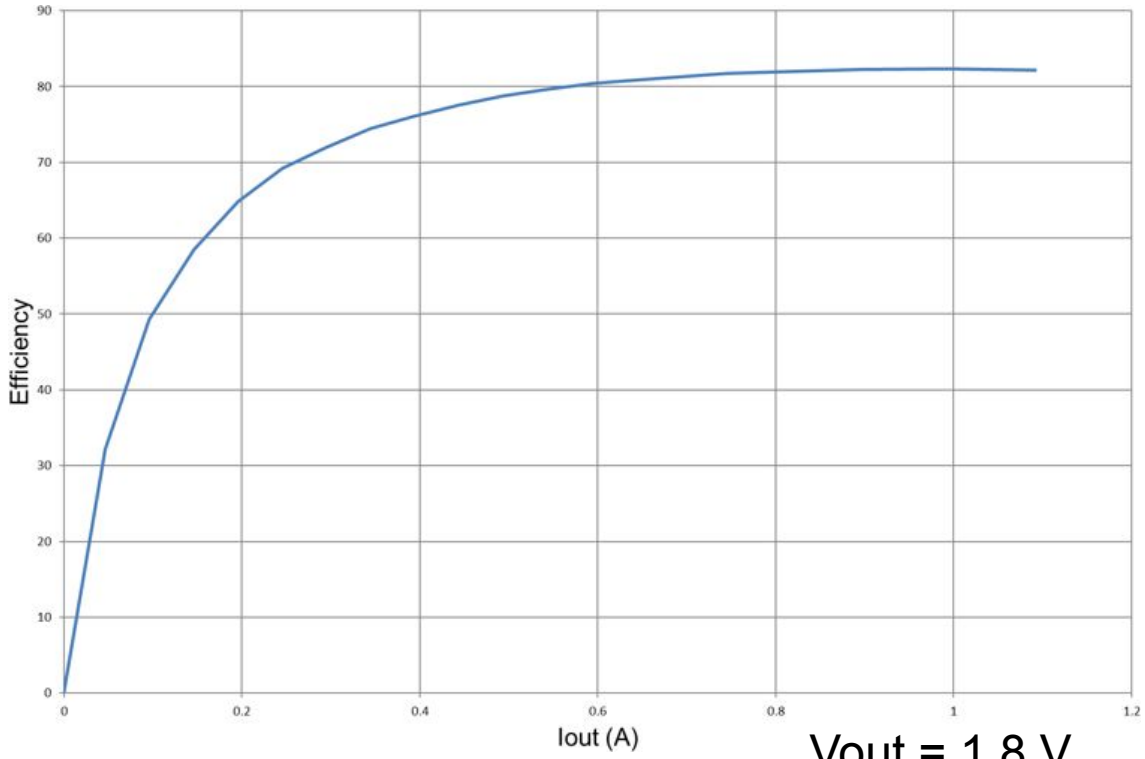
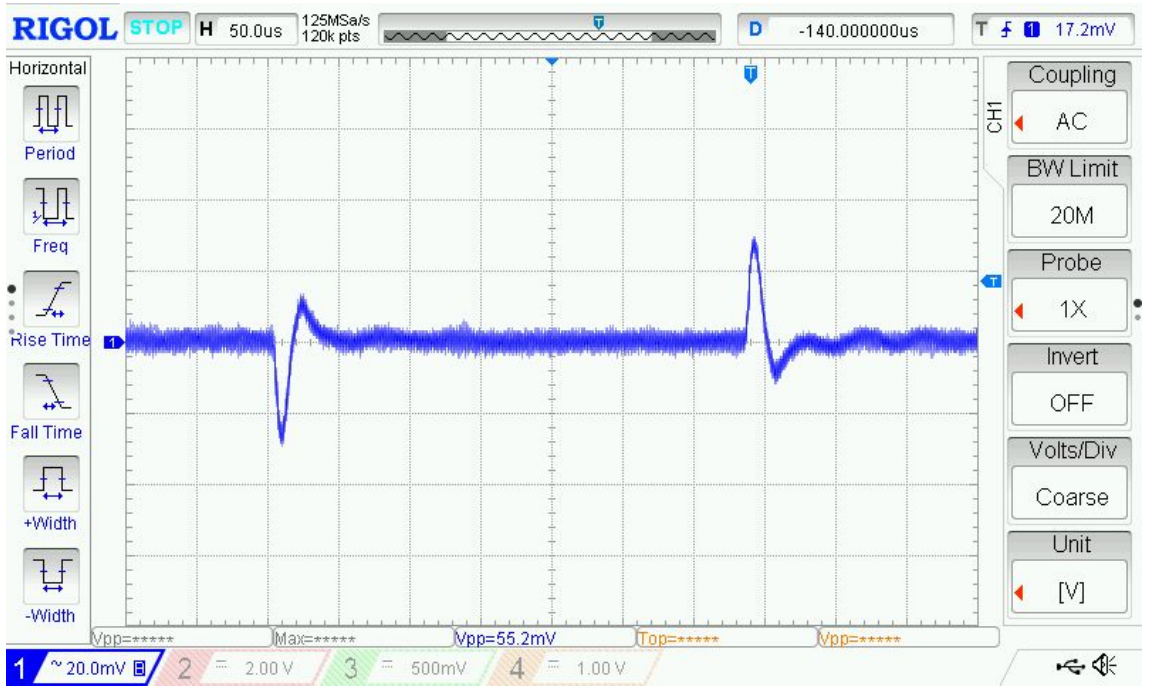
VCCAUX: Efficiency & Transient





Vout = 1.8 V
Transient 0.75A to 1A @ 10 A/us V_{PP} = 55.2 mV
Lout = 1.1 µH, Cout = 4 x 47 µF

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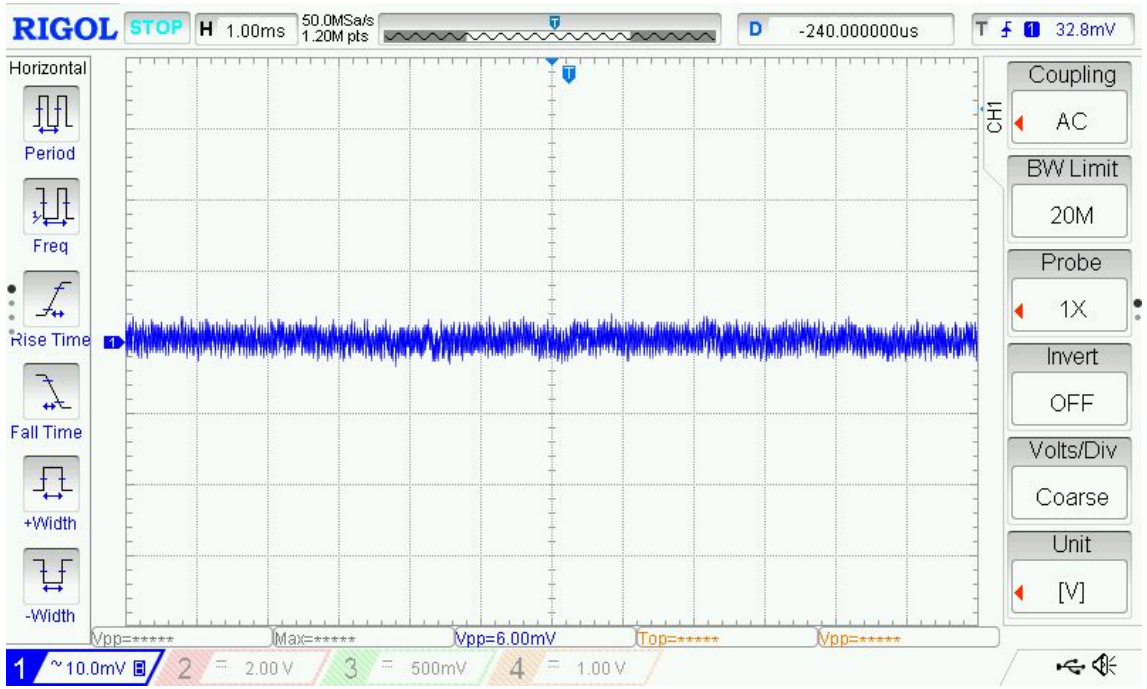
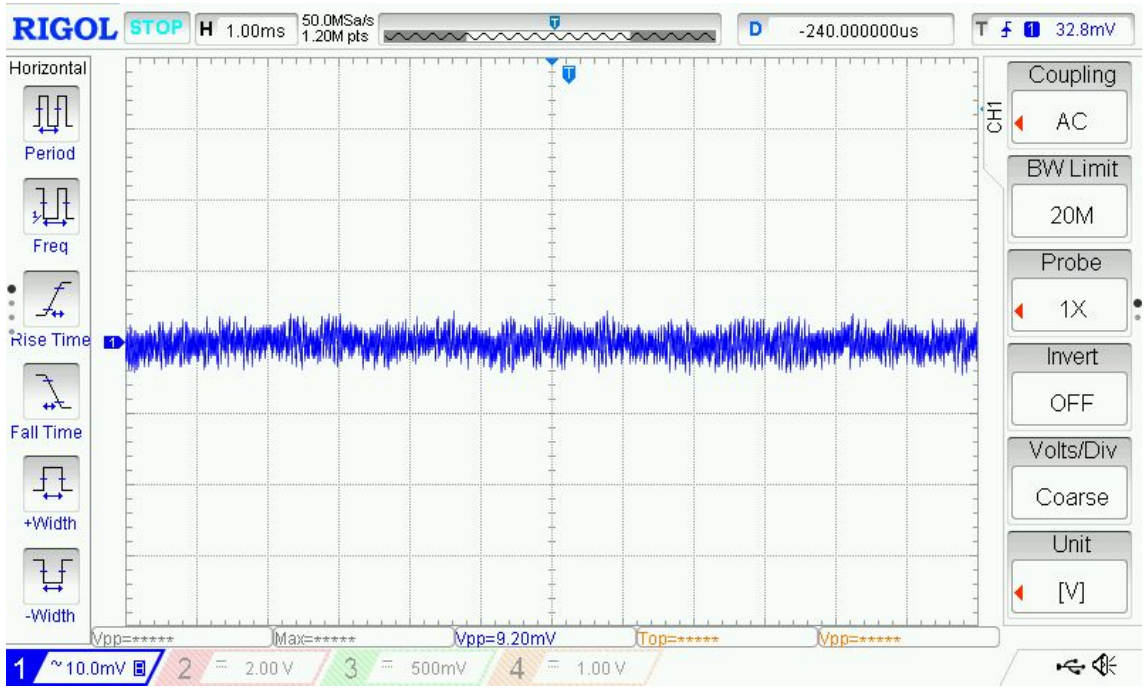
VCCAUX: Ripple



No Load

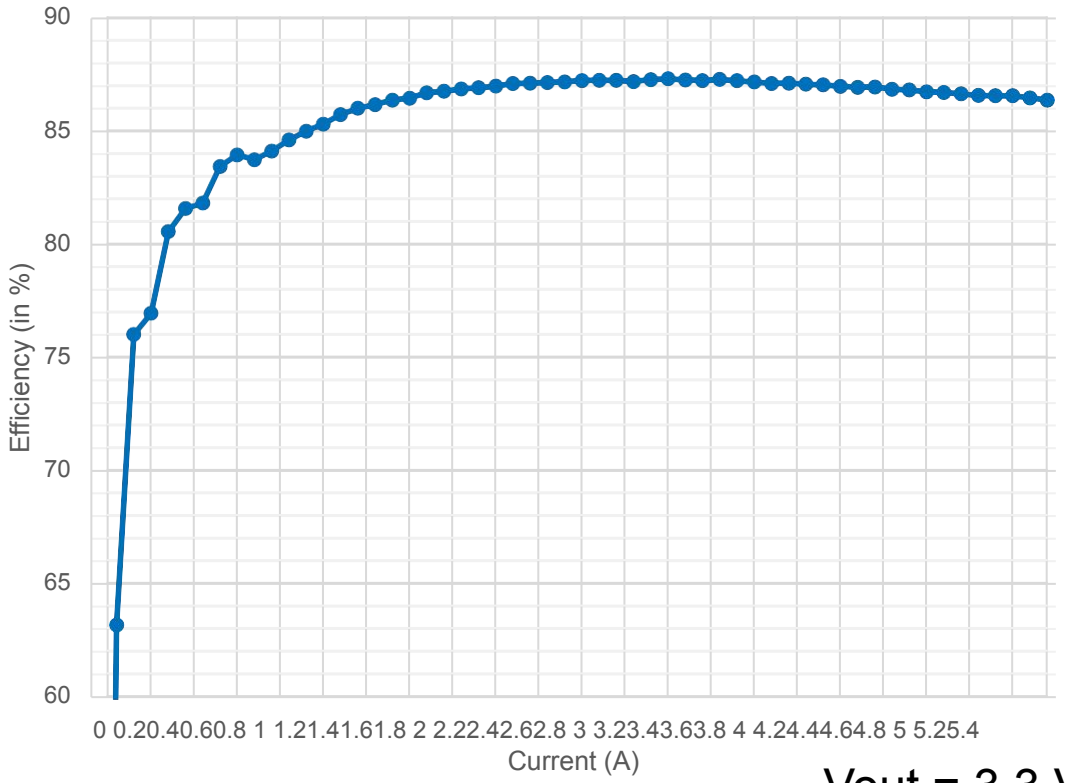
V_{PP} = 6 mV

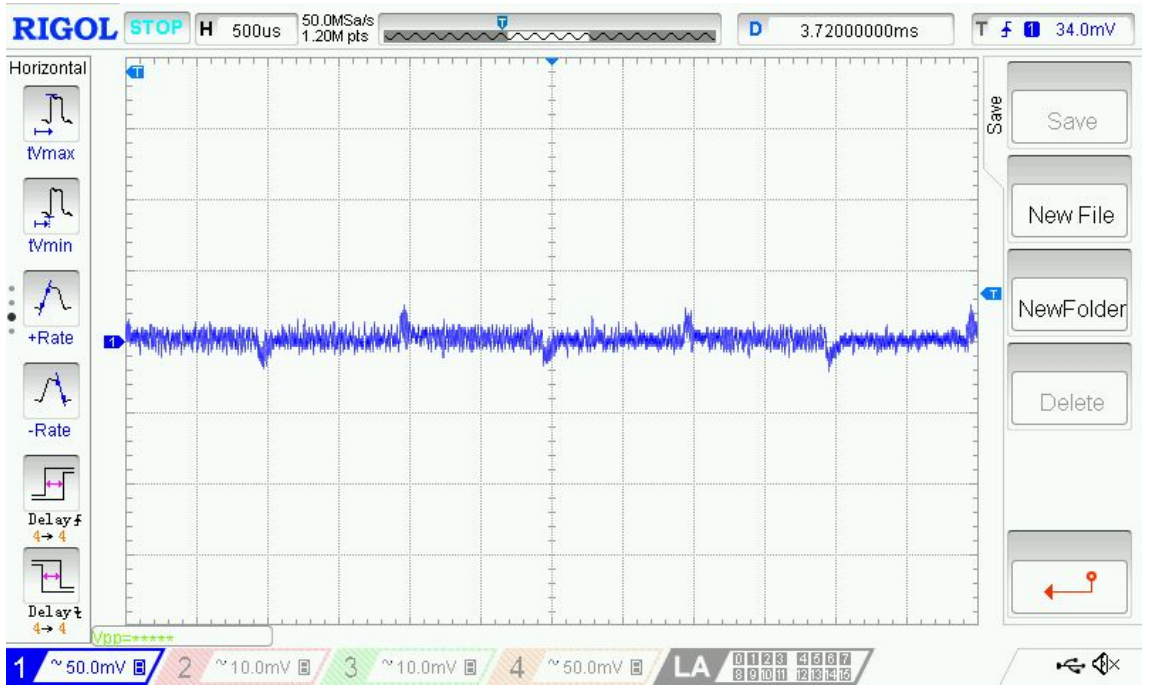


Full Load

V_{PP} = 9.2 mV

VCCO_PSIO: Efficiency & Transient





Vout = 3.3 V
Transient 0.15 A to 0.3 A @ 10 A/us V_{PP} = 42 mV
Lout = 47 µH, Cout = 10 µF

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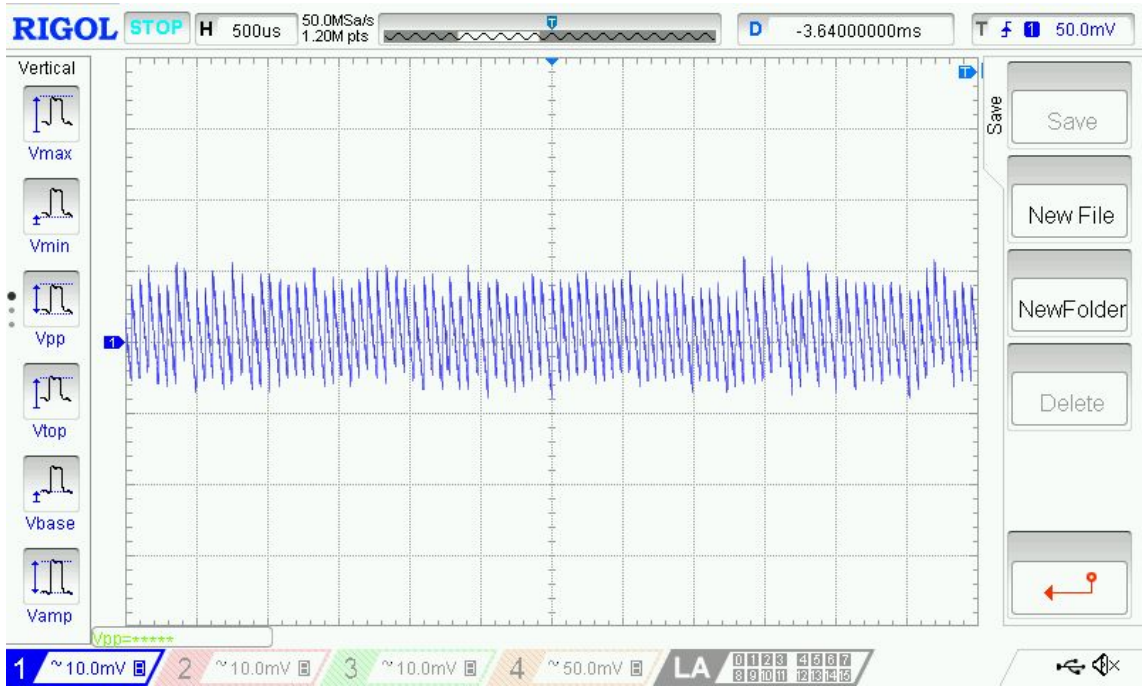
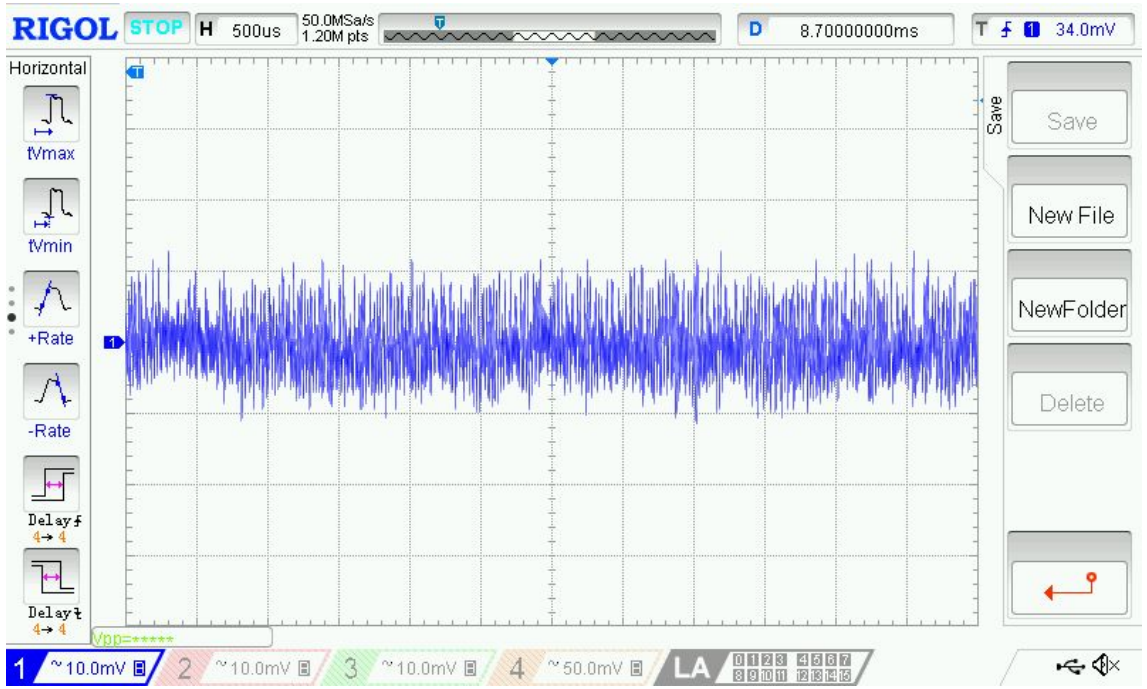
VCCO_PSIO: Ripple



No Load
V_{PP} = 19 mV



0.3 A Load
V_{PP} = 22 mV

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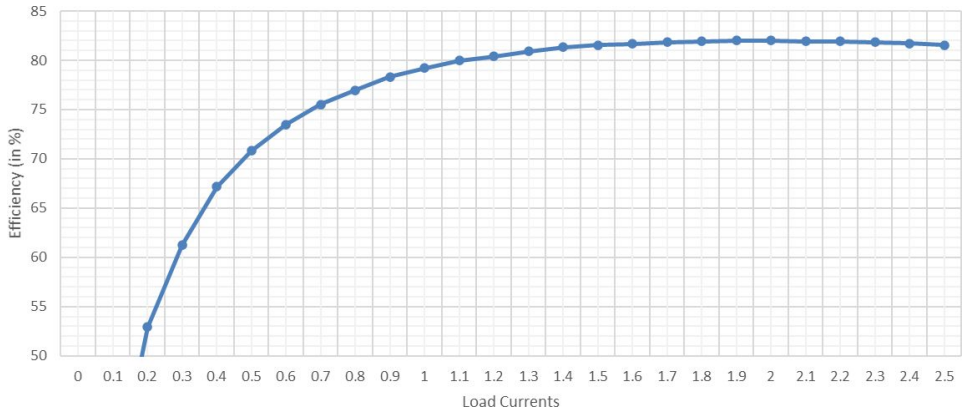
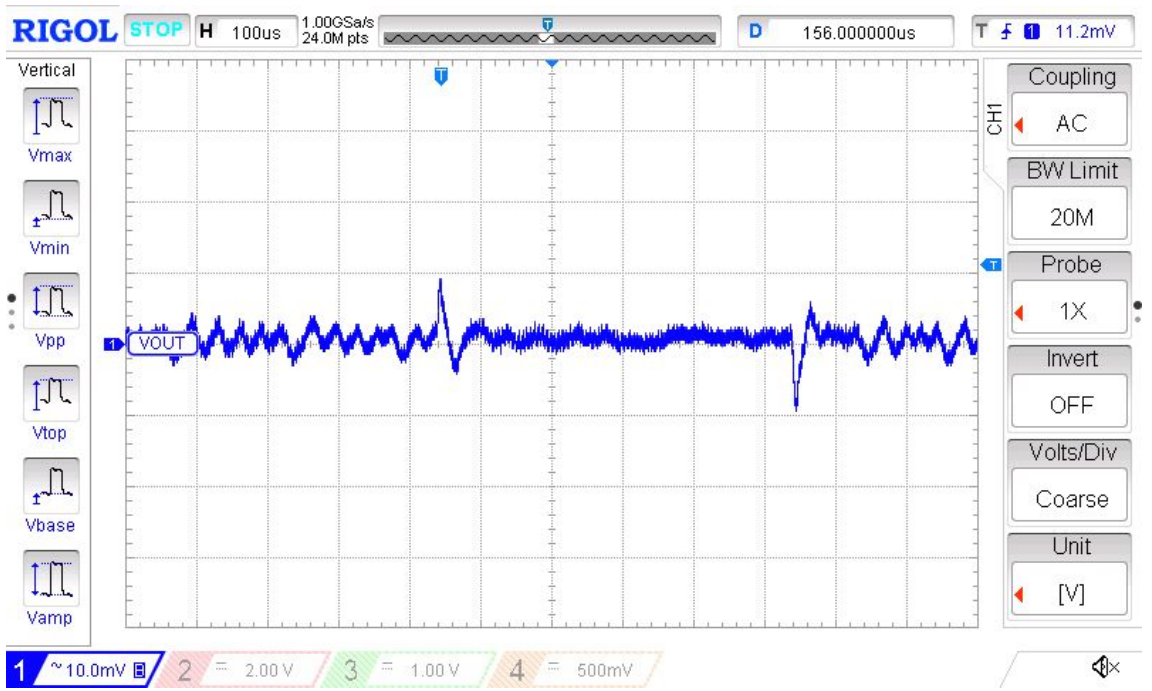
VCCINT_VCU: Efficiency & Transient





Vout = 0.9 V
Transient 1.5 A to 2 A @ 10 A/us
V_{PP} = 18.4 mV
Lout = 1.1 µH, Cout = 4 x 47 µF

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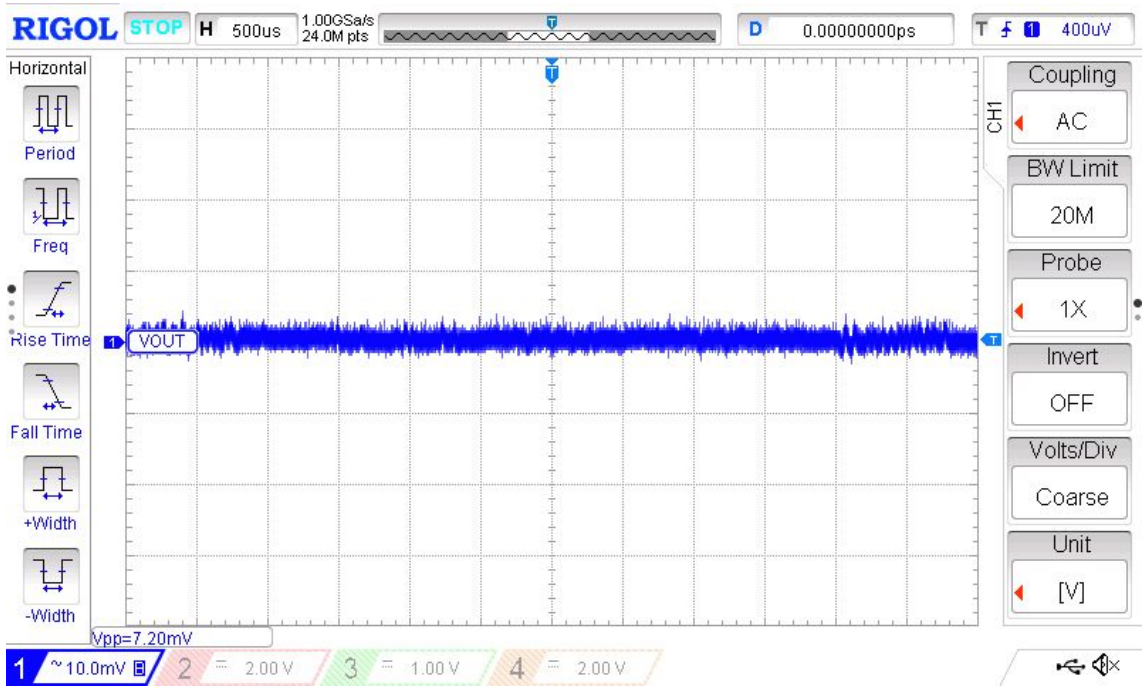
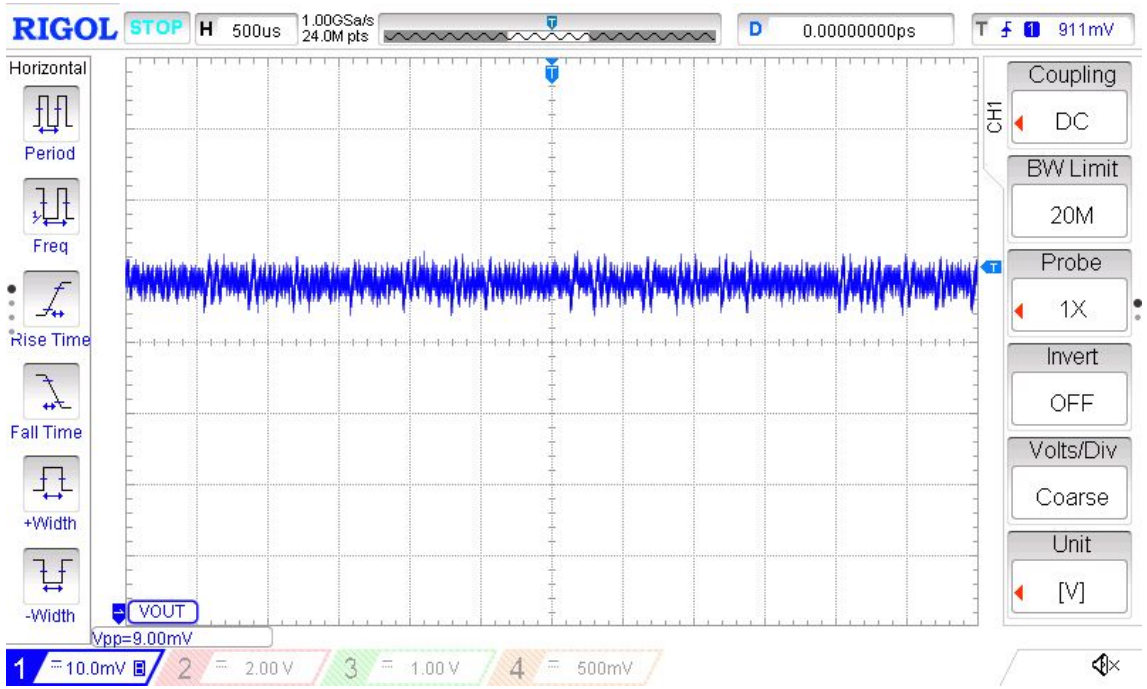
VCCINT_VCU: Ripple



No Load
V_{PP} = 7.2 mV



2 A Load
V_{PP} = 9.0 mV

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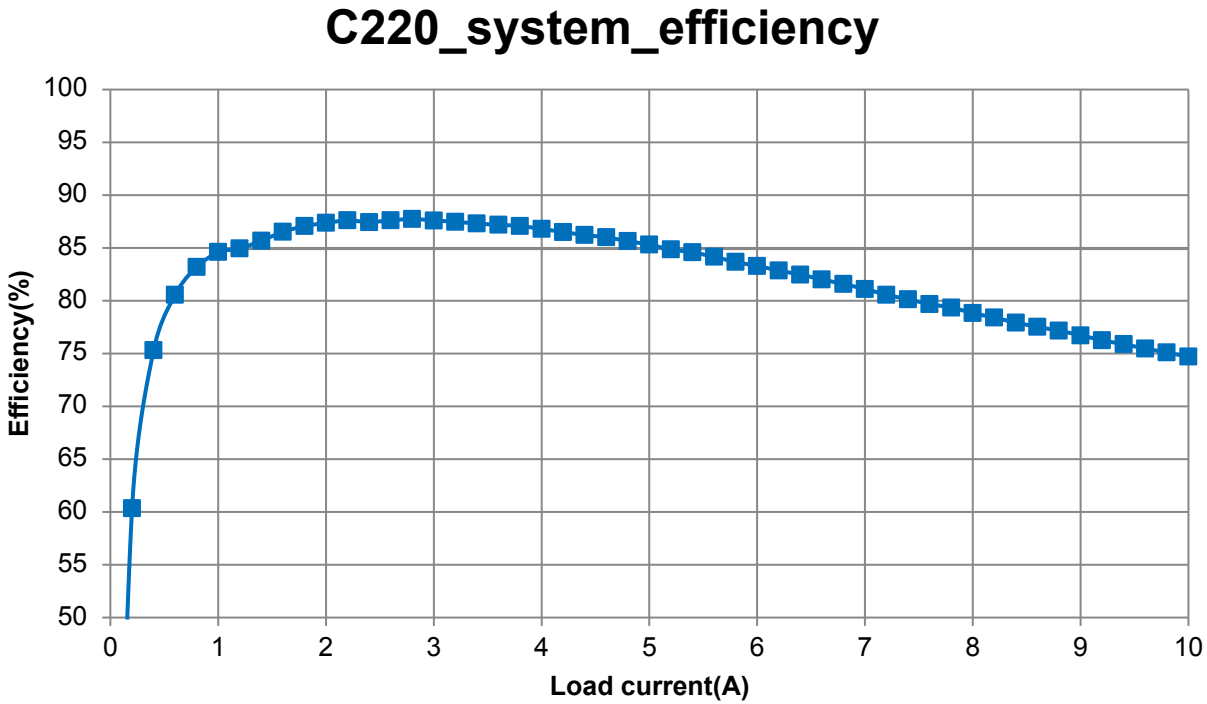
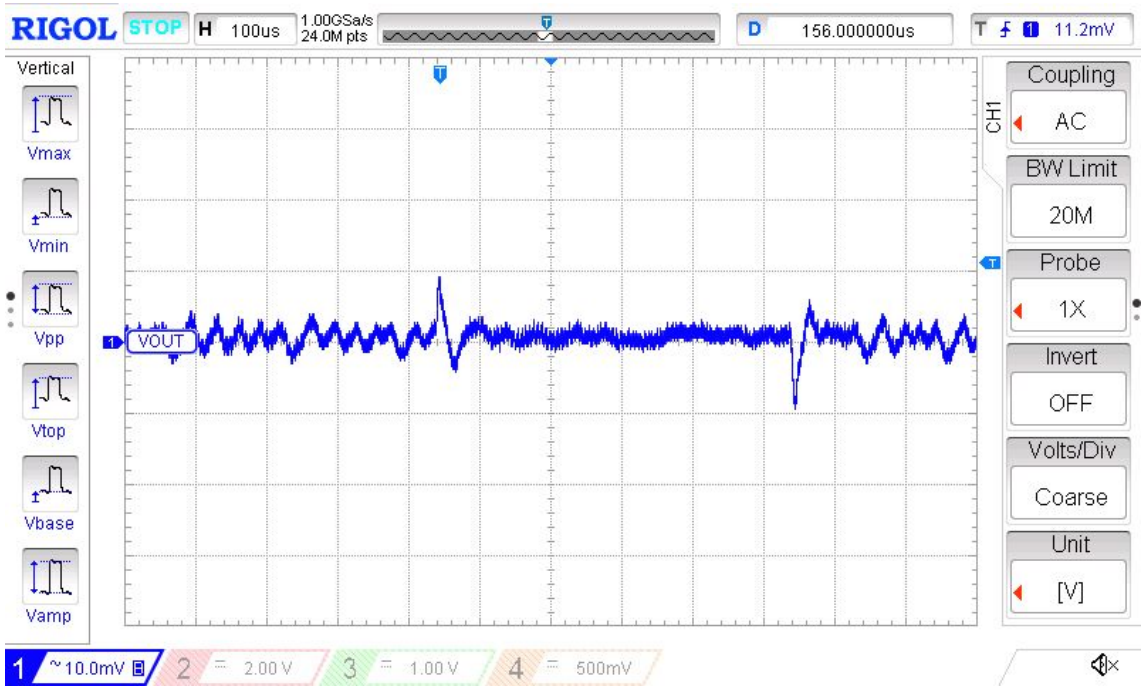
VMGTAVTT: Efficiency & Transient





Vout = 1.2 V
Transient 1.5 A to 2 A @ 10 A/us
V_{PP} = 18.4 mV
Lout = 0.72 µH, Cout = 4 x 47 µF

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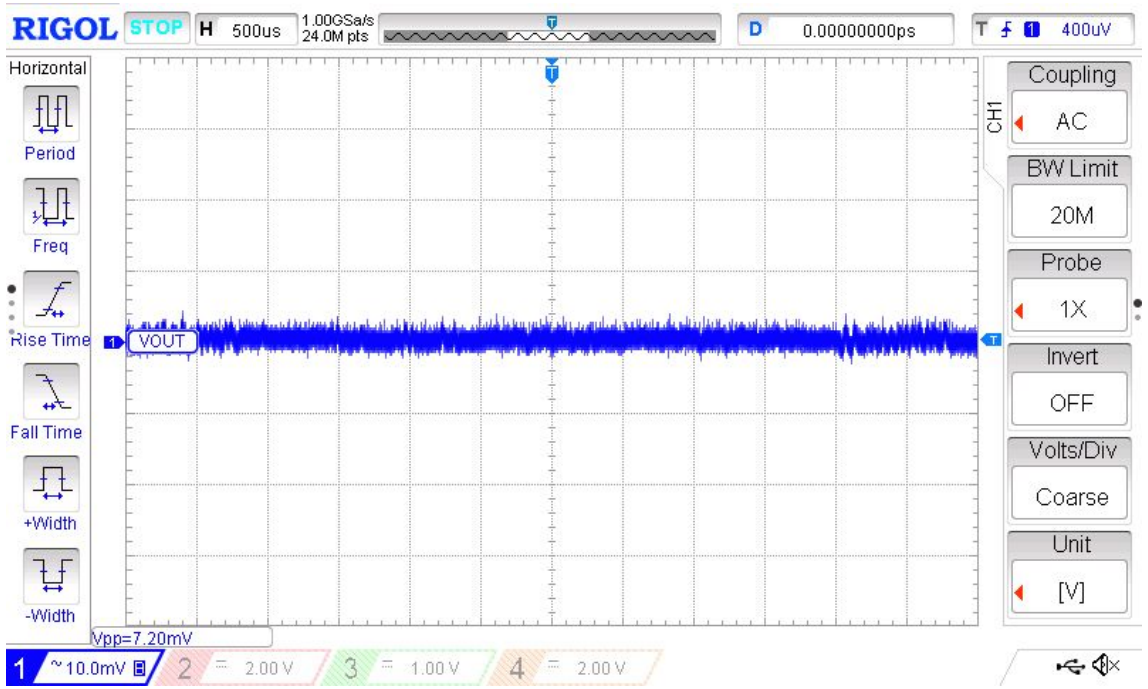
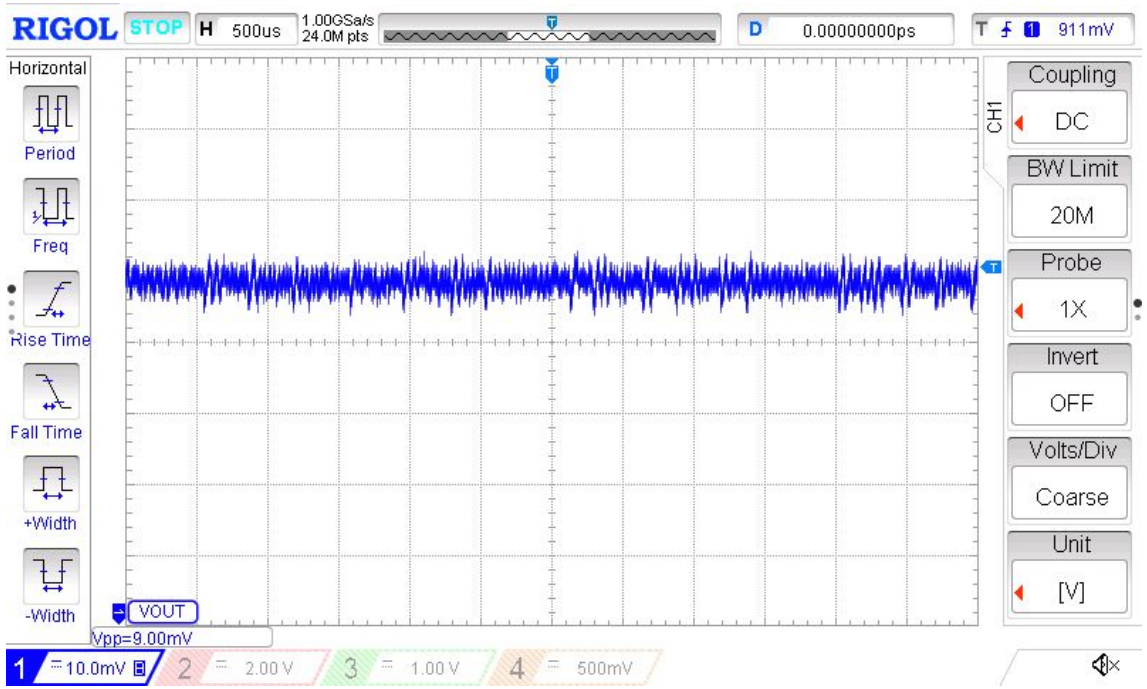
VMGTAVTT: Ripple

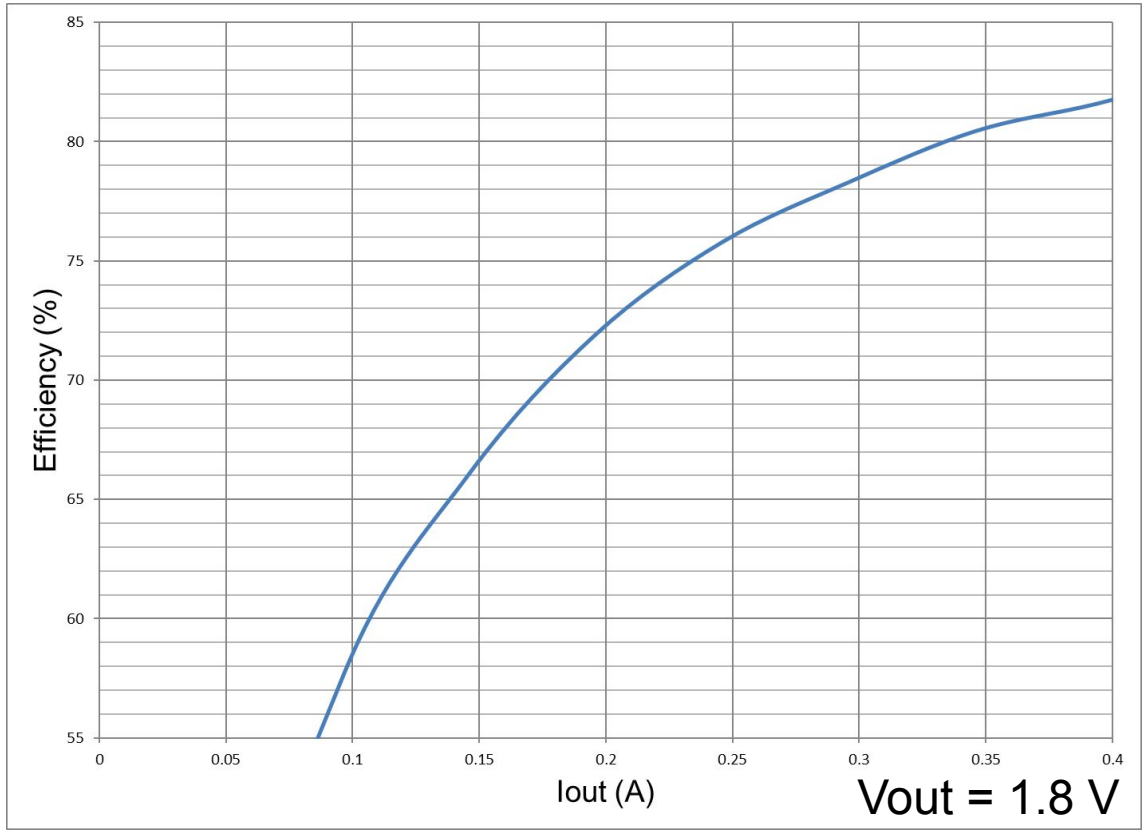


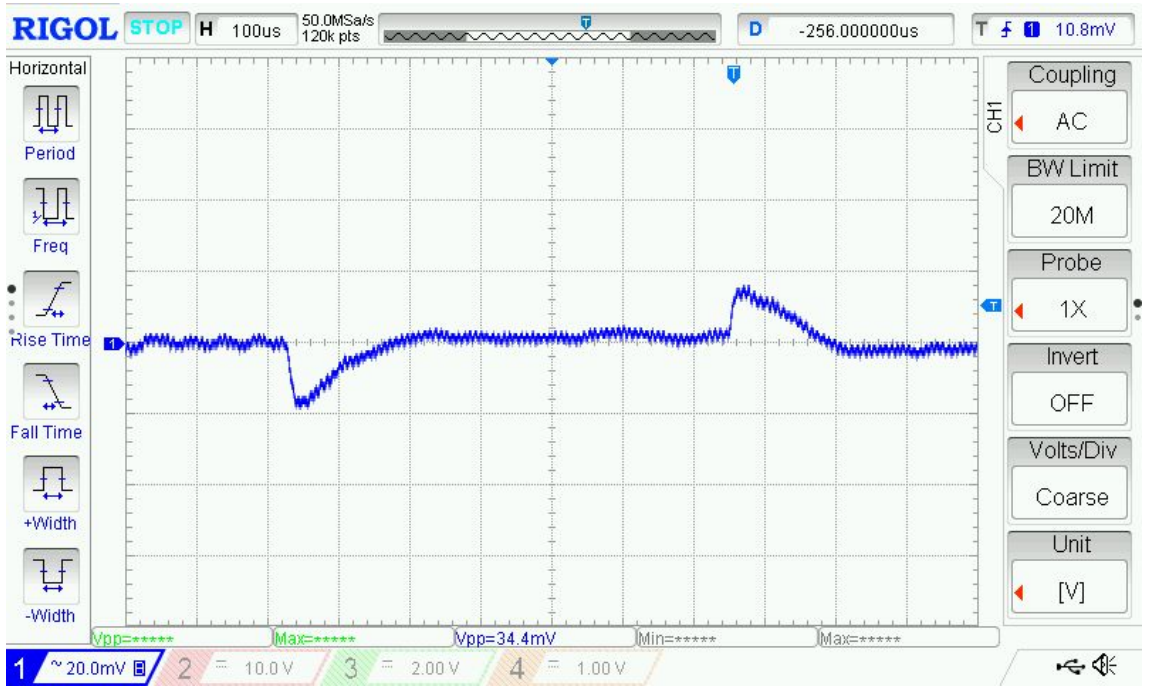
No Load
V_{PP} = 7.2 mV



2 A Load
V_{PP} = 9.0 mV

VMGTVCCAUX: Efficiency & Transient

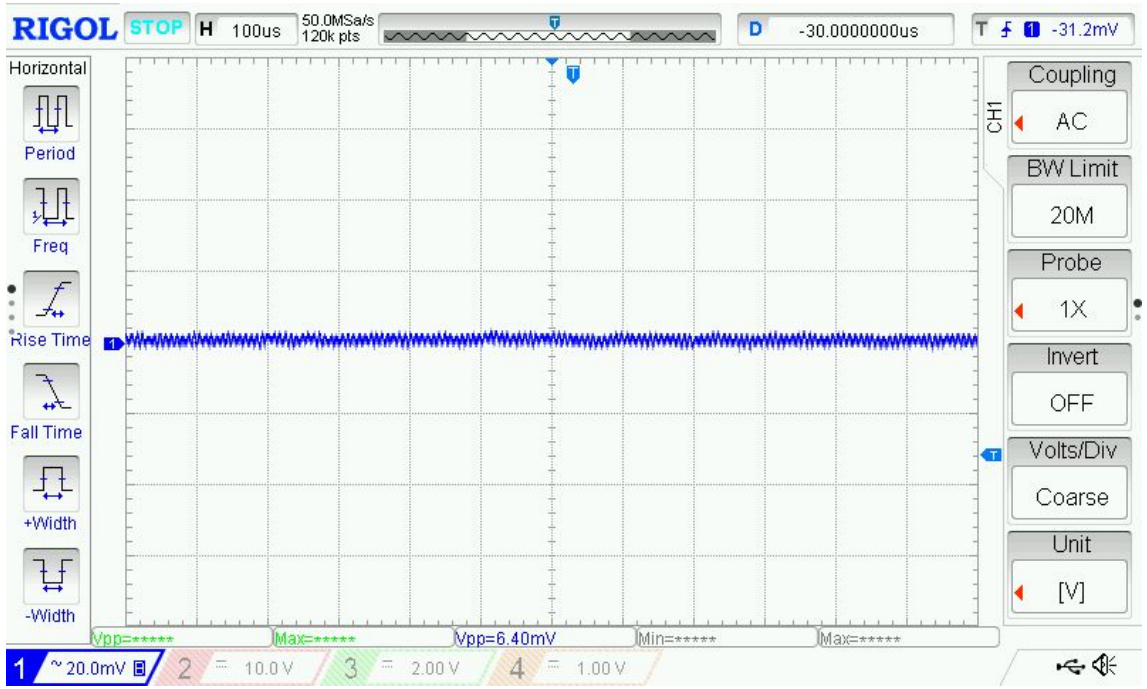




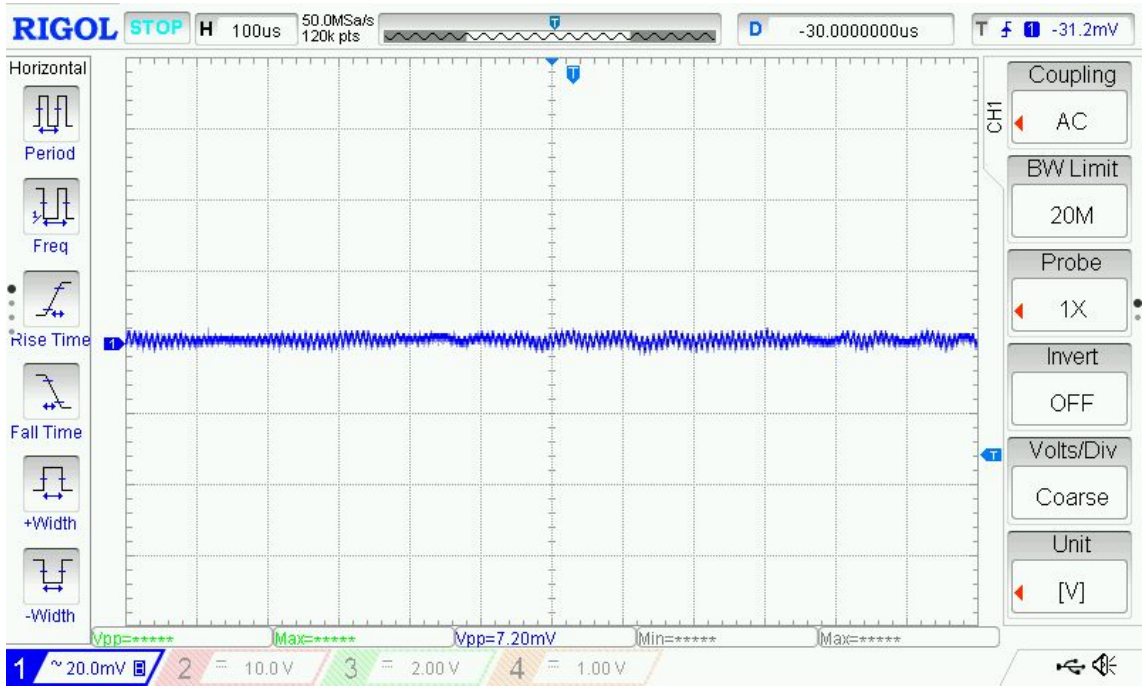
Vout = 1.8 V
Transient 0.12 A to 0.4 A @ 10 A/us V_{PP} = 42 mV
Lout = 10 µH, Cout = 47 µF

AnDAPT

VMGTVCCAUX: Ripple



No Load
V_{PP} = 6.4 mV



0.4 A Load
V_{PP} = 7.2 mV

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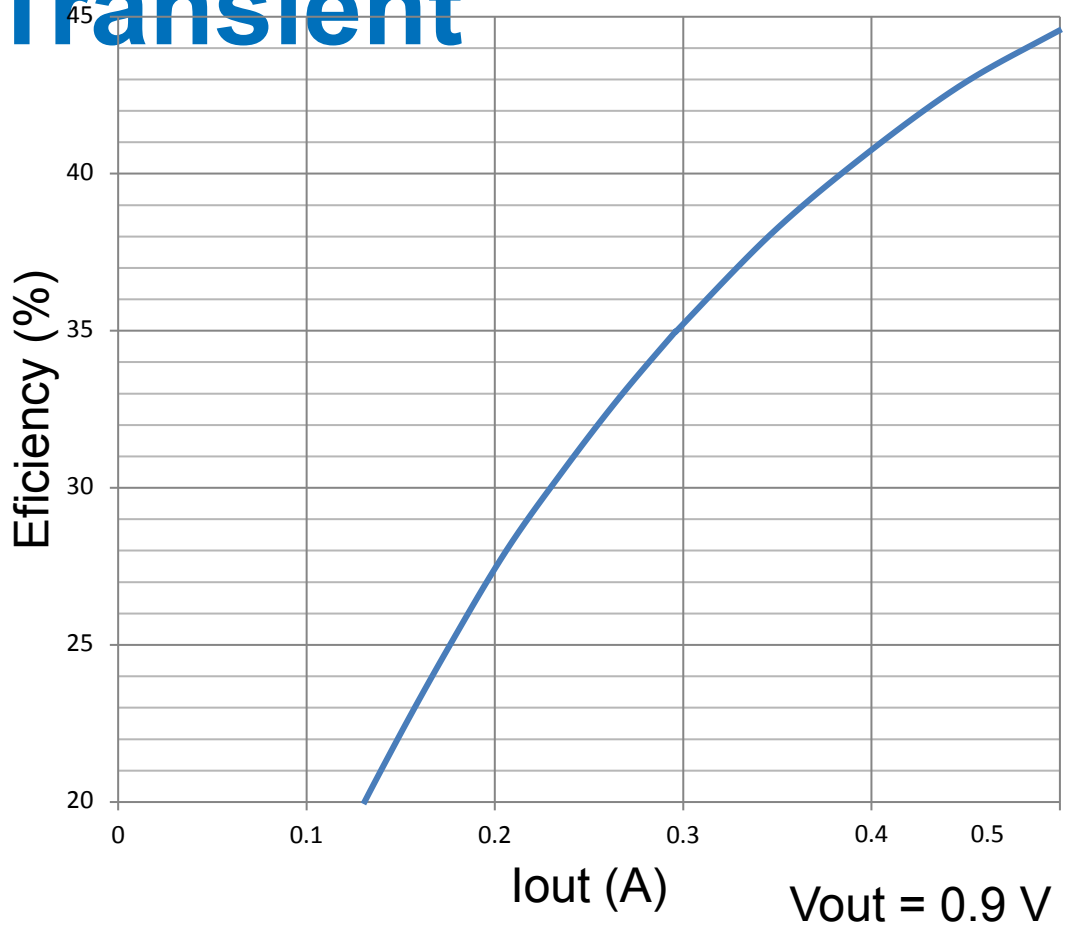
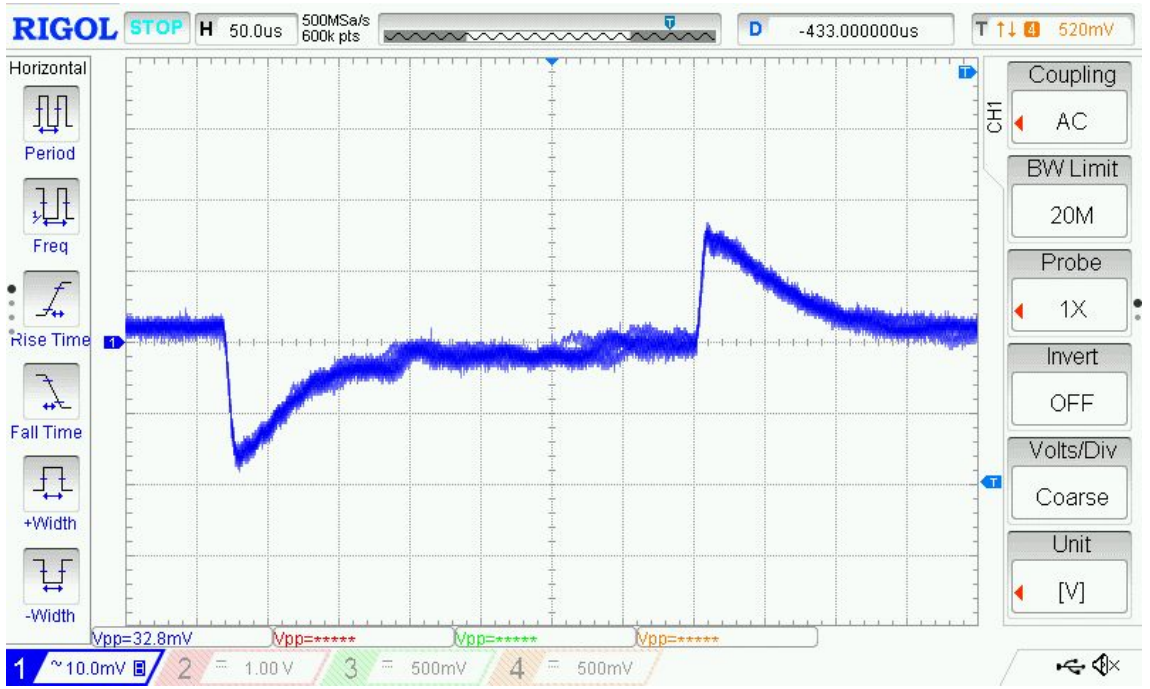
VMGTAVCC: Efficiency & Transient





Vout = 0.9 V
Transient 0.375 A to 0.5 A @ 10 A/us
V_{PP} = 32.8 mV
Lout = 10 µH, Cout = 1 x 47 µF

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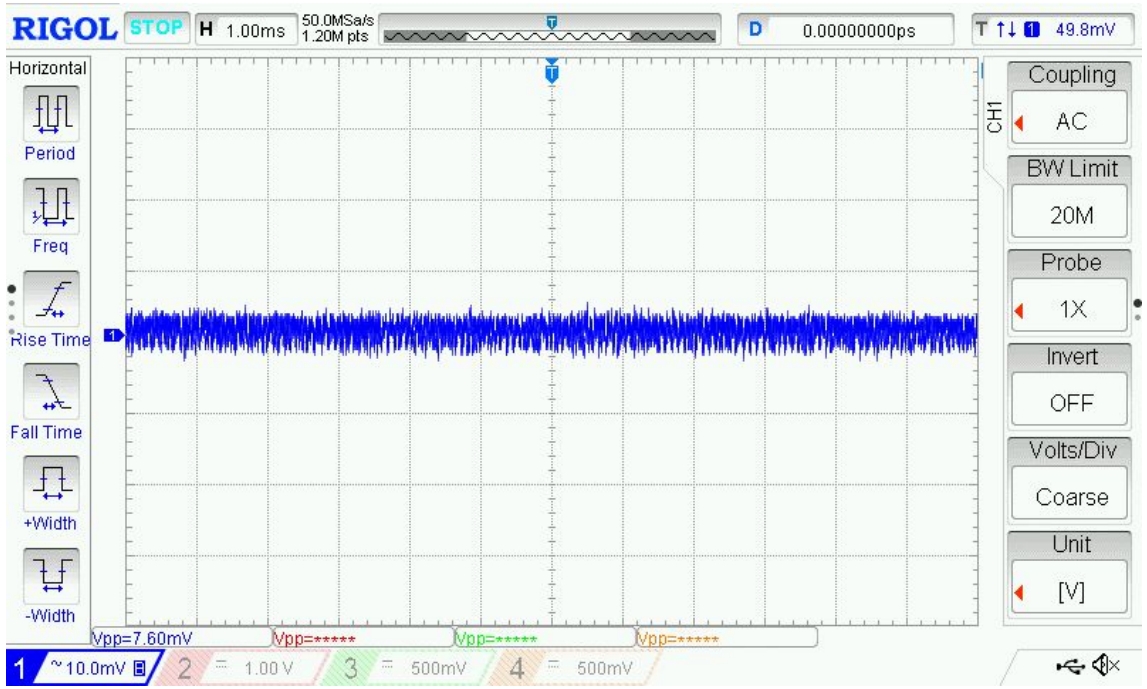
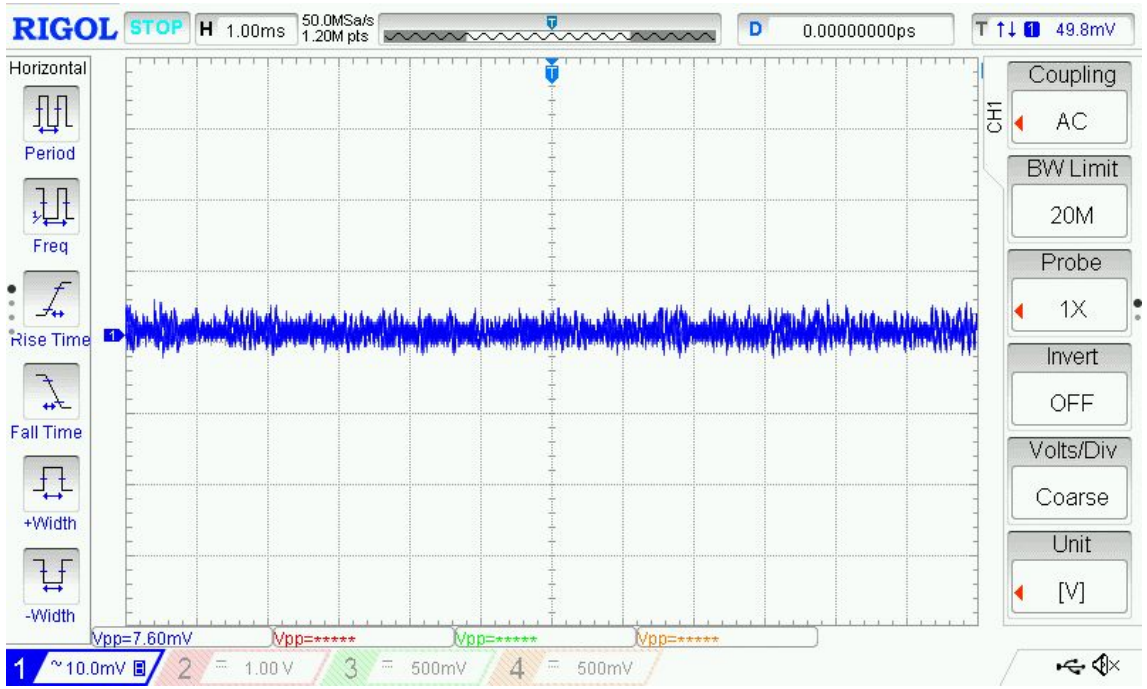
VMGTAVCC: Ripple



No Load
V_{PP} = 7.6 mV



2 A Load
V_{PP} = 10 mV

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Thank You

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