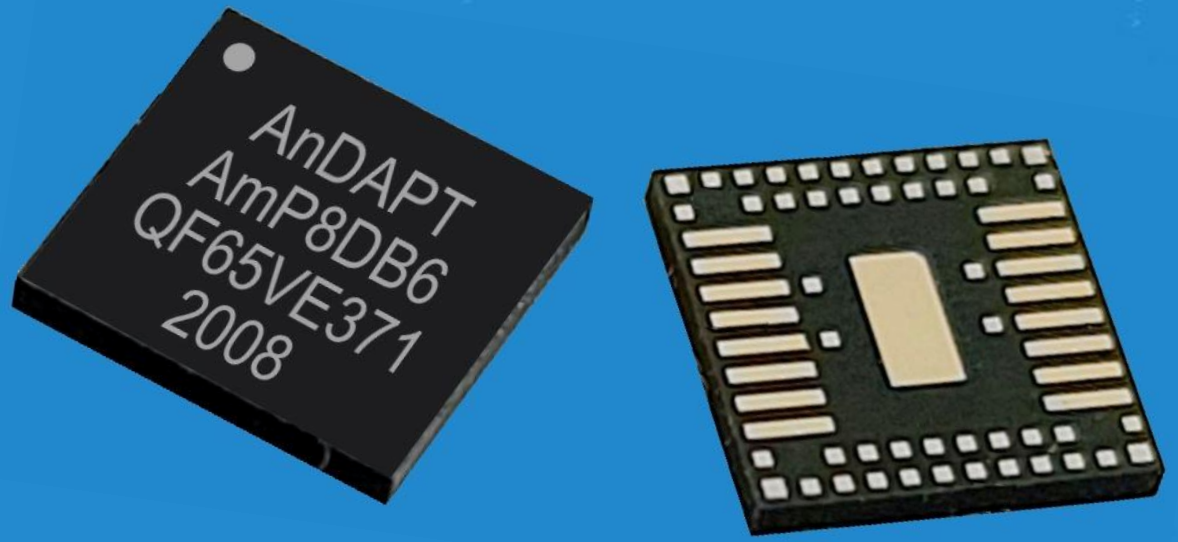


AnDAPT Power Solutions for Xilinx

Zynq Ultrascale+ MPSoC Mapping & Lab Data

Use-Case B1

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Zynq Ultrascale+ (ZU+) family of MPSoC devices' use-cases
- AnDAPT integrated power supply reference design availability for ZU+ MPSOC SKUs
- Lab data for each power rail for Cost-optimized with MGT rails (A2) use-case using AnDAPT PMICs

AnDAPT Confidential

Use-Cases (MPSoC Devices)

Devices (CG+EG+EV)	Cost-Optimized		Power Optimized	Performance Optimized	Full Power Management
	W/o MGT	With MGTs			
ZU2-ZU3	A1 (1x AnDAPT PMIC)	A2 (2x AnDAPT PMICs)	B (2x AnDAPT PMICs)	C (2x AnDAPT PMICs)	D1 (2x AnDAPT PMICs)
ZU4-ZU5					D2 (3x AnDAPT PMICs)
ZU6-ZU9					
ZU11-ZU19					

AnDAPT Confidential

AnDAPT

ZU+ MPSoC Rail Coverage with AmP Power Components

Use Case	SKU	VCCINT	VCCBRAM	VCCINT_IO	VCCINT_VCU	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	VCCAUX	VCCAUX_IO	VCCADC	VCC_PSAUX	VCC_PSDDR_PLL	VCC_PSADC	VMGTAVTT (GTH)	VMGTYATT (GTY)	VCC_PSPLL	VCCO_PSDDR	VCCO_PSIO	VPS_MGTRAVCC	VMGTVCCAUX (GTH)	VMGTYVCCAUX (GTY)	VPS_MGTRAVTT	VMGTAVCC (GTH)	VMGTYAVCC (GTY)	HDIOVCCO	HPIOVCCO
Cost-optimized	ZU2-ZU19 (w/o MGTs)	Rail 1			Rail 6	Rail 1			Rail 4						-	-	Rail 3	Rail 2	Rail 5	-	-	-	-	-	-	-	-
	ZU2-ZU19 (w MGTs)	Rail 1			Rail 5	Rail 1			Rail 3						Rail 6			Rail 2	Rail 4	Rail 7	Rail 8			Rail 9		-	-
Power-Optimized	ZU2-ZU19	Rail 1	Rail 2						Rail 4						Rail 3			Rail 8	Rail 5	Rail 9	Rail 6			Rail 7		-	-
Performance-Optimized	ZU2-ZU19	Rail 1			Rail 2	Rail 1			Rail 4						Rail 3			Rail 8	Rail 5	Rail 7	Rail 6			Rail 7		Rail 9	Rail 10
Full-Power Management	ZU2-ZU3	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	-	-	Rail 3	Rail 7	Rail 4	Rail 11	-	-	Rail 12	-	-	Rail 13	Rail 14
	ZU4-ZU19	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	Rail 13		Rail 3	Rail 7	Rail 4	Rail 11	Rail 15		Rail 12	Rail 14		Rail 16	Rail 17

C220 (Sync Buck HC)	
C200 (Sync Buck)	
C150 (Async Buck)	
C710 (SIM LDO)	
C750 (Load Switch)	
Corner LDO	

AnDAPT Confidential

AnDAPT

Zynq Ultrascale+ (ZU+) MPSoC Device SKUs Covered

CG Devices (Dual Application Processor)	**EG Devices** (Quad Application Processor & GPU)	**EV Devices** (Video Codec)
XCZU2CG	XCZU2EG	XCZU4EV
XCZU3CG	XCZU3EG	XCZU5EV
XCZU4CG	XCZU4EG	
XCZU5CG	XCZU5EG	
XCZU6CG	XCZU6EG	
XCZU7CG	XCZU9EG	
XCZU9CG	XCZU11EG	
	XCZU15EG	
	XCZU17EG	
	XCZU19EG	

List may not be exhaustive. Please contact AnDAPT for further details

AnDAPT Confidential

Zynq Ultrascale+ MPSoC (Always On, Power Optimized

Use Case: B1

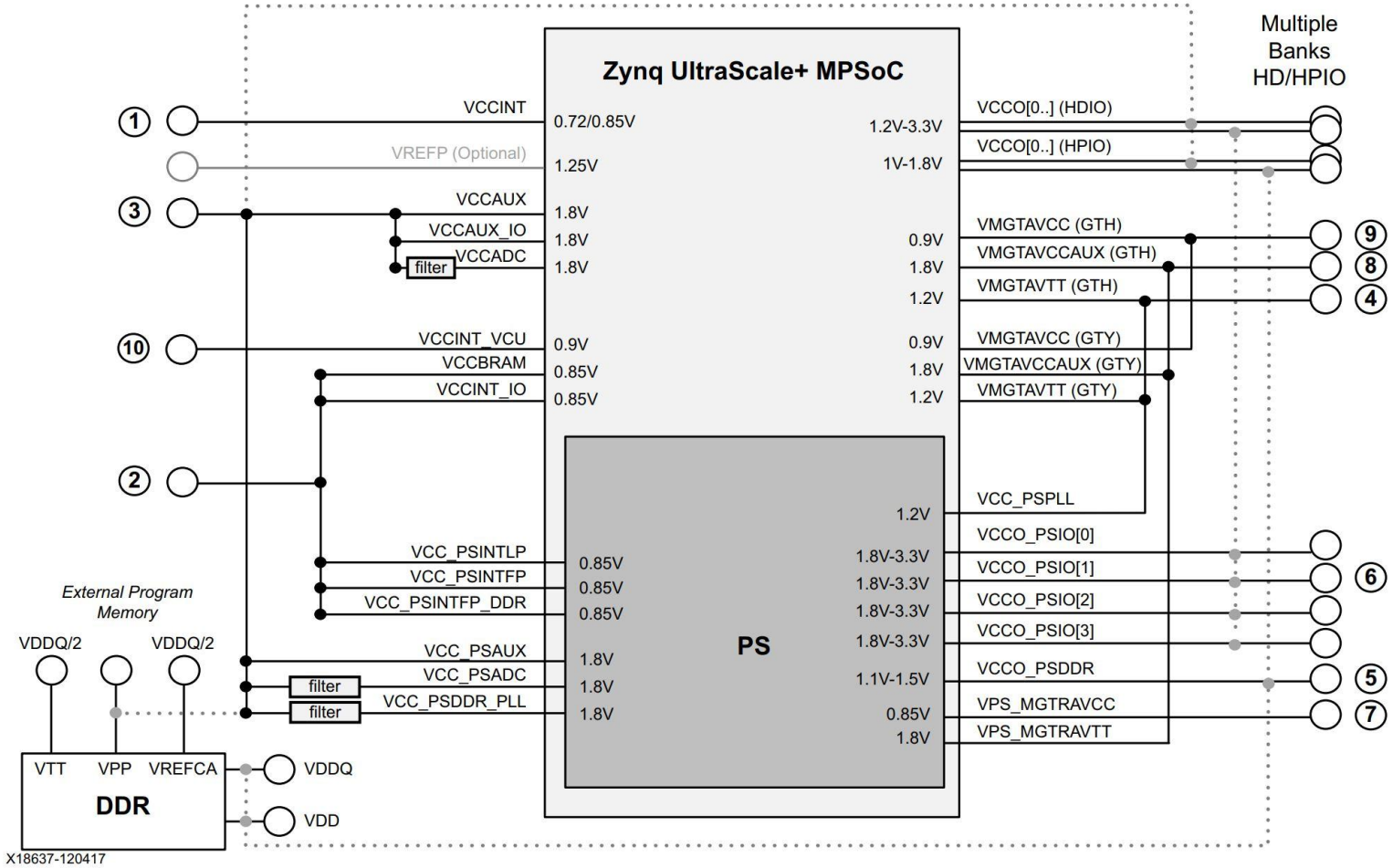


Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

AnDAPT Confidential

Power Tree- Use-Case: B1

V_{IN} = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCINT	1	C865	DrMOS Ctrl	V_{IN}	12	0.72	8.7	ARD_X_ZUM_B1_IC1
2	VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_VCU*	2	C220	Sync Buck HC	V_{IN}	12	0.85	9.55	ARD_X_ZUM_B1_IC1
3	VCC_PSPLL, VMGTAVTT(GTH), VMGTAVTT(GTY)	4	C200	Sync Buck	V_{IN}	12	1.2	1.4	ARD_X_ZUM_B1_IC1
4	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VCCO_HDIO, VCCO_HPIO	3	C200	Sync Buck	V_{IN}	12	1.8	1.04	ARD_X_ZUM_B1_IC1
5	VCCO_PSIO[3:0]	6	C200	Sync Buck	V_{IN}	12	1.8-3.3	0.3	ARD_X_ZUM_B1_IC2
6	VMGTAVCCAUX(GTH), VMGTAVCCAUX(GTY), VPS_MGTTRAVTT	8	C200	Sync Buck	V_{IN}	12	1.8	0.2	ARD_X_ZUM_B1_IC2
7	VMGTAVCC(GTH), VMGTAVCC(GTY)	9	C150	Async Buck	V_{IN}	12	0.9	1.3	ARD_X_ZUM_B1_IC2
8	VCCO_PSDDR	5	C200	Sync Buck	V_{IN}	12	1.1-1.5	0.5	ARD_X_ZUM_B1_IC2
9	VPS_MGTRAVCC	7	C710	LDO	VCCO_PSIO[3:0]	1.8	0.85	0.3	ARD_X_ZUM_B1_IC2

*Only required for EV devices

AnDAPT Confidential

AnDAPT

Power Tree- Use-Case: A2

V_{IN} = 12 V

#	Rail	Seq	Power Component	Vout (V)	Iout (A)	Comment
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR	1		0.85	35	
2	VCCO_PSDDR	1		1.1 – 1.5	0.5	User defined
3	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL	1		1.8	1.04	
4	VCCO_PSIO[0:3]	2		1.8 – 3.3	0.300	
5	VCCINT_VCU*	2		0.9	2	
6	VMGTAVTT(GTH), VMGTYAVTT(GTY), VCC_PSPLL	1		1.2	2.6-10.6	
7	VPS_MGTRAVCC	1		0.85/0.9	0.3	
8	VMGTVCCAUX(GTH), VMGTYVCCAUX(GTY), VPS_MGTRAVTT	1		1.8	0.2	
9	VMGTAVCC(GTH), VMGTYAVCC(GTY)	1		0.9	0.5	

*Only required for EV devices

AnDAPT Confidential

AnDAPT

Power Tree Mapping- Use Case: A2

V_{IN} = 12 V

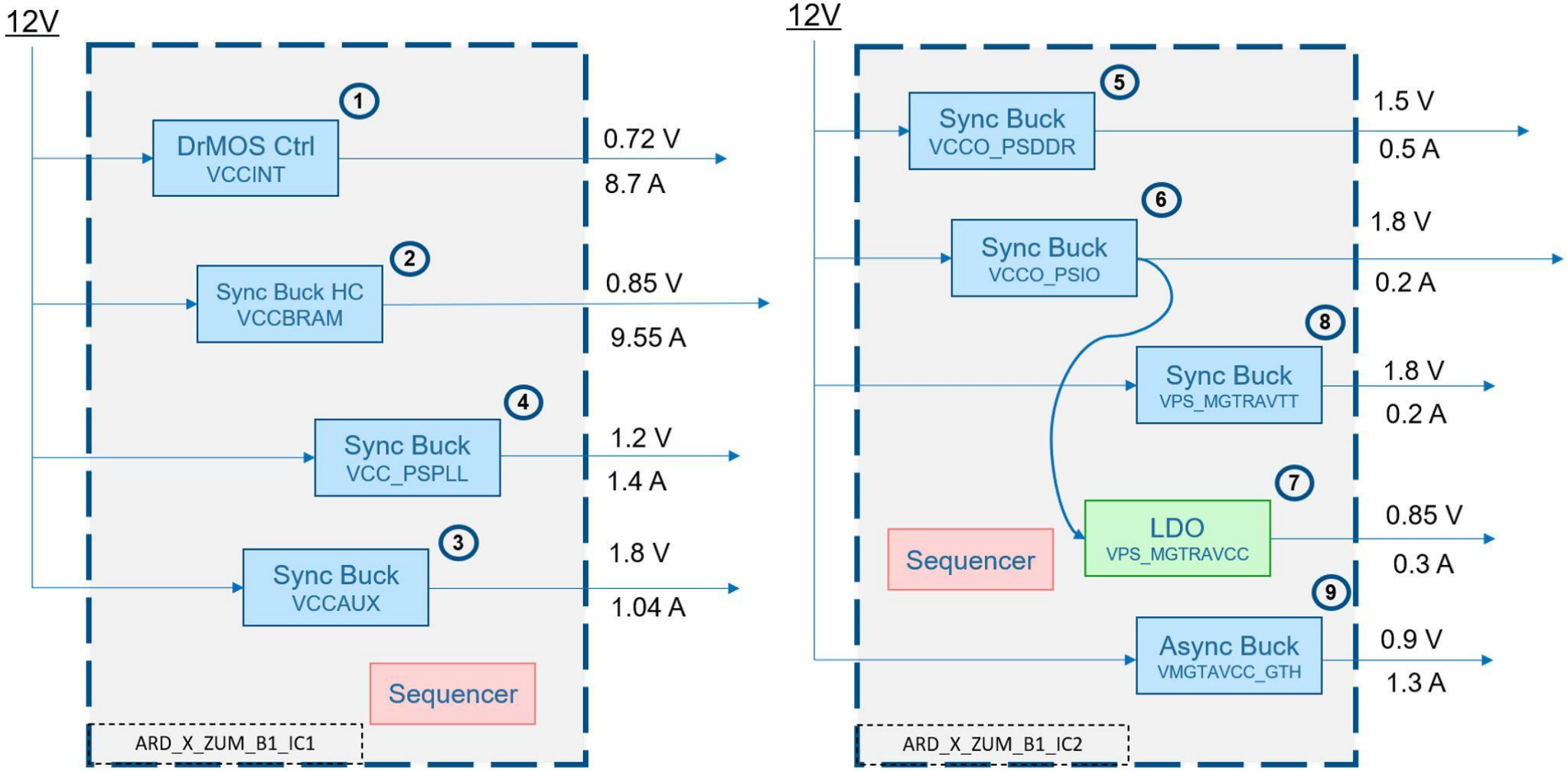
#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR	1	C860	DrMOS Ctrl	V_{IN}	12	0.85	35	ARD_X_ZUM_A2_IC1
2	VCCO_PSDDR	4	C710	SIM LDO	VCCAUX	1.8	1.1 – 1.5	0.5	ARD_X_ZUM_A2_IC1
3	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VCCO_HDIO, VCCO_HPIO	2	C200	Sync Buck	V_{IN}	12	1.8	1.04 + 0.5	ARD_X_ZUM_A2_IC1
4	VCCO_PSIO[0:3]	5	C200	Sync Buck	V_{IN}	12	1.8 – 3.3	0.300	ARD_X_ZUM_A2_IC2
5	VCCINT_VCU*	9	C200	Sync Buck	V_{IN}	12	0.9	2	ARD_X_ZUM_A2_IC2
6	VMGTAVTT(GTH), VMGTYAVTT(GTY), VCC_PSPLL	3	C220	Sync Buck HC	V_{IN}	12	1.2	2.6-10.6	ARD_X_ZUM_A2_IC1
7	VPS_MGTRAVCC	6	CLDO	Corner LDO	V_{IN}	12	0.85/0.9	0.3	ARD_X_ZUM_A2_IC2
8	VMGTVCCAUX(GTH), VMGTYVCCAUX(GTY), VPS_MGTRAVTT	7	C200	Sync Buck	V_{IN}	12	1.8	0.2	ARD_X_ZUM_A2_IC2
9	VMGTAVCC(GTH), VMGTYAVCC(GTY)	8	C200	Sync Buck	V_{IN}	12	0.9	0.5	ARD_X_ZUM_A2_IC2

*Only required for EV devices

AnDAPT Confidential

AnDAPT

Proposed Solution (2xPMICs)
Use-Case B1

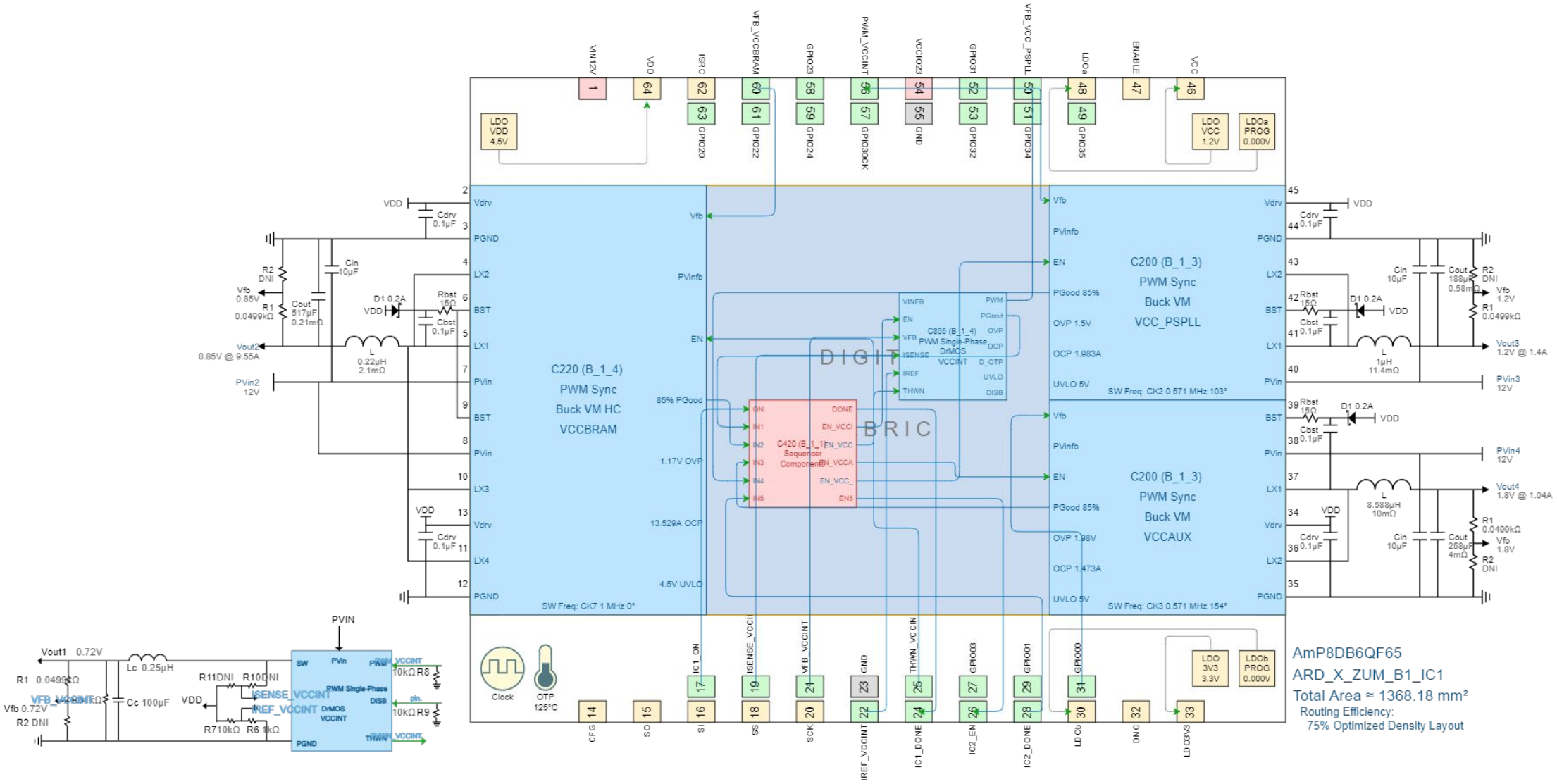


Estimated Total Area = 1876.77 mm^2

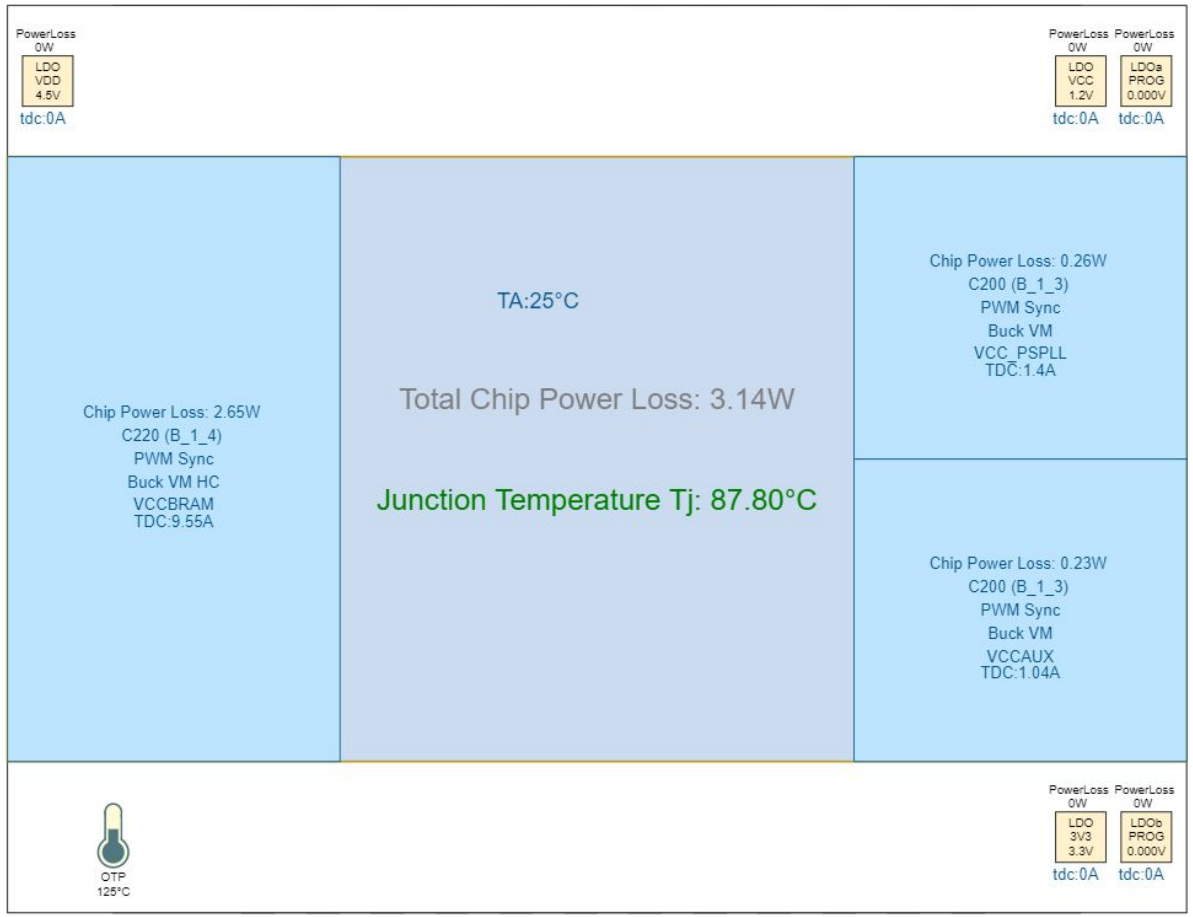
AnDAPT

Mapping IC1 (WebAmp View)

Use-Case B1



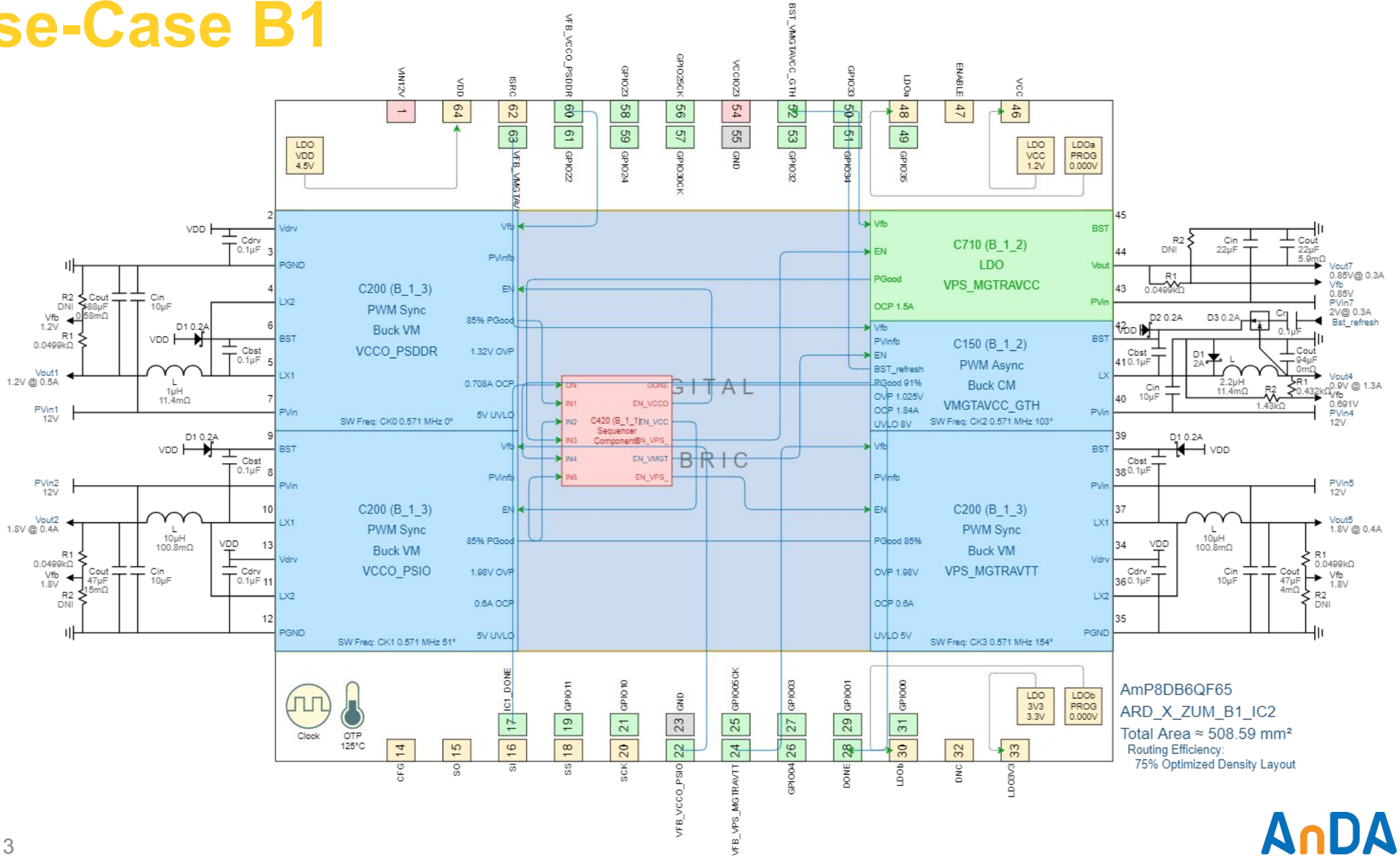
Thermal Design View (IC1)
Use-Case B1



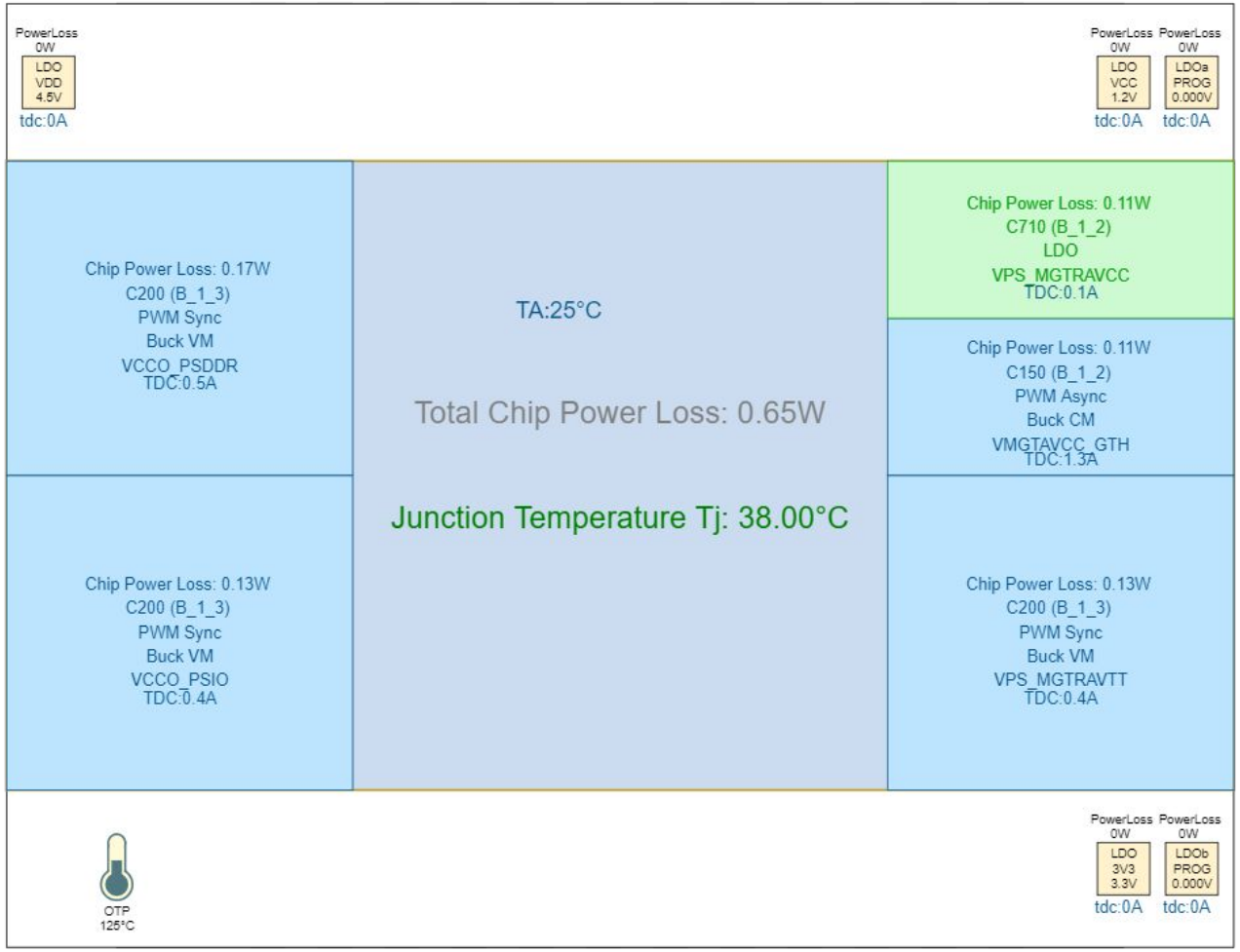
AmP8DB6QF65
ARD_X_ZUM_B1_IC1
Total Area ≈ 1368.18 mm²
Routing Efficiency:
75% Optimized Density Layout

Mapping IC2 (WebAmp View)

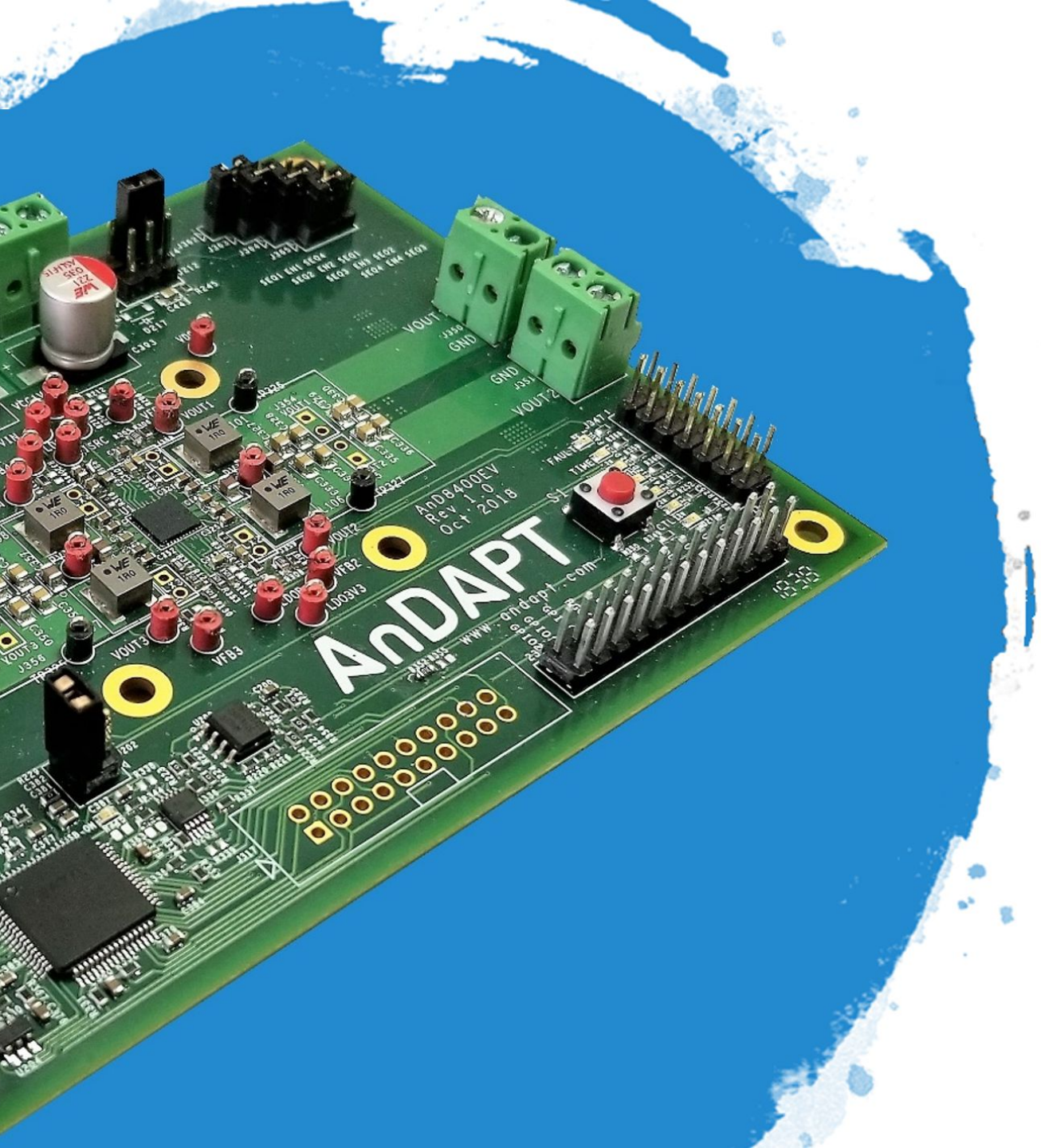
Use-Case B1



Thermal Design View (IC2)
Use-Case B1



AmP8DB6QF65
ARD_X_ZUM_B1_IC2
Total Area ≈ 508.59 mm²
Routing Efficiency:
75% Optimized Density Layout

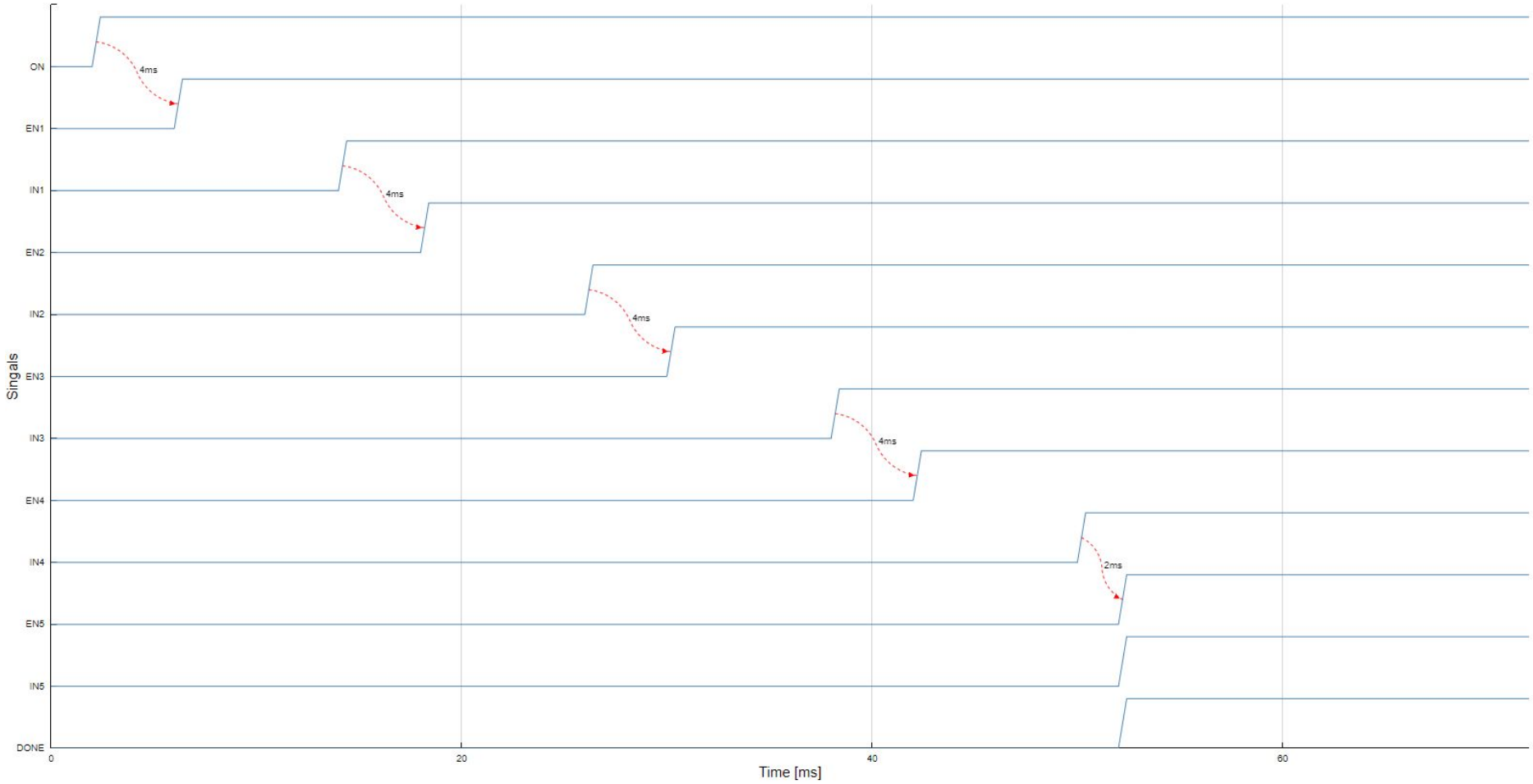


Bench Data

Use-Case B1

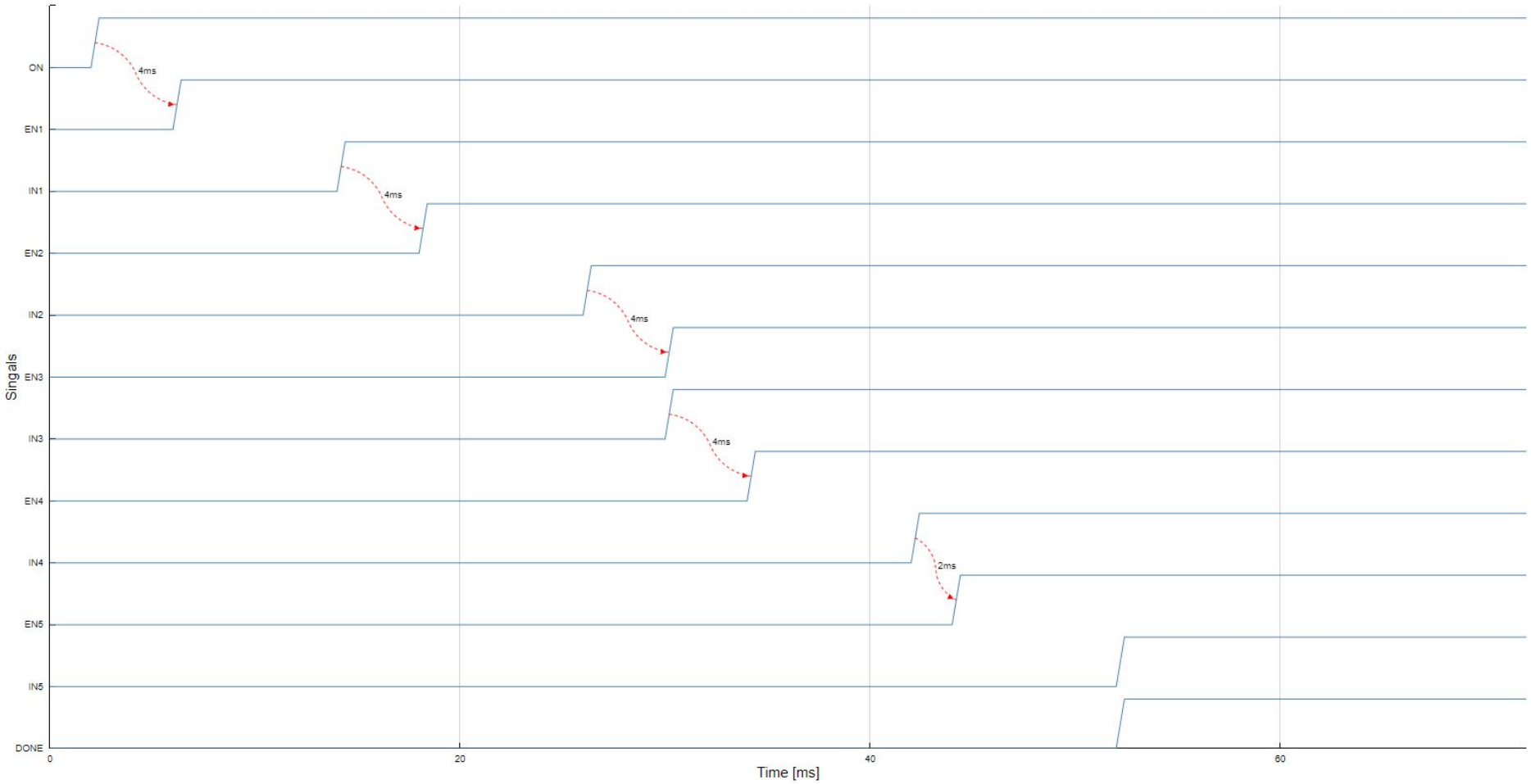
AnDAPT

WebAmp Sequencer Graphic (IC1)



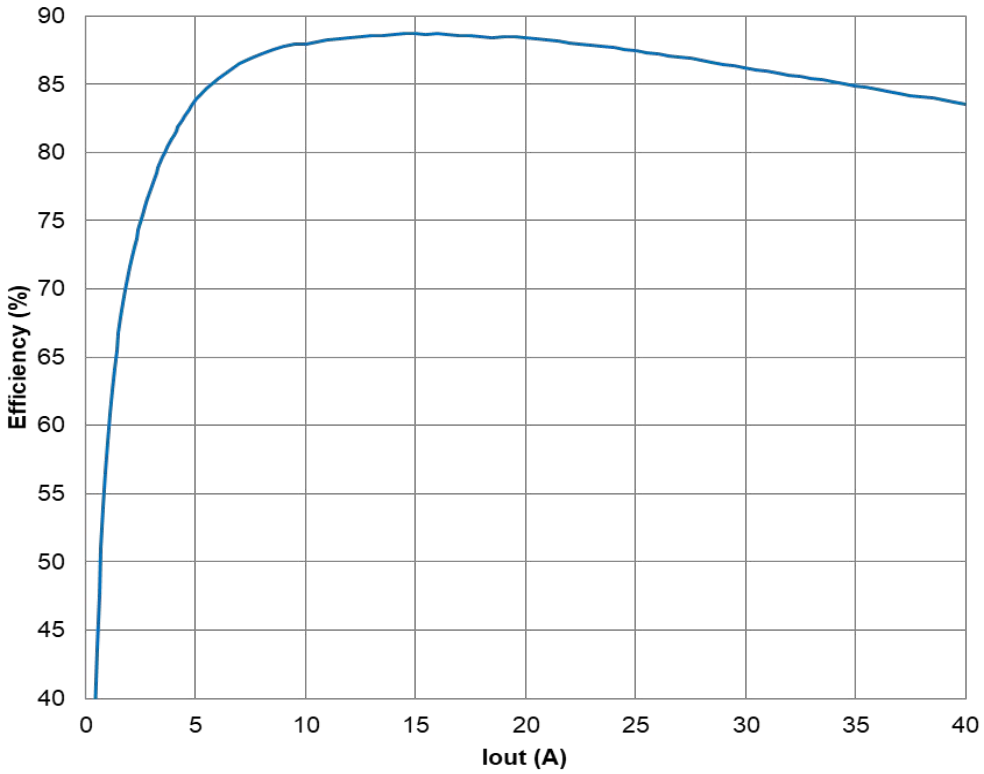
AnDAPT Confidential

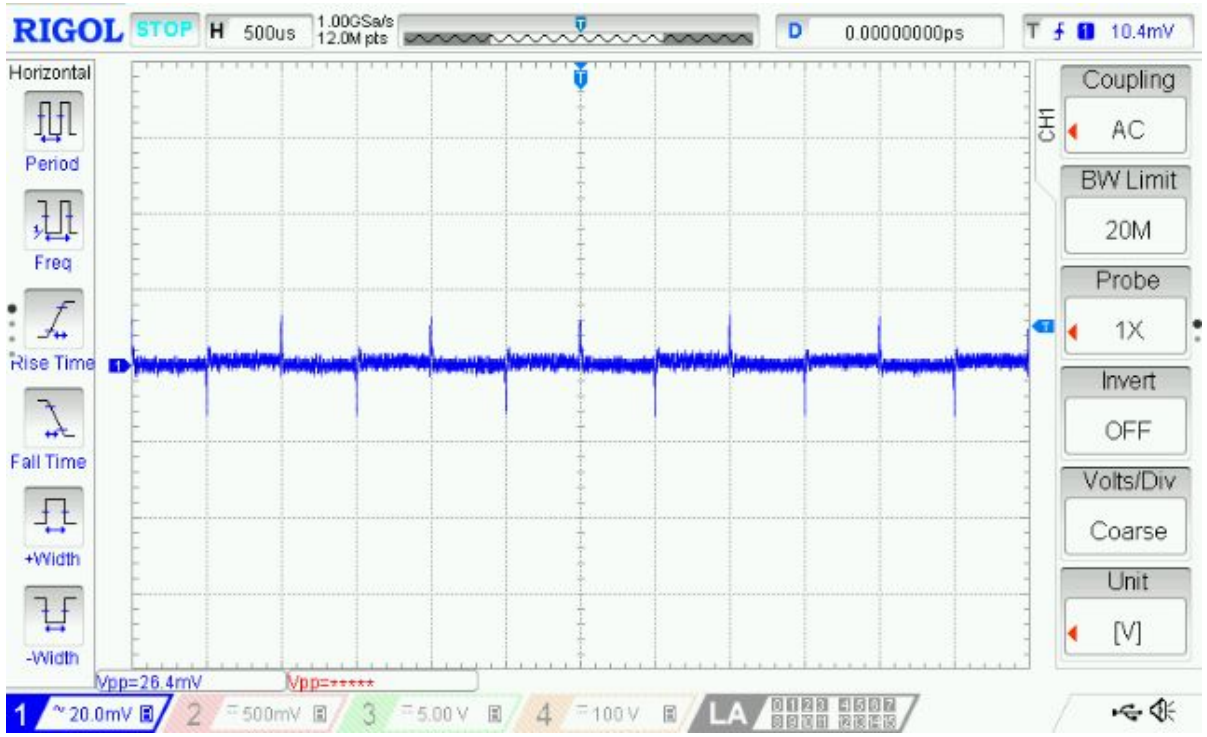
WebAmp Sequencer Graphic (IC2)



AnDAPT Confidential

VCCINT: Efficiency & Transient

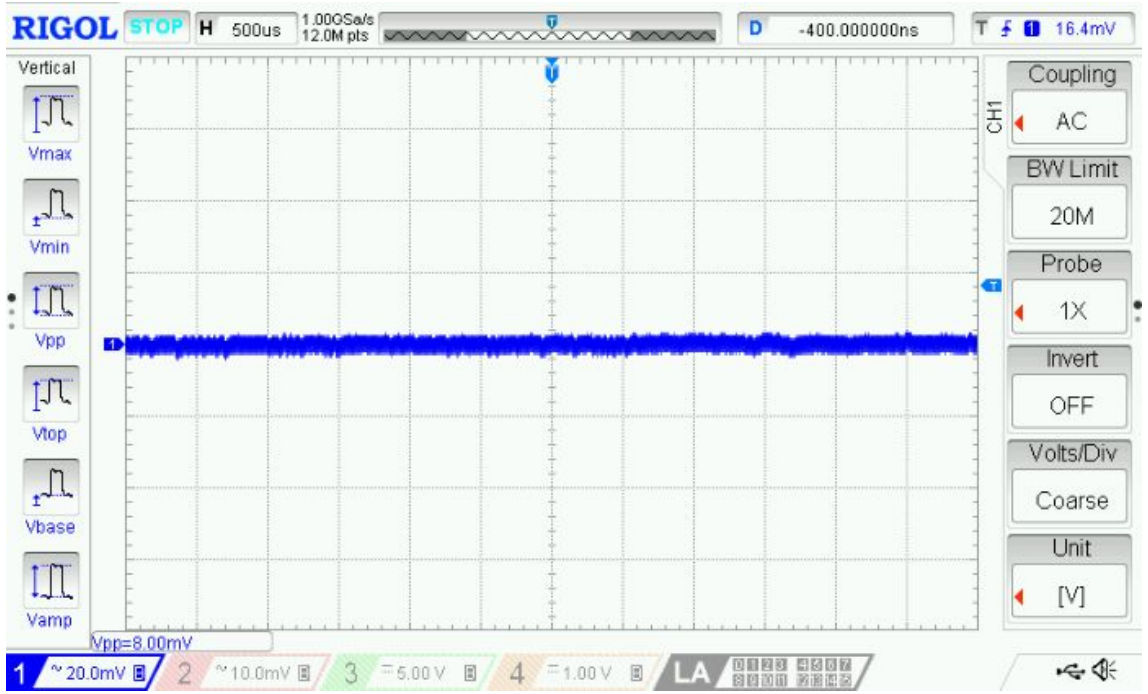




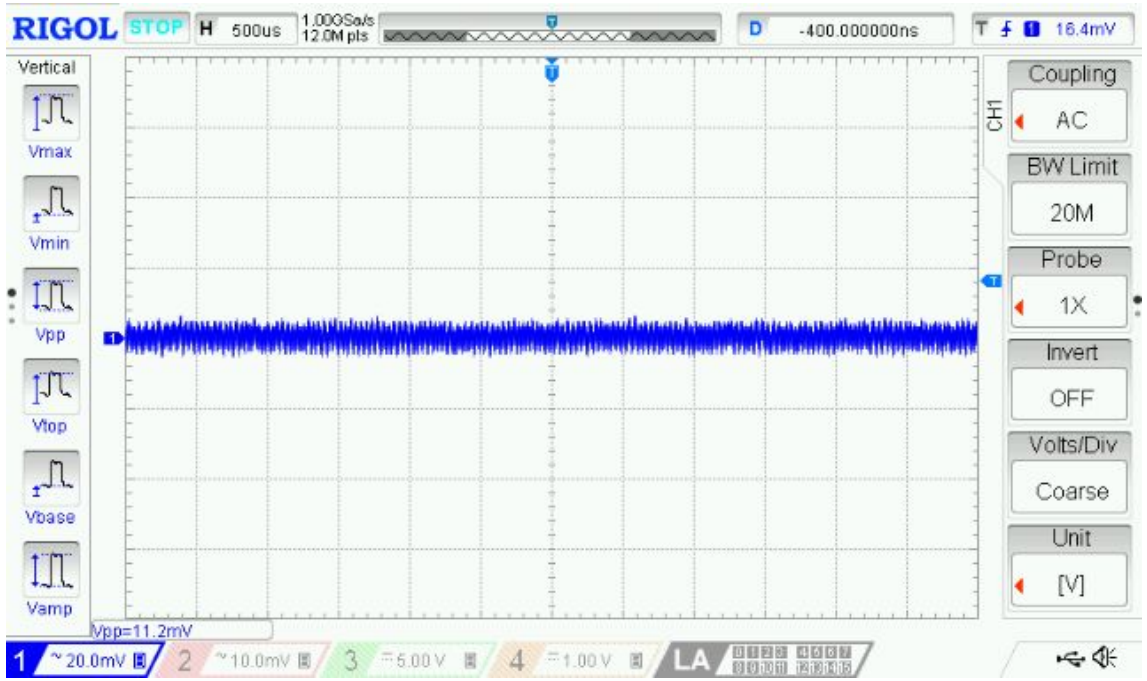
Vout = 0.85 V
Transient: 6.525 A – 8.7A @ 100 A/us
V_{PP} = 28 mV
Lout = 240 nH, Cout = 910 µF

AnDAPT Confidential

VCCINT: Ripple



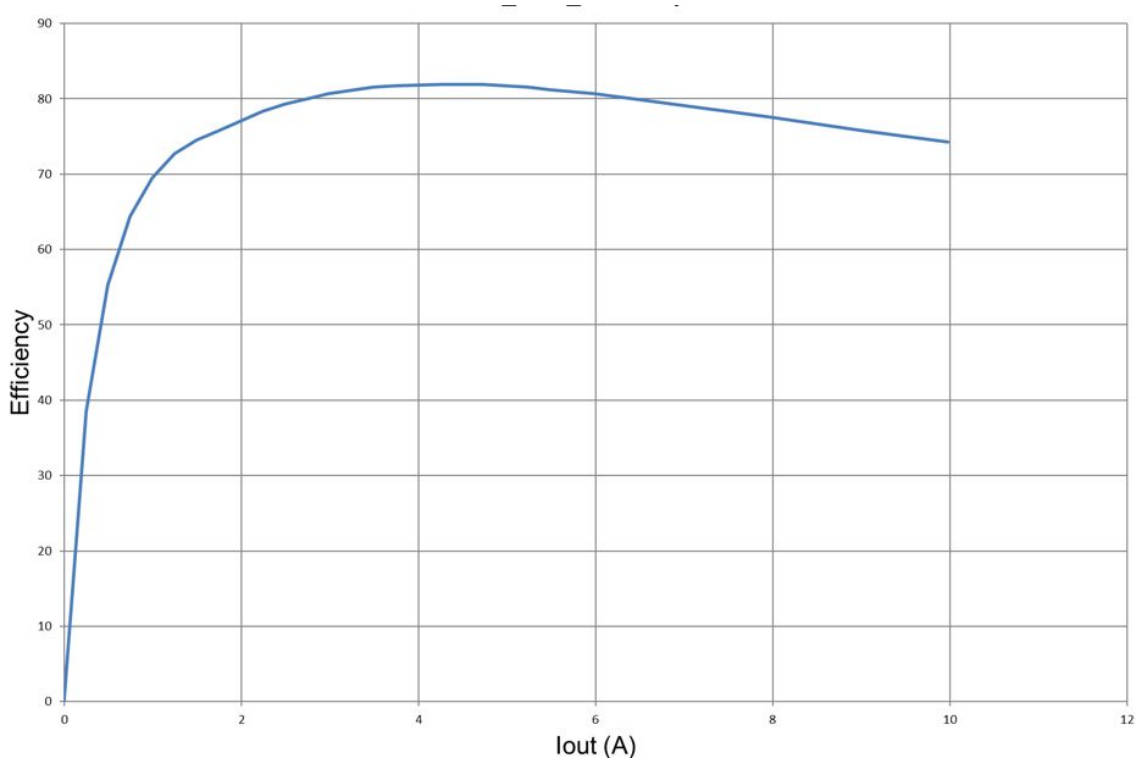
No Load Ripple
V_{PP} = 8 mV

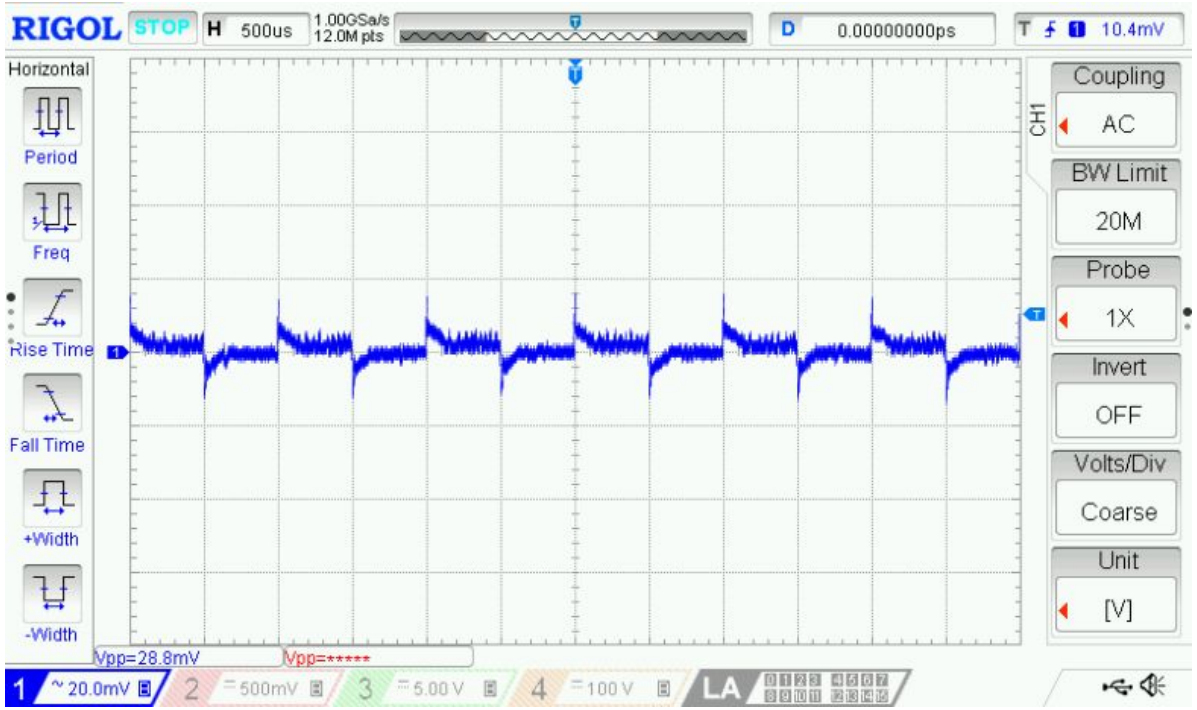


Full Load Ripple
V_{PP} = 11.2 mV

AnDAPT Confidential

VCCBRAM: Efficiency & Transient

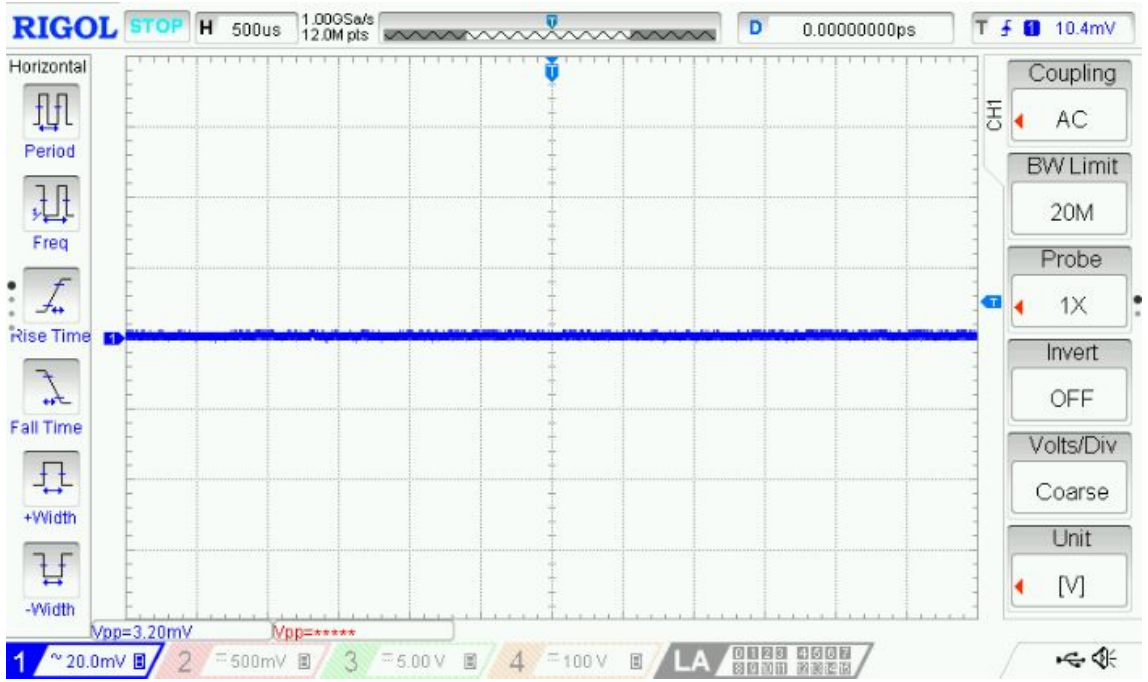




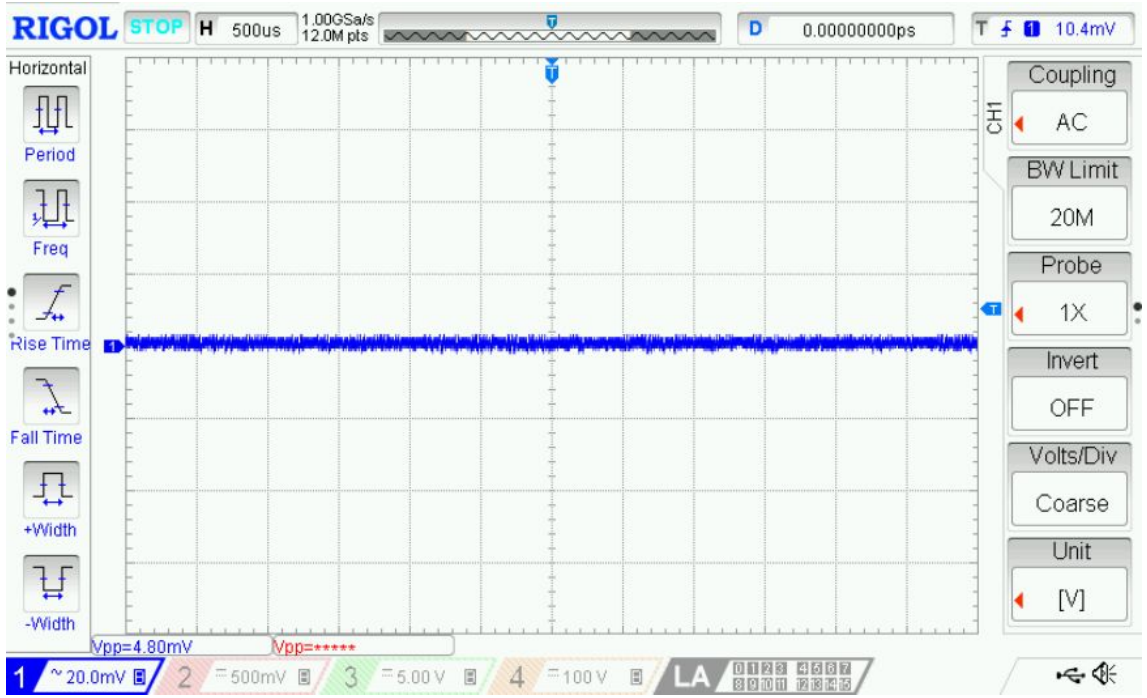
Vout = 0.85 V
Transient: 5.73 A – 9.55A @ 10 A/us
V_{PP} = 28.8 mV
Lout = 220 nH, Cout = 502 µF

AnDAPT Confidential

VCCBRAM: Ripple



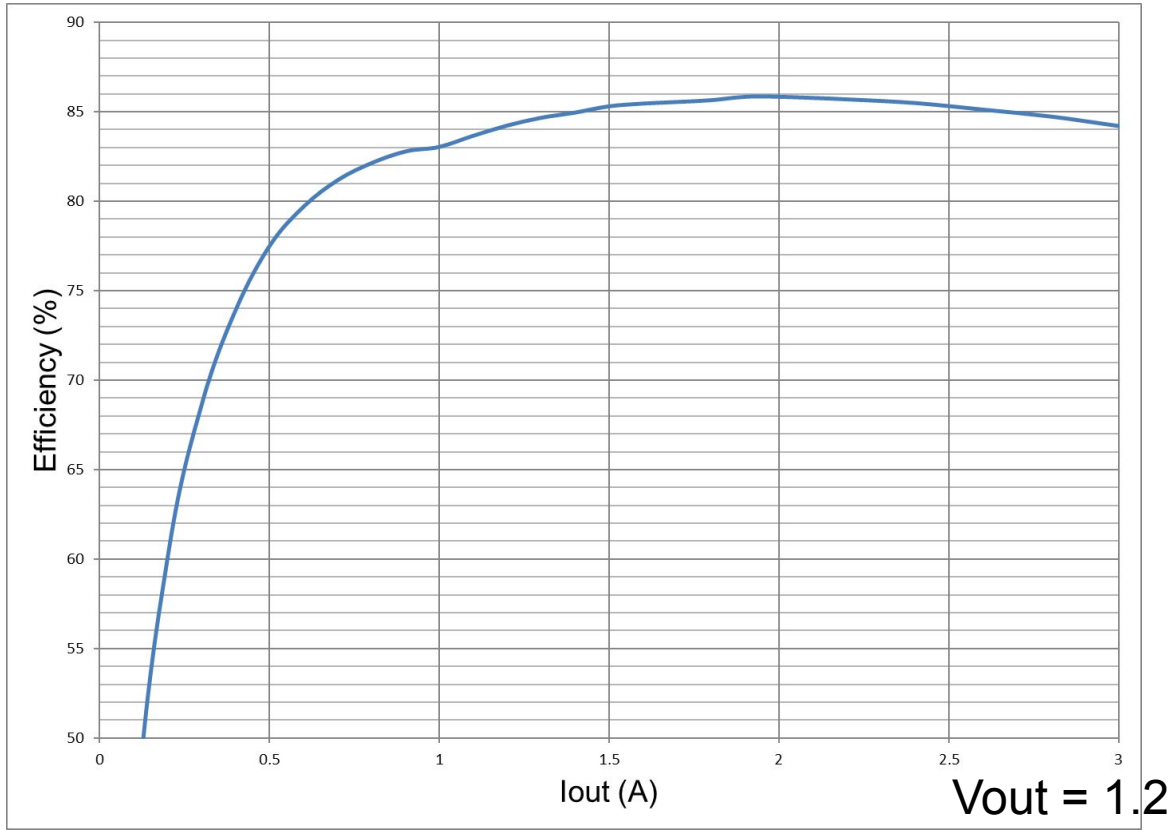
No Load Ripple
V_{PP} = 3.2 mV

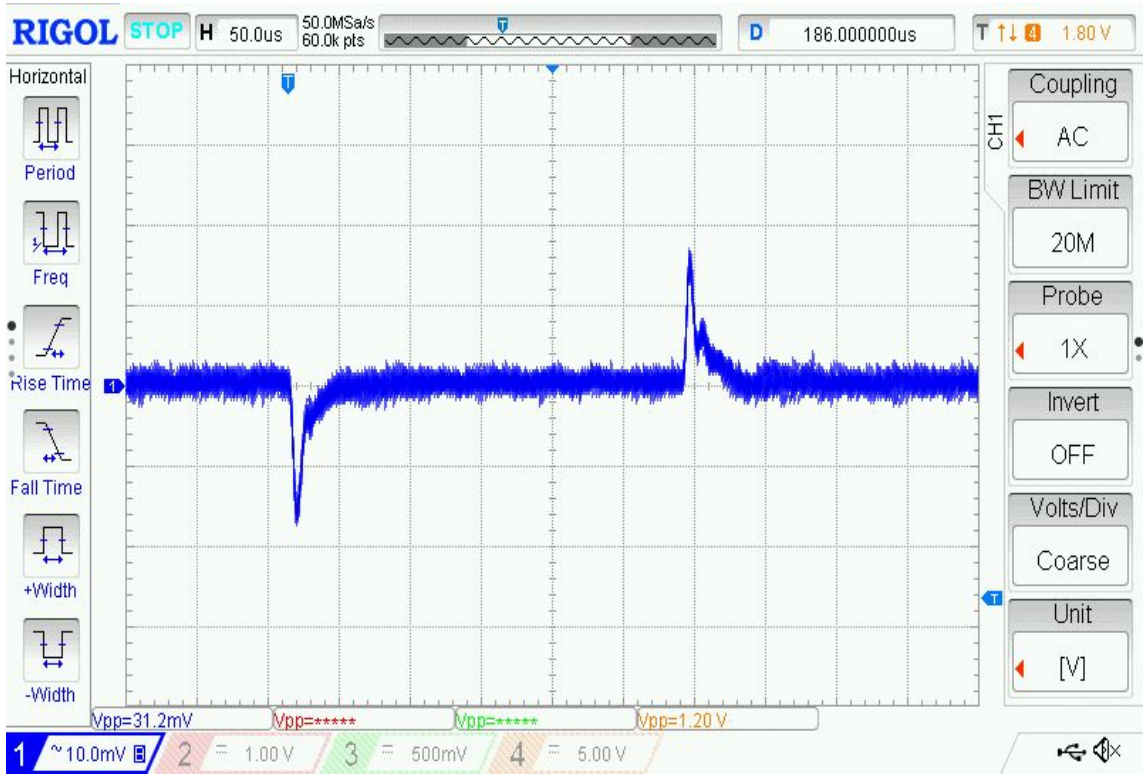


Full Load Ripple
V_{PP} = 4.8 mV

AnDAPT Confidential

VCC_PSPLL: Efficiency & Transient





Vout = 1.2 V

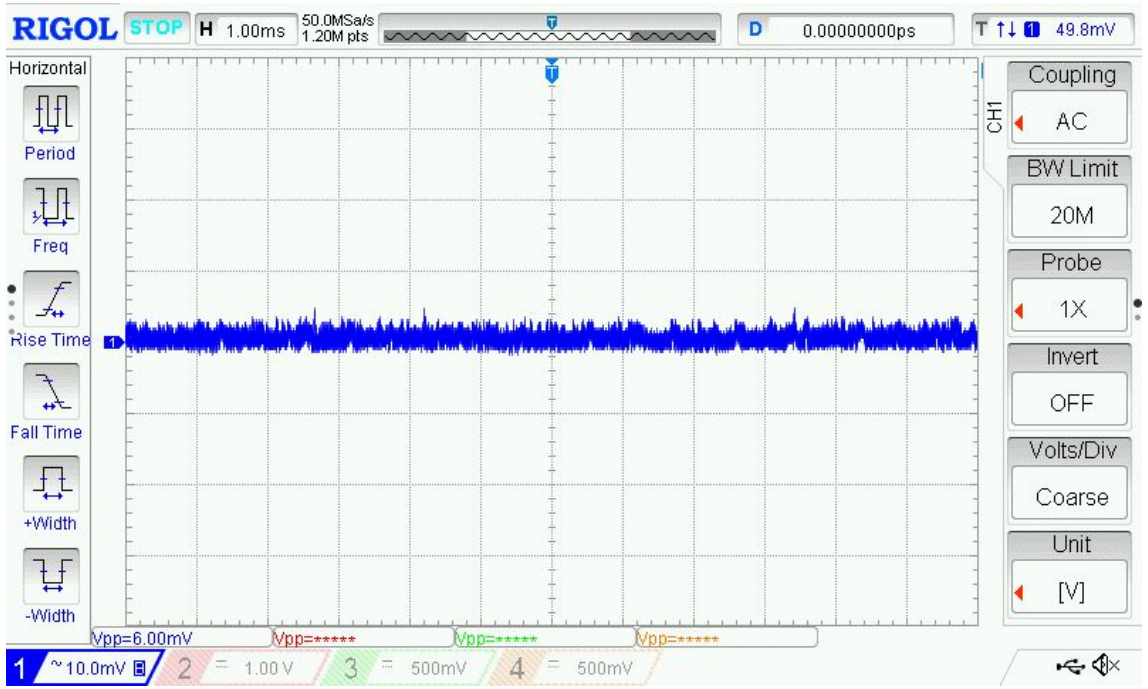
Transient: 2.25 A – 3A @ 2.5 A/us

V_{PP} = 31.2 mV

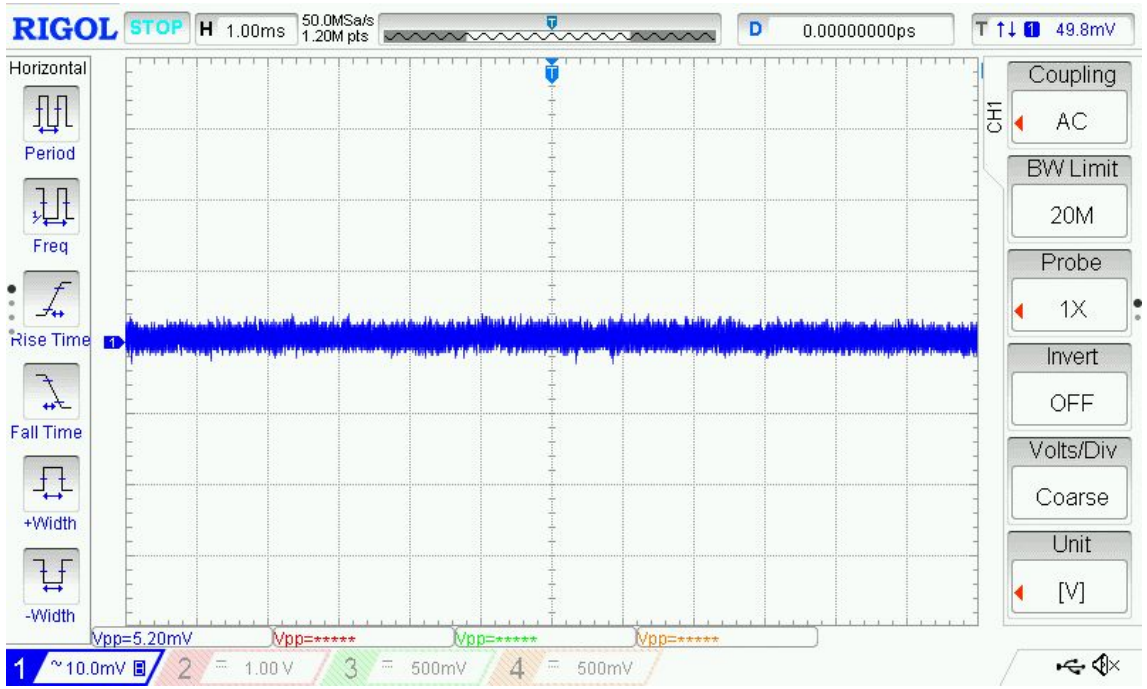
Lout = 1 µH, Cout = 188 µF

AnDAPT Confidential

VCC_PSPLL: Ripple



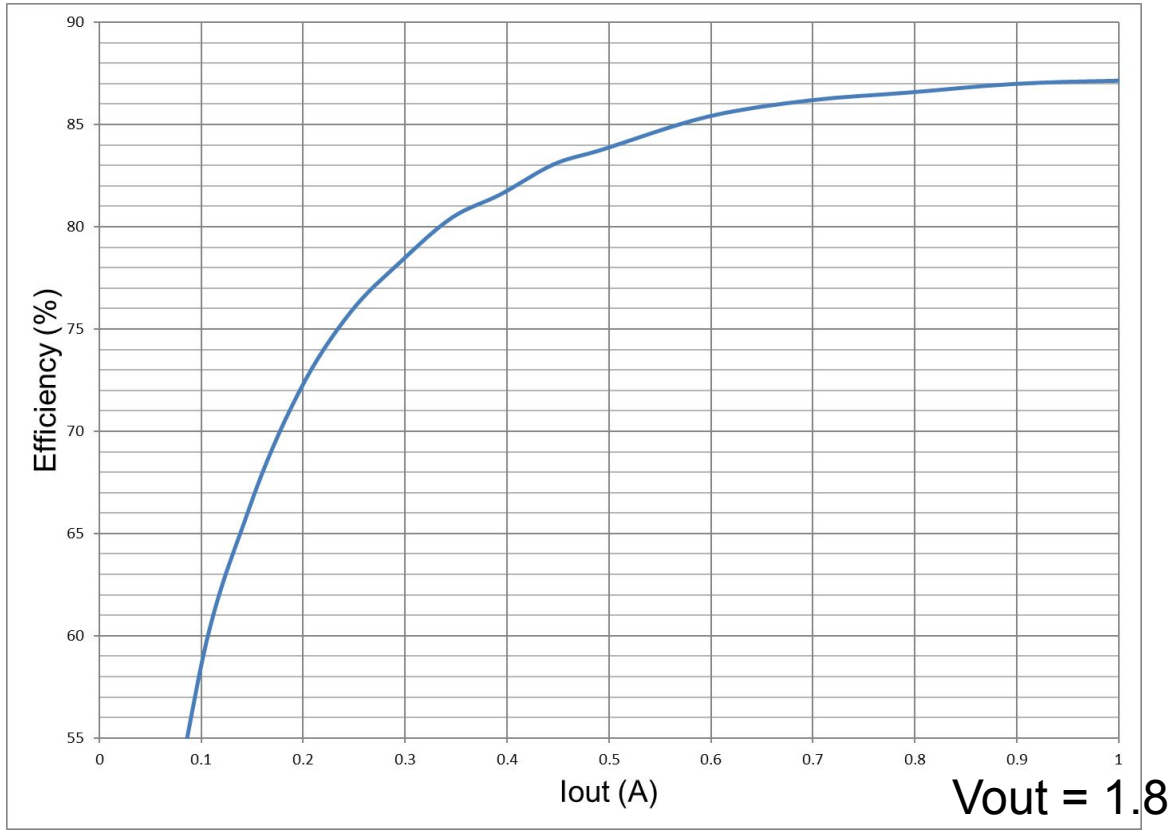
No Load Ripple
V_{PP} = 6 mV



Full Load Ripple
V_{PP} = 5.2 mV

AnDAPT Confidential

VCCAUX: Efficiency & Transient



Vout = 1.8 V

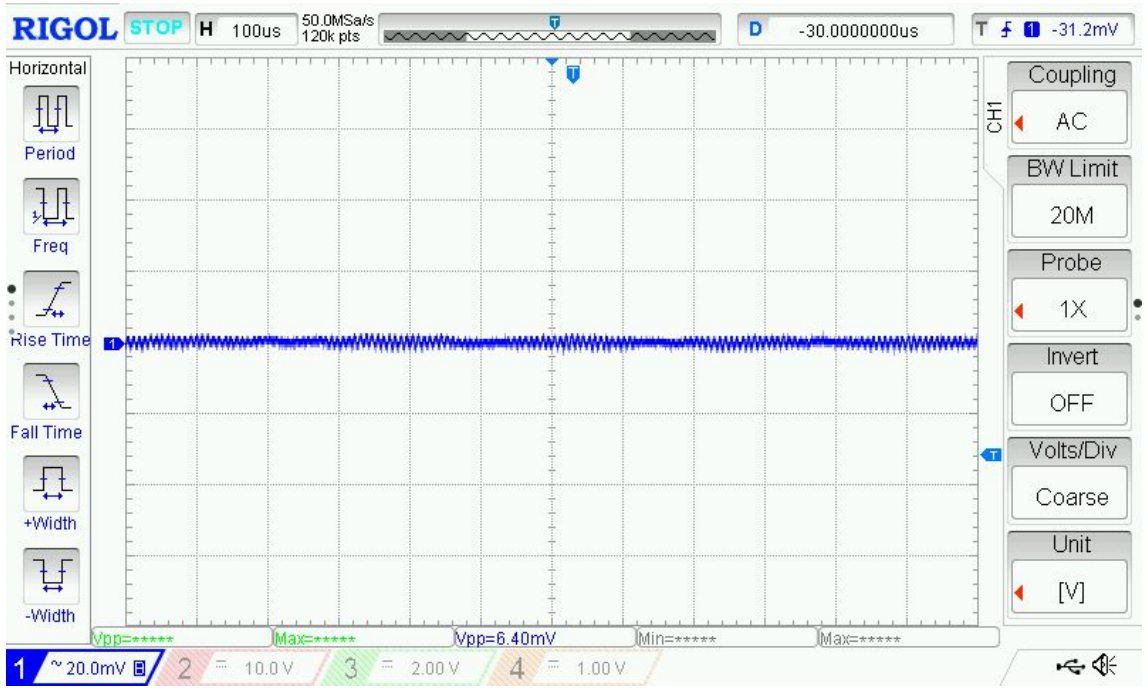
Transient 0.3 A – 1A @ 2.5 A/us

V_{PP} = 56 mV

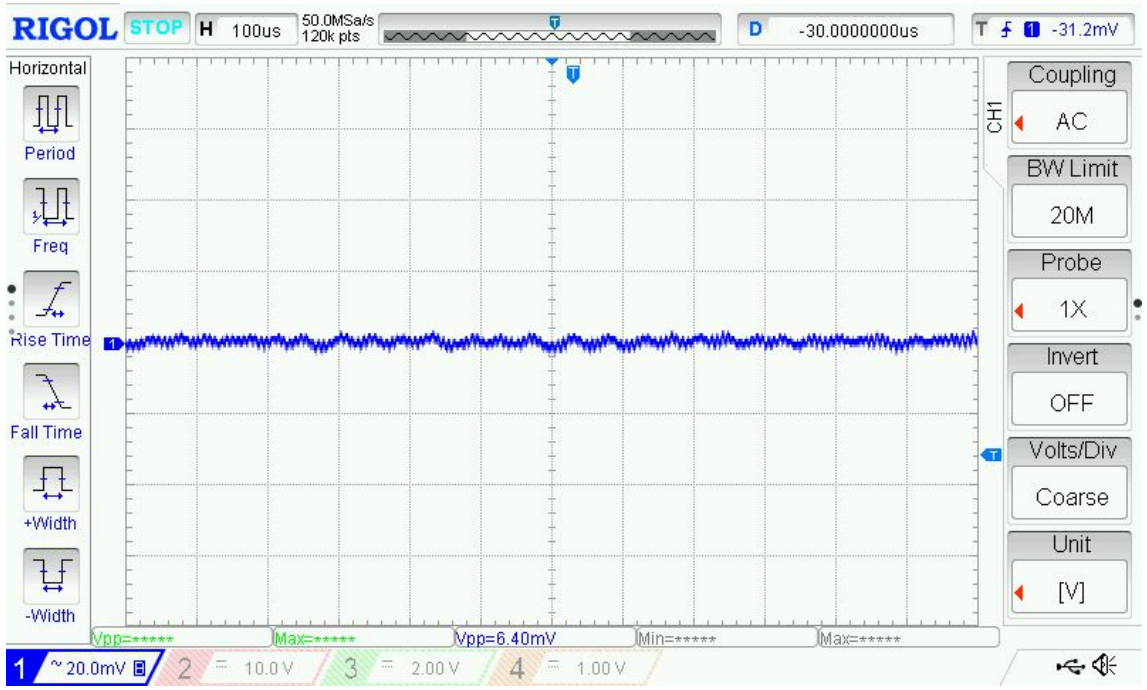
Lout = 6.8 µH, Cout = 141 µF

AnDAPT Confidential

VCCAUX: Ripple



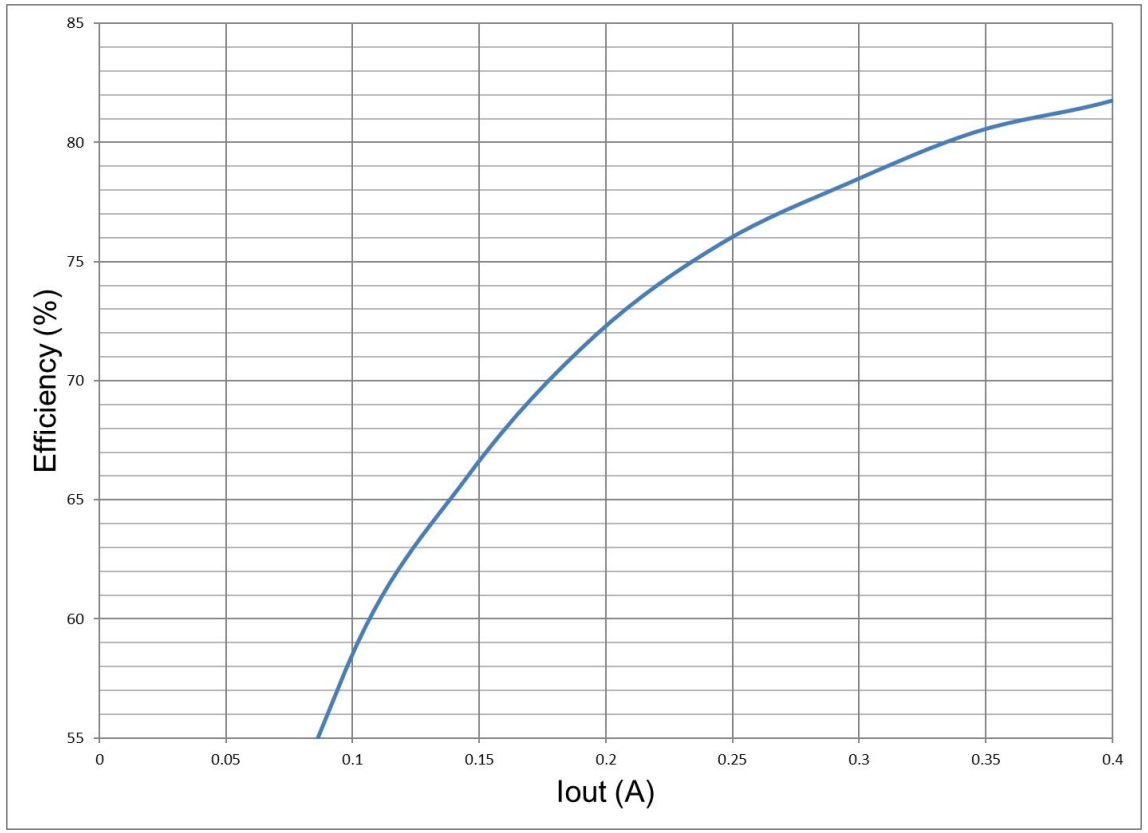
No Load Ripple
V_{PP} = 6.4 mV



Full Load Ripple
V_{PP} = 6.4 mV

AnDAPT Confidential

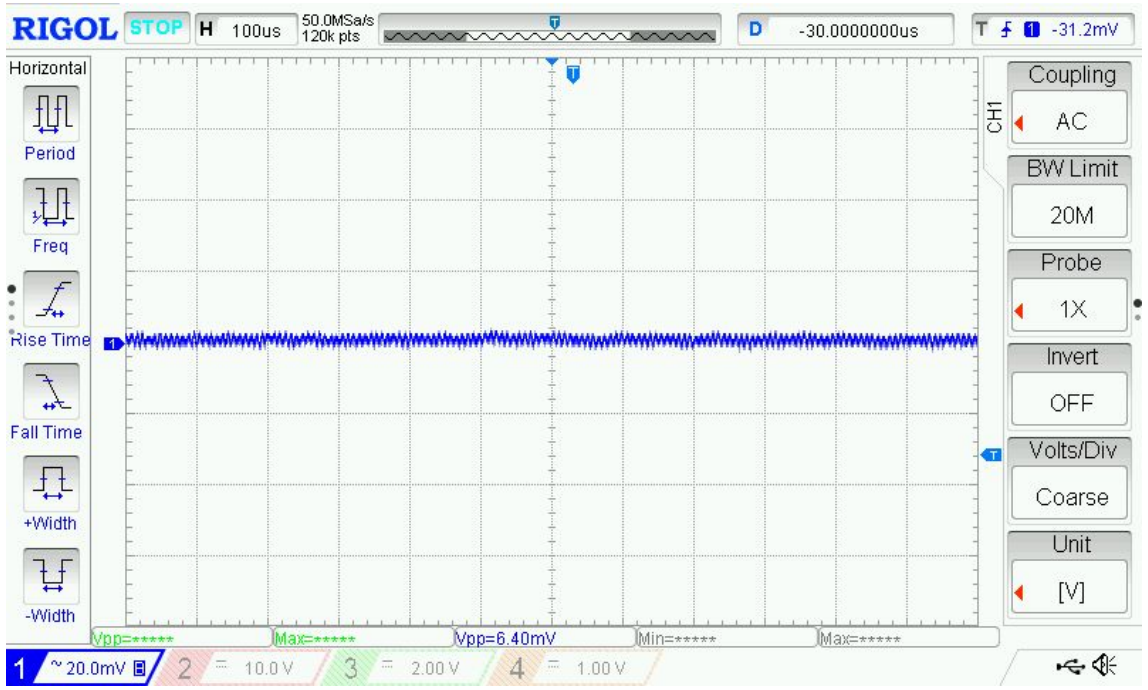
VCCO_PSIO: Efficiency & Transient



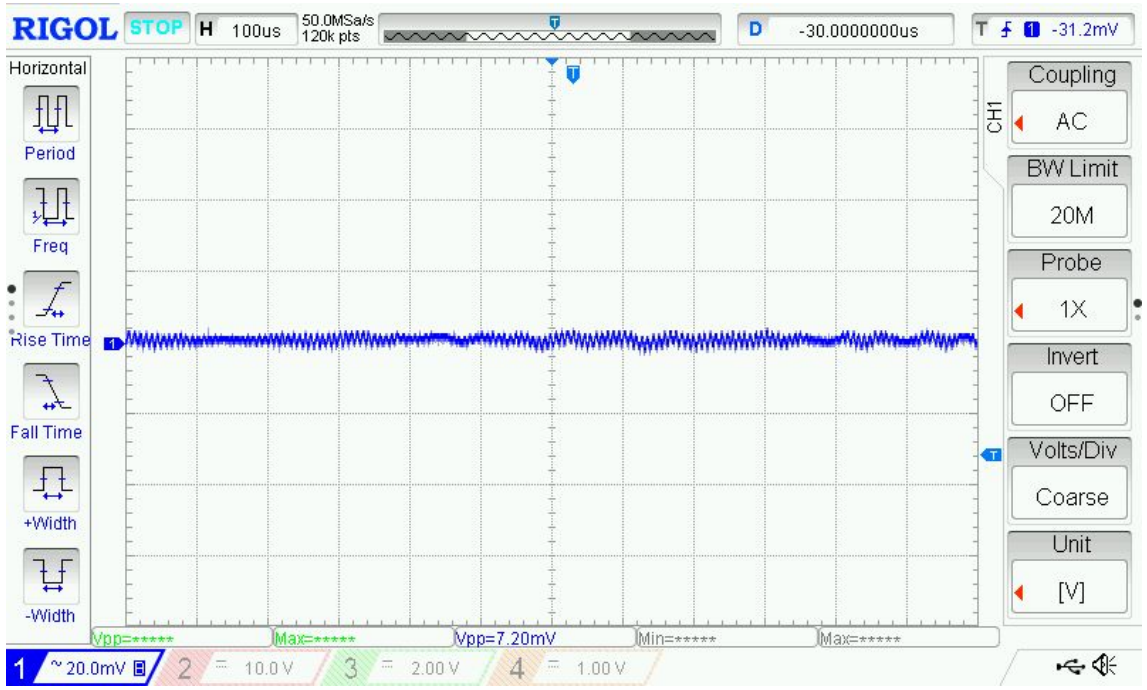
Vout = 1.8 V
Transient 0.12 A – 0.4 A @ 2.5 A/us
V_{PP} = 34.4 mV
Lout = 10 µH, Cout = 47 µF

AnDAPT Confidential

VCCO_PSIO: Ripple



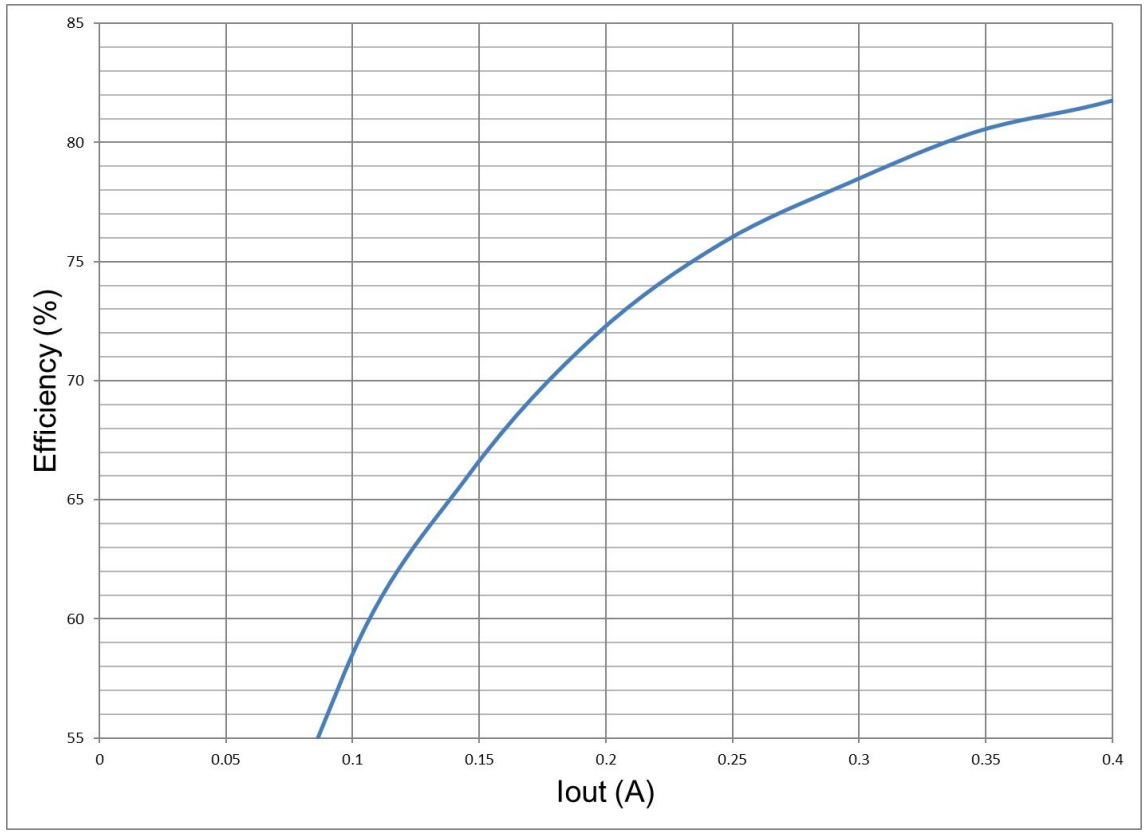
No Load Ripple
V_{PP} = 6.4 mV



Full Load Ripple
V_{PP} = 7.2 mV

AnDAPT Confidential

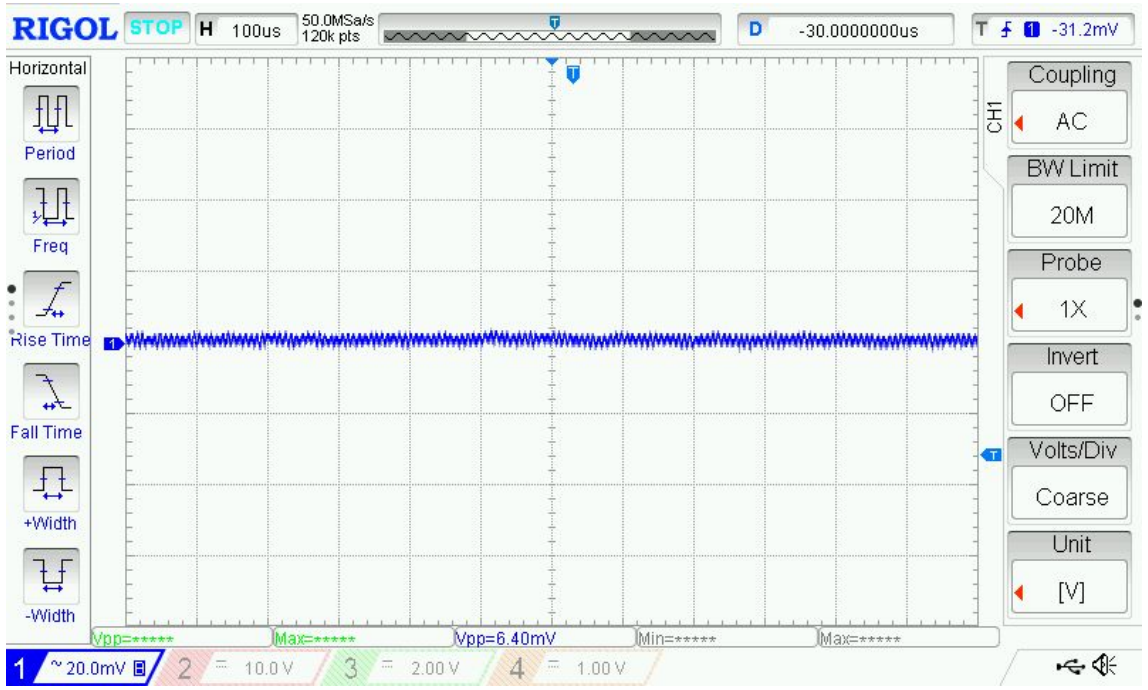
VPS_MGTRAVTT: Efficiency & Transient



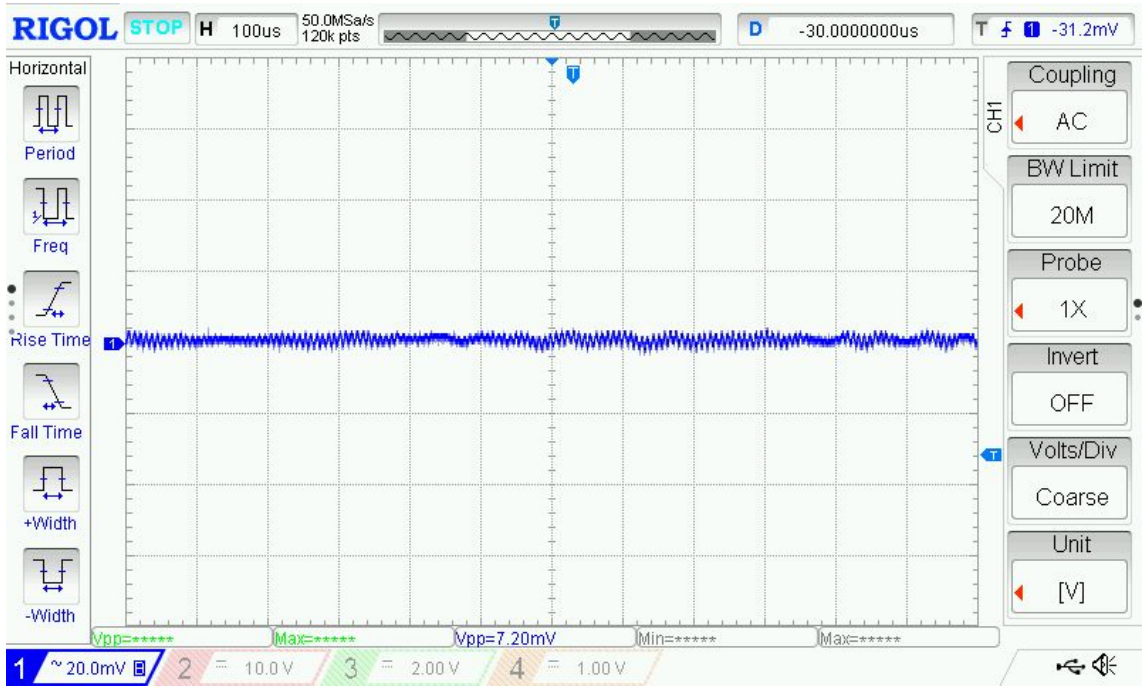
Vout = 1.8 V
Transient 0.12 A – 0.4 A @ 2.5 A/us
V_{PP} = 34.4 mV
Lout = 10 µH, Cout = 47 µF

AnDAPT Confidential

VPS_MGTRAVTT: Ripple



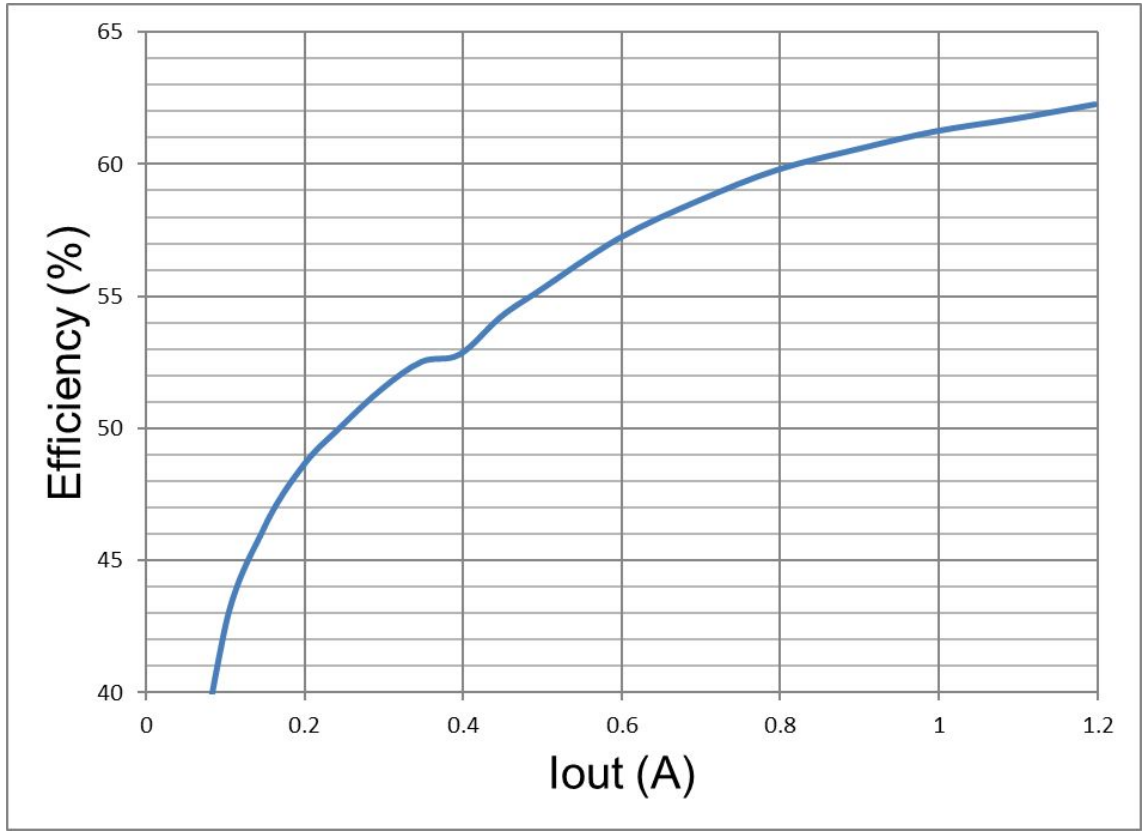
No Load Ripple
V_{PP} = 6.4 mV

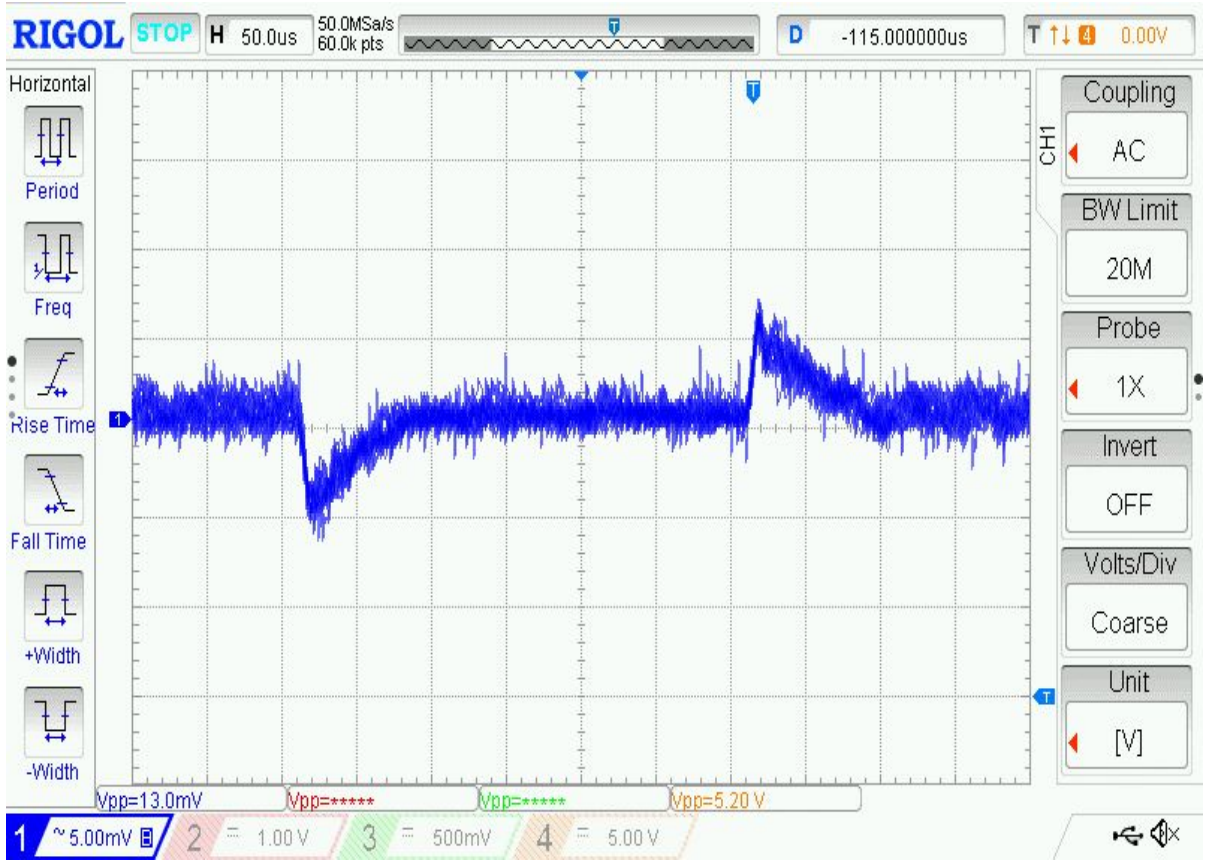


Full Load Ripple
V_{PP} = 7.2 mV

AnDAPT Confidential

VMGTAVCC_GTH: Efficiency & Transient

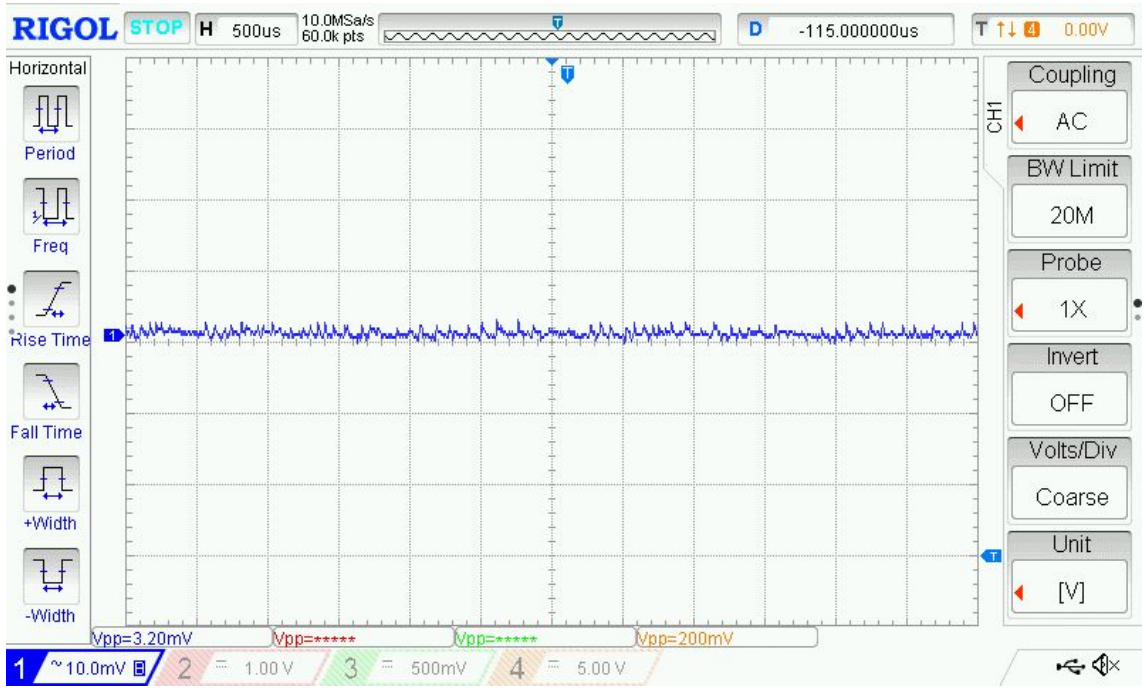




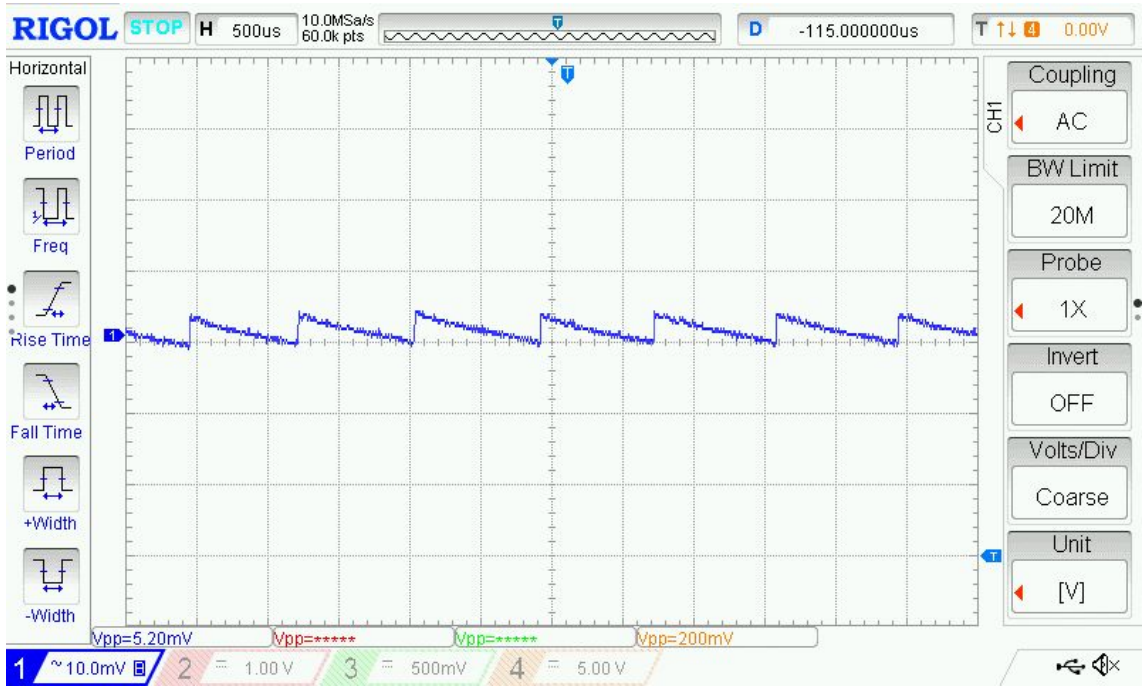
Vout = 0.9 V
Transient: 0.9 A – 1.3 A @ 2.5 A/us
V_{PP} = 28 mV
Lout = 1 µH, Cout = 910 µF

AnDAPT Confidential

VMGTAVCC _GTH : Ripple



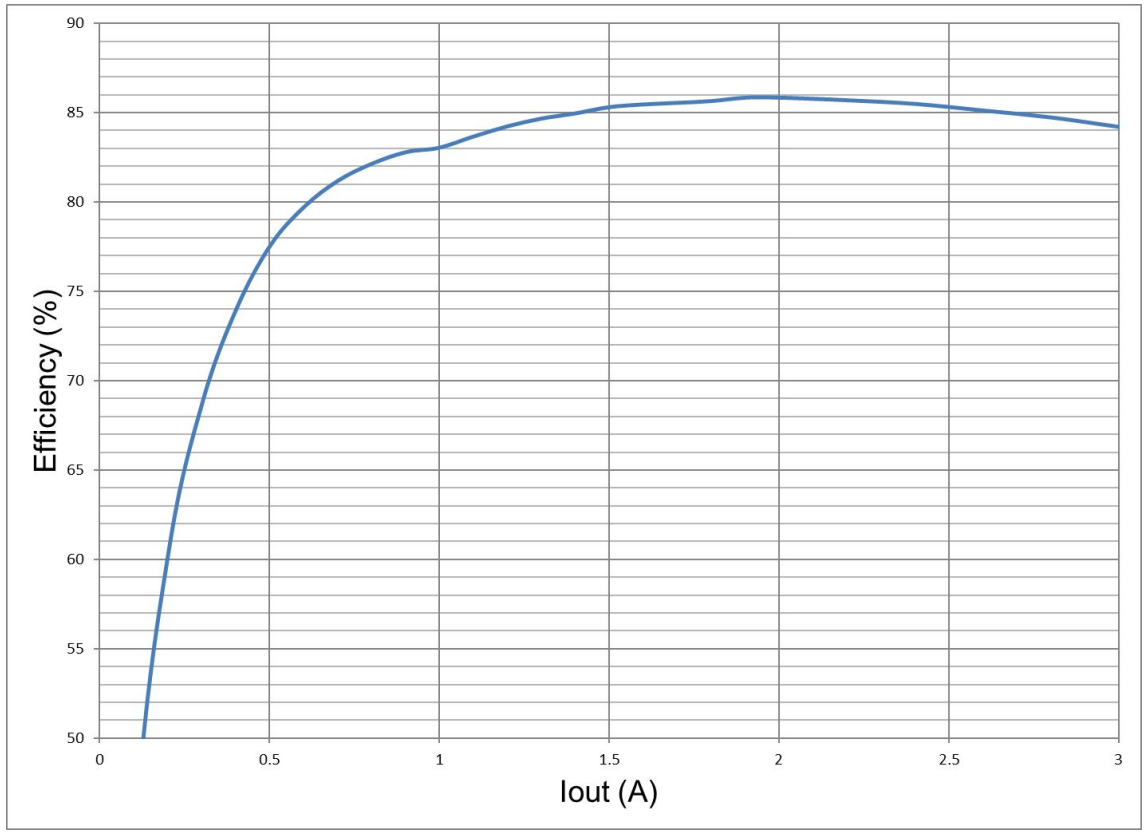
No Load Ripple
V_{PP} = 3.2 mV

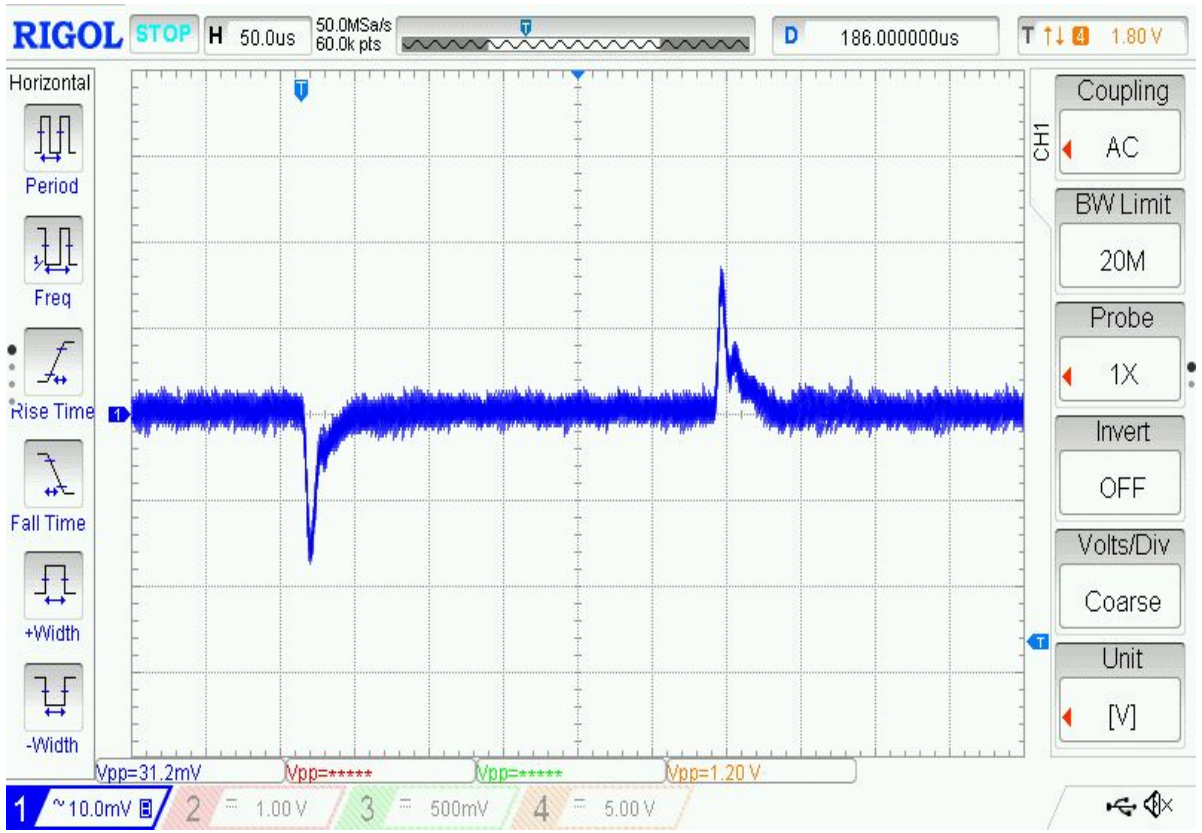


Full Load Ripple
V_{PP} = 5.2 mV

AnDAPT Confidential

VCCO_PSDDR: Efficiency & Transient

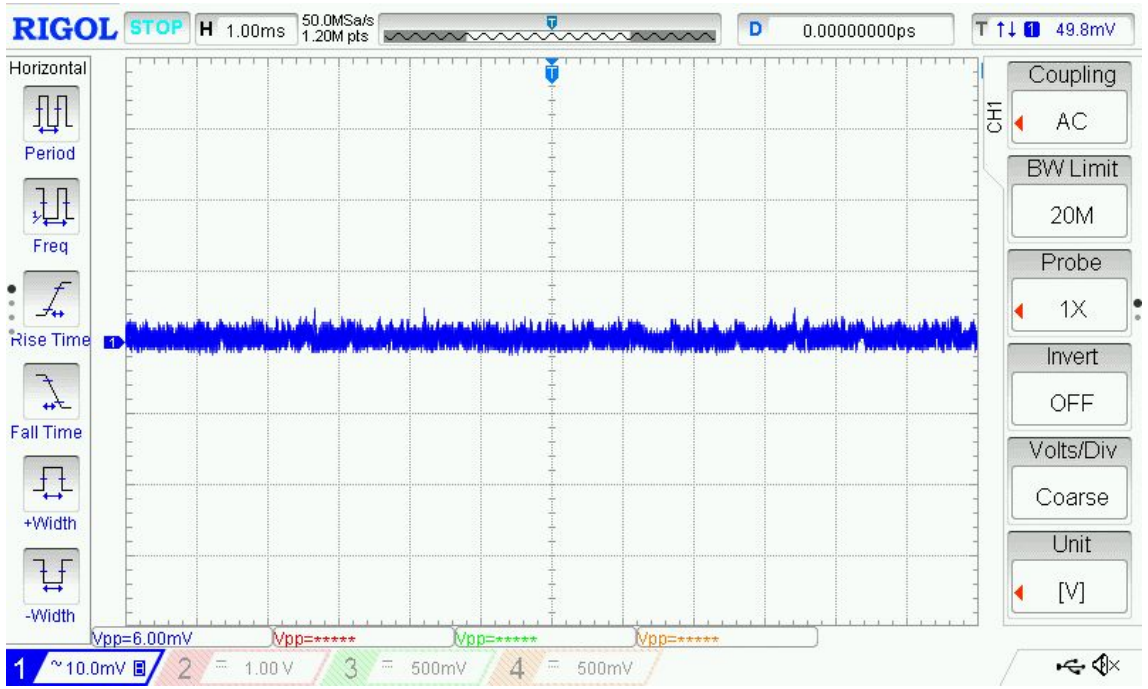




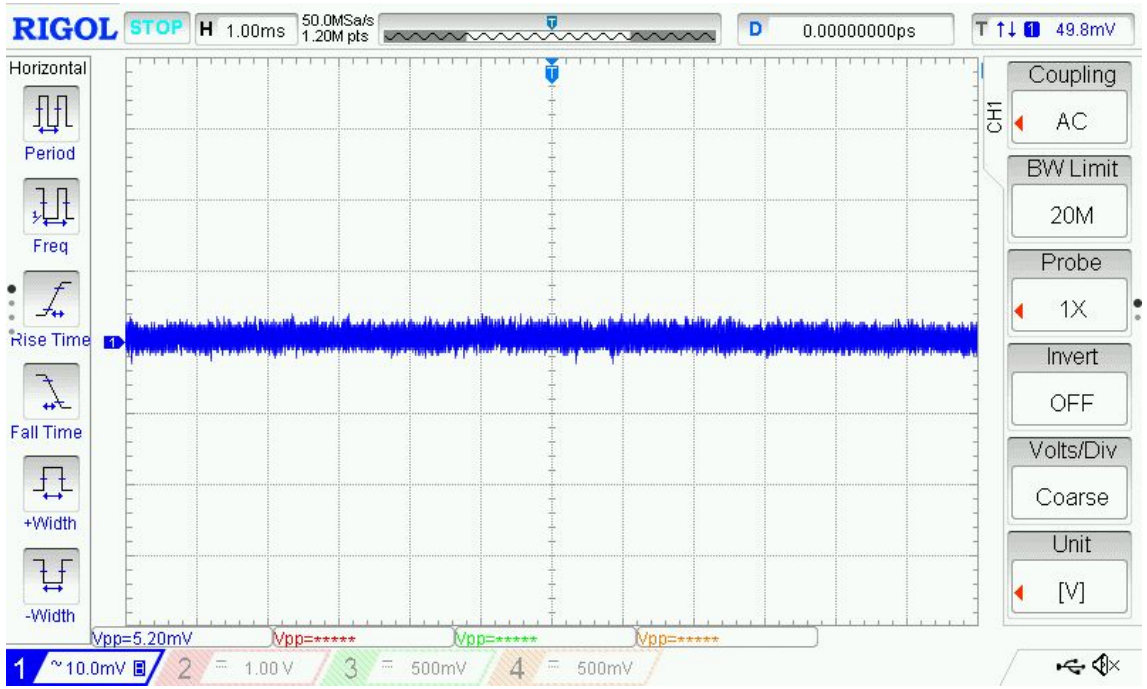
Vout = 1.2 V
Transient: @ 2.5 A/us
V_{PP} = 28 mV
Lout = µ H, Cout = 4 x 47 µF

AnDAPT Confidential

VCCO_PSDDR: Ripple



No Load Ripple
V_{PP} = 6 mV



Full Load Ripple
V_{PP} = 5.2 mV

AnDAPT Confidential

Thank You

AnDAPT