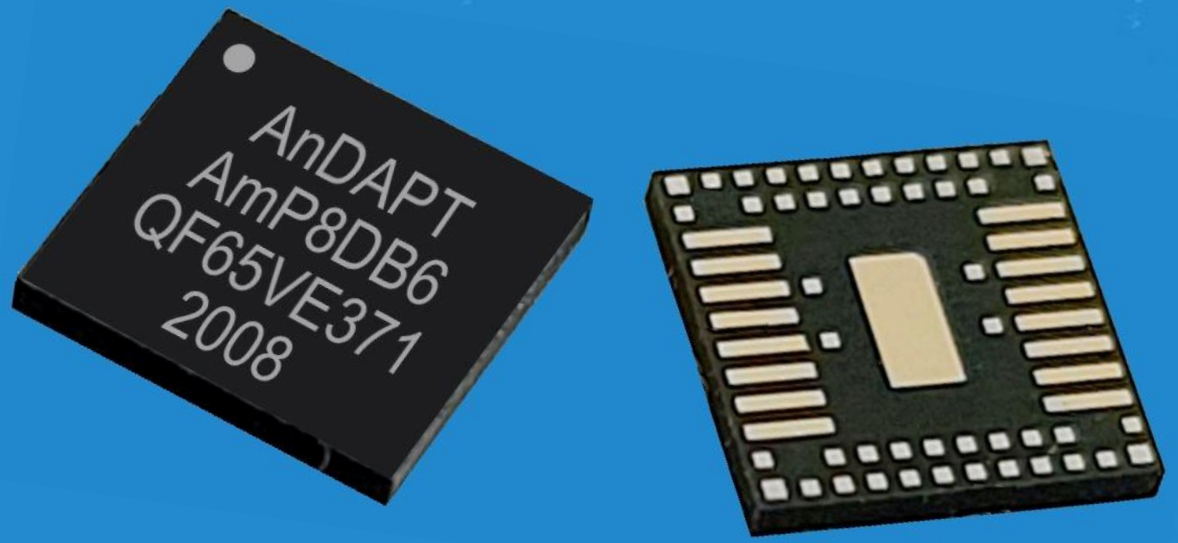


AnDAPT Power Solutions for Xilinx FPGAs

Zynq Ultrascale+ MPSoC Mapping & Lab Data

Use Case C

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Zynq Ultrascale+ (ZU+) family of MPSoC devices' use-cases
- AnDAPT integrated power supply reference design availability for ZU+ MPSOC SKUs
- Always-On, PL performance-optimized use-case mapping using AnDAPT PMIC
- Data including efficiency, transients, ripple for each power rail for the use-case
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for ZU+ MPSoC family FPGA

*Xilinx document: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

AnDAPT Confidential

Xilinx Zynq Ultrascale+ (MPSoC Devices) use-cases

ZU2-ZU3	Cost Optimized without MGT Reference Design	Cost Optimized with MGT Reference Design	Power Optimized Reference Design	Performance Optimized Reference Design	Full Power Management Reference Design
ZU4-ZU5					Full Power Management Reference Design
ZU6-ZU9					
ZU11-ZU19					

AnDAPT's first reference designs includes Zynq family power solutions

AnDAPT Confidential

ZU+ MPSoC Rail Coverage with AmP Power Components

Use Case	SKU	VCCINT	VCCBRAM	VCCINT_IO	VCCINT_VCU	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	VCCAUX	VCCAUX_IO	VCCADC	VCC_PSAUX	VCC_PSDDR_PLL	VCC_PSADC	VMGTAVTT (GTH)	VMGTYATT (GTY)	VCC_PSPLL	VCCO_PSDDR	VCCO_PSIO	VPS_MGTRAVCC	VMGTVCCAUX (GTH)	VMGTYVCCAUX (GTY)	VPS_MGTRAVTT	VMGTAVCC (GTH)	VMGTYAVCC (GTY)	HDIO VCCO	HPIO VCCO
Cost-optimized	ZU2-ZU19 (w/o MGTs)	Rail 1			Rail 6	Rail 1			Rail 4						-	-	Rail 3	Rail 2	Rail 5	-	-	-	-	-	-	-	-
	ZU2-ZU19 (w MGTs)	Rail 1			Rail 5	Rail 1			Rail 3						Rail 6			Rail 2	Rail 4	Rail 7	Rail 8			Rail 9		-	-
Power-Optimized	ZU2-ZU19	Rail 1	Rail 2						Rail 4						Rail 3			Rail 8	Rail 5	Rail 9	Rail 6			Rail 7		-	-
Performance-Optimized	ZU2-ZU19	Rail 1			Rail 2	Rail 1			Rail 4						Rail 3			Rail 8	Rail 5	Rail 7	Rail 6			Rail 7		Rail 9	Rail 10
Full-Power Management	ZU2-ZU3	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	-	-	Rail 3	Rail 7	Rail 4	Rail 11	-	-	Rail 12	-	-	Rail 13	Rail 14
	ZU4-ZU19	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	Rail 13		Rail 3	Rail 7	Rail 4	Rail 11	Rail 15		Rail 12	Rail 14		Rail 16	Rail 17

C220 (Sync Buck HC)	
C200 (Sync Buck)	
C150 (Async Buck)	
C710 (SIM LDO)	
C750 (Load Switch)	
Corner LDO	

AnDAPT Confidential

AnDAPT

Zynq Ultrascale+ (ZU+) MPSoC Device SKUs Covered

CG Devices (Dual Application Processor)	**EG Devices** (Quad Application Processor & GPU)	**EV Devices** (Video Codec)
XCZU2CG	XCZU2EG	XCZU4EV
XCZU3CG	XCZU3EG	XCZU5EV
XCZU4CG	XCZU4EG	
XCZU5CG	XCZU5EG	
XCZU6CG	XCZU6EG	
XCZU7CG	XCZU9EG	
XCZU9CG	XCZU11EG	
	XCZU15EG	
	XCZU17EG	
	XCZU19EG	

List may not be exhaustive. Please contact AnDAPT for further details

AnDAPT Confidential

Zynq Ultrascale+ MPSoC (Always On, PL Performance-Optimized)

Use Case: C

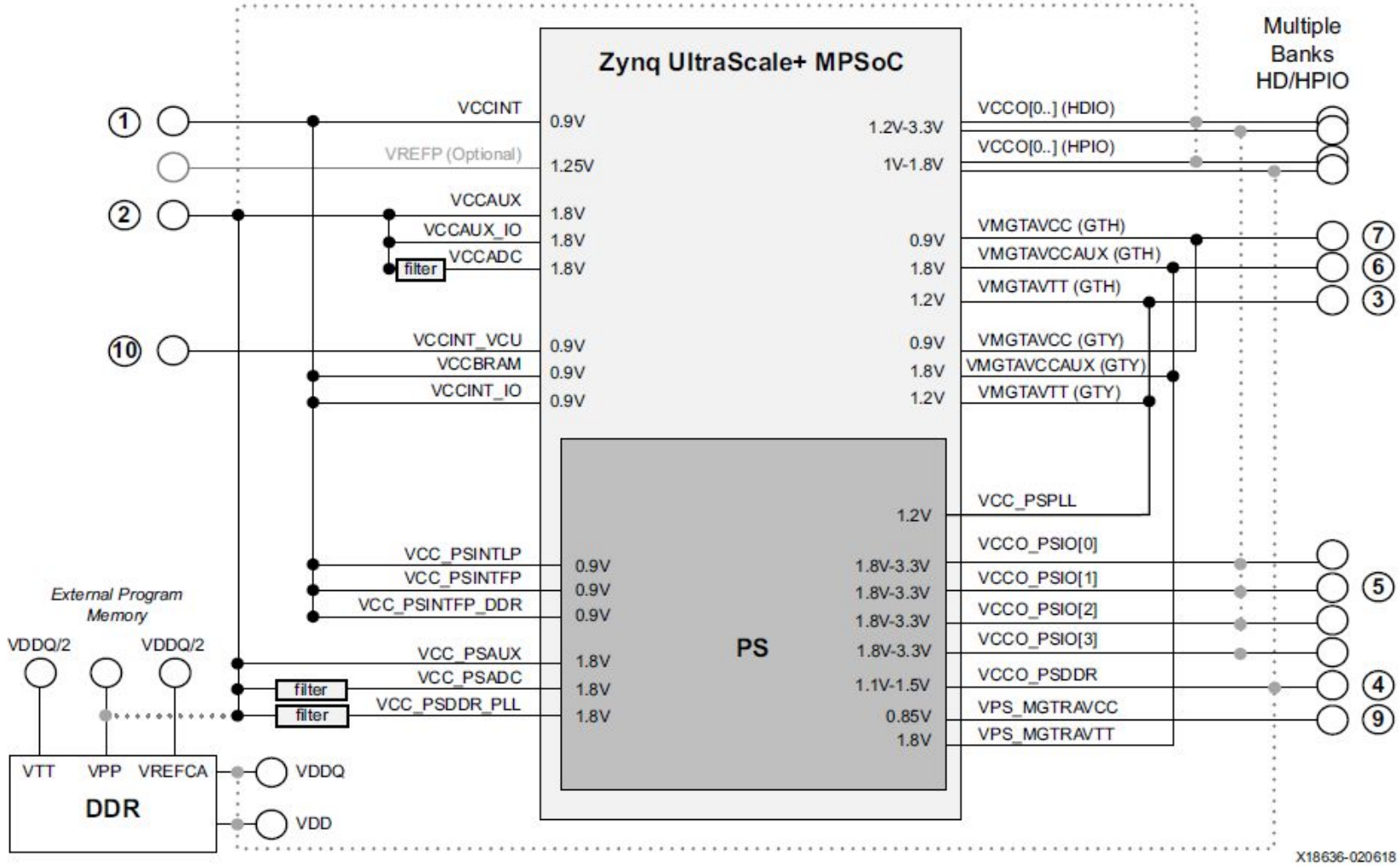


Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

AnDAPT Confidential

AnDAPT

Power Tree: Performance-Optimized
Use-Case C

V_{IN} = 12V

#	Rail	Seq	Power Component	Vout (V)	Iout (A)	Comment
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR	1		0.9	32.35	
2	VCCINT_VCU*	1		0.9	3	*EV devices only
3	VCC_PSPLL, VMGTAVTT(GTH), VMGTAVTT(GTY)	3		1.2	6	
4	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL	2		1.8	2.04	
5	VCCO_PSIO[3:0]	5		1.8-3.3	0.4	
6	VMGTAVCCAUX(GTH), VMGTAVCCAUX(GTY), VPS_MGTTRAVTT	6		1.8	0.4	
7	VMGTAVCC(GTH), VMGTAVCC(GTY), VPS_MGTRAVCC	7		0.9	2.3	
8	VCCO_PSDDR	4		1.1-1.5	0.5	
9	HDIO_VCCO	-		1.2-3.3	0.5	
10	HPIO_VCCO	-		1-1.8	1	

AnDAPT Confidential

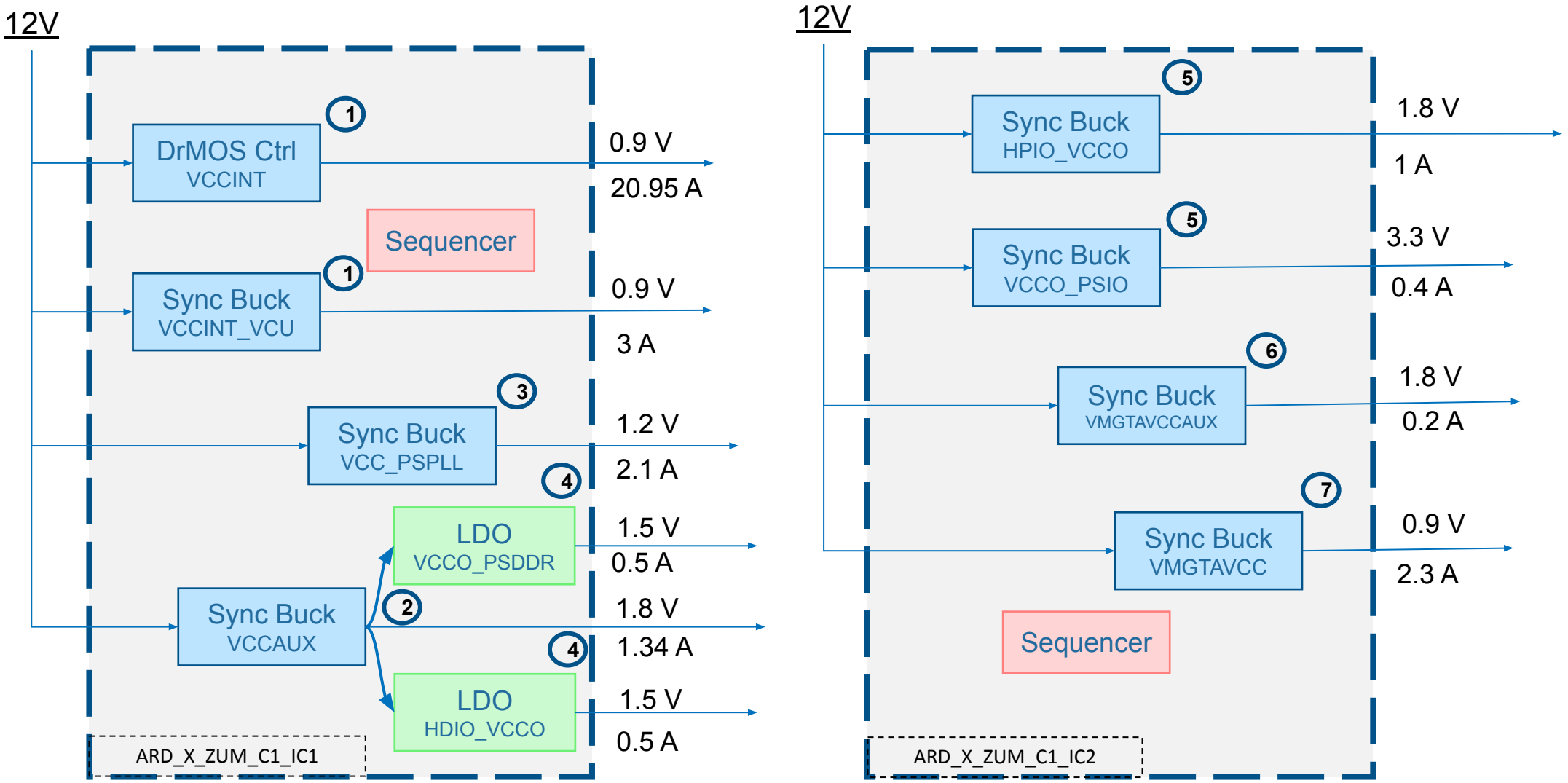
Power Tree Mapping: Performance-Optimized Use-Case C

V_{IN} = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC	Comment
1	VCCINT, VCCBRAM, VCCINT_IO, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR	1	C860	DrMOS Ctrl	V_{IN}	12	0.9	3.15-20.95	ARD_X_ZUM_C1_IC1	
2	VCCINT_VCU*	1	C200	Sync Buck	V_{IN}	12	0.9	3	ARD_X_ZUM_C1_IC1	VCCINT_VCU* for EV devices only
3	VCC_PSPLL, VMGTAVTT(GTH), VMGTAVTT(GTY)	3	C200	Sync Buck	V_{IN}	12	1.2	2.1	ARD_X_ZUM_C1_IC1	
4	VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL	2	C200	Sync Buck	V_{IN}	12	1.8	1.34	ARD_X_ZUM_C1_IC1	
5	VCCO_PSIO[3:0]	5	C200	Sync Buck	V_{IN}	12	1.8-3.3	0.4	ARD_X_ZUM_C1_IC2	
6	VMGTAVCCAUX(GTH), VMGTAVCCAUX(GTY), VPS_MGTTRAVTT	6	C200	Sync Buck	V_{IN}	12	1.8	0.1-0.2	ARD_X_ZUM_C1_IC2	
7	VMGTAVCC(GTH), VMGTAVCC(GTY), VPS_MGTRAVCC	7	C200	Sync Buck	V_{IN}	12	0.9	2.3	ARD_X_ZUM_C1_IC2	
8	VCCO_PSDDR	4	C710	SIM LDO	VCCAUX	1.8	1.1-1.5	0.5	ARD_X_ZUM_C1_IC1	
9	HDIO_VCCO	4	C710	SIM LDO	VCCAUX	1.8	1.5	0.5	ARD_X_ZUM_C1_IC1	
10	HPIO_VCCO	5	C200	Sync Buck	V_{IN}	12	1-1.8	1	ARD_X_ZUM_C1_IC2	

AnDAPT Confidential

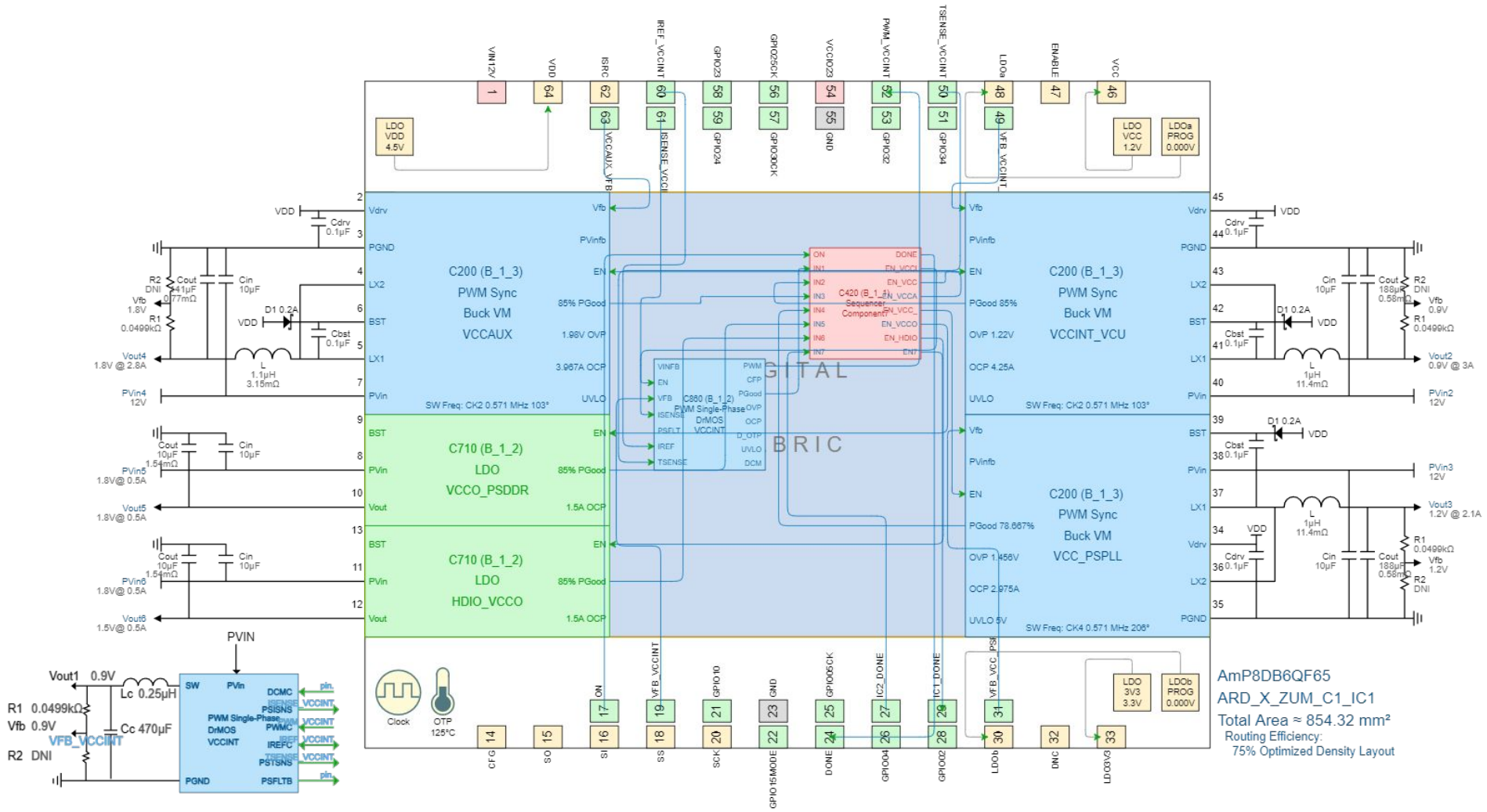
Proposed Solution (2xPMICs)
Use-Case C



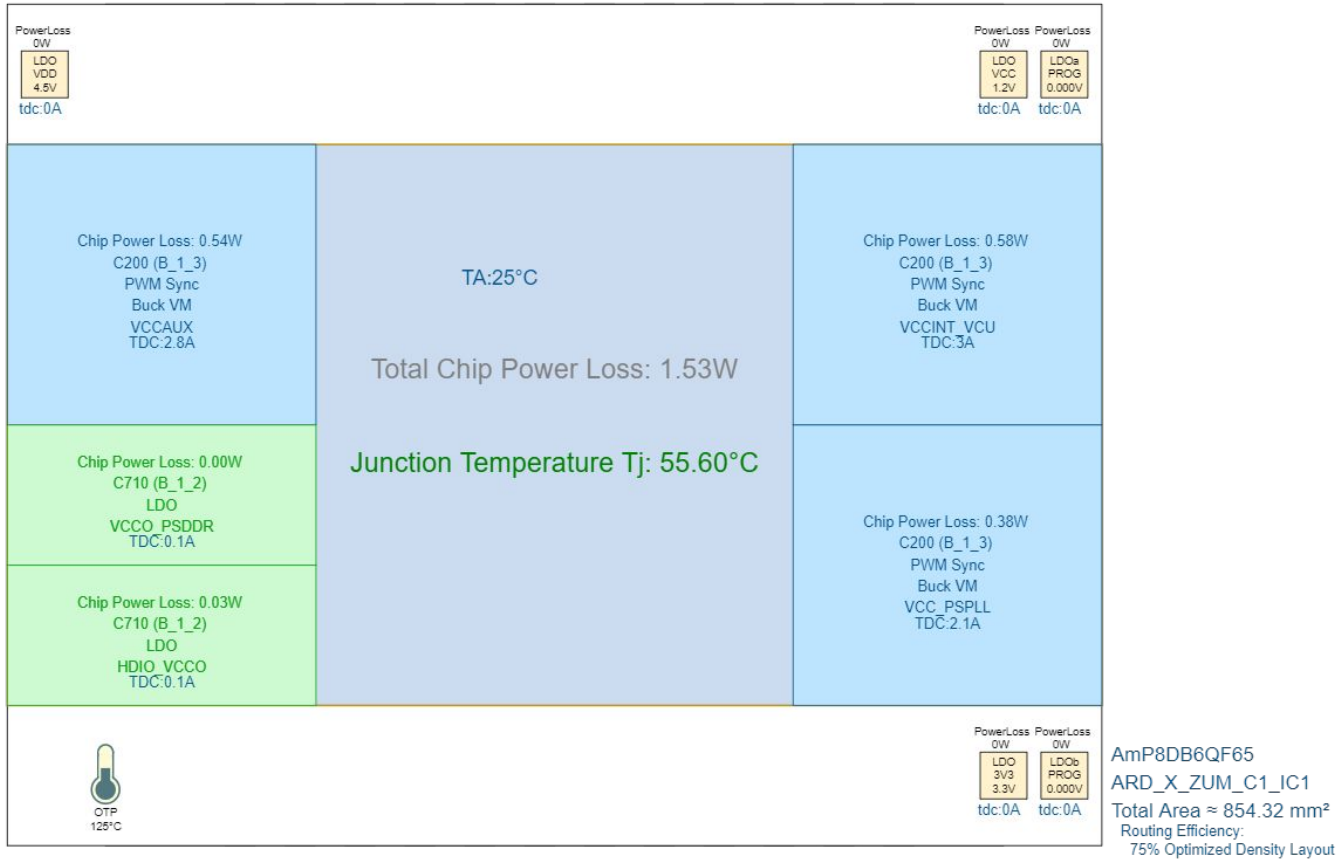
Estimated Total Area = 1237.73 mm^2

AnDAPT

Mapping IC1 (WebAmp View)
Use-Case C

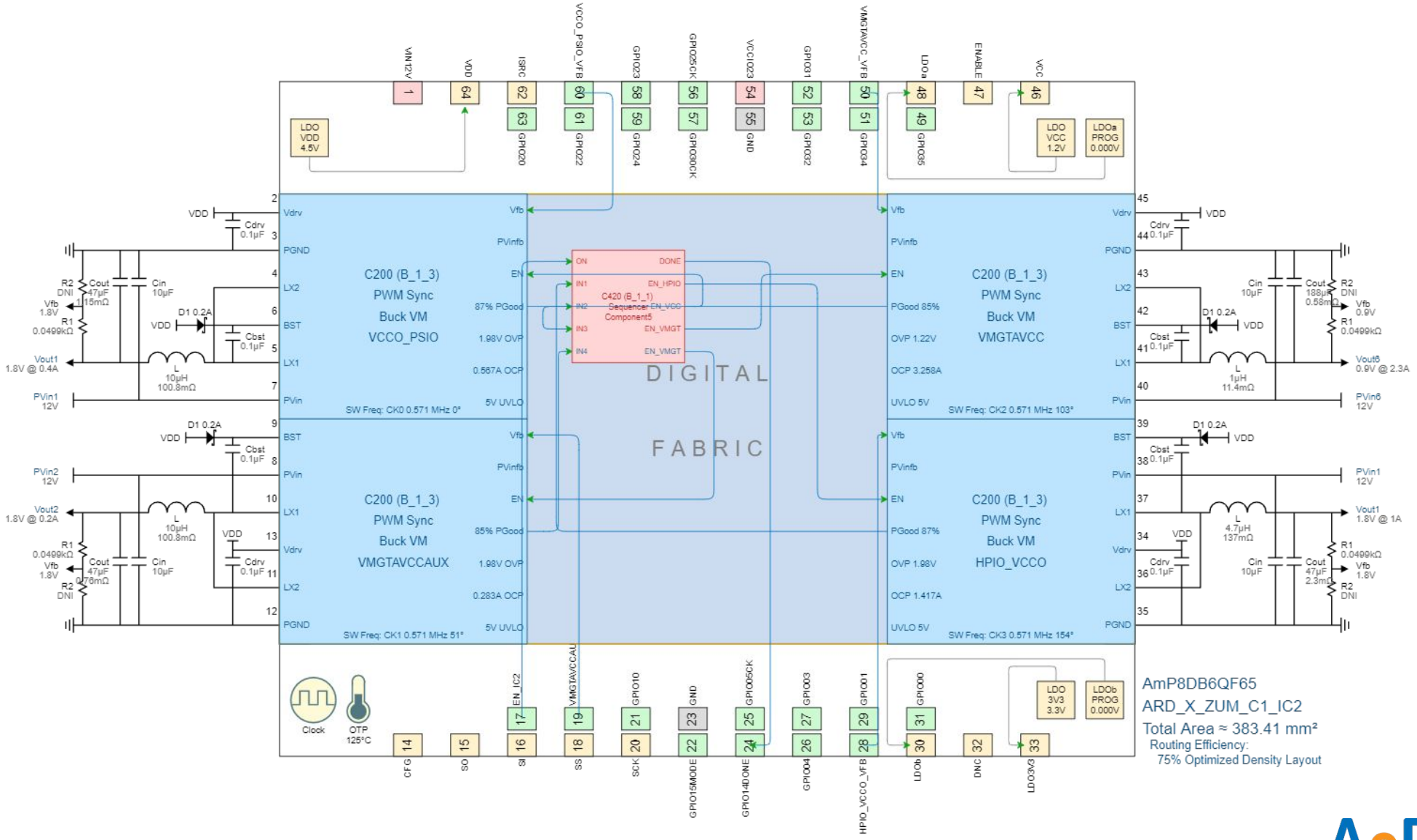


Thermal Design View (IC1)
Use-Case C1

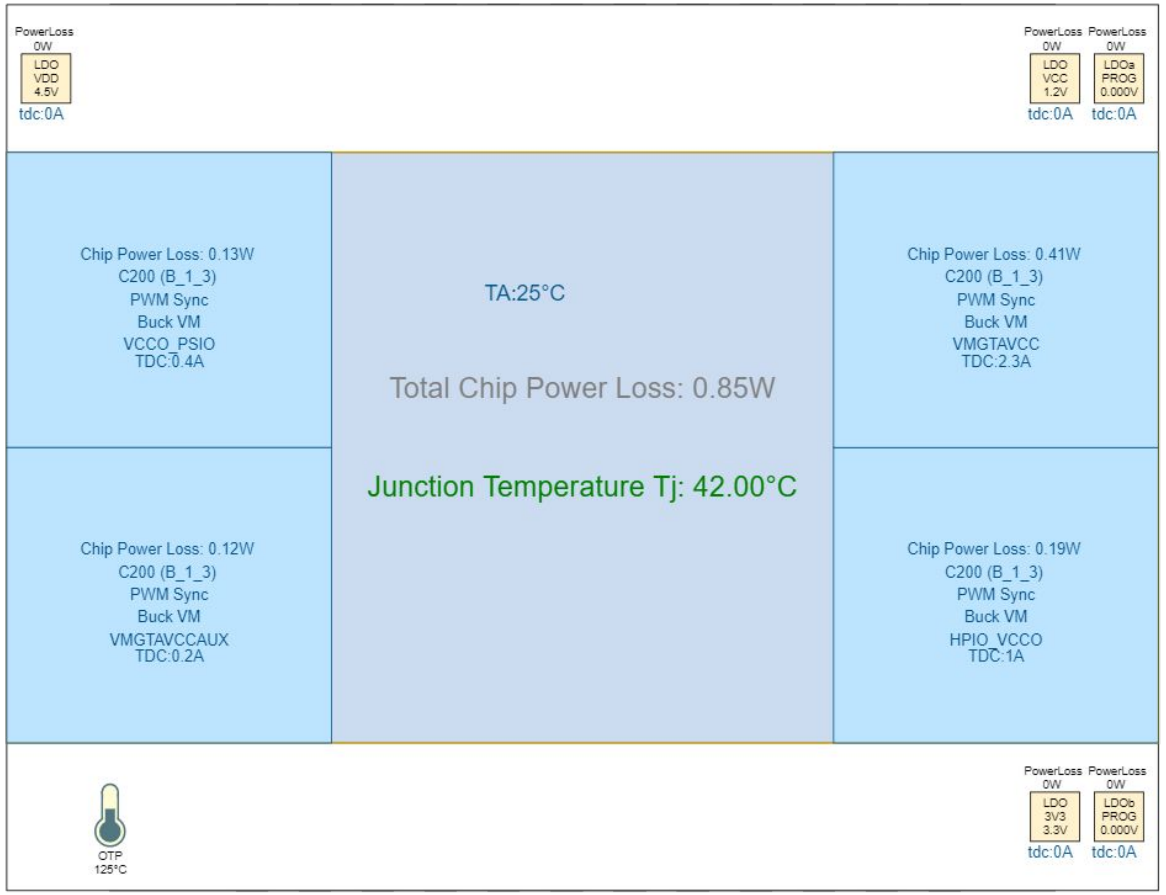


AnDAPT Confidential

Mapping IC2 (WebAmp View)
Use-Case C

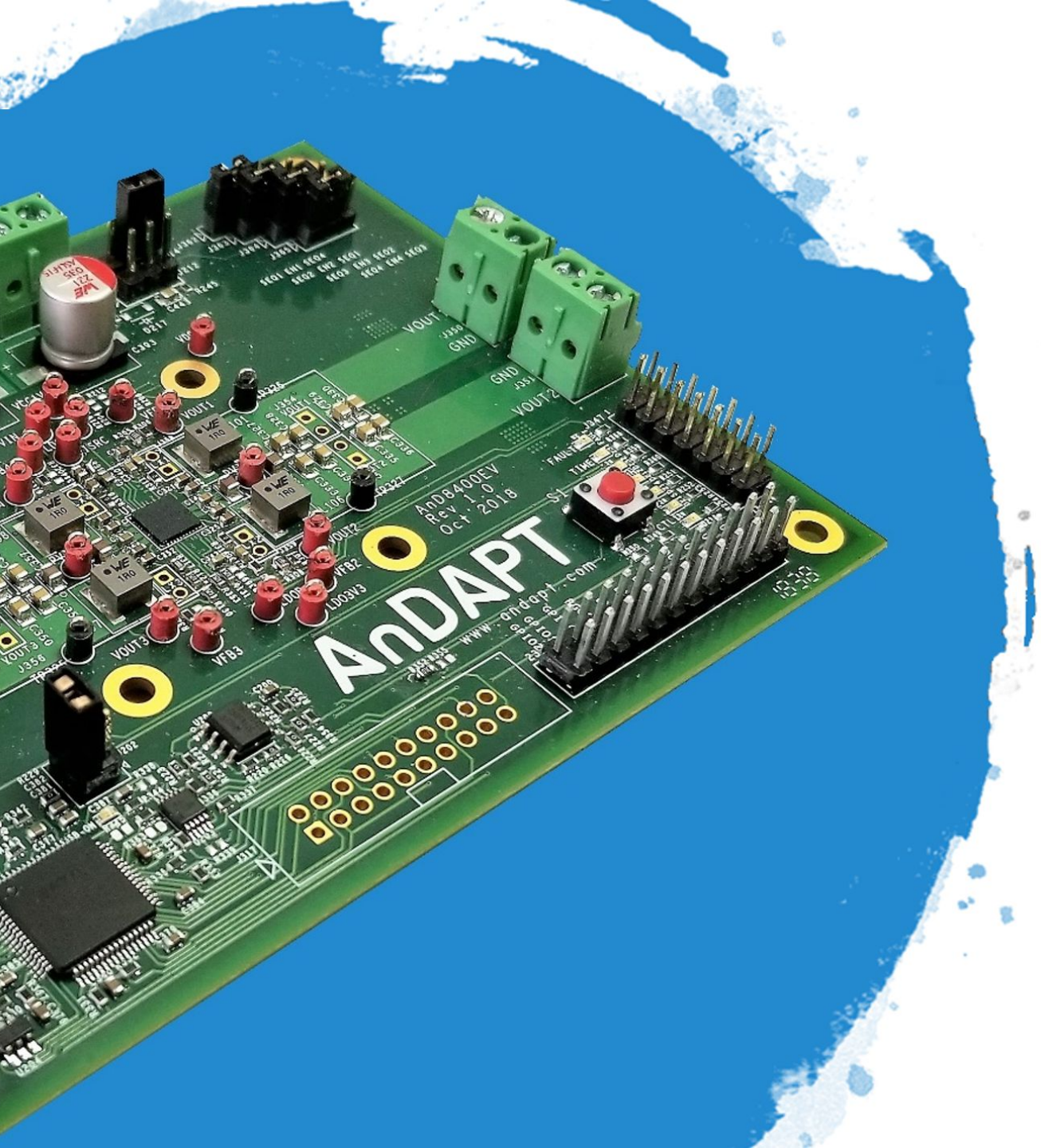


Thermal Design View (IC2)
Use-Case C1



AmP8DB6QF65
ARD_X_ZUM_C1_IC2
Total Area ≈ 383.41 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT Confidential

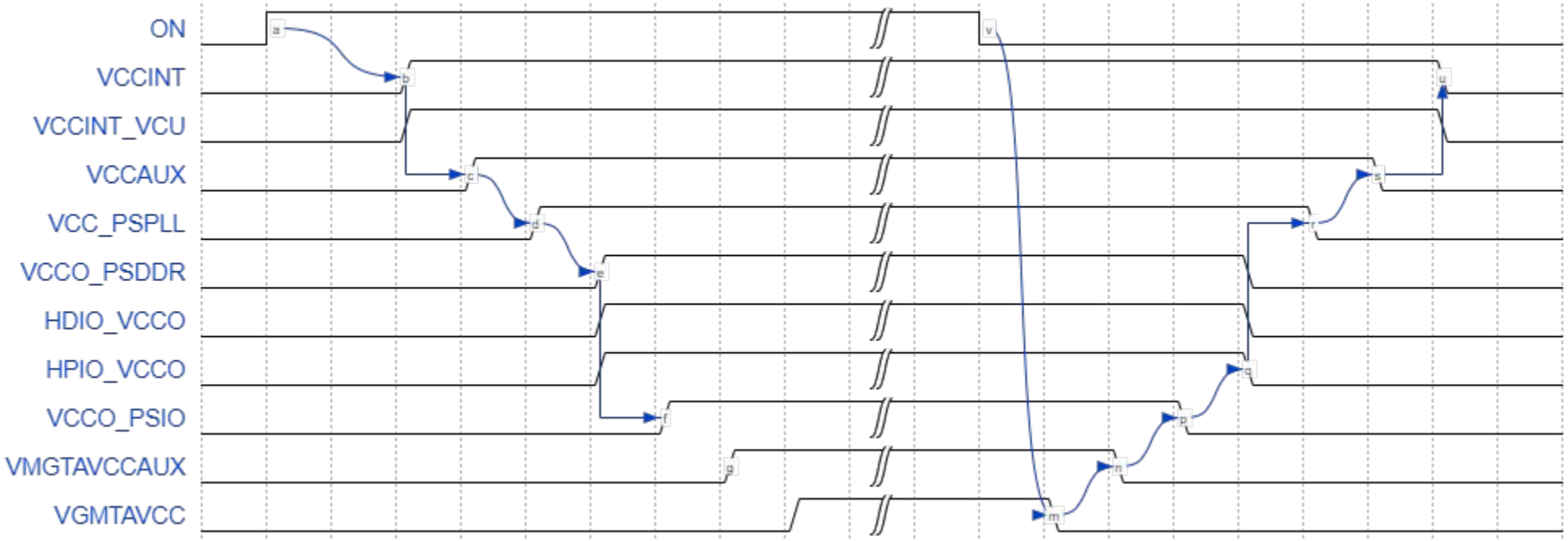


Bench Data

Use-Case C

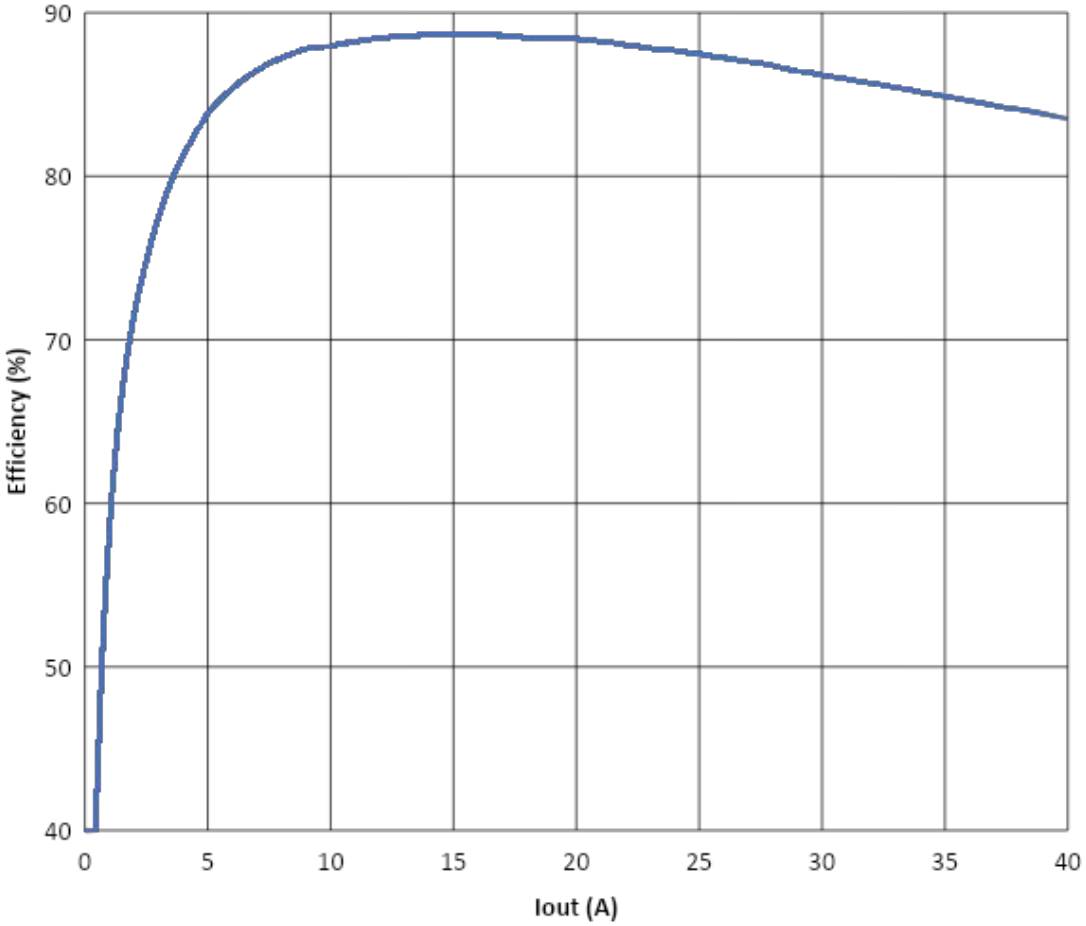
AnDAPT

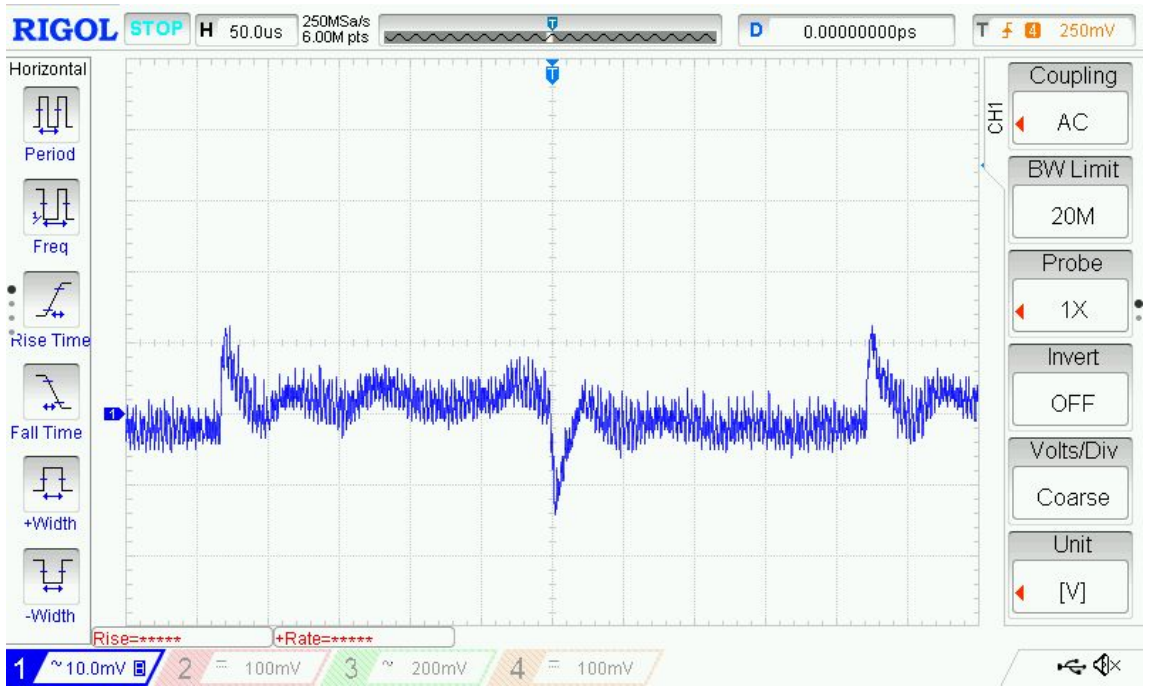
Integrated Sequencer Graphic (Turn ON/OFF)



AnDAPT Confidential

VCCINT: Efficiency & Transient

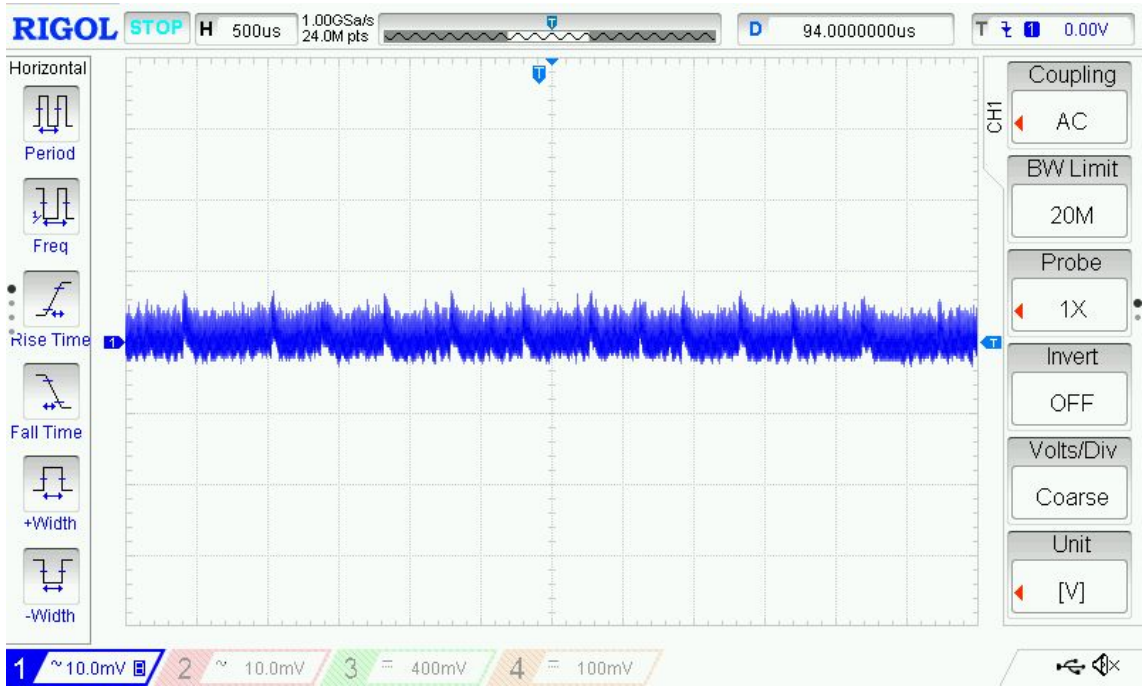




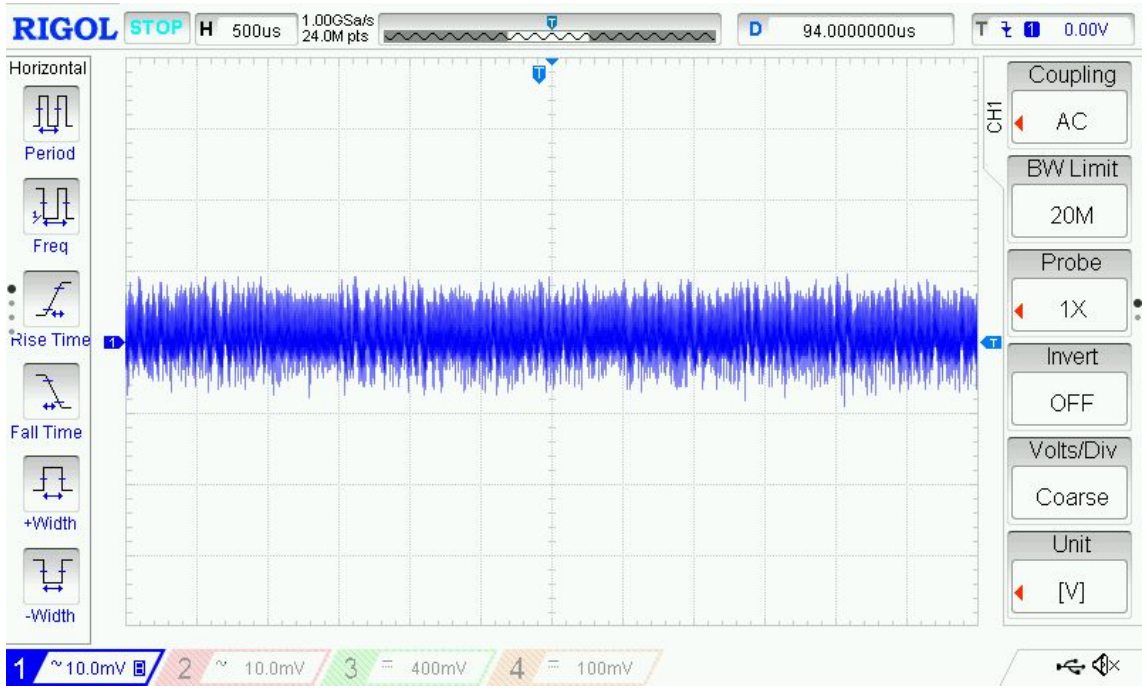
Vout = 0.85 V
Transient 23 A – 32.25 A @ 100 A/us
V_{PP} = 26 mV
Fsw = 800 kHz
Lout = 250 nH, Cout = 20 x 47 µF

AnDAPT Confidential

VCCINT: Ripple



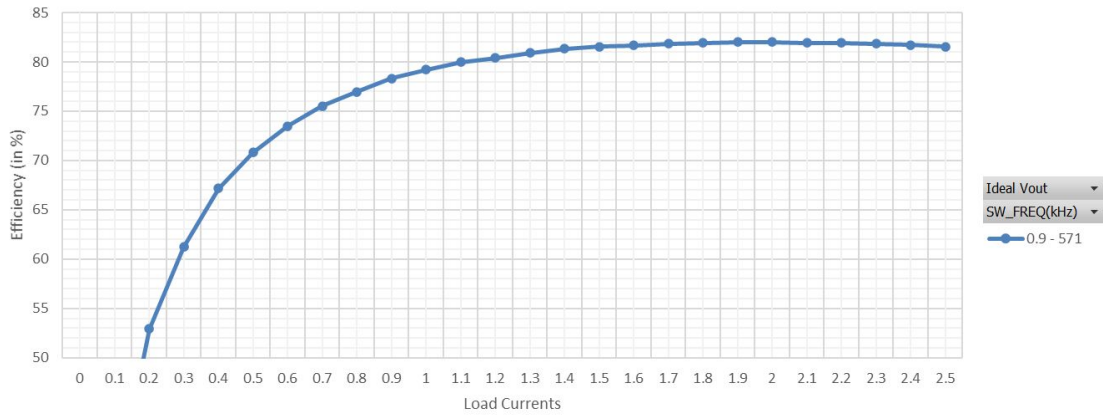
No Load
V_{PP} = 10 mV

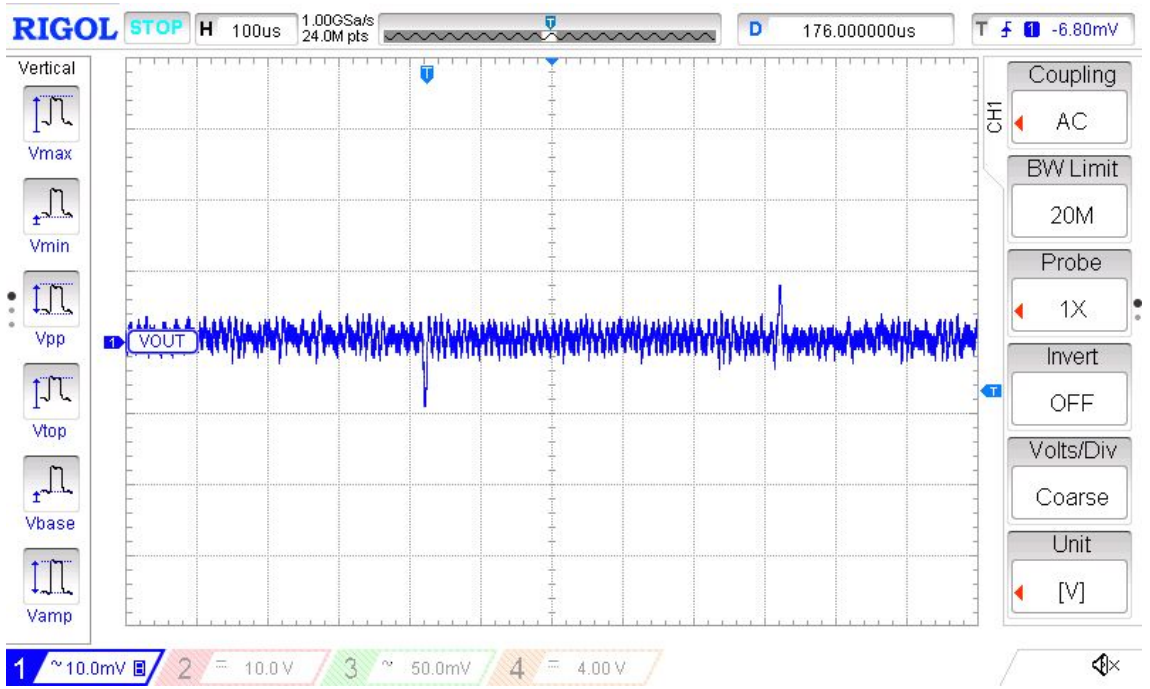


40A Load
V_{PP} = 16.4 mV

AnDAPT Confidential
AnDAPT

VCCINT_VCU: Efficiency & Transient

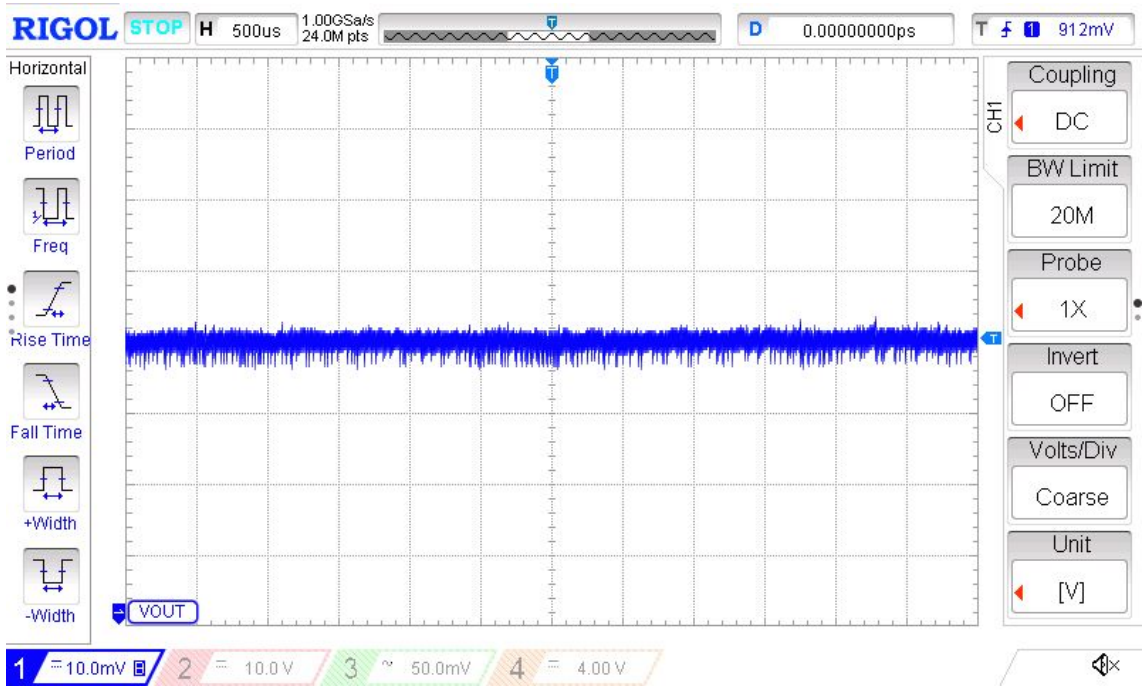




Vout = 0.9V
Transient 2.25 A to 3 A
V_{PP} = 17.2 mV
Lout = 1 µH, Cout = 4 x 47 µF

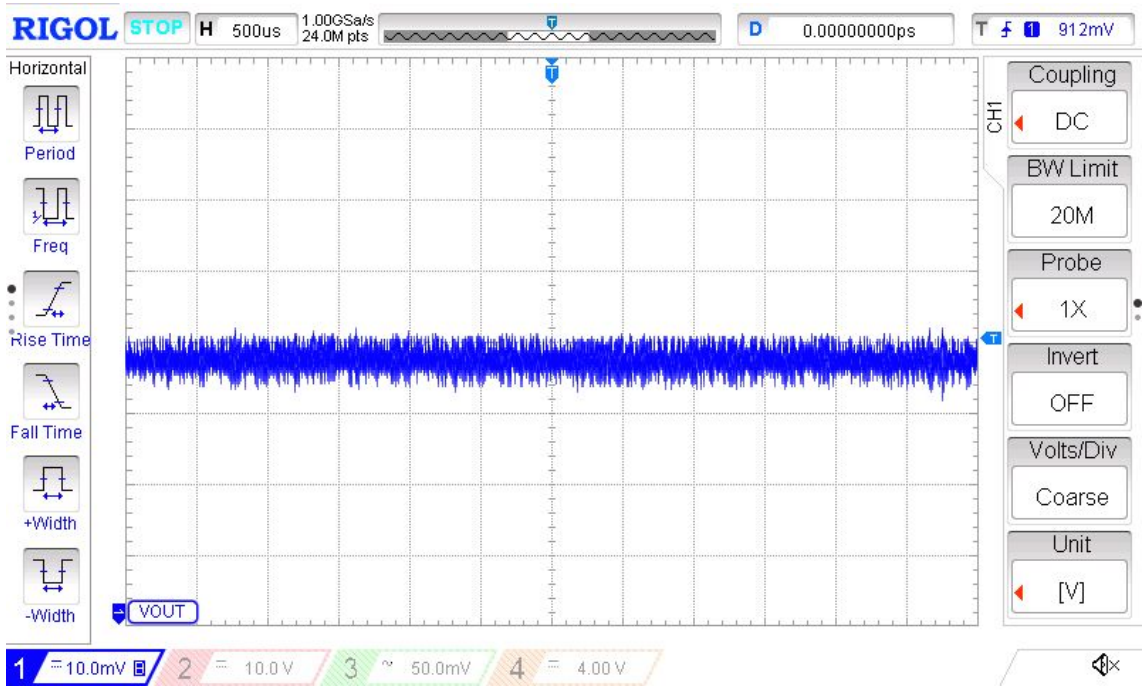
AnDAPT Confidential
AnDAPT

VCCINT_VCU: Ripple



No Load

V_{PP} = 6.4 mV



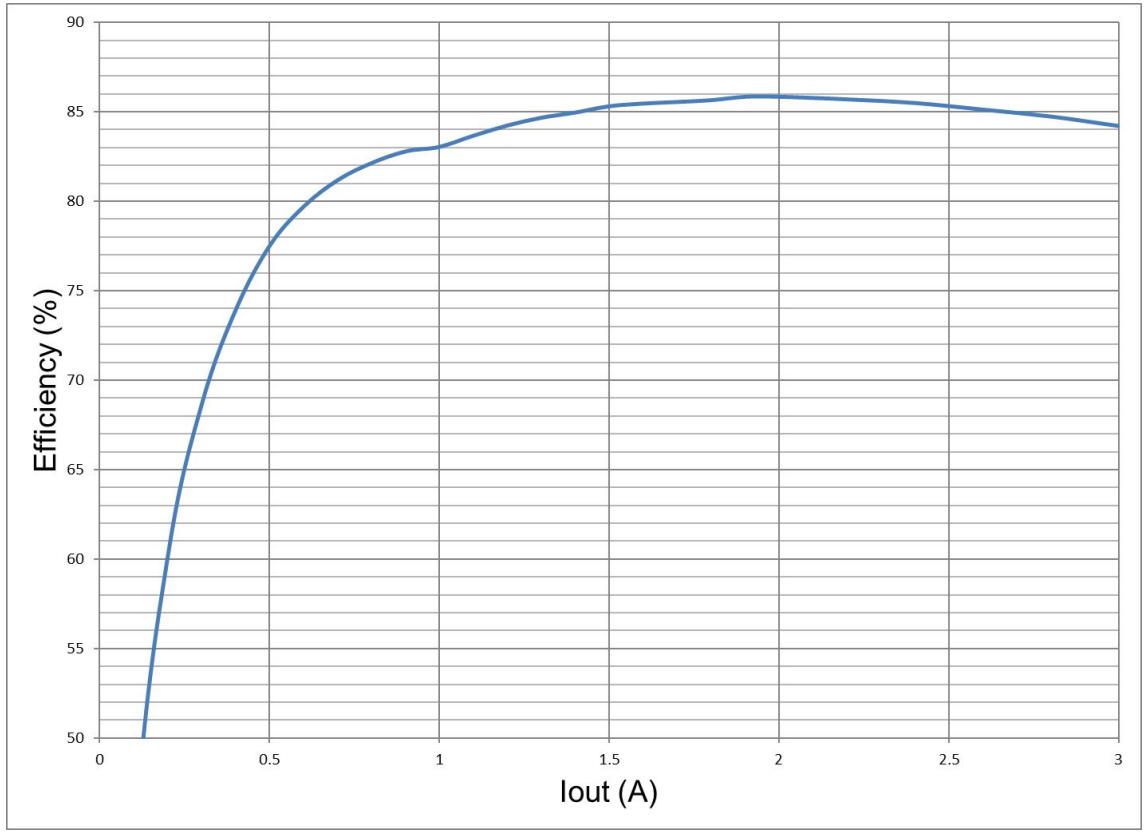
3A Load

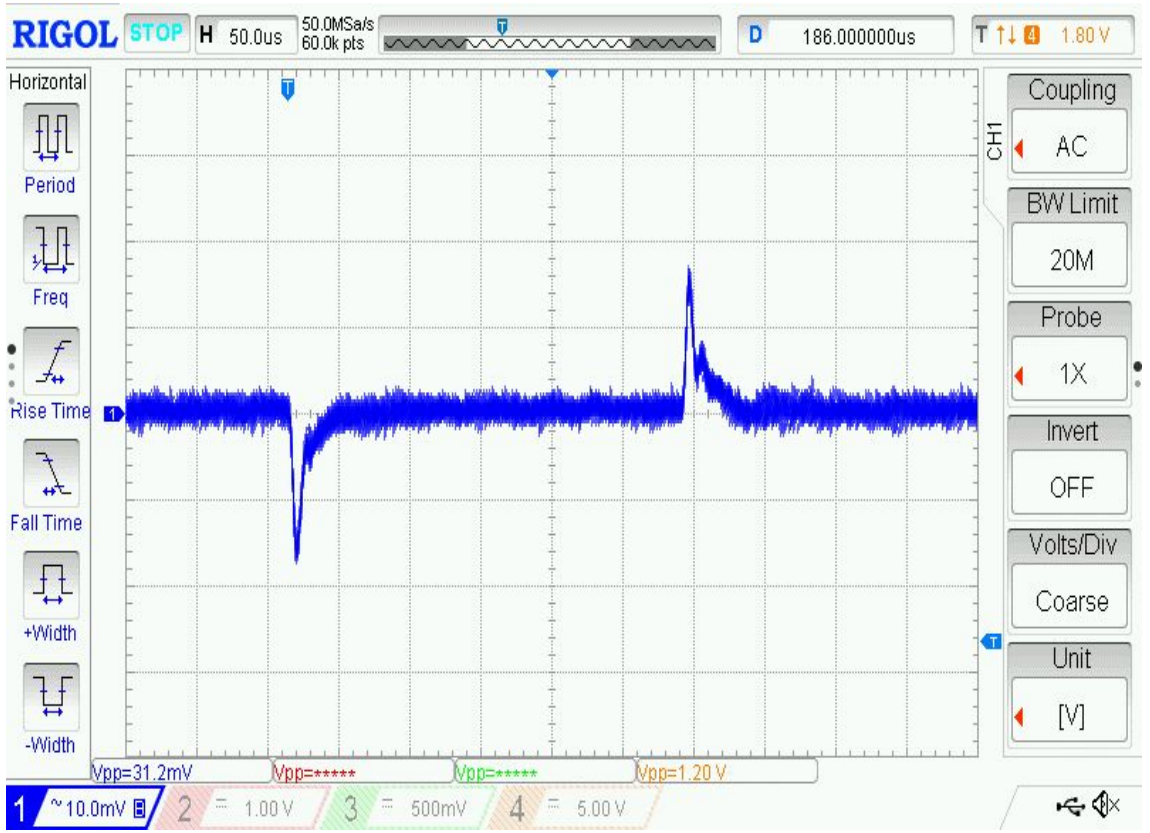
V_{PP} = 8 mV

AnDAPT Confidential

AnDAPT

VCC_PSPLL: Efficiency & Transient

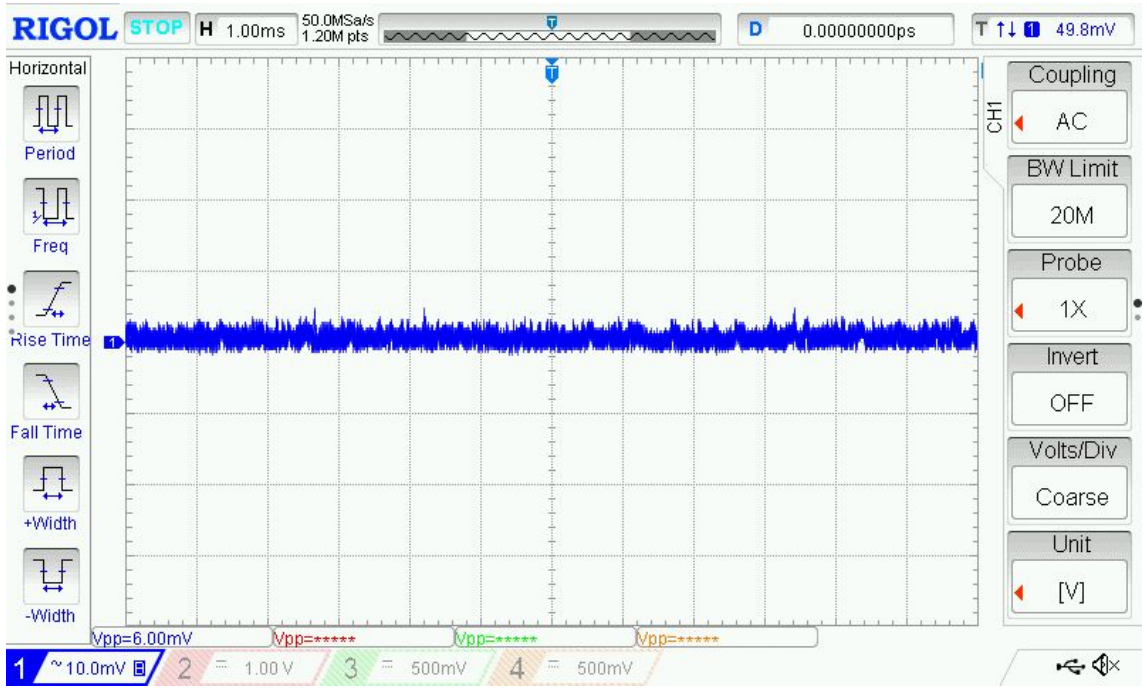




Vout = 1.2 V
Transient 2.25 A to 3 A
V_{PP} = 31.2 mV
Lout = 1 µH, Cout = 4 x 47 µF

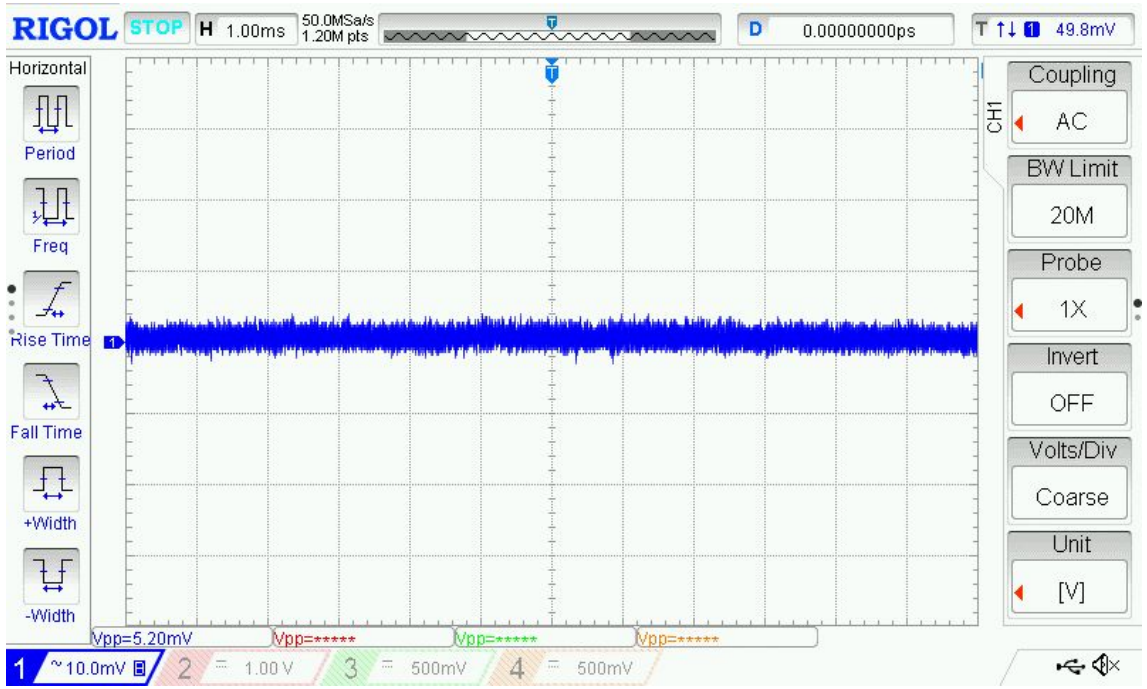
AnDAPT Confidential

VCC_PSPLL: Ripple



No Load

V_{PP} = 6 mV

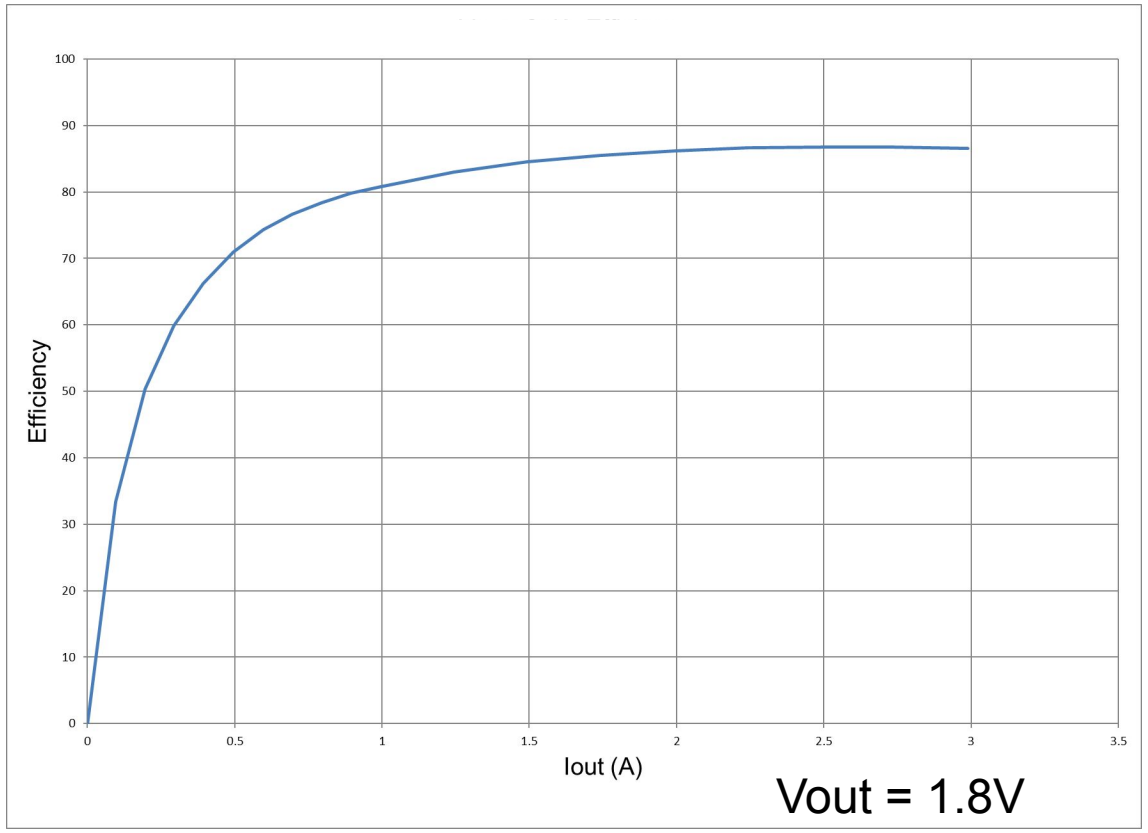


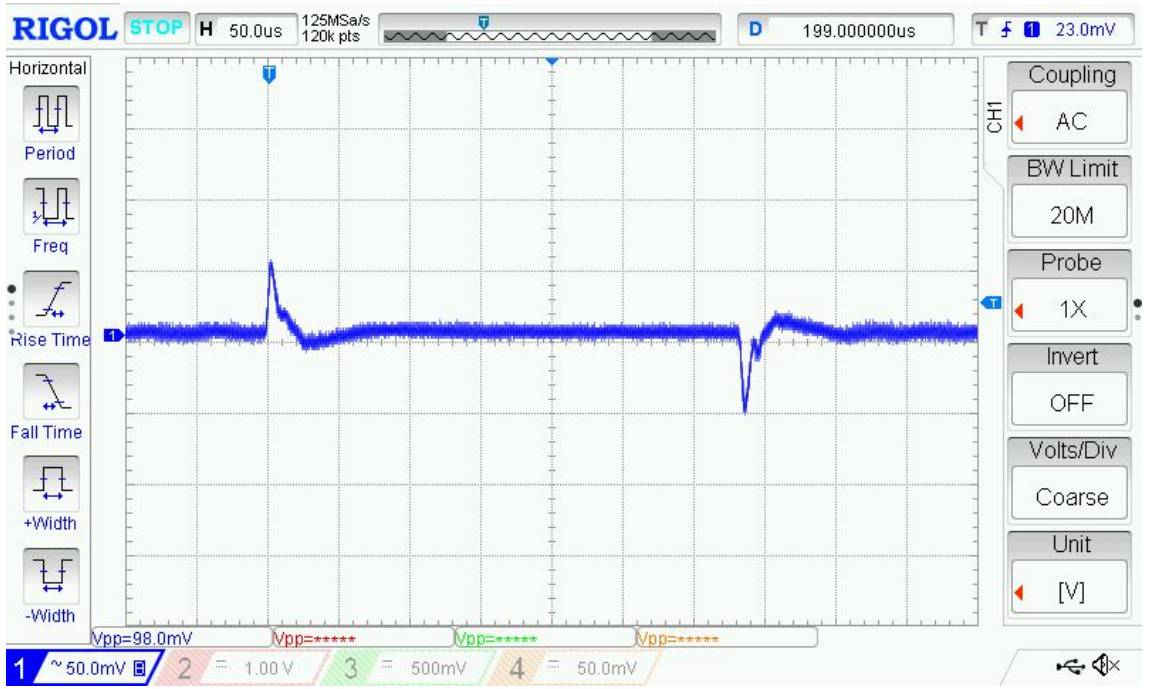
6 A Load

V_{PP} = 5.2 mV

AnDAPT Confidential

VCCAUX: Efficiency & Transient

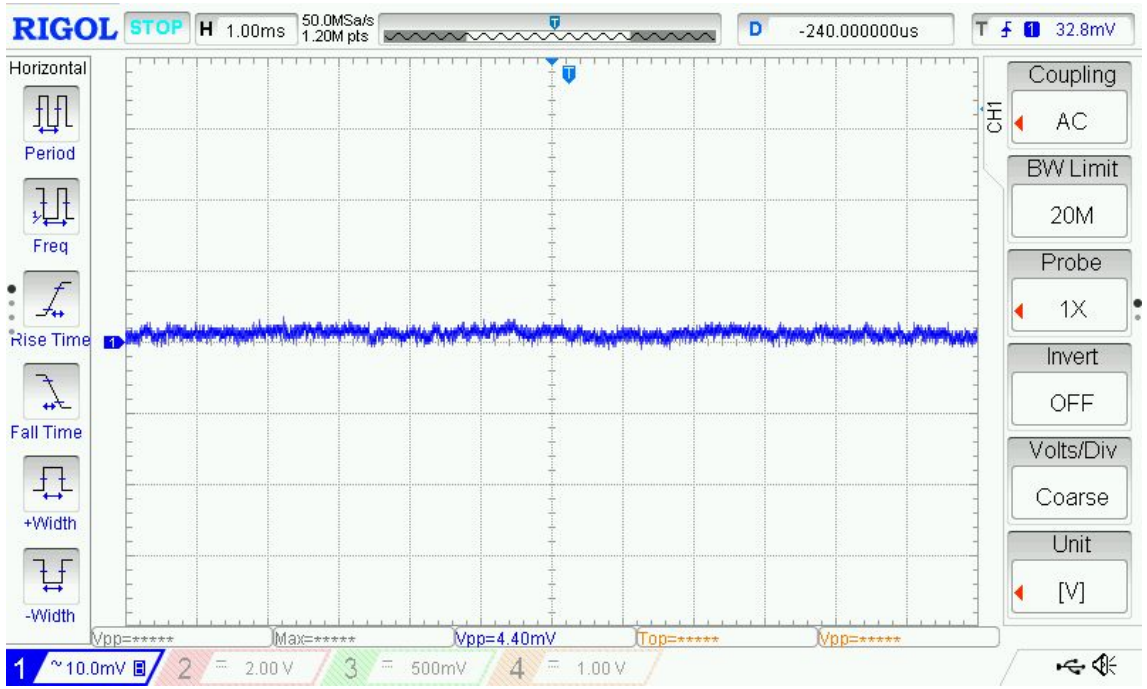




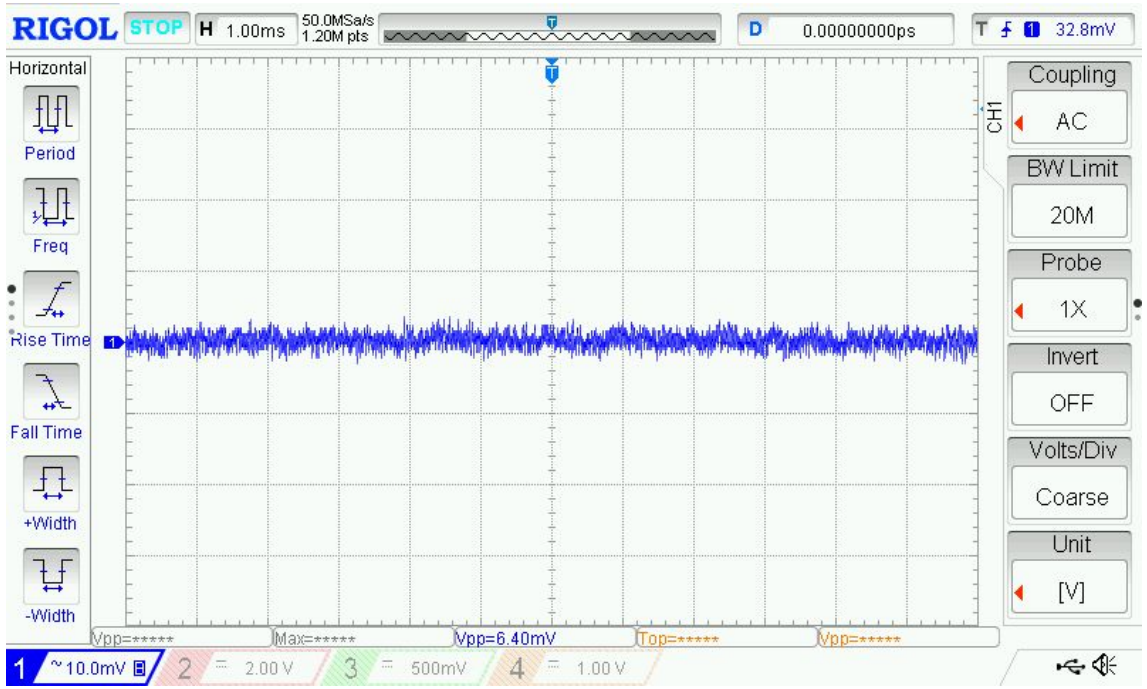
Vout = 1.8V
Transient 0.3A to 3A,
V_{PP} = 28 mV
L = 1.1 µH, C = 3 x 47 µF

AnDAPT Confidential

VCCAUX: Ripple



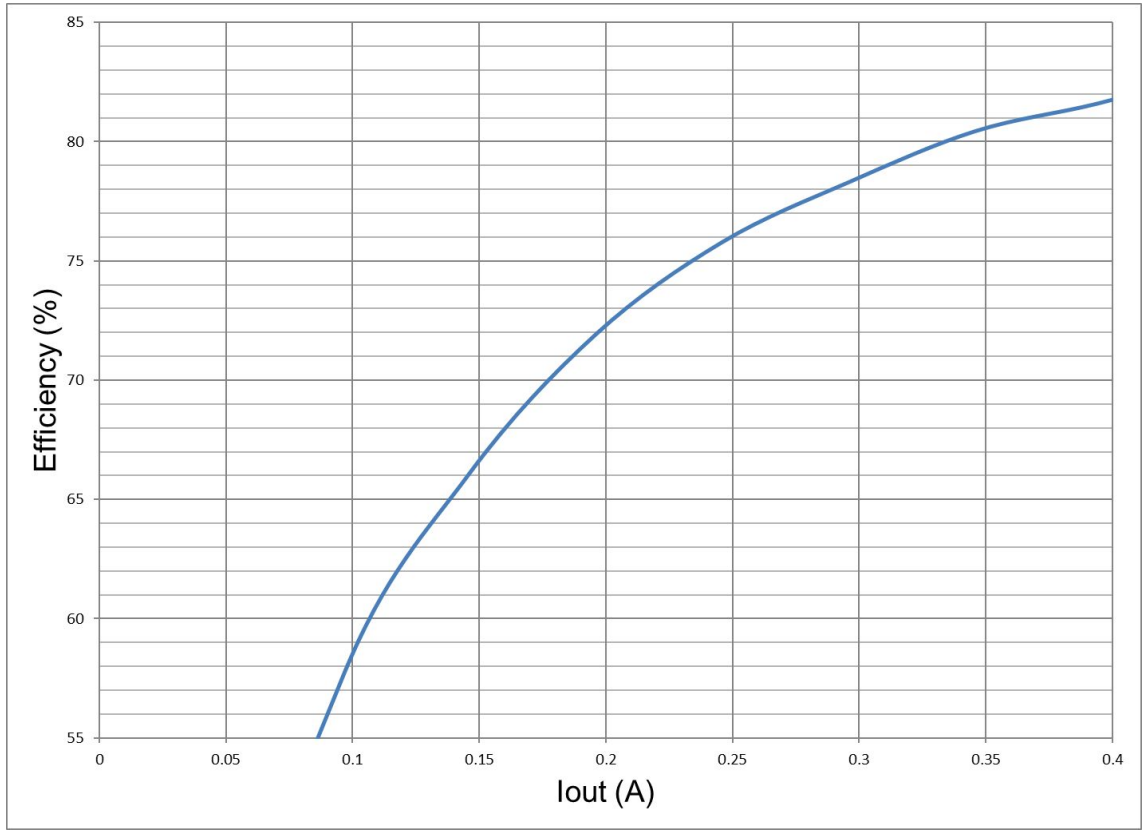
No Load
V_{PP} = 4.4 mV

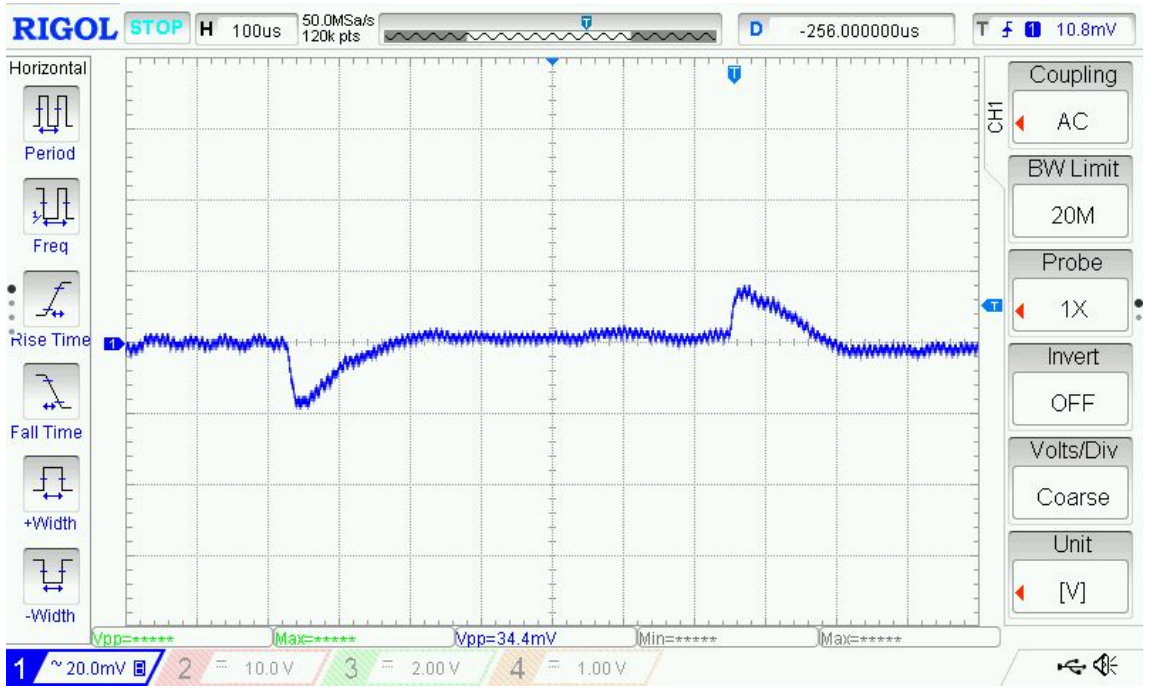


1.64 A Load
V_{PP} = 6.4 mV

AnDAPT Confidential

VCCO_PSIO: Efficiency & Transient

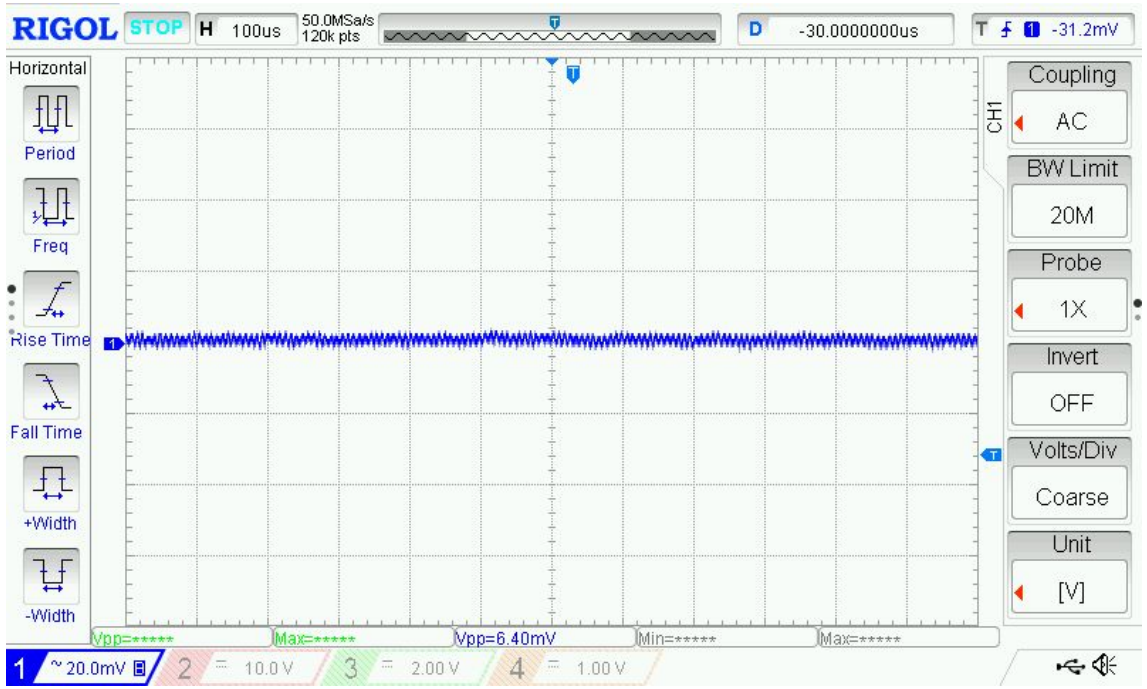




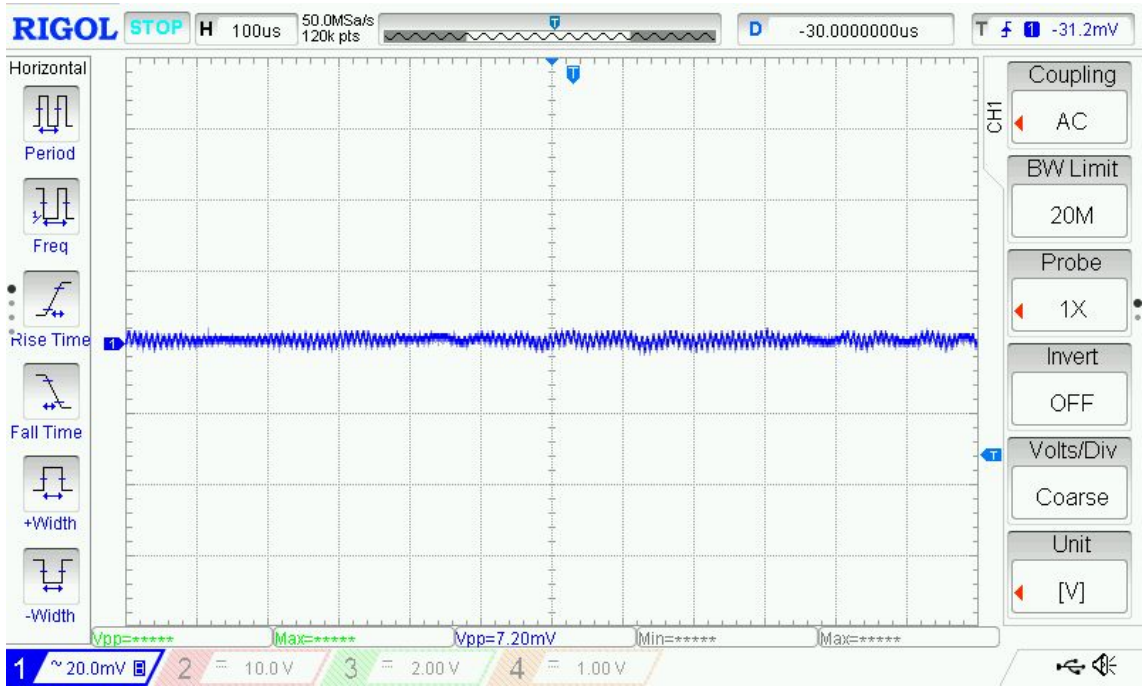
Vout = 1.8 V
Transient 0.12 A to 0.4 A
V_{PP} = 34.4 mV
Lout = 10 µH, Cout = 1 x 47 µF
Fsw = 1MHz

AnDAPT Confidential

VCCO_PSIO: Ripple



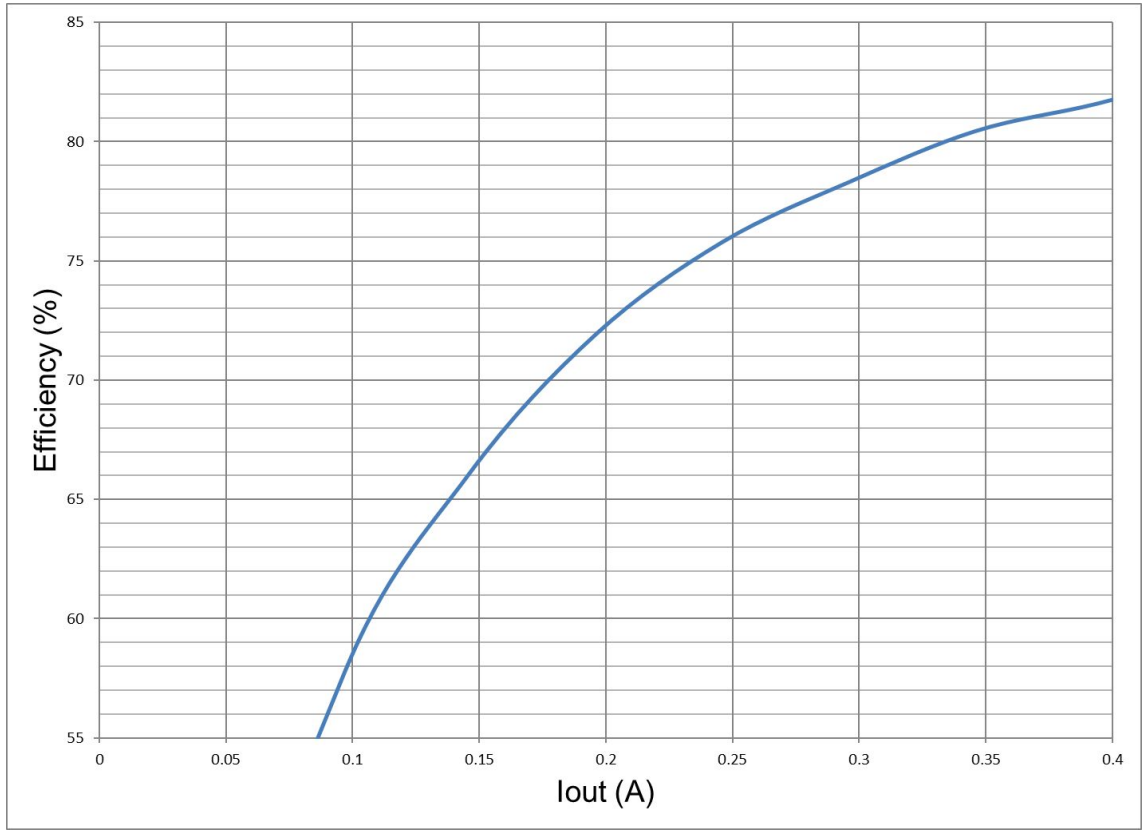
No Load
V_{PP} = 6.4 mV

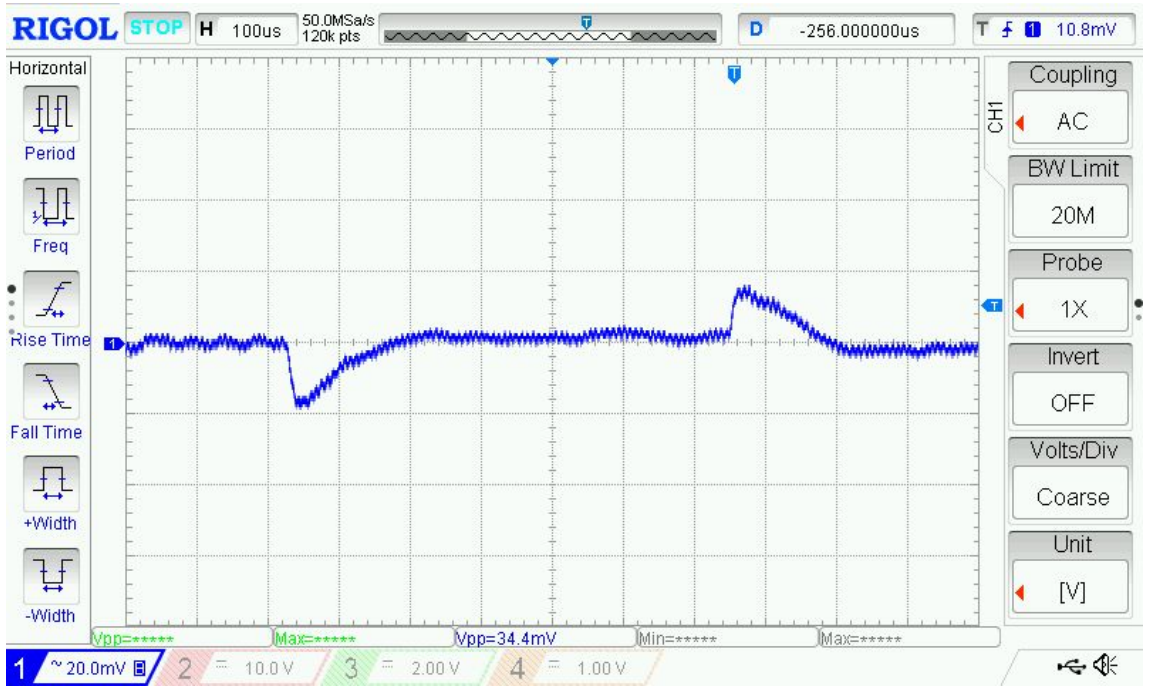


0.4 A Load
V_{PP} = 7.2 mV

AnDAPT Confidential

VMGTAVCCAUX: Efficiency & Transient

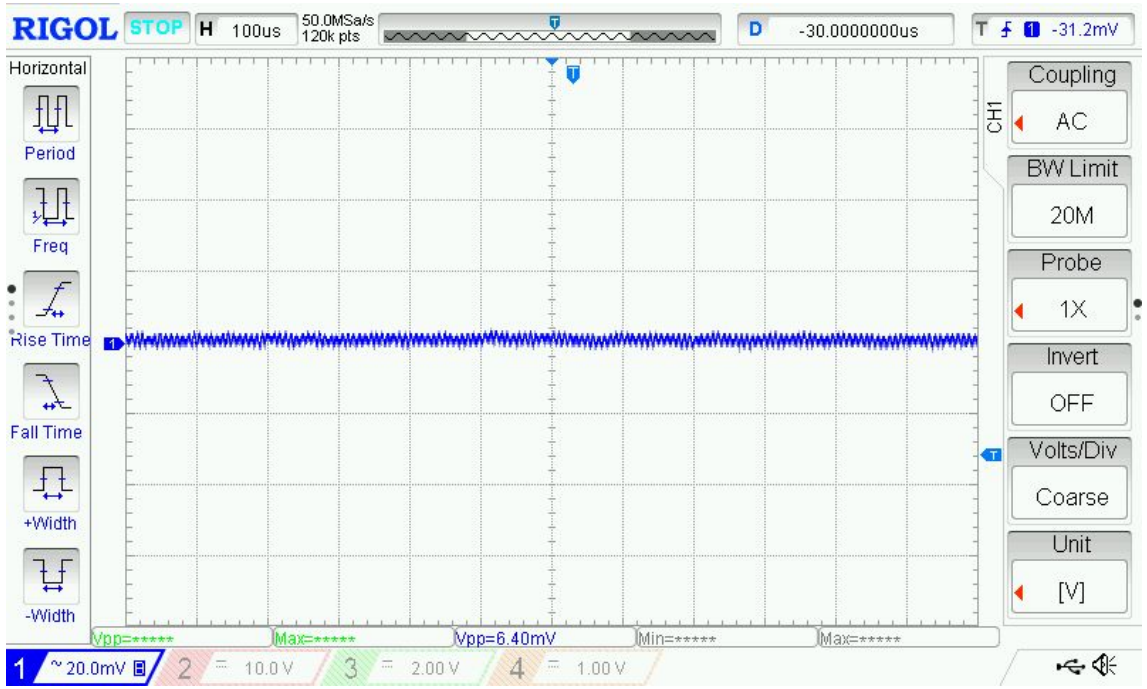




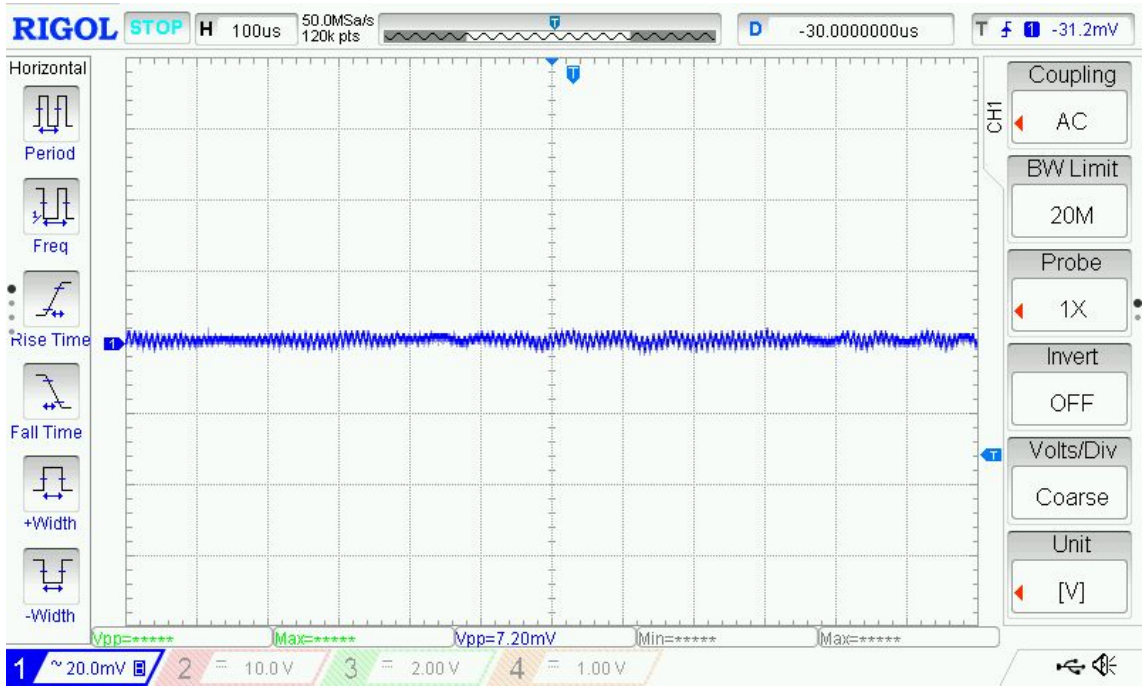
Vout = 1.8 V
Transient 0.12 A to 0.4 A
V_{PP} = 34.4 mV
Lout = 10 µH, Cout = 1 x 47 µF
Fsw = 1MHz

AnDAPT Confidential

VMGTAVCCAUX: Ripple



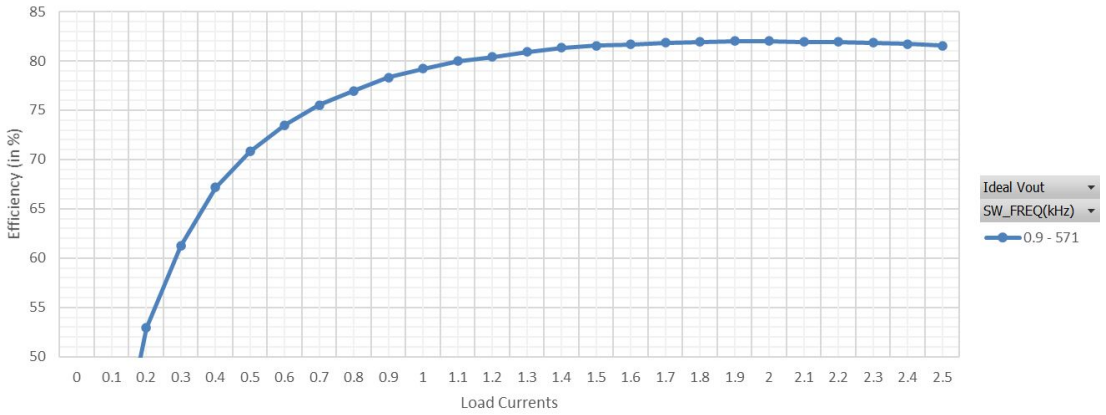
No Load
V_{PP} = 6.4 mV

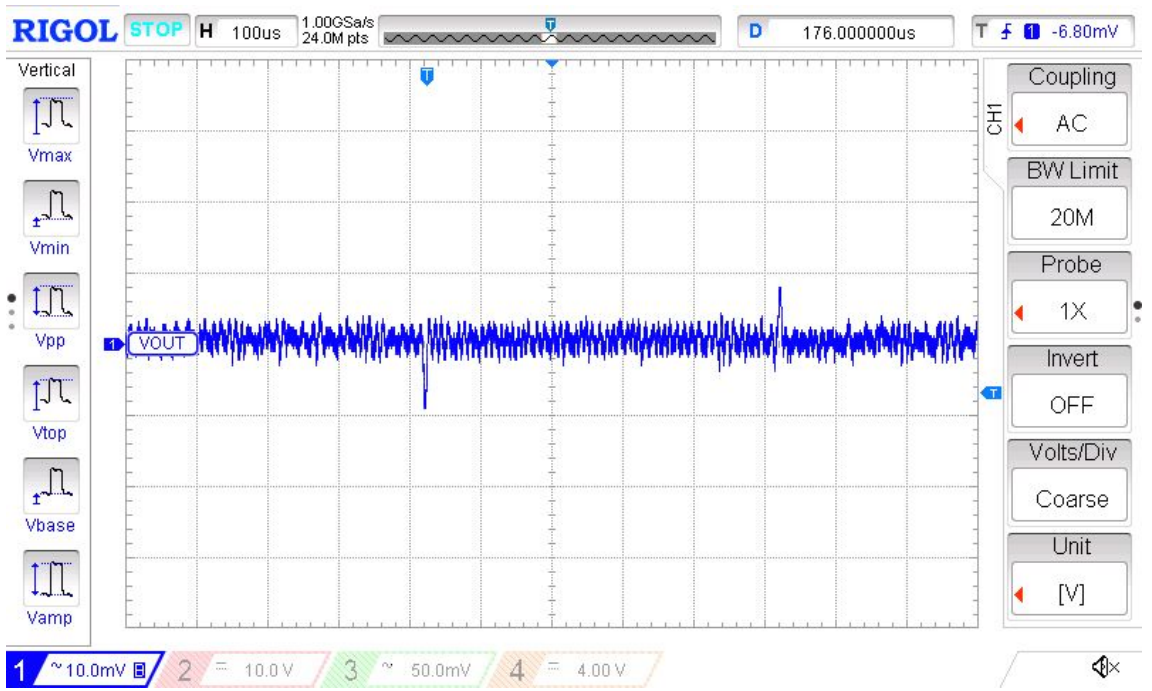


0.4 A Load
V_{PP} = 7.2 mV

AnDAPT Confidential
AnDAPT

VMGTAVCC: Efficiency & Transient

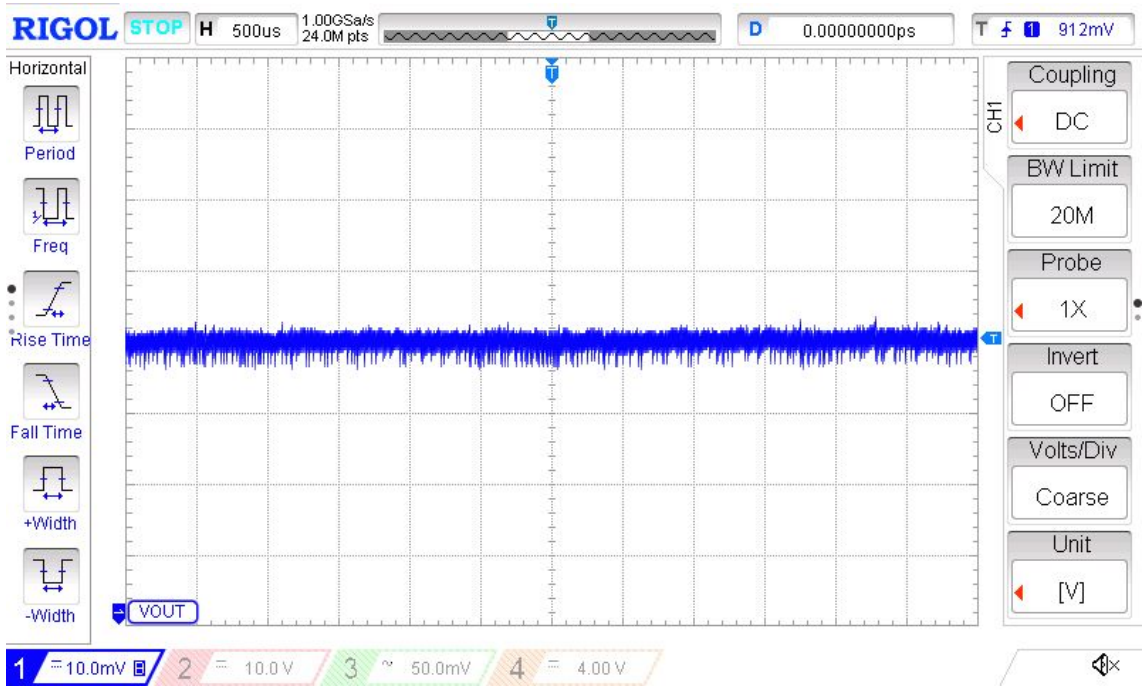




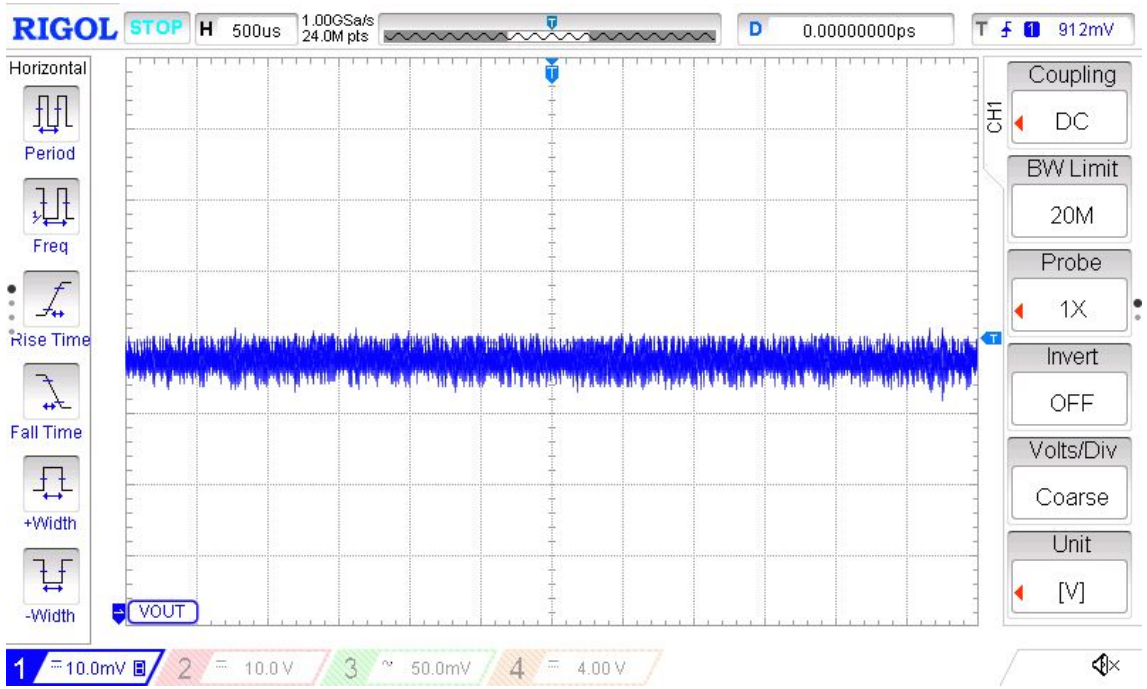
Vout = 0.9 V
Load transient 2.25A to 3A
V_{PP} = 17.2 mV
L = 1 µH, C = 4 x 47 µF

AnDAPT Confidential

VMGTAVCC: Ripple



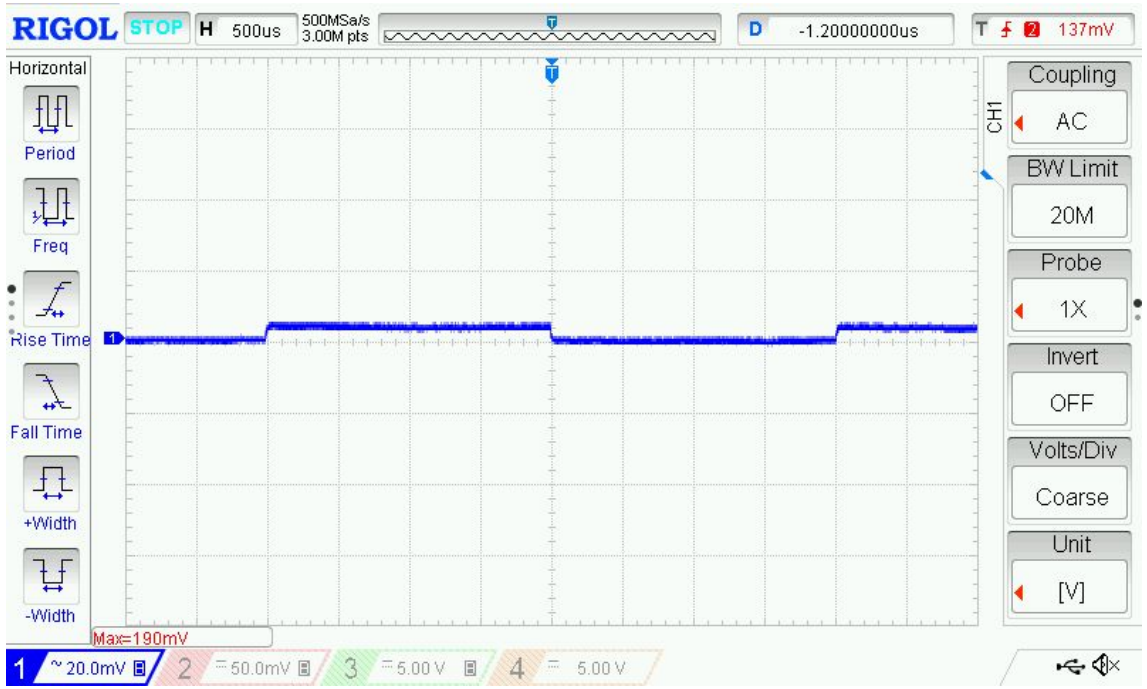
No Load
V_{PP} = 6.4 mV



3 A Load
V_{PP} = 8 mV

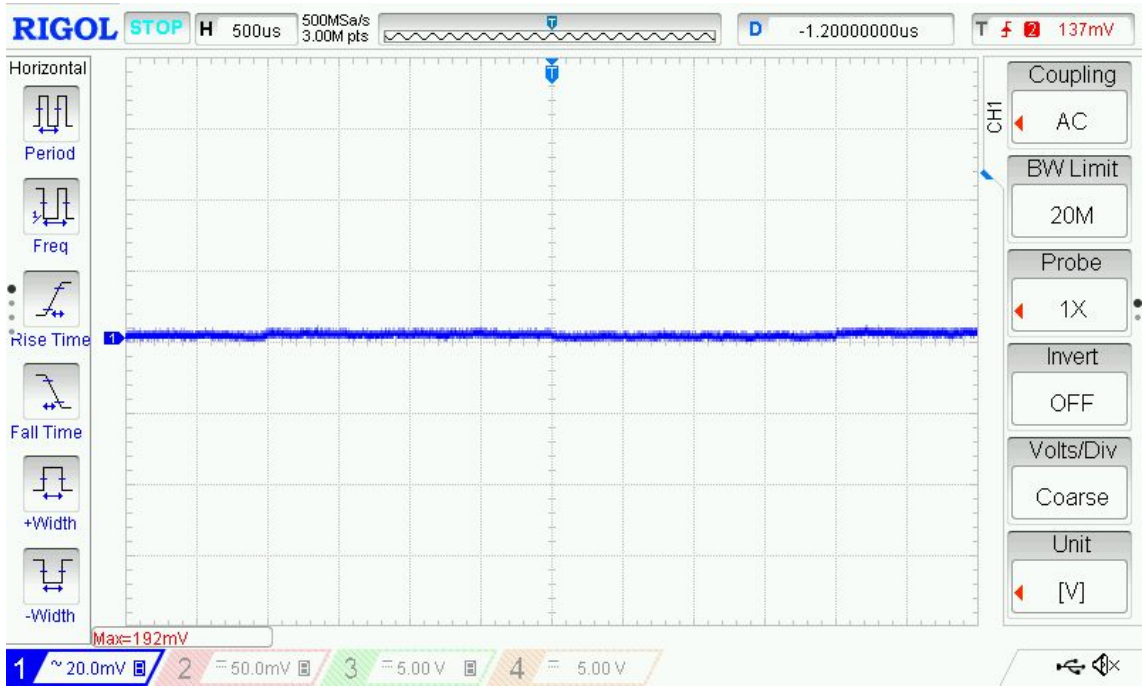
AnDAPT Confidential

LDO Rails: Transient



Internal

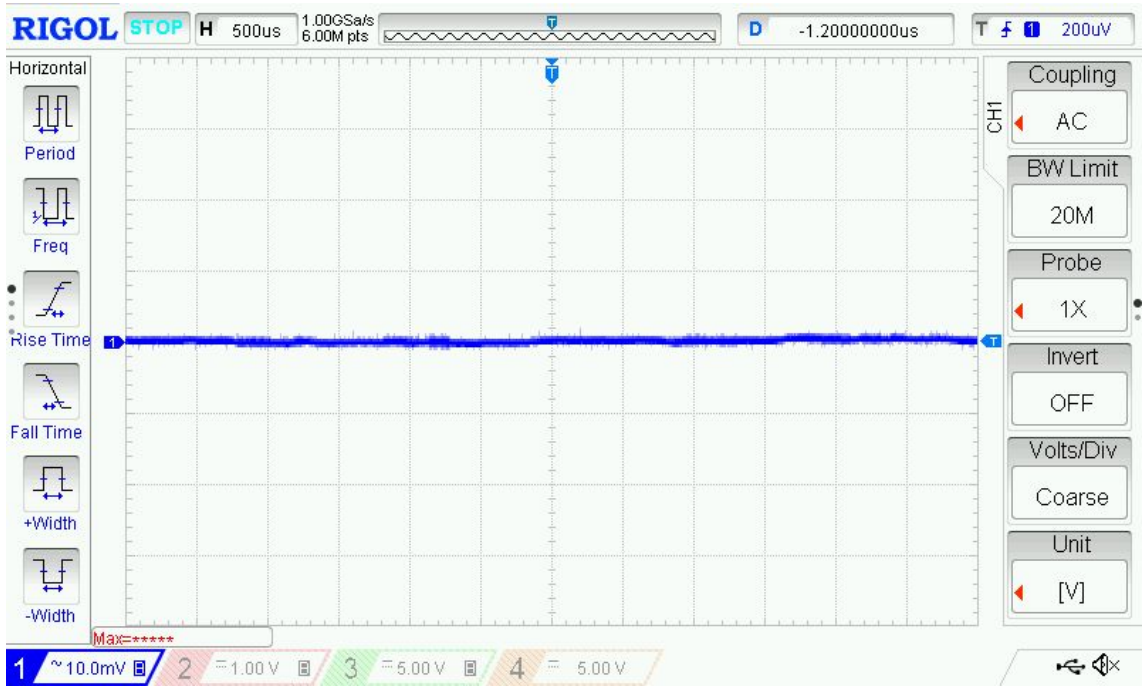
Vout = 1.5 V
Transient 0.25 A to 0.5 A
V_{PP} = 17.2 mV
Cout = 22uF



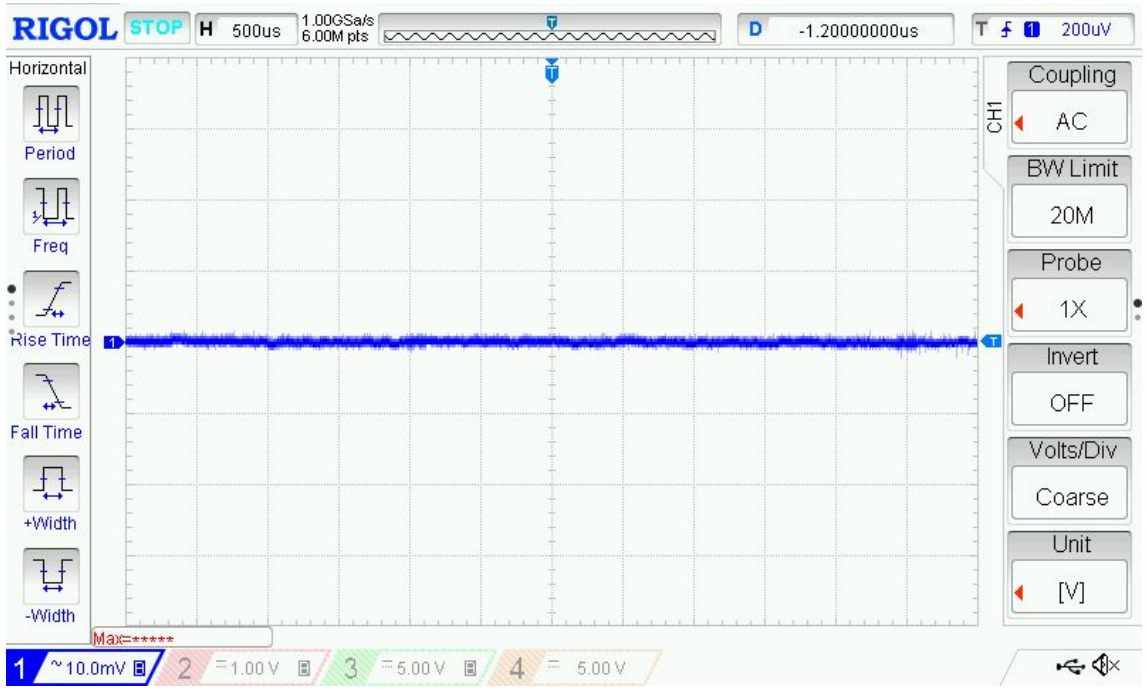
External

AnDAPT Confidential

LDO Rails: Ripple



No Load



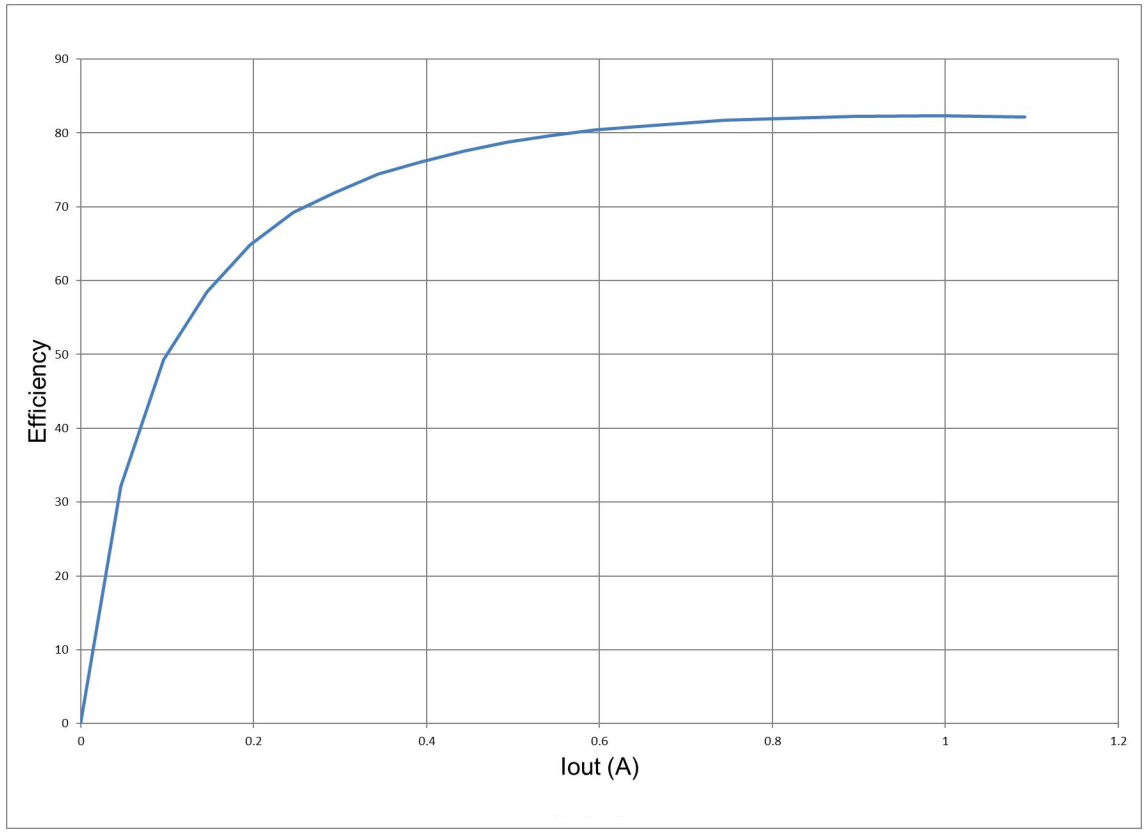
Cout = 22uF

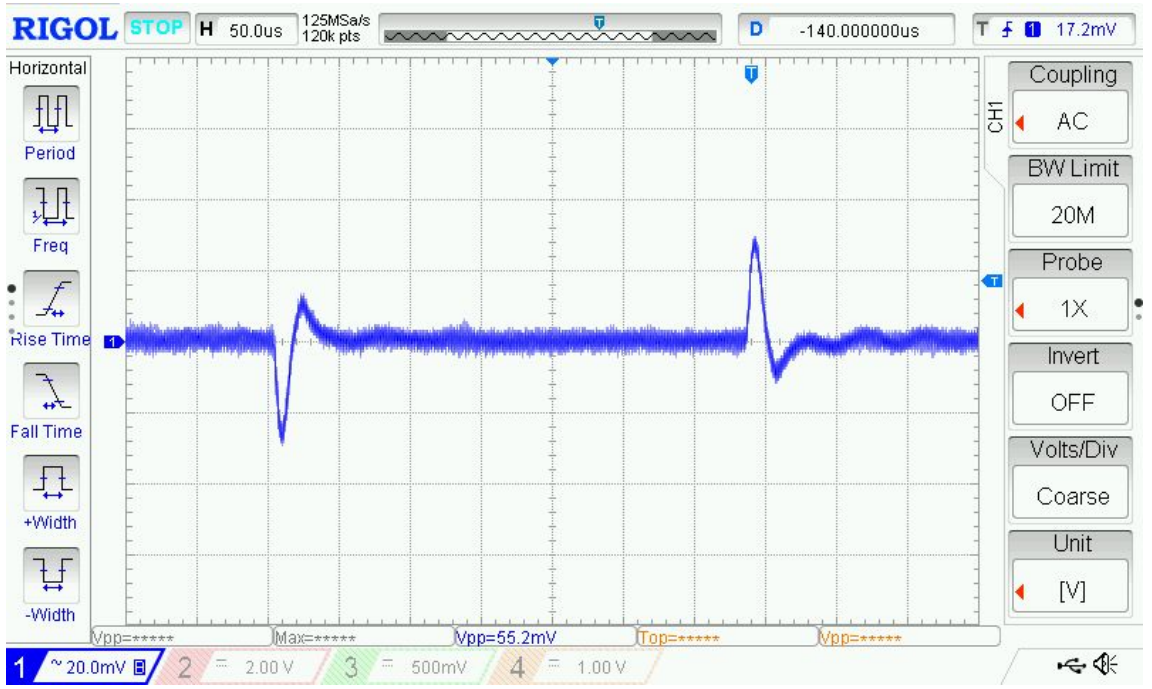
0.5 A Load

AnDAPT Confidential

AnDAPT

HPIO_VCCO: Efficiency & Transient

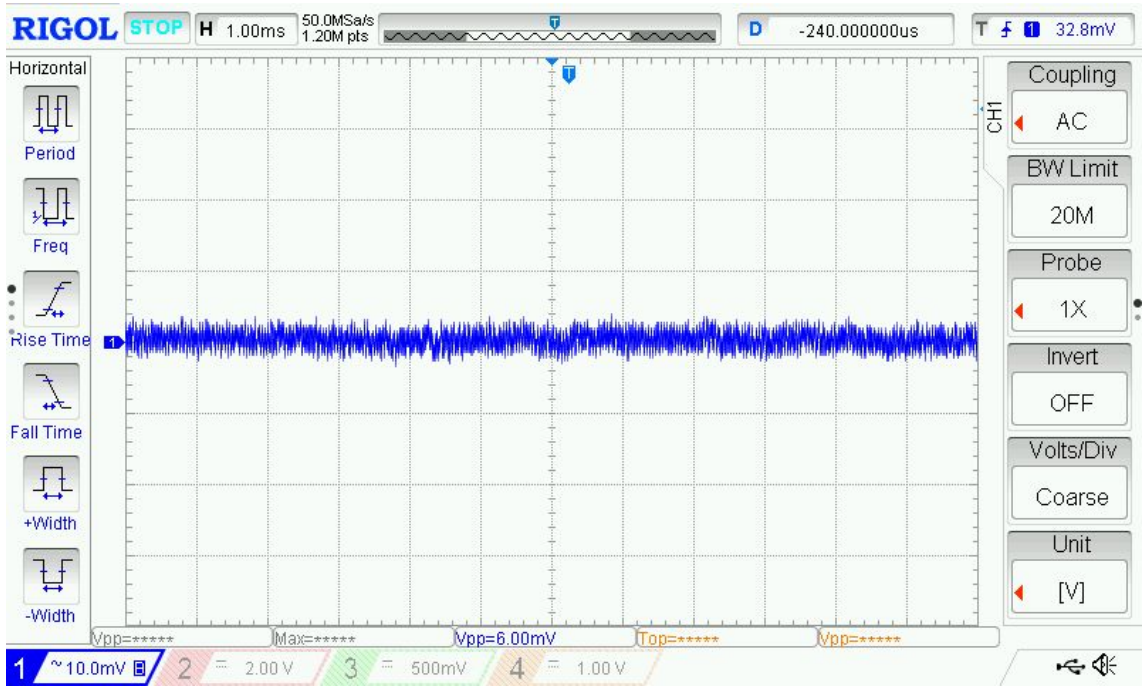




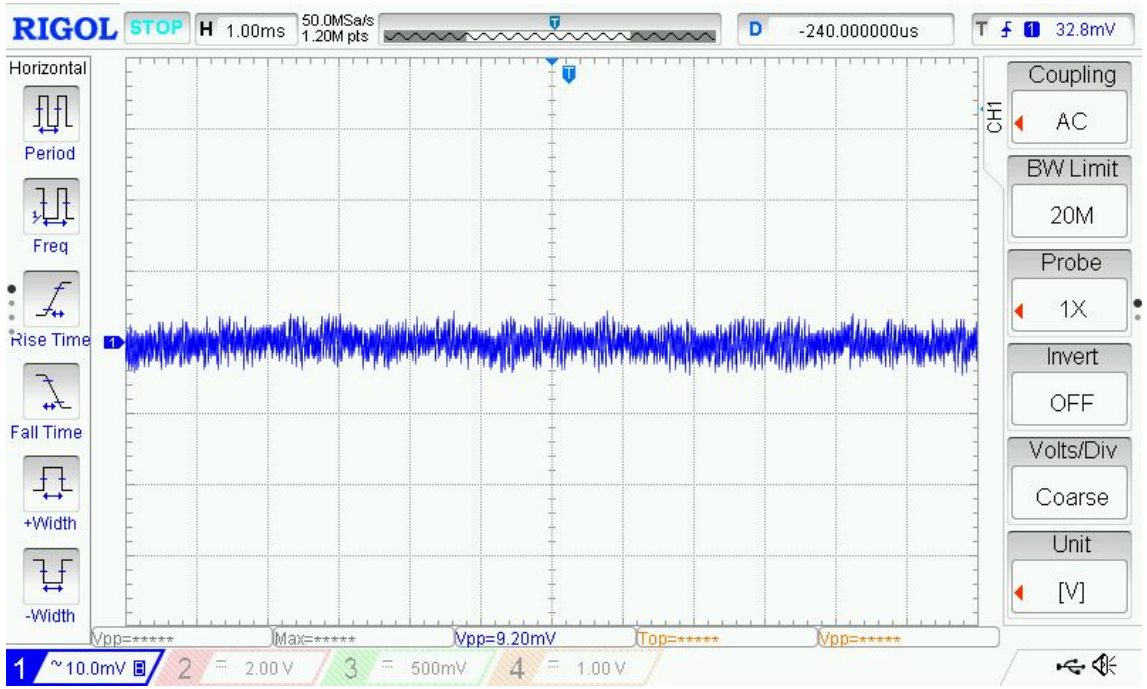
Vout = 1.8 V
Transient 0.3 A to 1 A
V_{PP} = 55.2 mV
Lout = 1.1 µH, Cout = 4 x 47 µF

AnDAPT Confidential

HPIO_VCCO : Ripple



No Load
V_{PP} = 6 mV



1 A Load
V_{PP} = 9.2 mV

AnDAPT Confidential