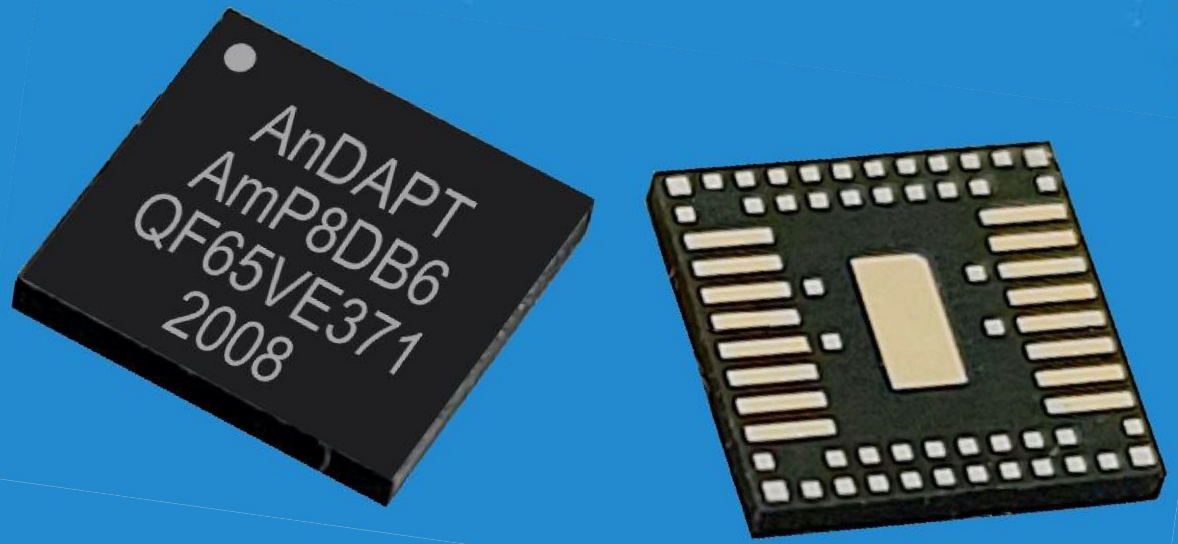

Zynq UltraScale+ (Full Power Management) Cost-optimized Portfolio

Mapping & Test Data

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Zynq UltraScale+ (ZU+) family of devices SKUs (full-power management) in cost-optimized portfolio
- Zynq US+ power maps
- AnDAPT integrated power supply design
- Bench data including efficiency, transients, ripple for each power rail
- AnDAPT PMICs meet or exceed all power performance specs provided by Xilinx for ZU+ family FPGAs

*Xilinx document:
https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Zynq UltraScale+ (ZU+) Device SKUs Covered- Full Power Management

Supported SKUs
XCZU1
XCZU2
XCZU3

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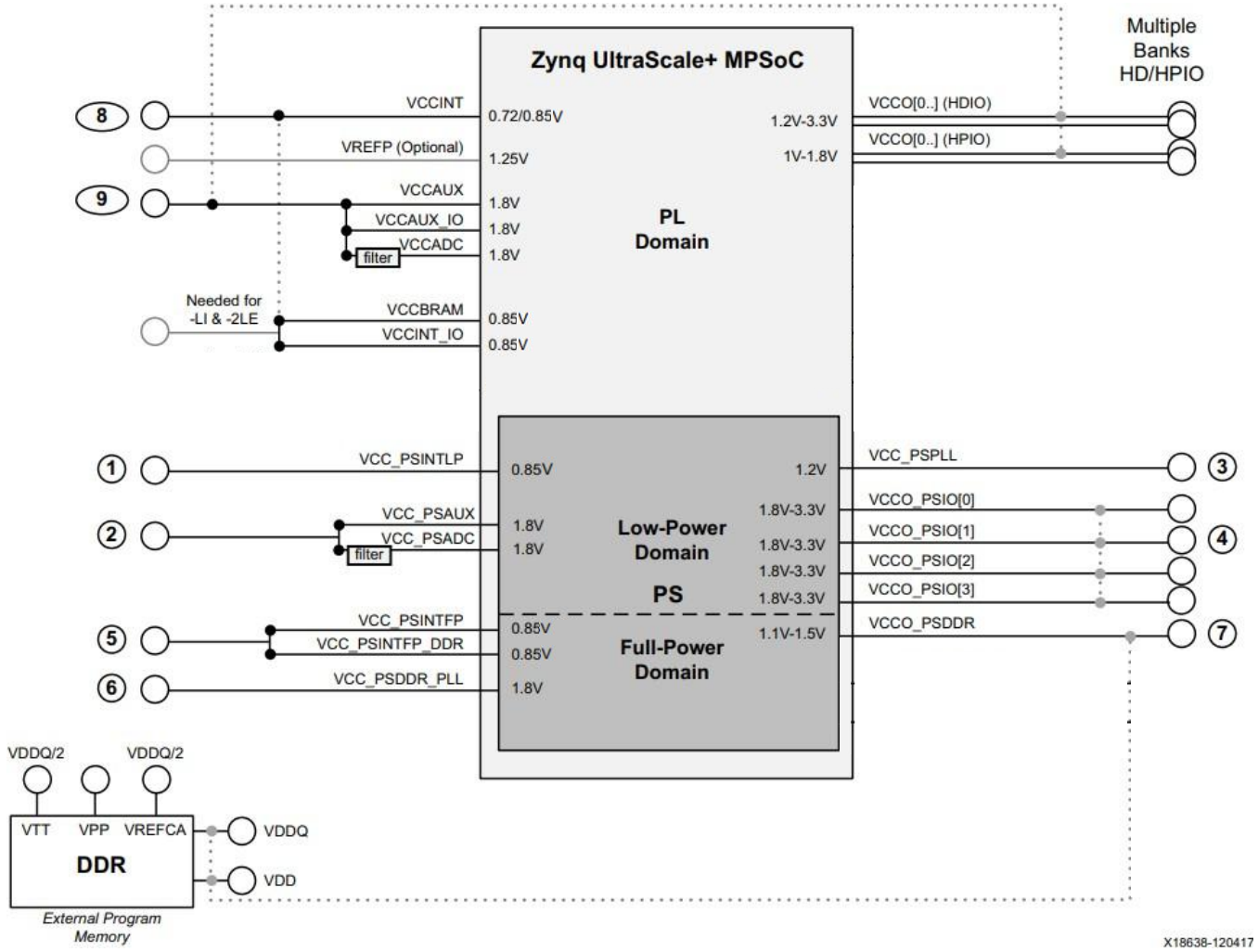
Zynq UltraScale+ (Full Power Management)



*VCCINT separated out for 0.72V Devices

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree: Zynq UltraScale+ (Full Power)

PVIN = 12V

#	Rail	Seq	Vout (V)	Iout (A)	Comment
1	VCC_PSINTLP	1	0.85	0.7	
2	VCC_PSAUX, VCC_PSADC	2	1.8	0.15	
3	VCC_PSPLL	3	1.2	0.035	
4	VCCO_PSIO	4	1.8-3.3	0.5	
5	VCC_PSINTFP, VCC_PSINTFP_DDR	5	0.85	1.4	
6	VCC_PSDDR_PLL	6	1.8	0.010	
7	VCC0_PSDDR, DDR_VDDQ/ VDD	7	1.1-1.5	3A	
8	VCCINT, VCCBRAM, VCCINT_IO	8	0.85/0.72	1-3.5	
9	VCCBRAM	8	0.85	1	IO for 0.85 V
10	VCCAUX, VCCAUX_IO, VCCADC	9	1.8	0.4	

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Power Tree Mapping: Zynq UltraScale+ (Full Power)

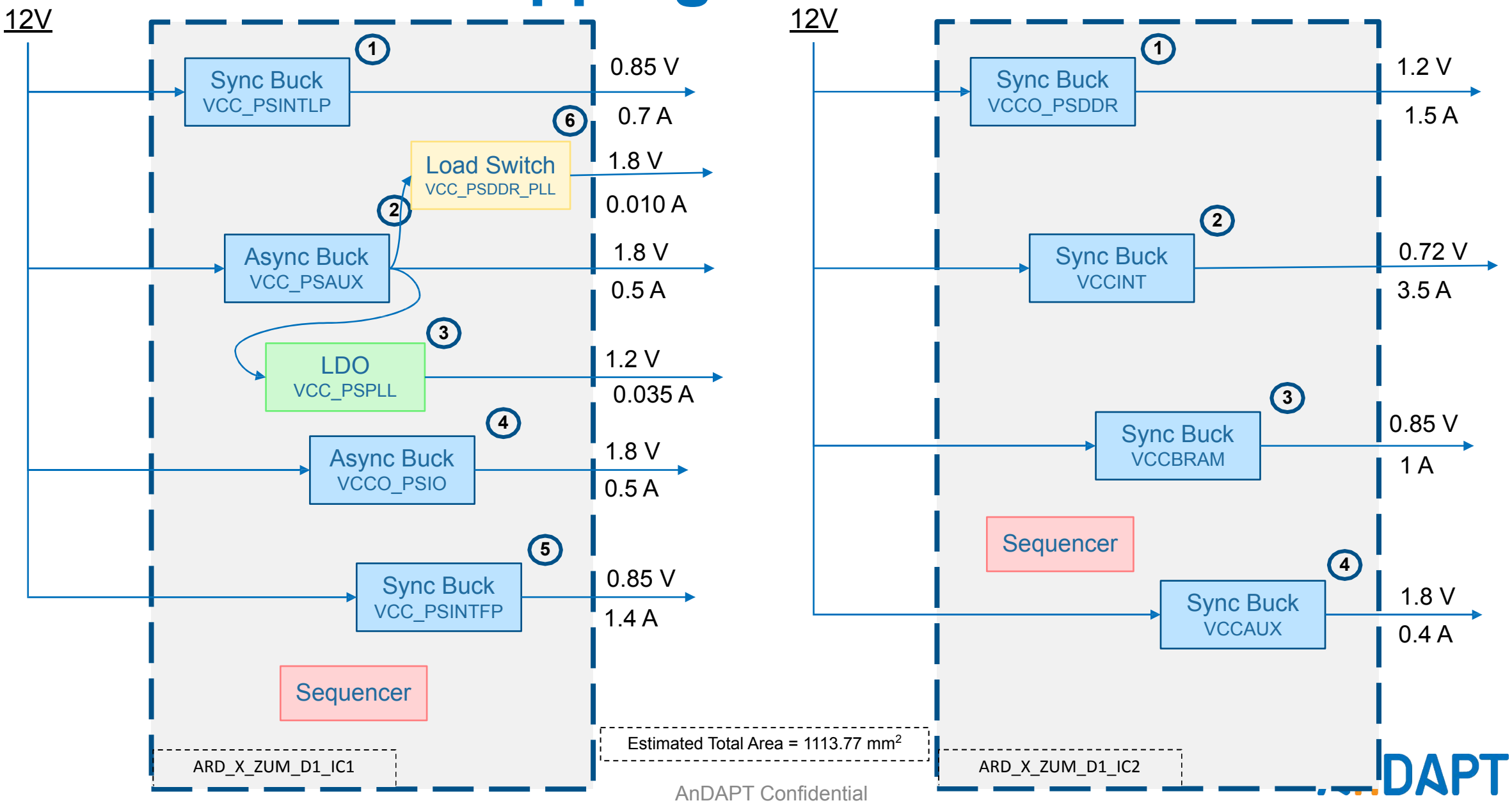
PVIN = 12V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCC_PSINTLP	1	C200	Sync Buck	PVIN	12	0.85	0.7	ARD_X_ZUM_D1_IC1
2	VCC_PSAUX (VCC_PSAUX, VCC_PSADC)	2	C150	Async Buck	PVIN	12	1.8	0.5 + 0.010 + 0.035	ARD_X_ZUM_D1_IC1
3	VCC_PSPLL	3	C710	LDO	VCC_PSAUX	1.8	1.2	0.035	ARD_X_ZUM_D1_IC1
4	VCCO_PSIO	4	C150	Async Buck	PVIN	12	1.8-3.3	0.5	ARD_X_ZUM_D1_IC1
5	VCC_PSINTFP (VCC_PSINTFP, VCC_PSINTFP_DDR)	5	C200	Sync Buck	PVIN	12	0.85	1.4	ARD_X_ZUM_D1_IC1
6	VCC_PSDDR_PLL	6	C750	Load Switch	VCC_PSAUX	1.8	1.8	0.010	ARD_X_ZUM_D1_IC1
7	VCC0_PSDDR (VCC0_PSDDR, DDR_VDDQ/ VDD)	7	C200	Sync Buck	PVIN	12	1.1-1.5	3	ARD_X_ZUM_D1_IC2
8	VCCINT (VCCINT, VCCBRAM, VCCINT_IO)	8	C200	Sync Buck	PVIN	12	0.85/0.72	1-3.5	ARD_X_ZUM_D1_IC2
9	VCCBRAM	8	C200	Sync Buck	PVIN	12	0.85	1	ARD_X_ZUM_D1_IC2
10	VCCAUX (VCCAUX, VCCAUX_IO, VCCADC	9	C200	Sync Buck	PVIN	12	1.8	0.4	ARD_X_ZUM_D1_IC2

Estimated total area estimated = 514 mm^2

AnDAPT

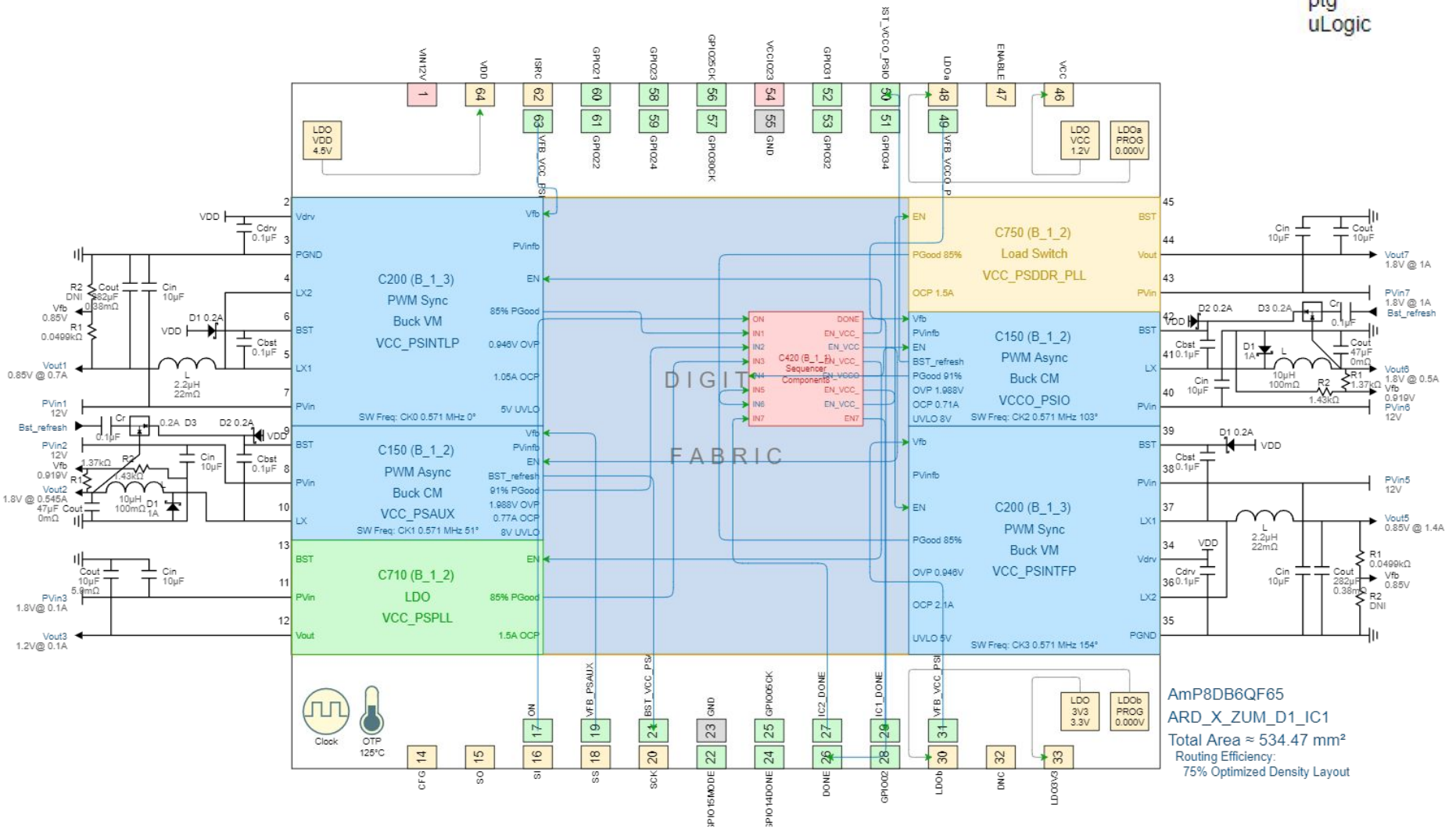
Power Tree Mapping



Mapping (WebAmP View) –IC1

Resource Usage...

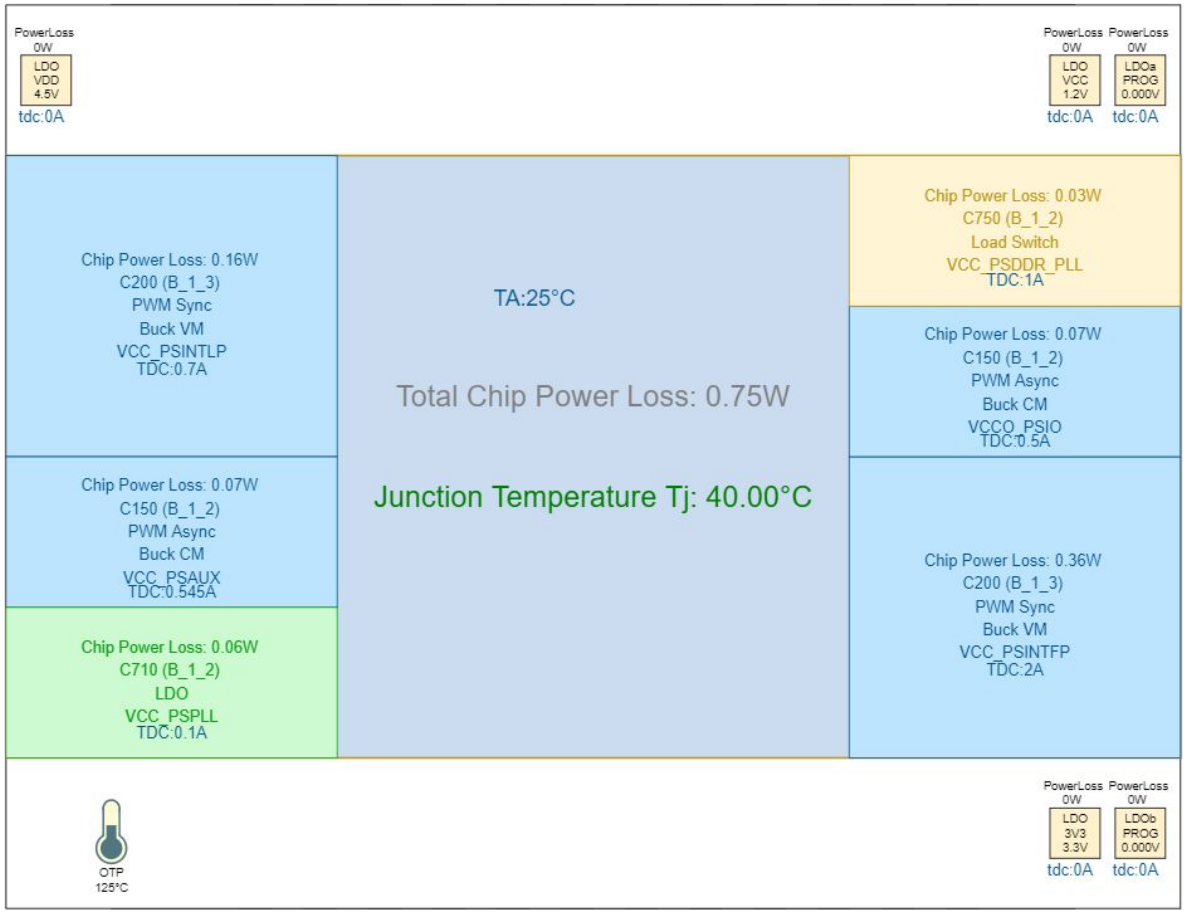
io	8 used (Capacity 24)
clb	58 used (Capacity 64)
cm	8 used (Capacity 8)
pmt	13 used (Capacity 16)
sim	8 used (Capacity 8)
atc	5 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	1 used (Capacity 2)
uLogic	459 used (Capacity 512)



Mapping (Thermal View) –IC1

Resource Usage...

io	8 used (Capacity 24)
clb	58 used (Capacity 64)
cm	8 used (Capacity 8)
pmt	13 used (Capacity 16)
sim	8 used (Capacity 8)
atc	5 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	1 used (Capacity 2)
uLogic	459 used (Capacity 512)



AmP8DB6QF65
ARD_X_ZUM_D1_IC1
Total Area ≈ 534.47 mm²
Routing Efficiency:
75% Optimized Density Layout

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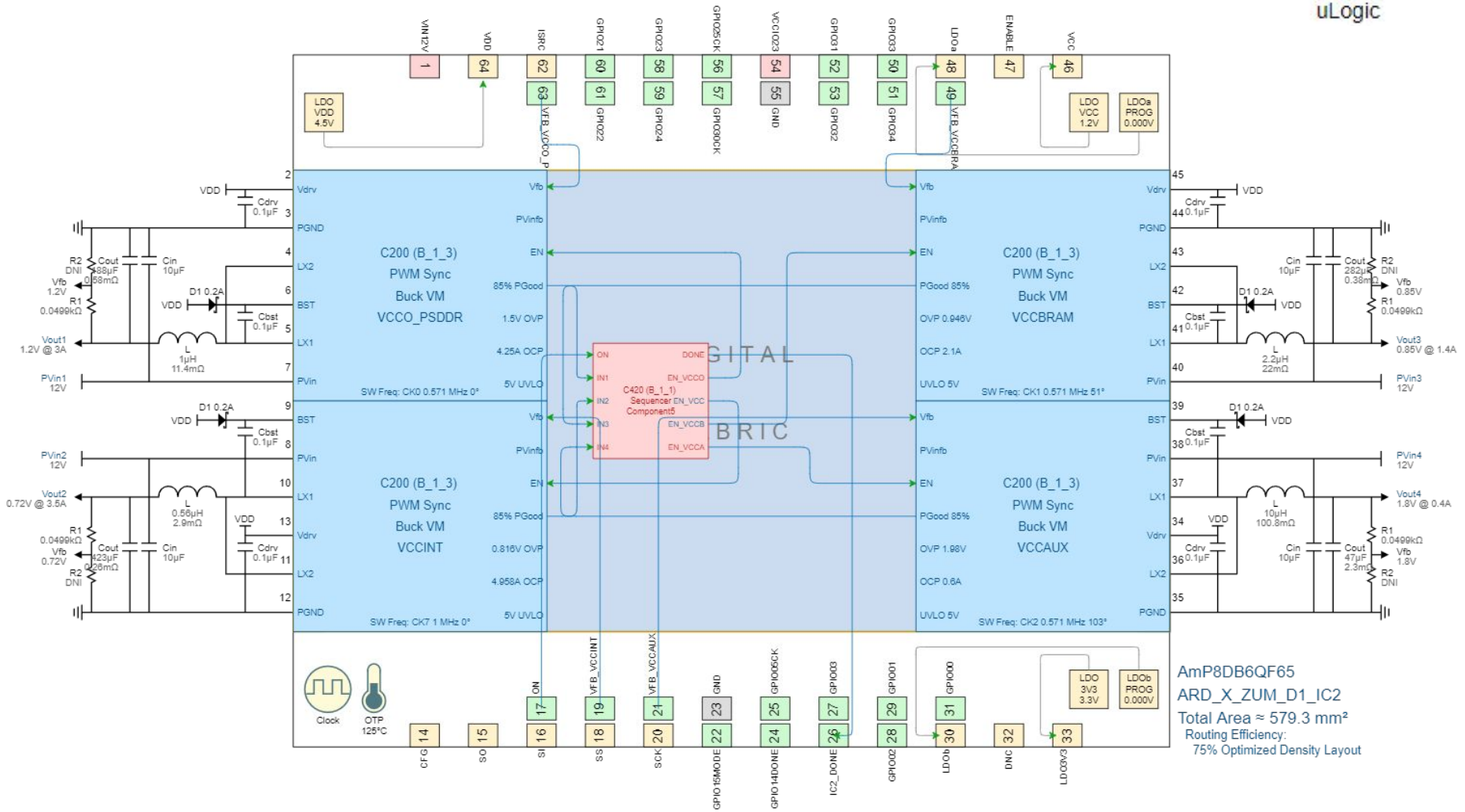
Mapping (WebAmP View) –IC2

Resource Usage...

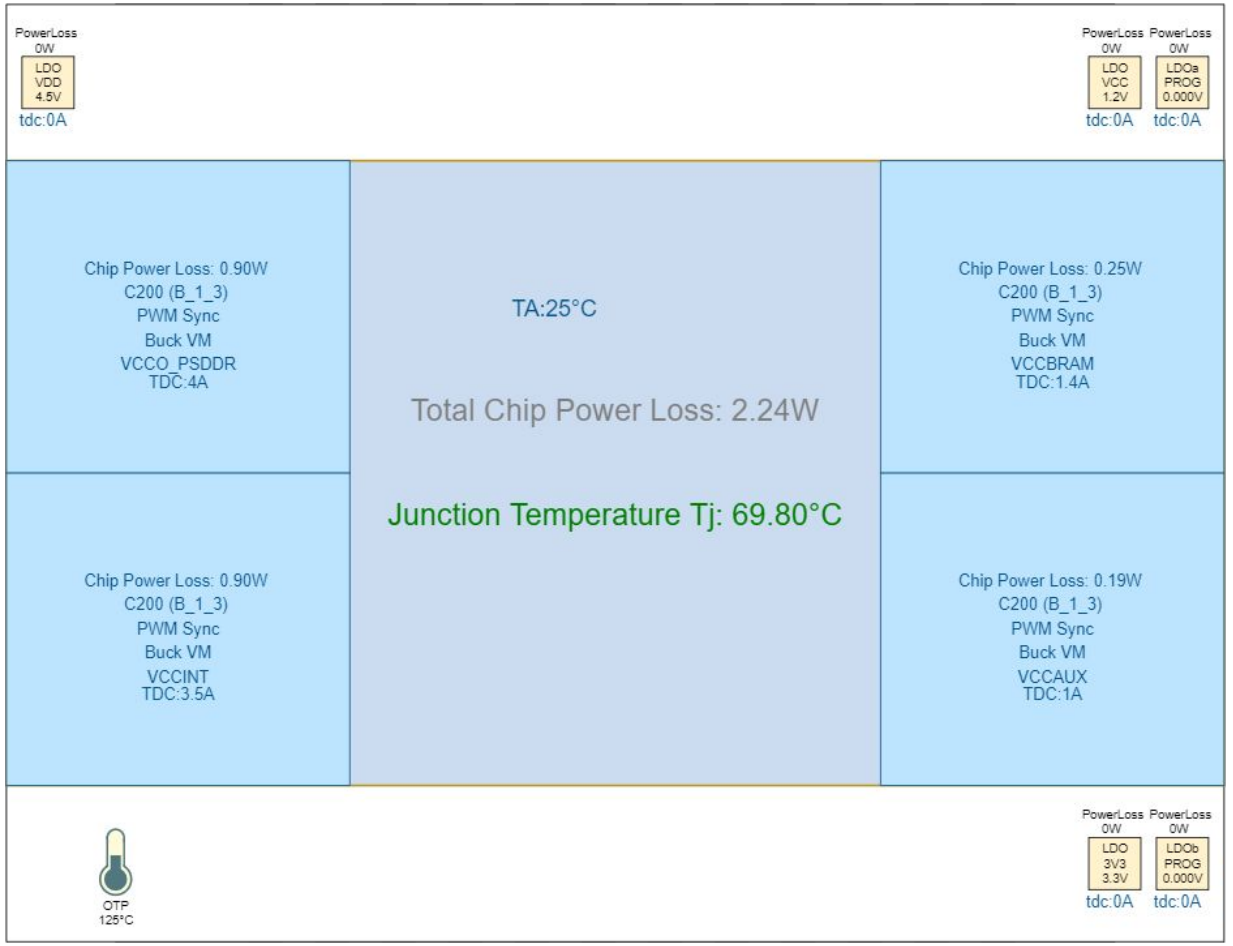
io	6 used (Capacity 24)
clb	54 used (Capacity 64)
cm	8 used (Capacity 8)
pmt	13 used (Capacity 16)
sim	8 used (Capacity 8)
atc	5 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	2 used (Capacity 2)
uLogic	429 used (Capacity 512)



Mapping (Thermal View) –IC2

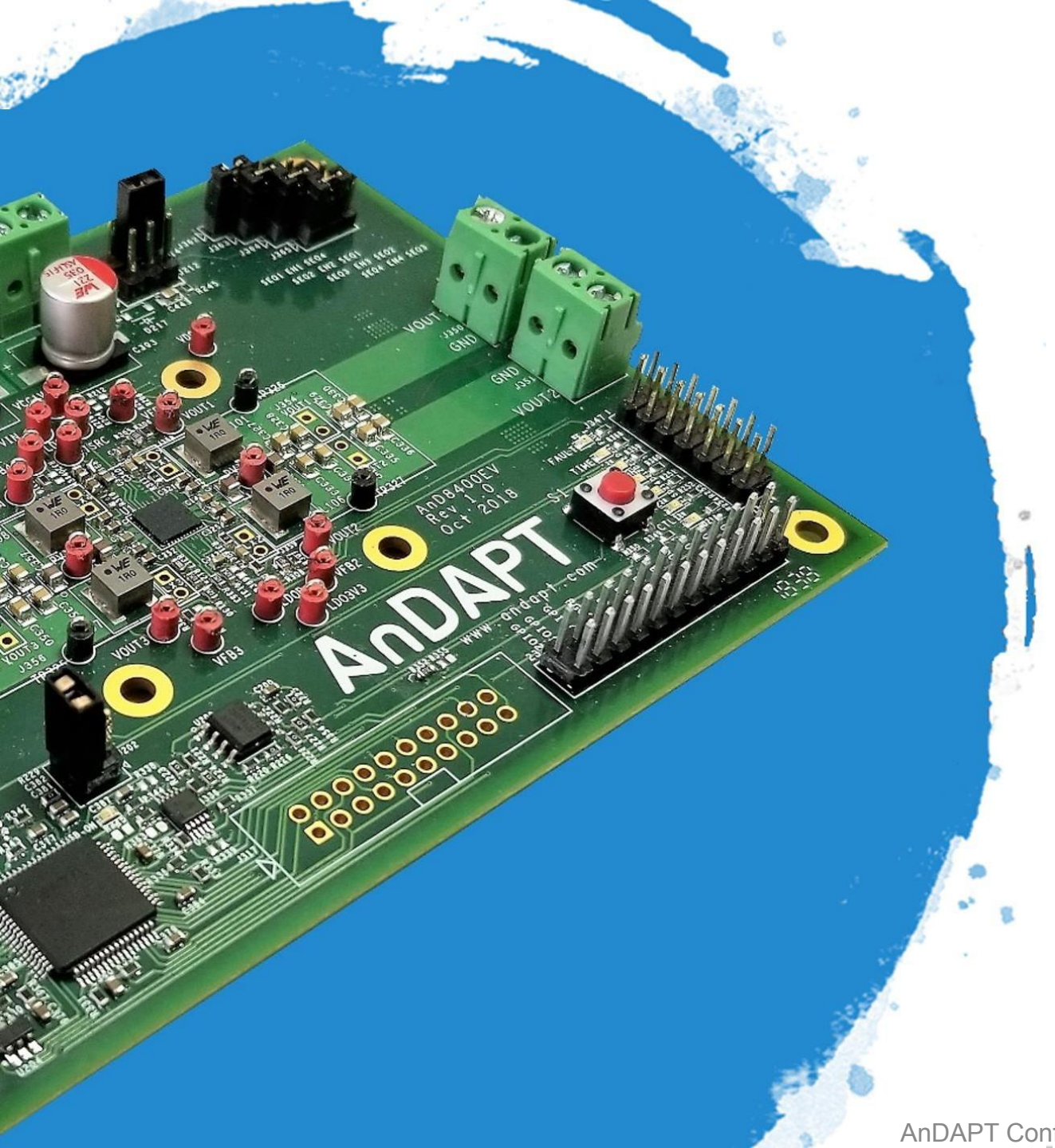
Resource Usage...

io	6 used (Capacity 24)
clb	54 used (Capacity 64)
cm	8 used (Capacity 8)
pmt	13 used (Capacity 16)
sim	8 used (Capacity 8)
atc	5 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	2 used (Capacity 2)
uLogic	429 used (Capacity 512)



AmP8DB6QF65
ARD_X_ZUM_D1_IC2
Total Area ≈ 579.3 mm²
Routing Efficiency:
75% Optimized Density Layout

AnDAPT

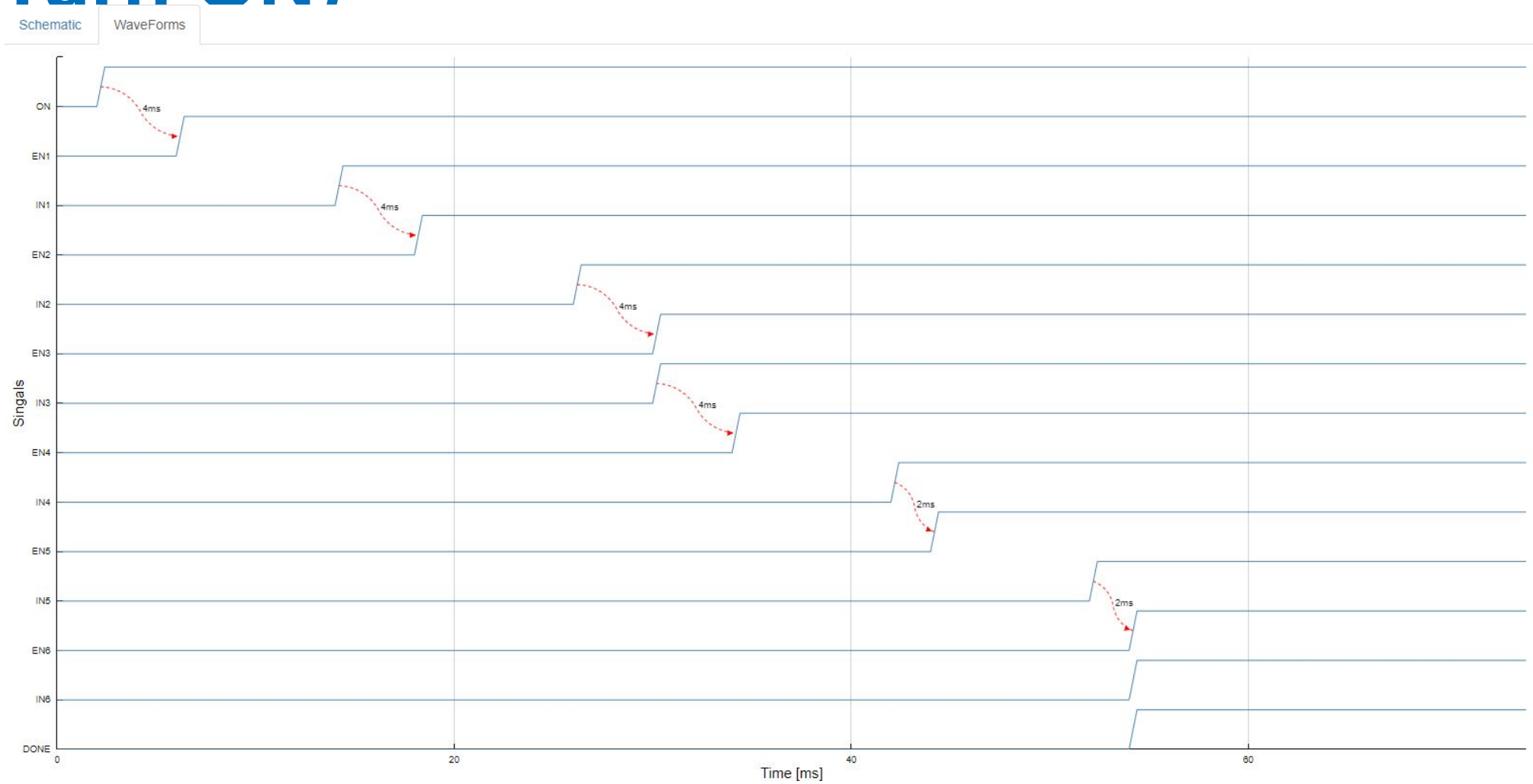


Test Data

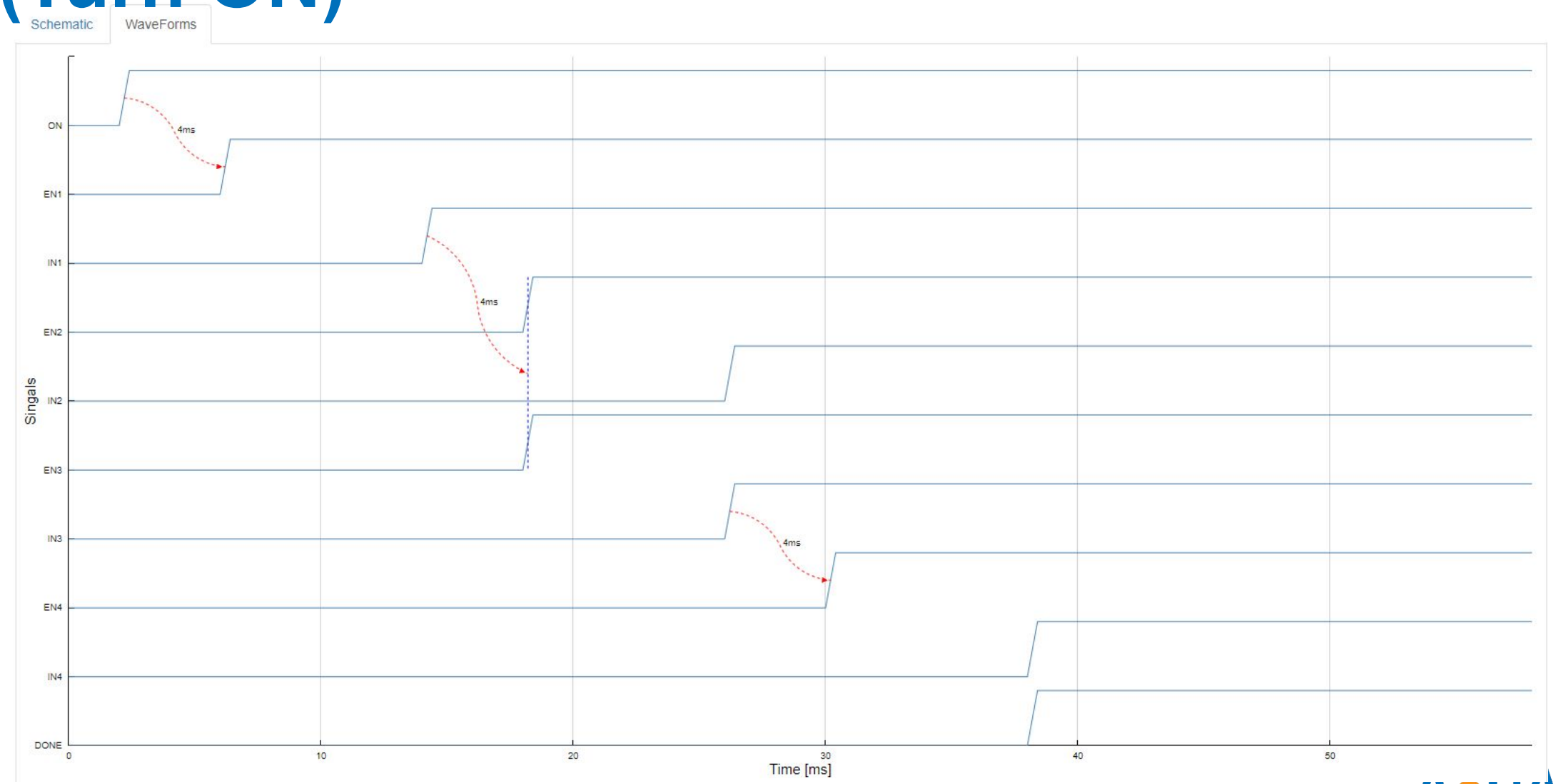
Zynq UltraScale+ (Full Power)

AnDAPT

Integrated Sequencer Graphic IC1 (Turn ON)



Integrated Sequencer Graphic IC2 (Turn ON)

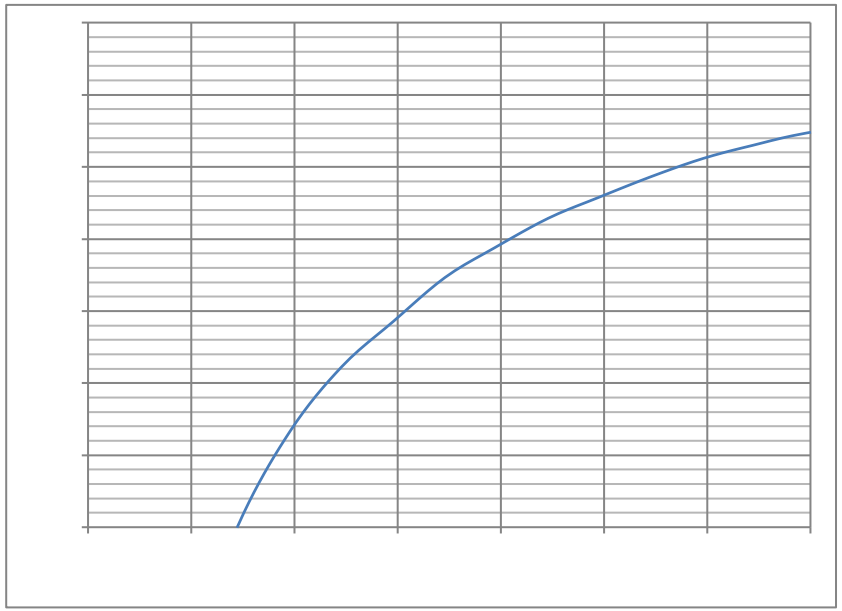


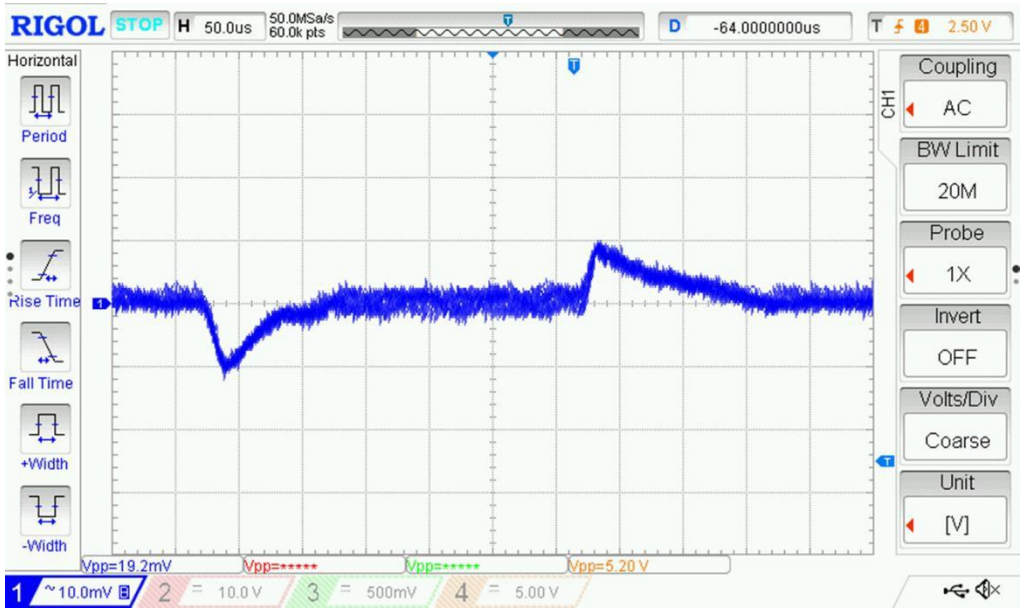
VCC_PSINTLP
0.85 V / 0.7 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 74438357022
- C = 6x47 uF

AnDAPT

Efficiency & Transient

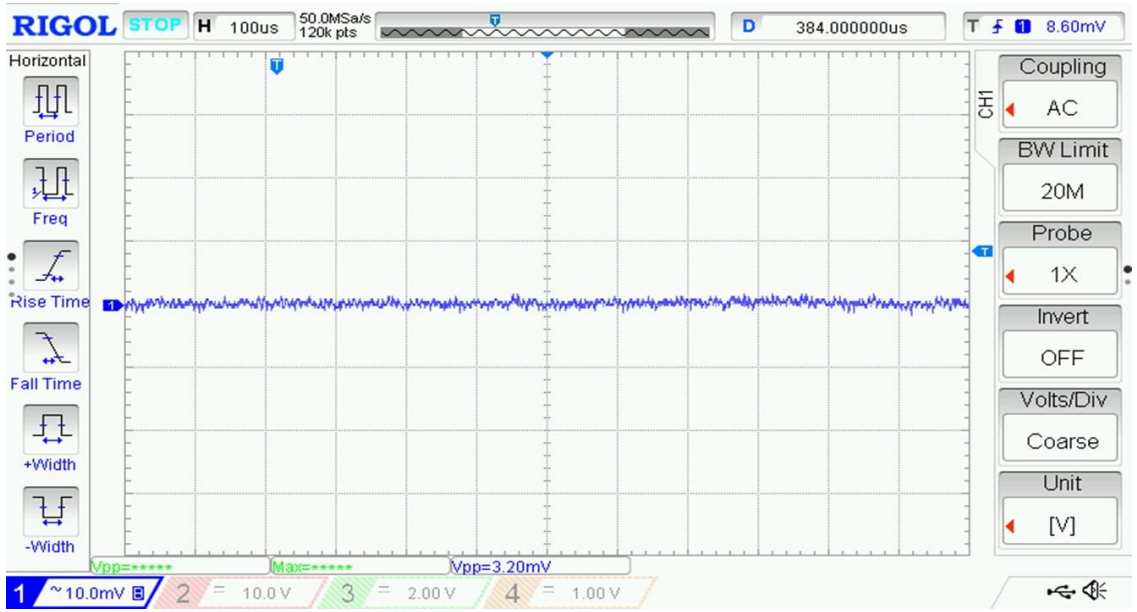




Vout = 0.85 V
Transient 0.21A – 0.7A @ 2.5
A/µs V_{PP} = 19.2 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 6 x 47 µF

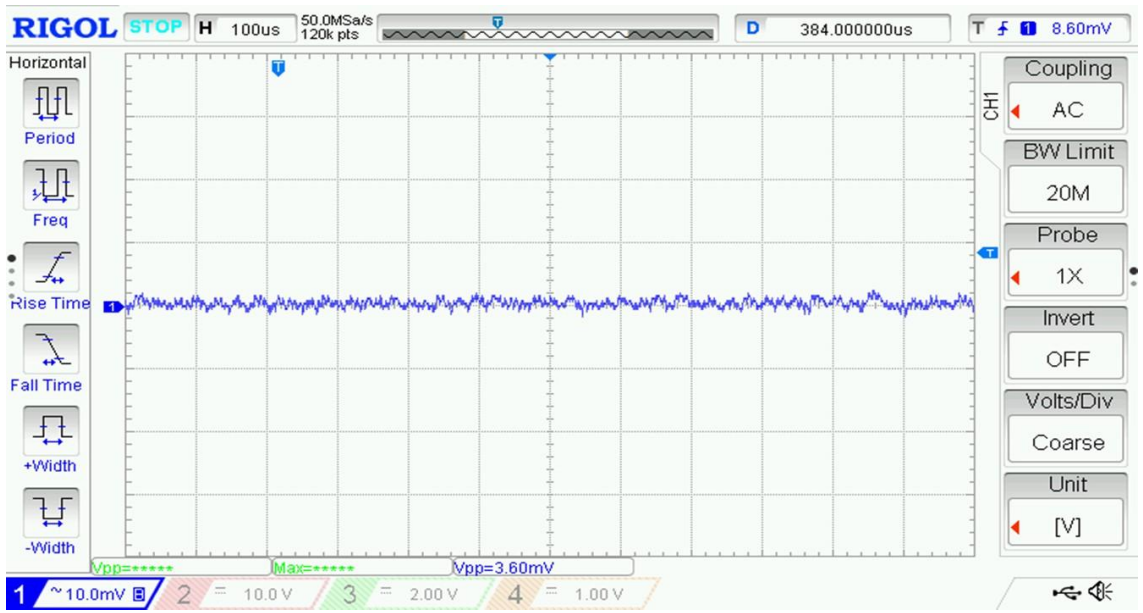
AnDAPT

Ripple



No Load
V_{PP} = 3.2 mV

Vout = 0.85 V



0.7A Load
V_{PP} = 3.6 mV

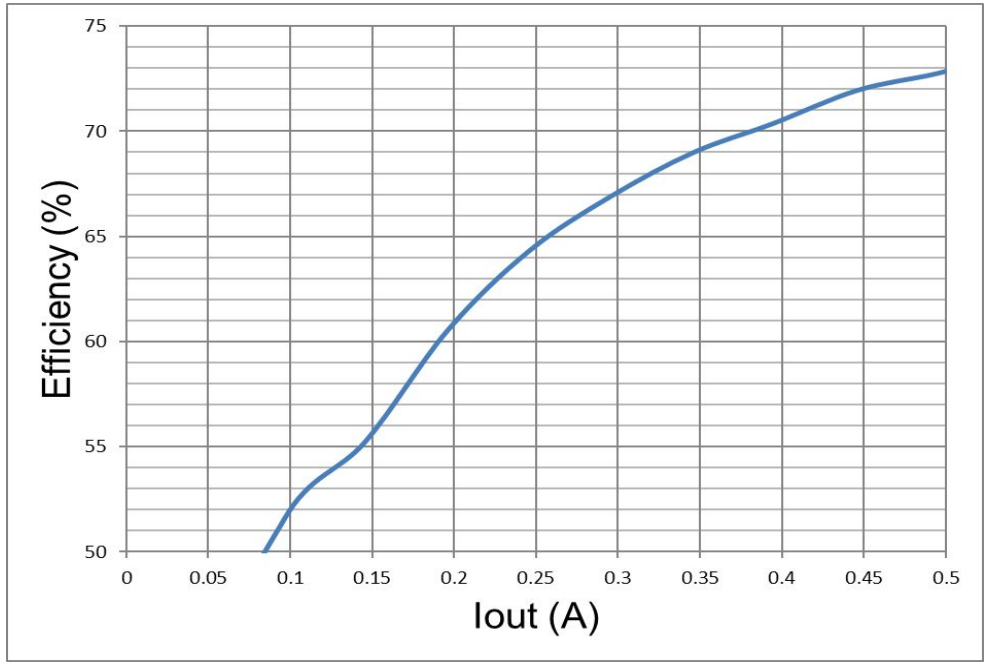
AnDAPT

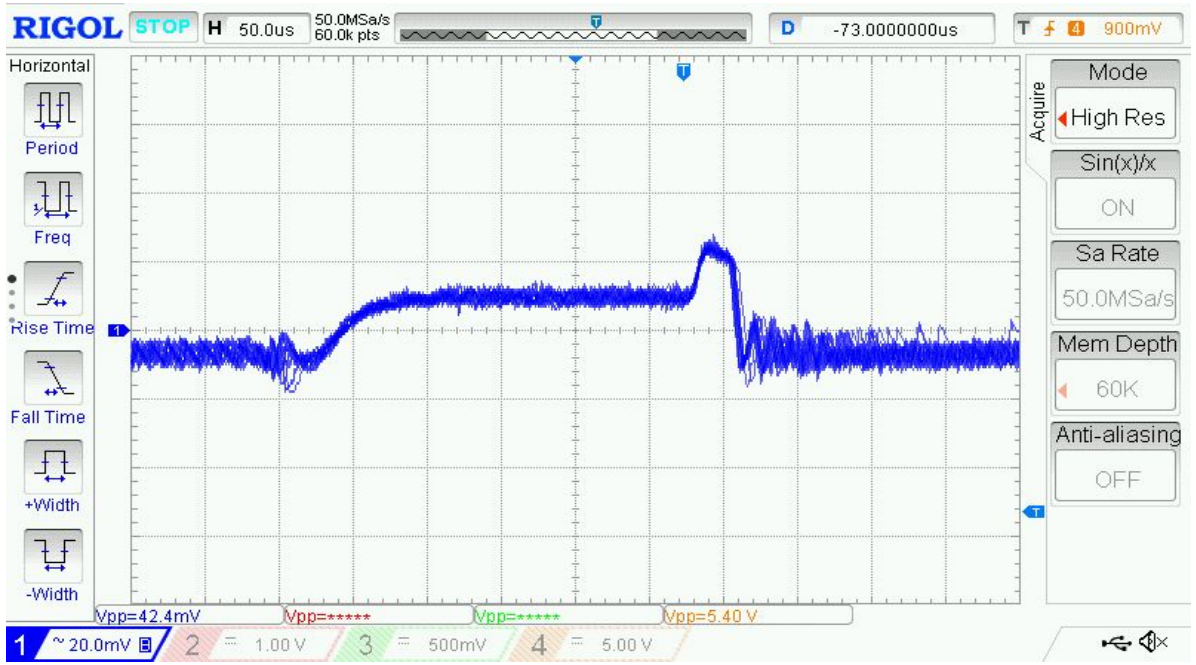
VCC_PSAUX (VCC_PSAUX, VCC_PSADC) 1.8 V / 0.5 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74437334100
- C = 1x47 uF

AnDAPT

Efficiency & Transient

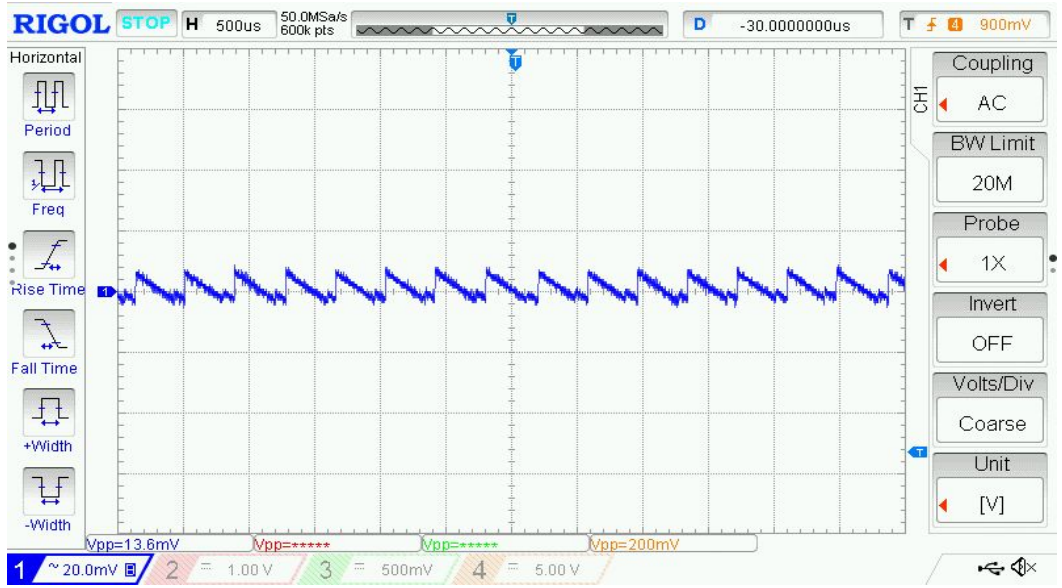


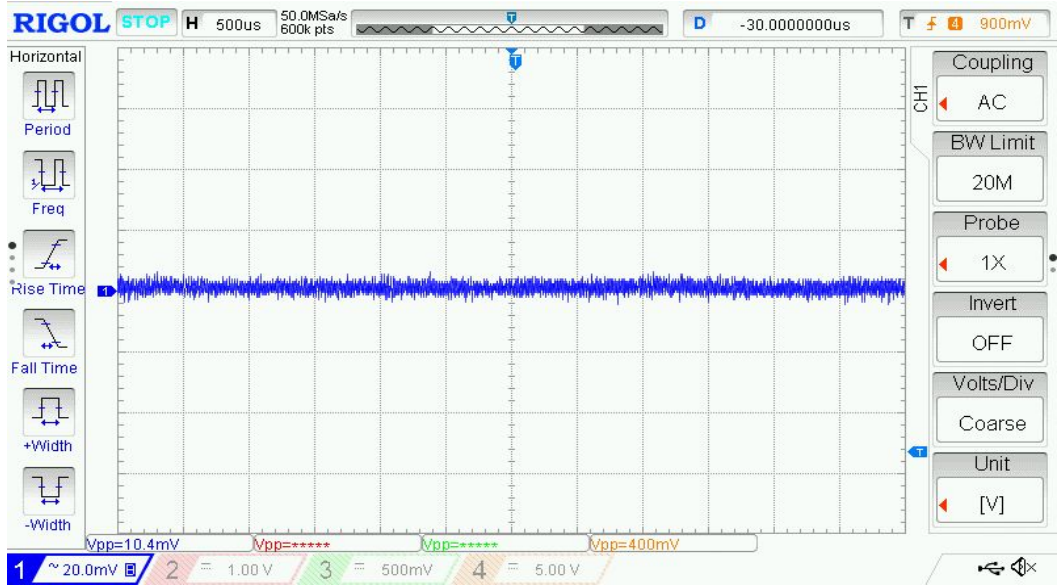


Vout = 1.8 V
Transient 0.0 A – 0.5 A @ 2.5 A/µs
V_{PP} = 42.4 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1 x 47 µF

AnDAPT

Ripple





No Load
V_{PP} = 13.6 mV

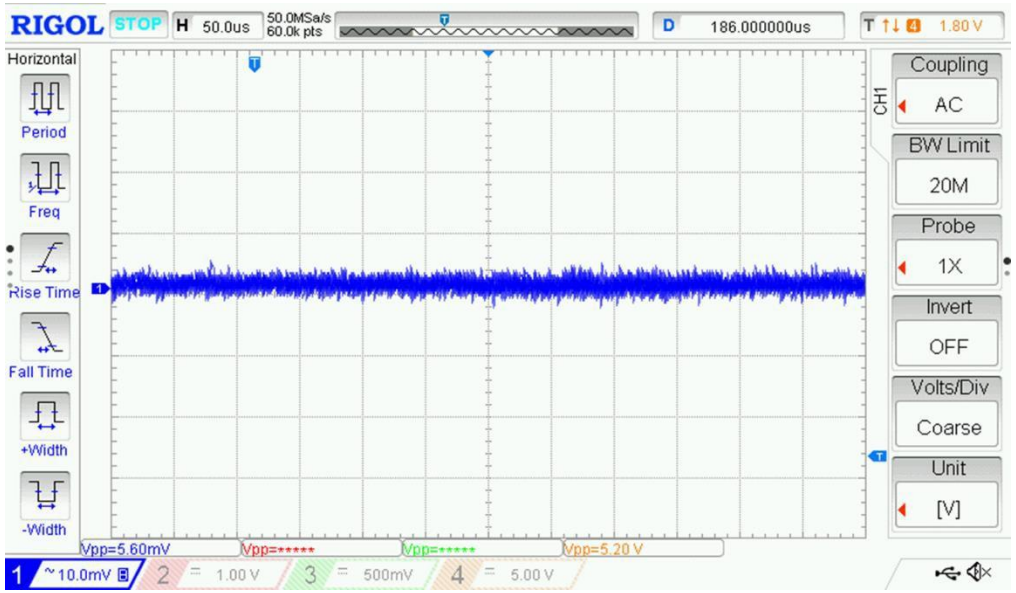
Vout = 1.8 V

0.5 A Load
V_{PP} = 10.4 mV

VCC_PSPLL
1.2 V / 0.035 A

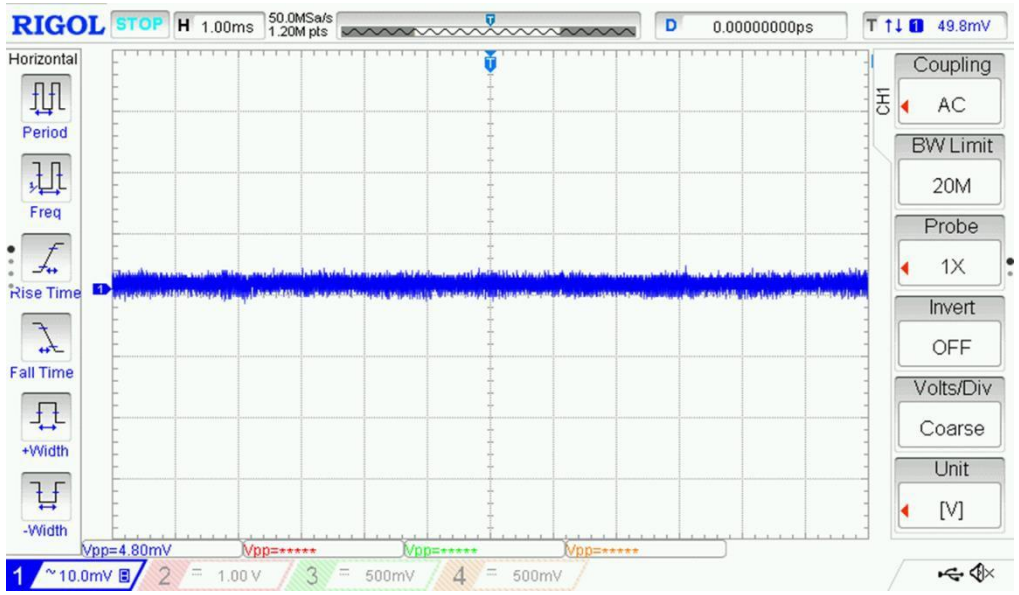
- C710 LDO

Transient



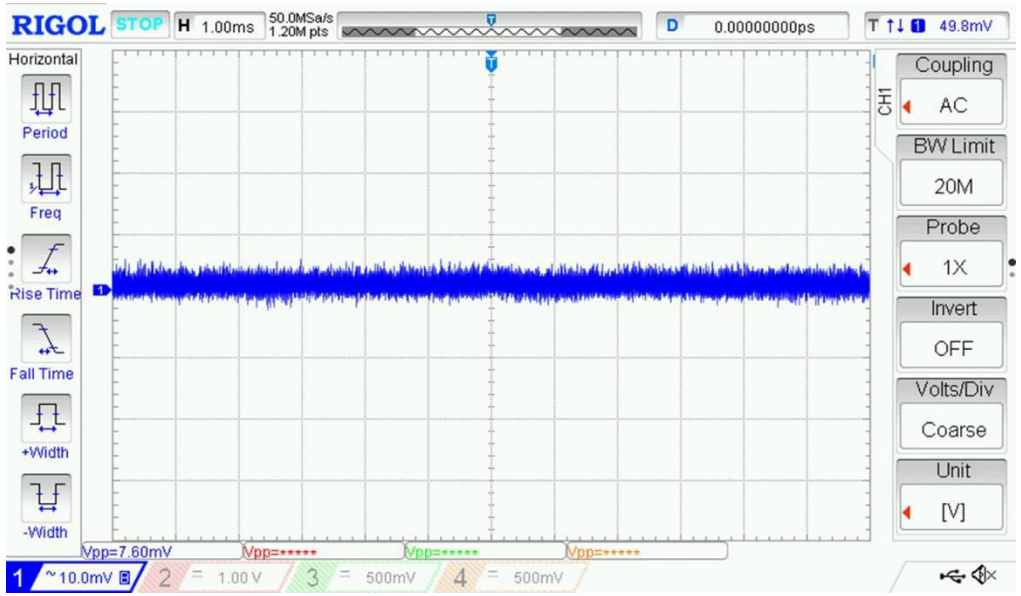
Vout = 1.2 V
Transient 0 A – 0.035 A @ 2.5 A/µs V_{PP} = 5.6 mV

Ripple



No Load
V_{PP} = 4.8 mV

Vout = 1.2 V



0.035 A Load
V_{PP} = 7.6 mV

AnDAPT

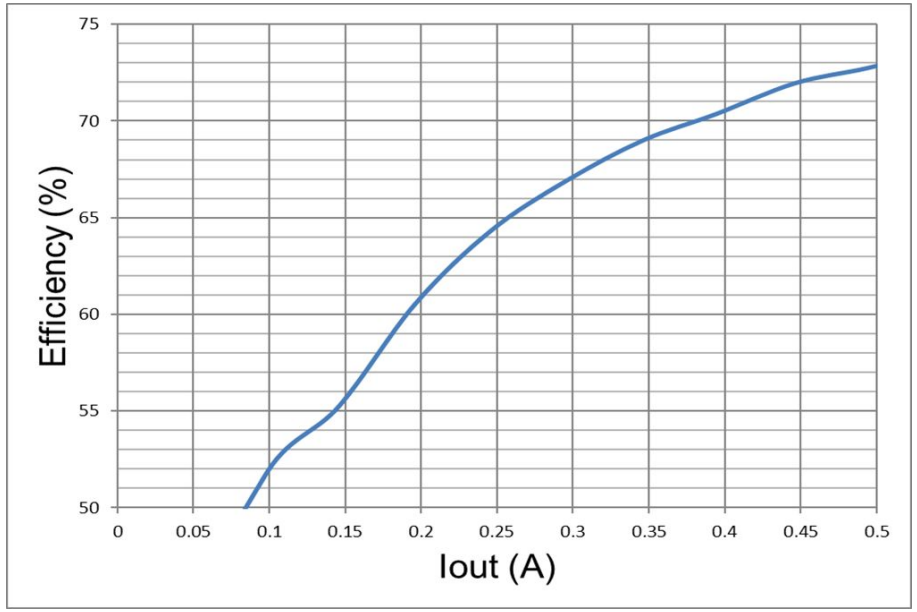
VCCO_PSIO

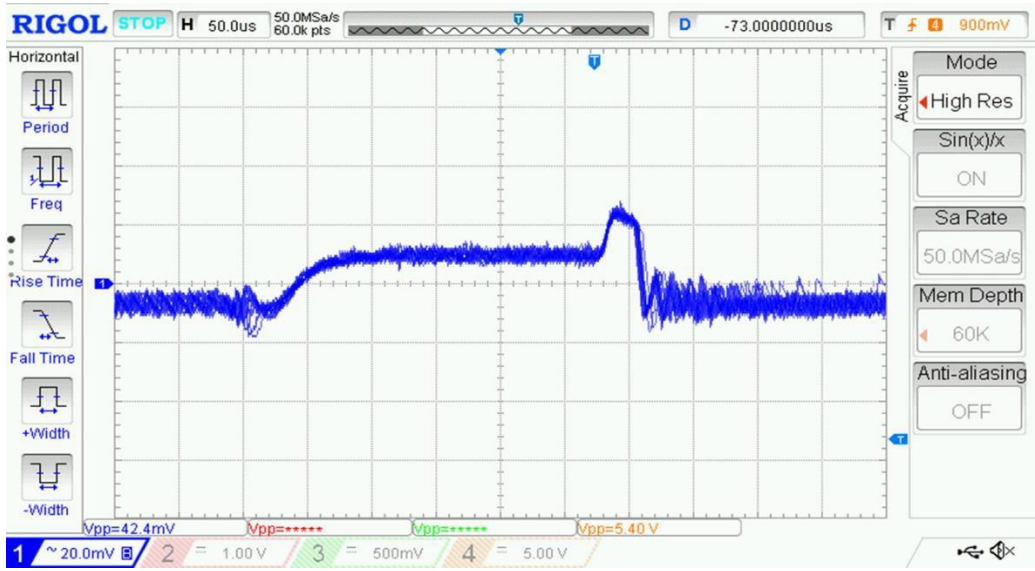
1.8 V / 0.5 A

- C150 Async Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74437334100
- C = 1x47 uF

AnDAPT

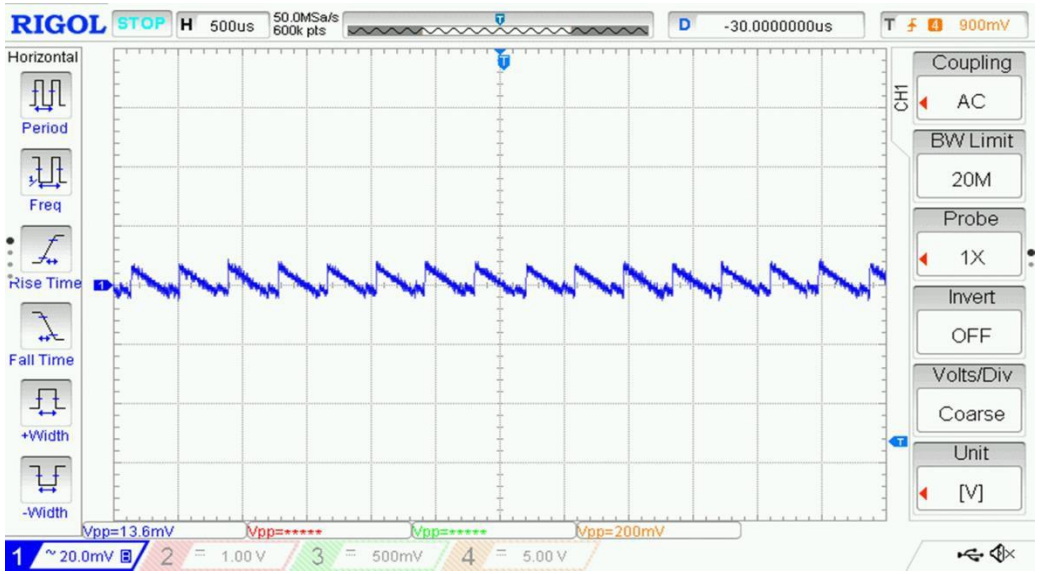
Efficiency & Transient





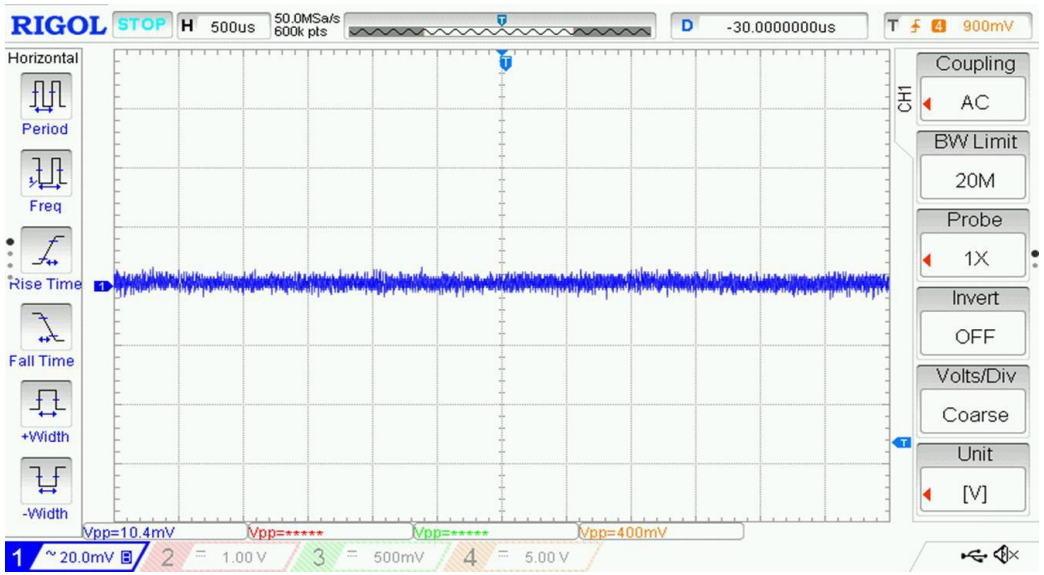
Vout = 1.8 V
Transient 0 A – 0.5 A @ 2.5
A/µs V_{PP} = 42.4 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1 x 47 µF

Ripple



No Load
V_{PP} = 13.6 mV

Vout = 1.8 V



0.5 A Load
V_{PP} = 10.4 mV

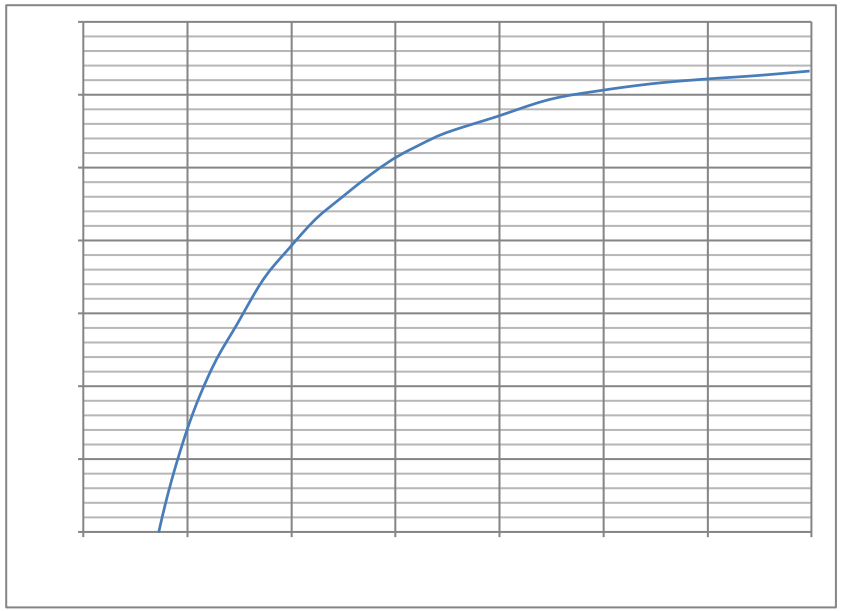
AnDAPT

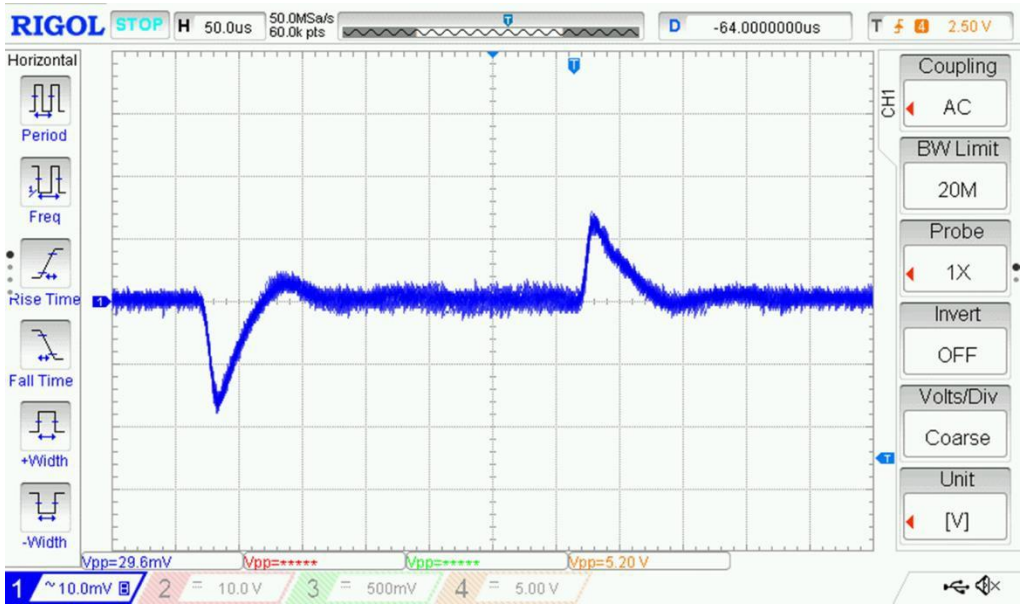
VCC_PSINTFP (VCC_PSINTFP, 0.85 V / 14 A, VCC_PSINTFP_DDR)

- C200 Sync Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 74438357022
- C = 6x47 uF

AnDAPT

Efficiency & Transient

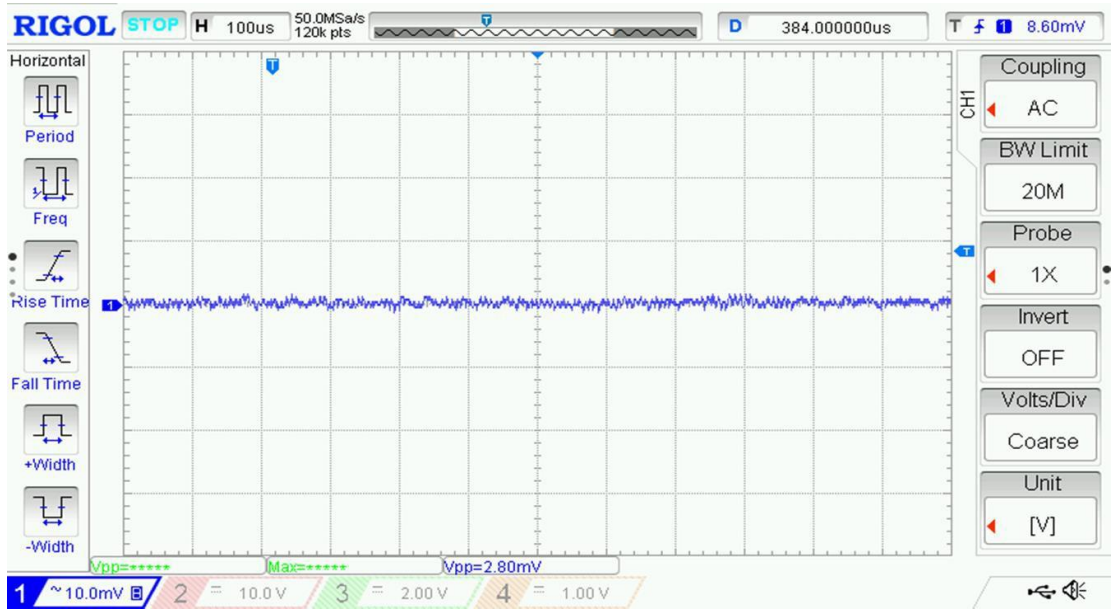




Vout = 0.85 V
Transient 0.42A – 1.4A @ 2.5
A/µs V_{PP} = 29.6 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 6 x 47 µF

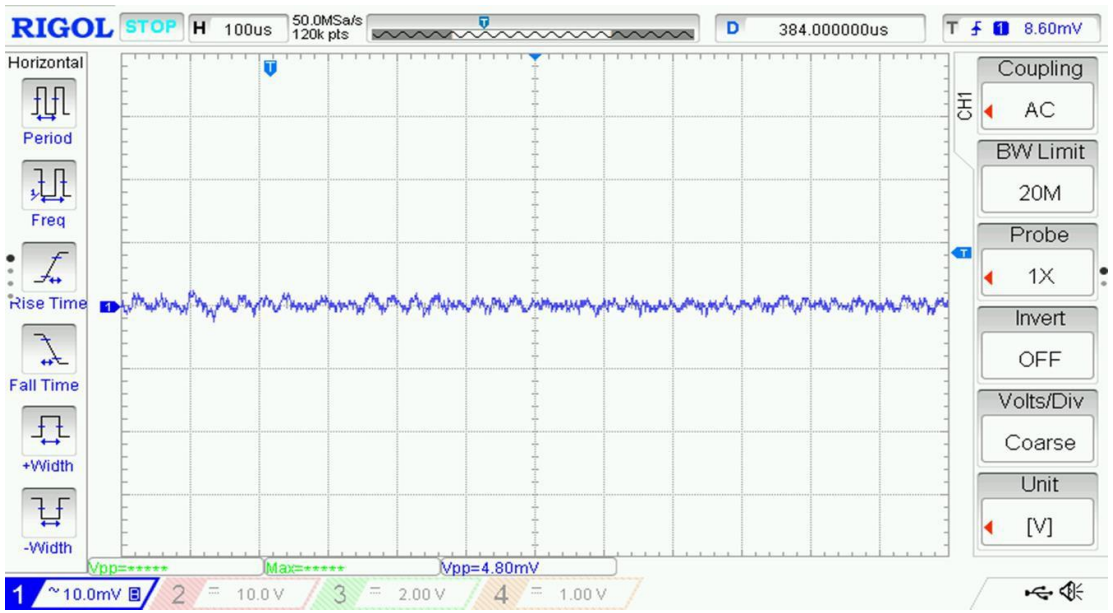
AnDAPT

Ripple



No Load
V_{PP} = 2.8 mV

Vout = 0.85 V



1.4A Load
V_{PP} = 4.8 mV

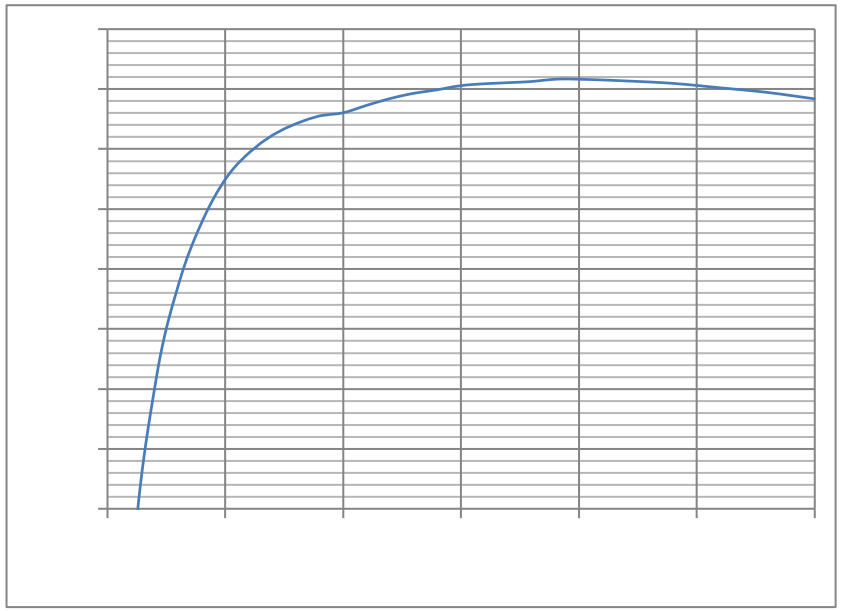
AnDAPT

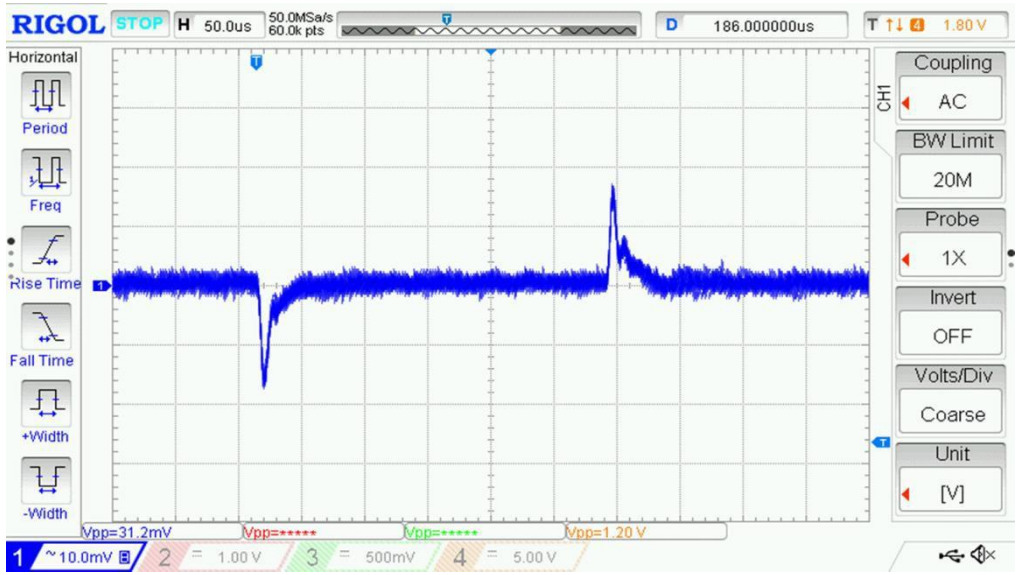
VCC0_PSDDR (VCC0_PSDDR, DDR_VDDQ/ VDD) 1.2 V / 3 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 1 µH, P/N Wurth 74438366010
- C = 4x47 uF

AnDAPT

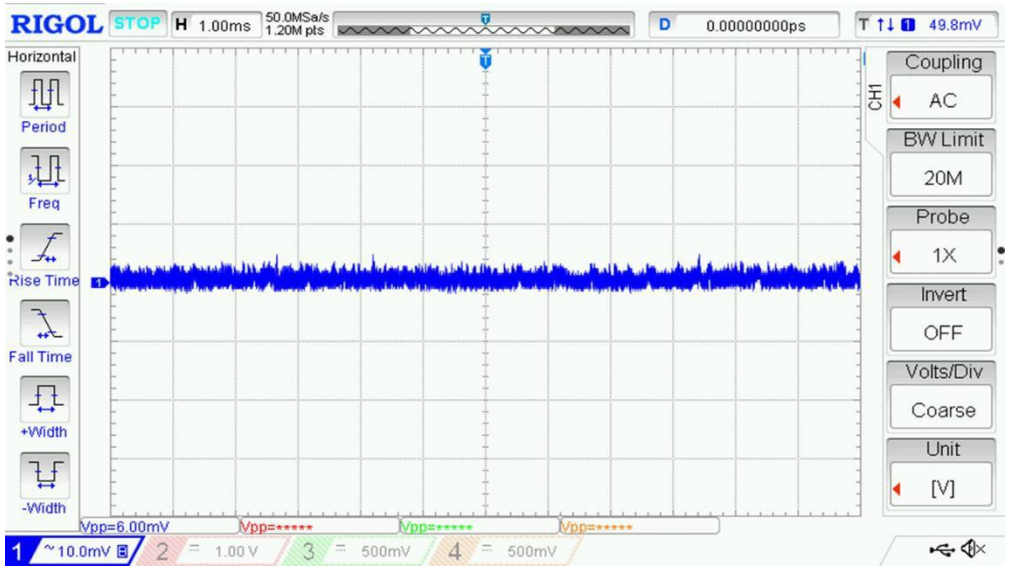
Efficiency & Transient





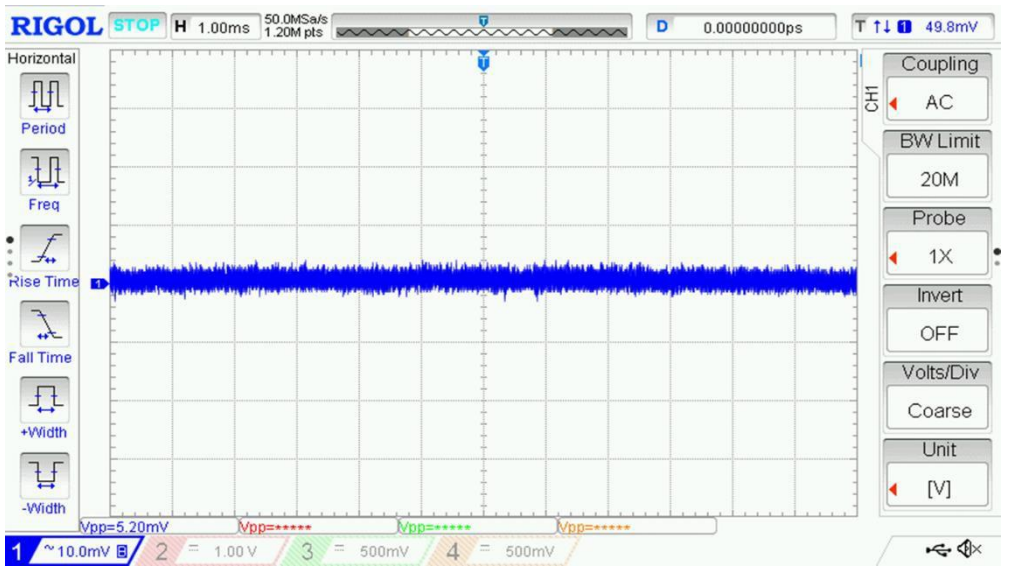
Vout = 1.2 V
Transient 2.25A – 3A @ 2.5
A/µs V_{PP} = 31.2 mV
Fsw = 571 kHz
Lout = 1 µH, Cout = 4 x 47 µF

Ripple



No Load
V_{PP} = 6.0 mV

Vout = 1.2 V



3 A Load
V_{PP} = 5.2 mV

AnDAPT

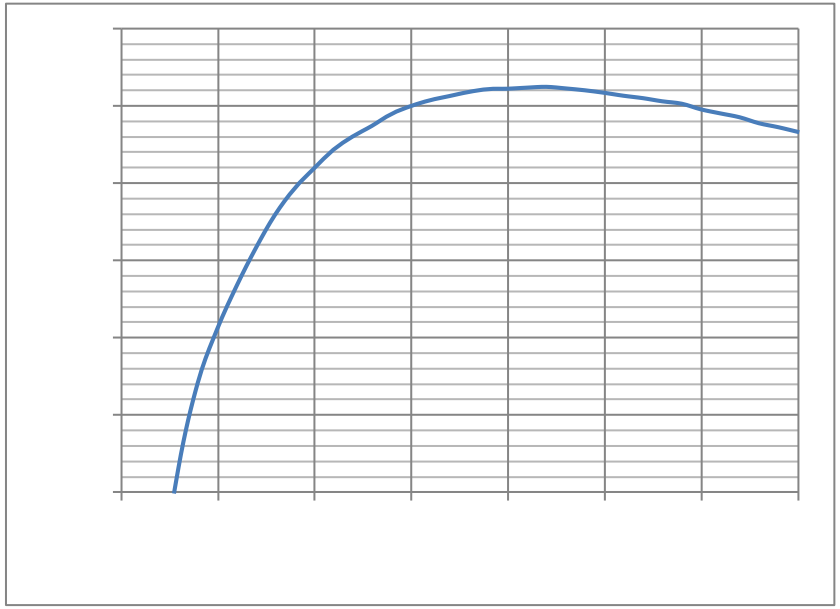
VCCINT

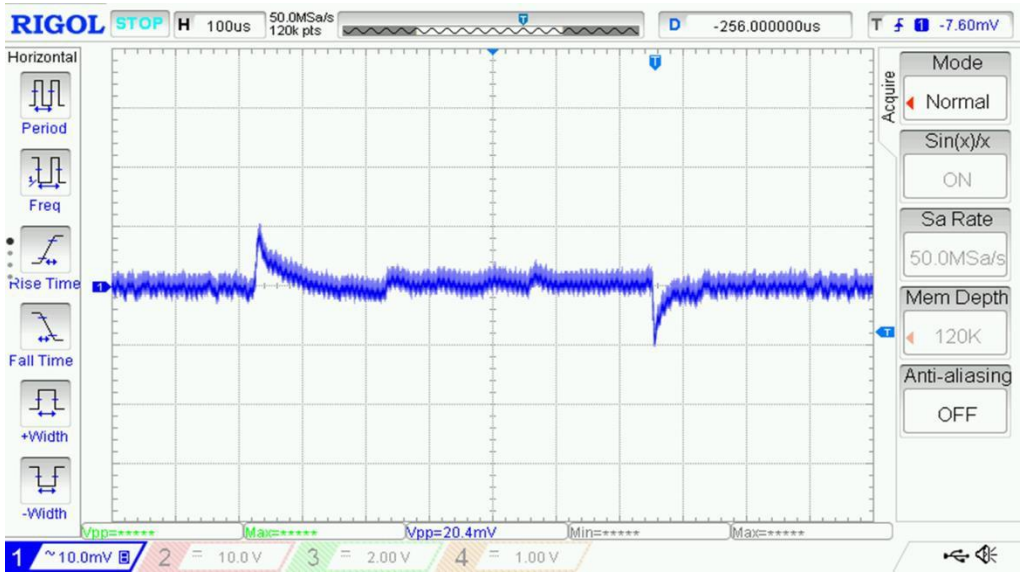
(VCCINT, VCCBRAM, VCCINT_IO)
0.72 V / 3.5 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

AnDAPT

Efficiency & Transient

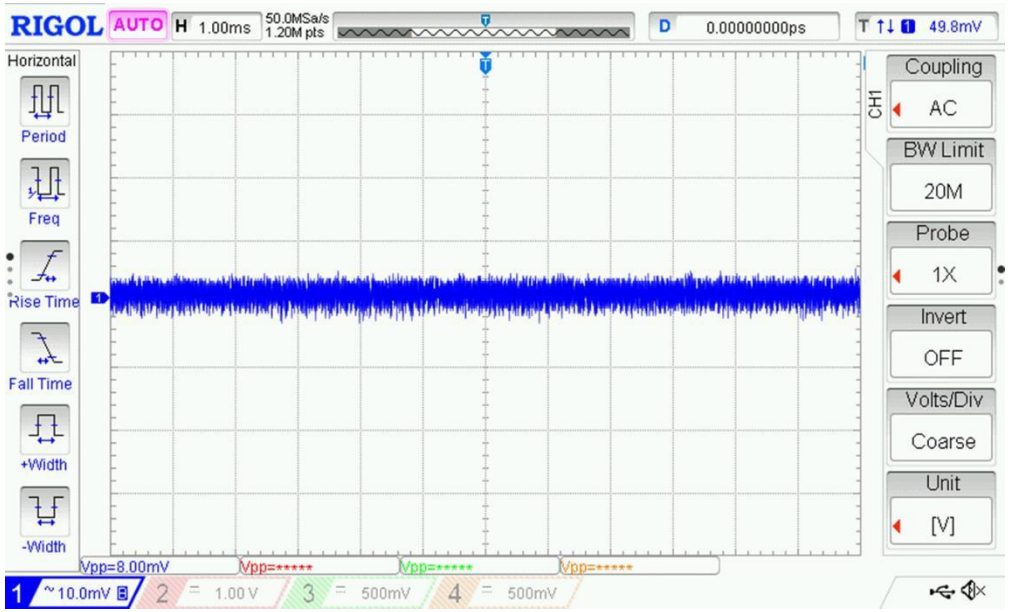




Vout = 0.72 V
Transient 2.625A – 3.5A @ 100
A/µs V_{PP} = 20.4 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

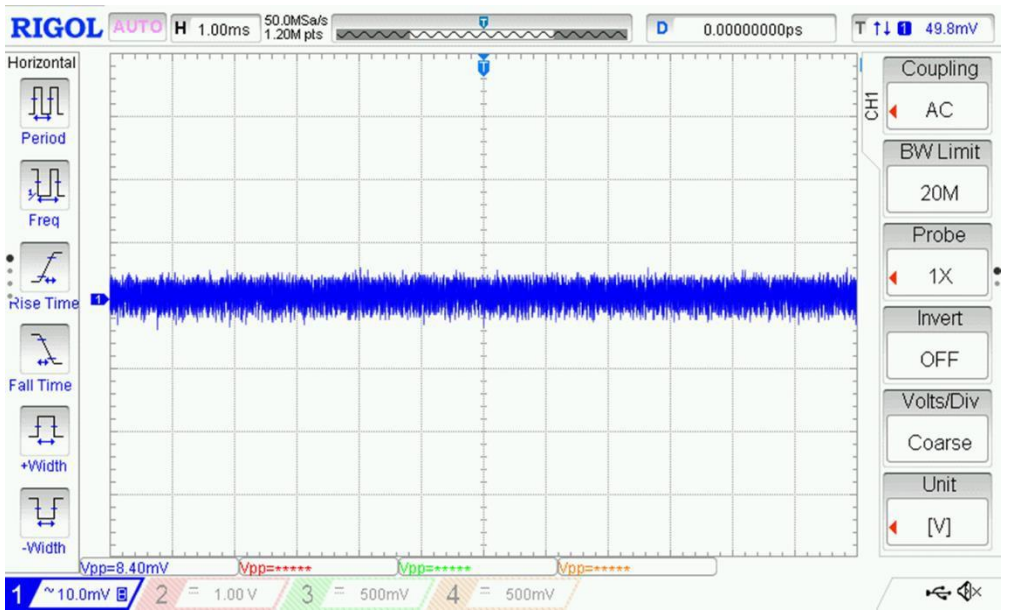
AnDAPT

Ripple



No Load
V_{PP} = 8.0 mV

Vout = 0.72 V



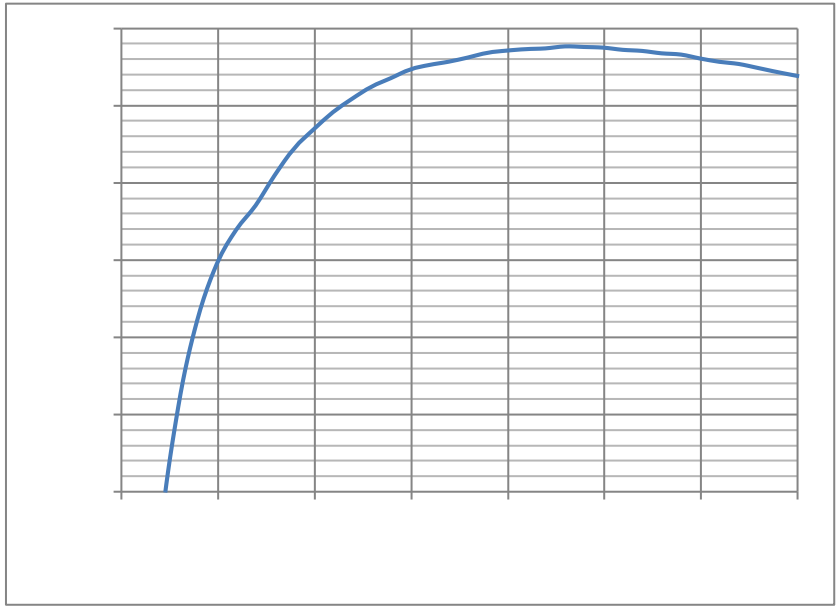
3.5A Load
V_{PP} = 8.4 mV

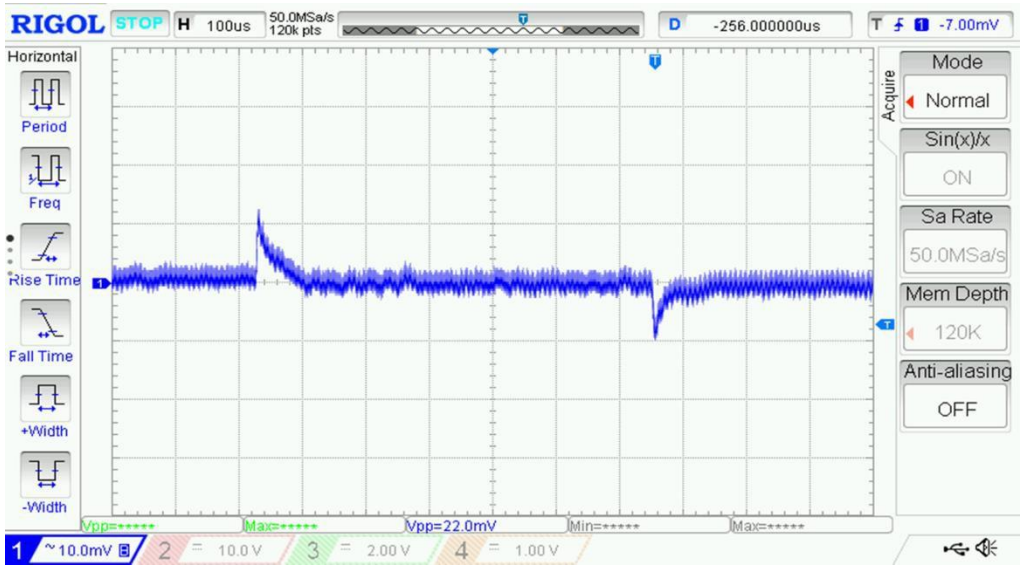
AnDAPT

VCCINT
(VCCINT, VCCBRAM, VCCINT_IO)
0.85 V / 3.5 A

- C200 Sync Buck
- Fsw = 1 MHz
- L = 0.56 µH, P/N Wurth 744393440056
- C = 9x47 uF

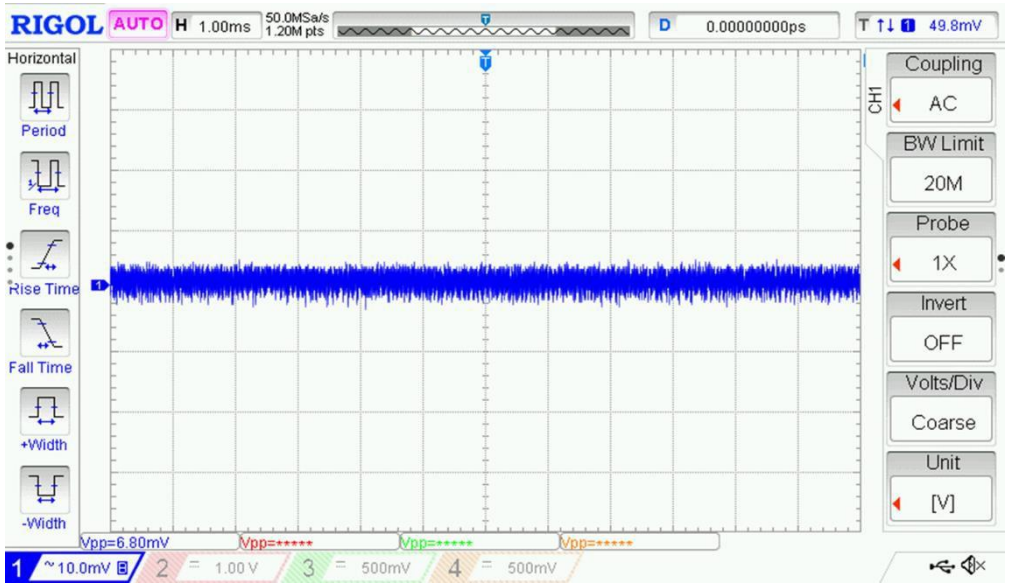
Efficiency & Transient





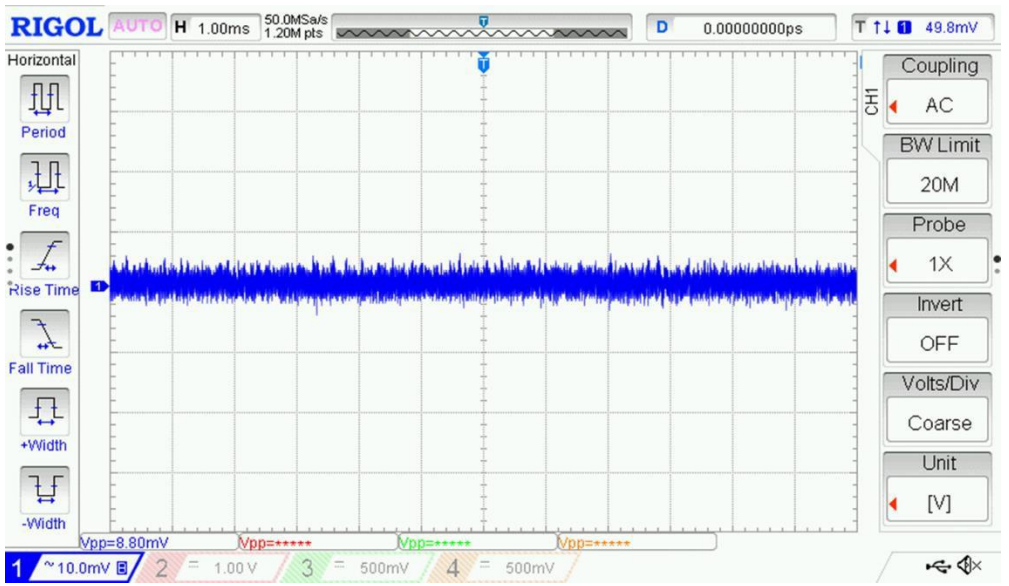
Vout = 0.85 V
Transient 2.625A – 3.5A @ 100
A/µs V_{PP} = 22.0 mV
Fsw = 1 MHz
Lout = 0.56 µH, Cout = 9 x 47 µF

Ripple



No Load
V_{PP} = 6.8 mV

Vout = 0.85 V



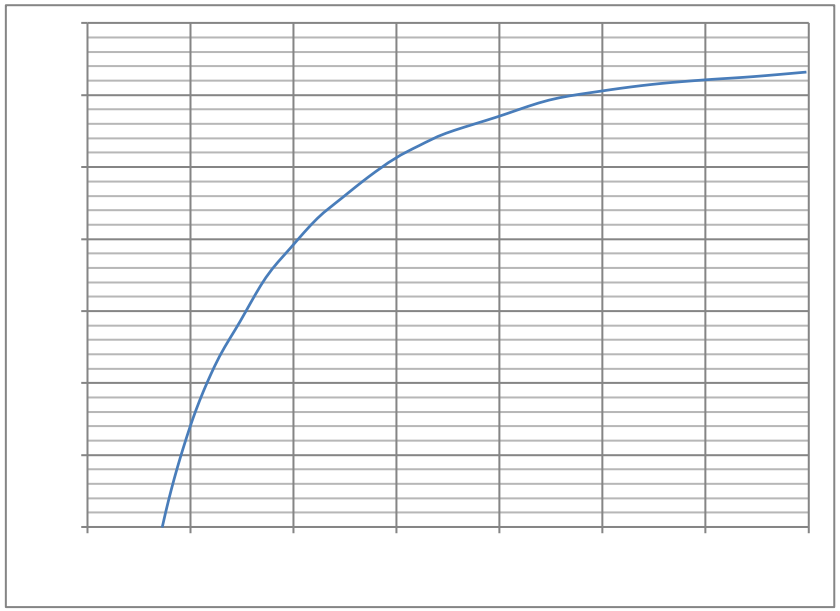
3.5A Load
V_{PP} = 8.8 mV

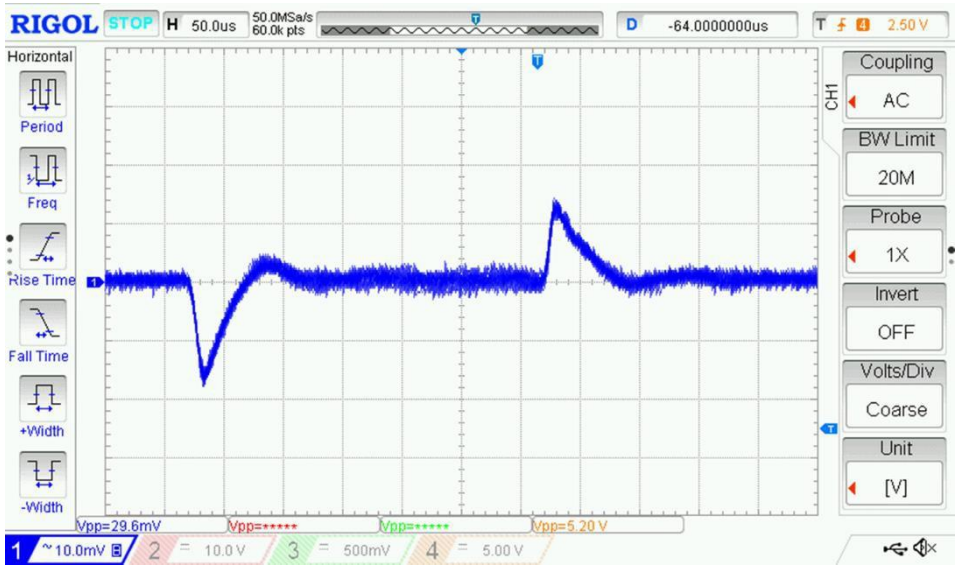
AnDAPT

VCCBRAM
0.85 V / 1.4 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 2.2 µH, P/N Wurth 74438357022
- C = 6x47 uF

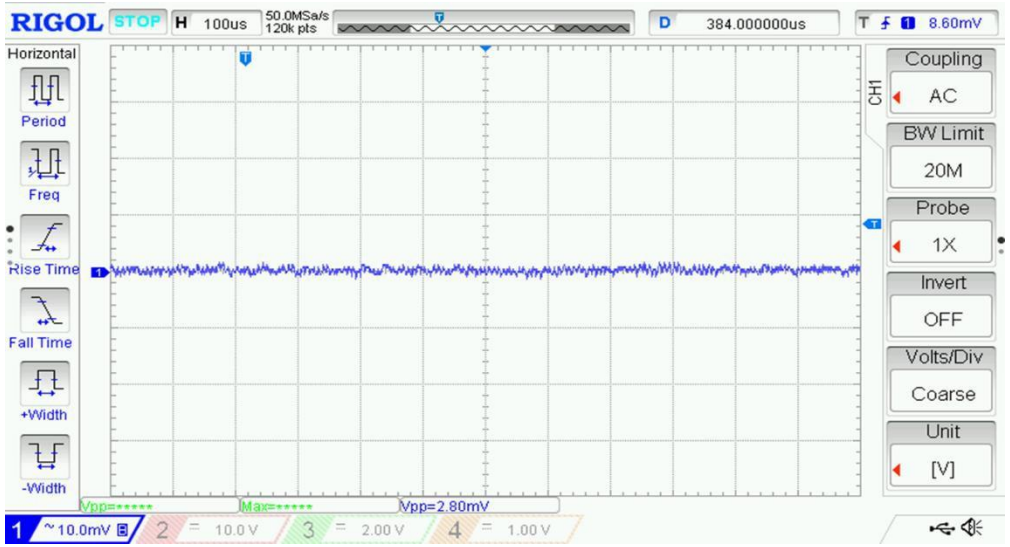
Efficiency & Transient





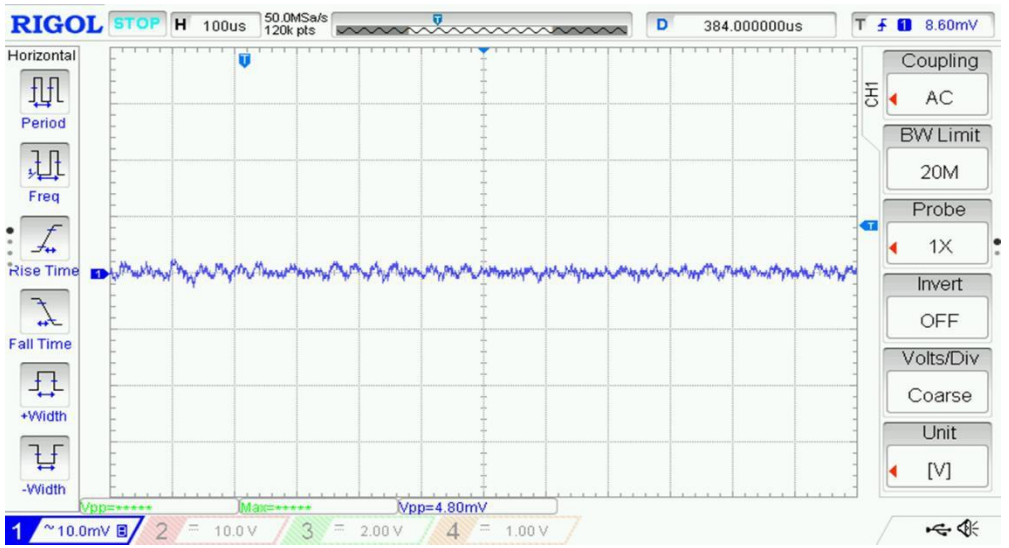
Vout = 0.85 V
Transient 0.42A – 1.4A @ 2.5
A/µs V_{PP} = 29.6 mV
Fsw = 571 kHz
Lout = 2.2 µH, Cout = 6 x 47 µF

Ripple



No Load
V_{PP} = 2.8 mV

Vout = 0.85 V



1.4A Load
V_{PP} = 4.8 mV

AnDAPT

VCCAUX (VCCAUX, VCCAUX_IO, VCCADC) 1.8 V / 0.4 A

- C200 Sync Buck
- Fsw = 571 kHz
- L = 10 µH, P/N Wurth 74438357100
- C = 1x47 uF

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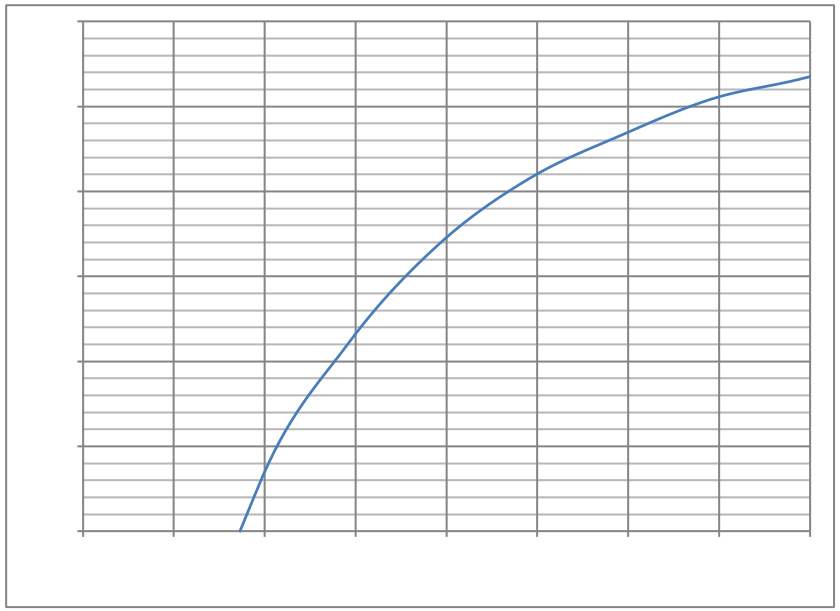
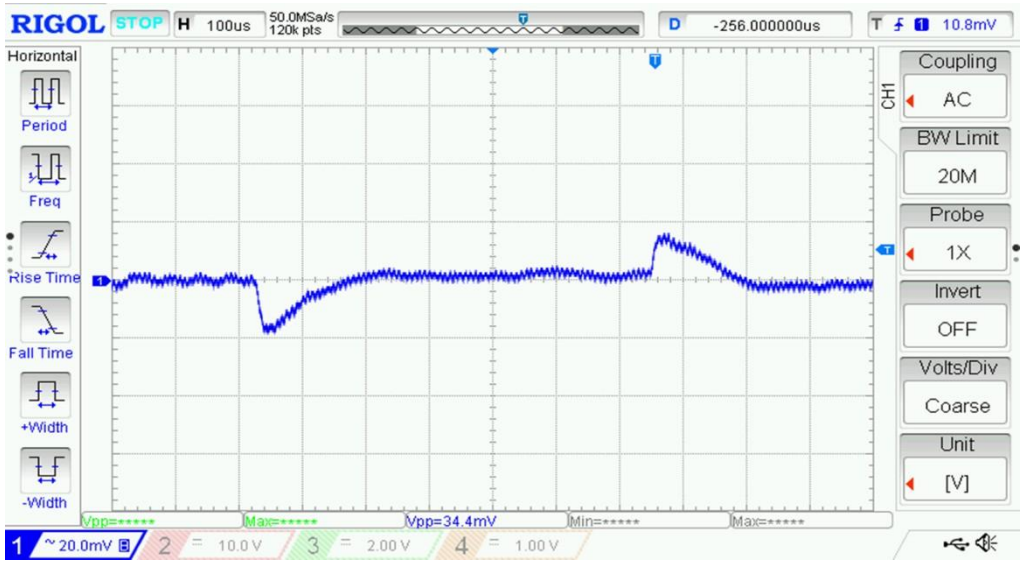
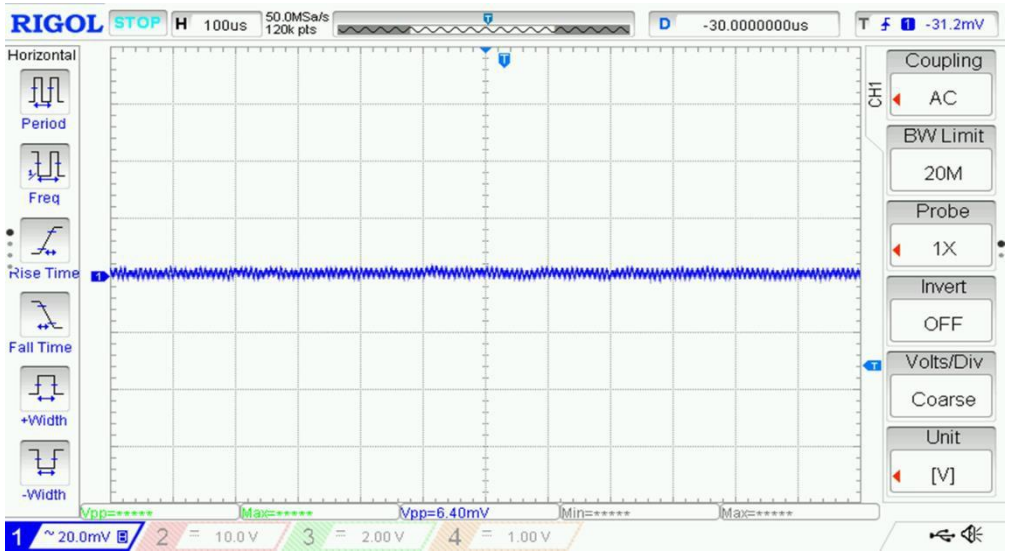
Efficiency & Transient

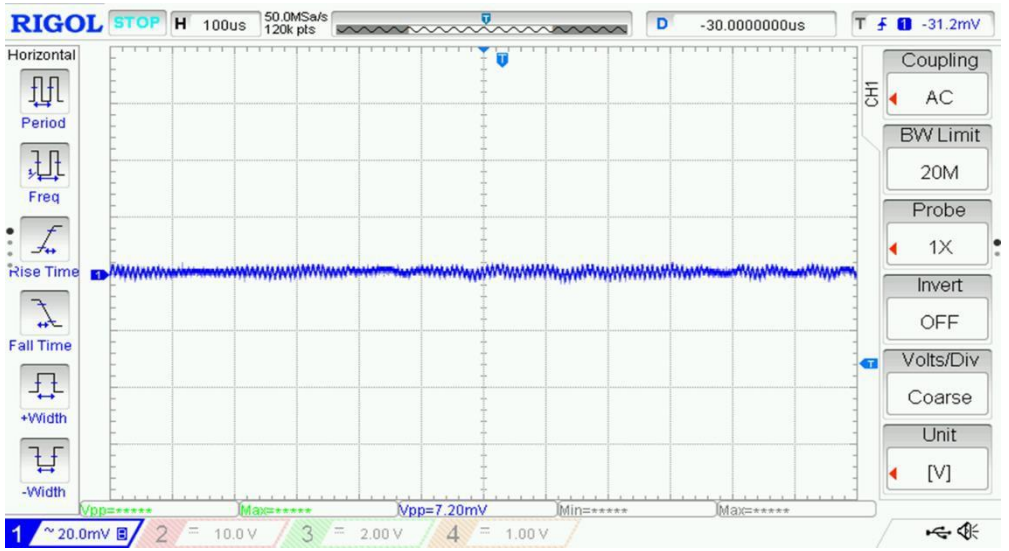




Vout = 1.8 V
Transient 0.12A – 0.4A @ 2.5
A/µs V_{PP} = 34.4 mV
Fsw = 571 kHz
Lout = 10 µH, Cout = 1x 47 µF

Ripple





No Load
V_{PP} = 6.4mV

Vout = 1.8 V

0.4A Load
V_{PP} = 7.2 mV

Thank You

AnDAPT