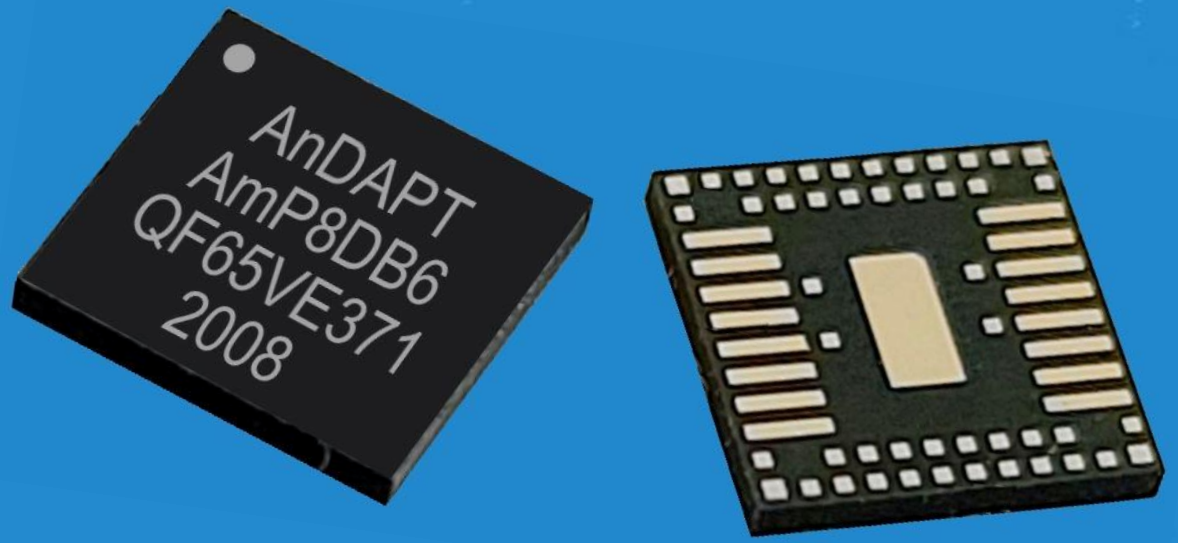

AnDAPT Power Solutions for Xilinx

Zynq Ultrascale+ MPSoC Mapping & Lab Data

Use-Case D2

AnDAPT Marketing Team

AnDAPT

Contents

- Xilinx Zynq Ultrascale+ (ZU+) family of MPSoC devices' use-cases
- AnDAPT integrated power supply reference design availability for ZU+ MPSoC SKUs
- Lab data for each power rail for Full Power Domain (D2) use-case using AnDAPT PMICs

Use-Cases (MPSoC Devices)

Devices (CG+EG+EV)	Cost-Optimized		Power Optimized	Performance Optimized	Full Power Management
	W/o MGT	With MGTs			
ZU2-ZU3	A1 (1x AnDAPT PMIC)	A2 (2x AnDAPT PMICs)	B (2x AnDAPT PMICs)	C (2x AnDAPT PMICs)	D1 (2x AnDAPT PMICs)
ZU4-ZU5					D2 (3x AnDAPT PMICs)
ZU6-ZU9					
ZU11-ZU19					

ZU+ MPSoC Rail Coverage with AmP Power Components

Use Case	SKU	VCCINT	VCCBRAM	VCCINT_IO	VCCINT_VCU	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	VCCAUX	VCCAUX_IO	VCCADC	VCC_PSAUX	VCC_PSDDR_PLL	VCC_PSADC	VMGTAVTT (GTH)	VMGTYATT (GTY)	VCC_PSPLL	VCCO_PSDDR	VCCO_PSIO	VPS_MGTRAVCC	VMGTVCCAUX (GTH)	VMGTYVCCAUX (GTY)	VPS_MGTRAVTT	VMGTAVCC (GTH)	VMGTYAVCC (GTY)	HDIO VCCO	HPIO VCCO
Cost-optimized	ZU2-ZU19 (w/o MGTs)	Rail 1			Rail 6	Rail 1			Rail 4						-	-	Rail 3	Rail 2	Rail 5	-	-	-	-	-	-	-	-
	ZU2-ZU19 (w MGTs)	Rail 1			Rail 5	Rail 1			Rail 3						Rail 6			Rail 2	Rail 4	Rail 7	Rail 8			Rail 9		-	-
Power-Optimized	ZU2-ZU19	Rail 1	Rail 2						Rail 4						Rail 3			Rail 8	Rail 5	Rail 9	Rail 6			Rail 7		-	-
Performance-Optimized	ZU2-ZU19	Rail 1			Rail 2	Rail 1			Rail 4						Rail 3			Rail 8	Rail 5	Rail 7	Rail 6			Rail 7		Rail 9	Rail 10
Full-Power Management	ZU2-ZU3	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	-	-	Rail 3	Rail 7	Rail 4	Rail 11	-	-	Rail 12	-	-	Rail 13	Rail 14
	ZU4-ZU19	Rail 8			Rail 9	Rail 1	Rail 5		Rail 10			Rail 2	Rail 6	Rail 2	Rail 13		Rail 3	Rail 7	Rail 4	Rail 11	Rail 15		Rail 12	Rail 14		Rail 16	Rail 17

C220 (Sync Buck HC)	
C200 (Sync Buck)	
C150 (Async Buck)	
C710 (SIM LDO)	
C750 (Load Switch)	
Corner LDO	

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Zynq Ultrascale+ (ZU+) MPSoC Device SKUs Covered

CG Devices (Dual Application Processor)	**EG Devices** (Quad Application Processor & GPU)	**EV Devices** (Video Codec)
XCZU2CG	XCZU2EG	XCZU4EV
XCZU3CG	XCZU3EG	XCZU5EV
XCZU4CG	XCZU4EG	
XCZU5CG	XCZU5EG	
XCZU6CG	XCZU6EG	
XCZU7CG	XCZU9EG	
XCZU9CG	XCZU11EG	
	XCZU15EG	
	XCZU17EG	
	XCZU19EG	

List may not be exhaustive. Please contact AnDAPT for further details

Zynq Ultrascale+ MPSoC (Always On, Cost-Optimized (With MGTs))

Use Case: D2

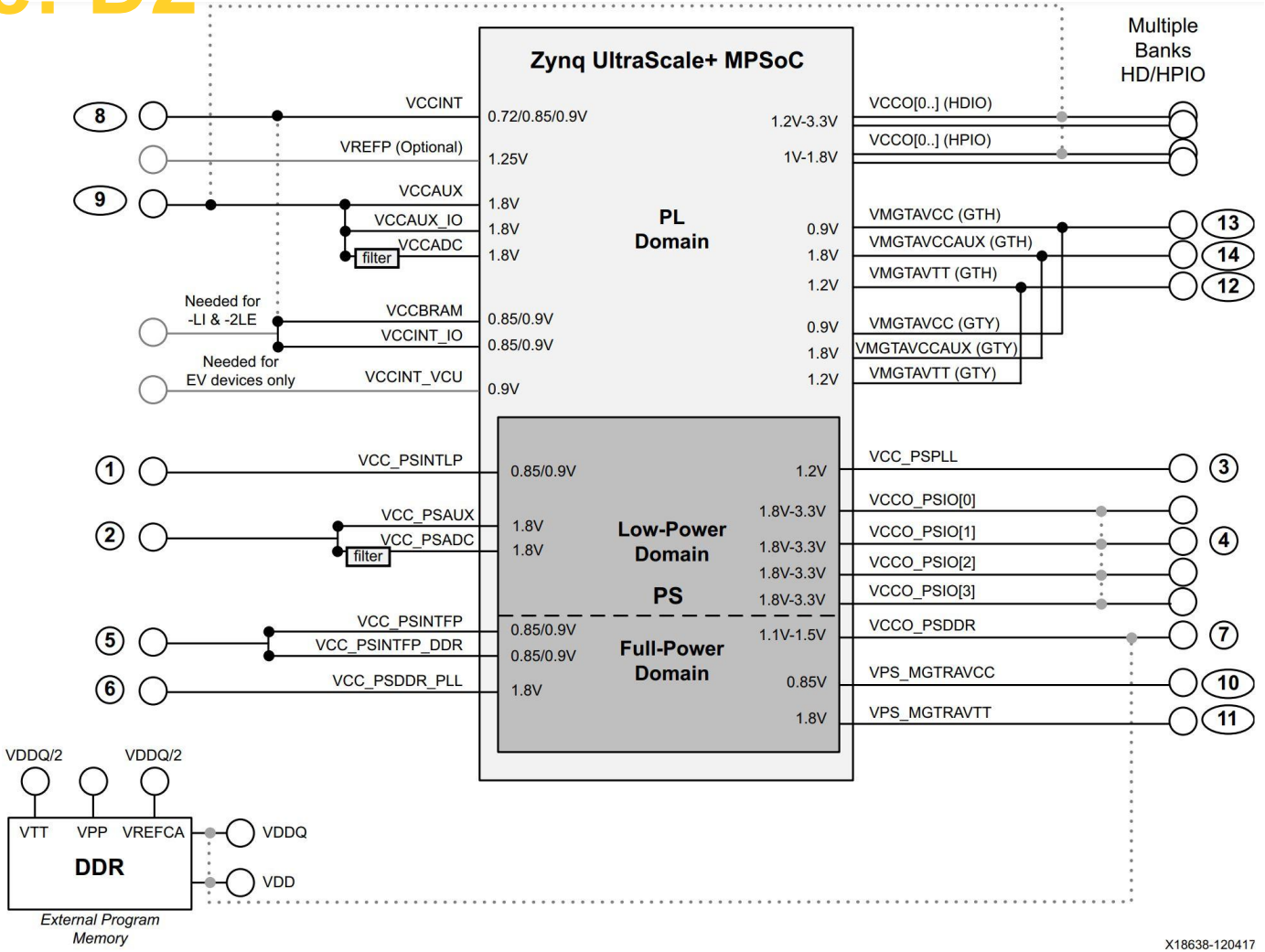

Image courtesy Xilinx: https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf

Power Tree- Use-Case: D2

V_{IN} = 12 V

#	Rail	Seq	Power Comp	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCC_PSINTLP	1	C200	Sync Buck	V_{IN}	12	0.85/0.9	3.15 + 2.75	ARD_X_ZUM_D2_IC1
2	VCC_PSAUX, VCC_PSADC	2	C200	Sync Buck	V_{IN}	12	1.8	1.2 + 0.1 + 0.5 + 1.82 + 0.1 + 0.3	ARD_X_ZUM_D2_IC1
3	VCC_PSPLL	3	C200	Sync Buck	V_{IN}	12	1.2	1.7	ARD_X_ZUM_D2_IC1
4	VCCO_PSIO	4	C150	Async Buck	V_{IN}	12	1.8-3.3	1	ARD_X_ZUM_D2_IC1
5	VCC_PSINTFP, VCC_PSINTFP_DDR	5	C750	Load Switch	VCC_PSINTLP	0.85/0.9	0.85/0.9	2.75	ARD_X_ZUM_D2_IC1
6	VCC_PSDDR_PLL	6	C750	Load Switch	VCC_PSAUX	1.8	1.8	0.1	ARD_X_ZUM_D2_IC2
7	VCCO_PSDDR	7	C710	SIM LDO	VCC_PSAUX	1.8	1.1-1.5	0.5	ARD_X_ZUM_D2_IC2
8	VCCINT, VCCBRAM, VCCINT_IO	8	C860	DrMOS Ctrl	V_{IN}	12	0.85	(1.6-29.2) + 0.3	ARD_X_ZUM_D2_IC2
9	VCCINT_VCU*	8	C200	Sync Buck	V_{IN}	12	0.85	3	ARD_X_ZUM_D2_IC2
10	VCCAUX, VCCAUX_IO, VCCADC, DDR_VPP1	9	C750	Load Switch	VCC_PSAUX	1.8	1.8	1.82	ARD_X_ZUM_D2_IC2
11	VPS_MGTRAVCC	10	C750	Load Switch	VCCINT	0.85	0.85	0.3	ARD_X_ZUM_D2_IC2
12	VPS_MGTRAVTT	11	C750	Load Switch	VCC_PSAUX	1.8	1.8	0.1	ARD_X_ZUM_D2_IC2
13	VMGTAVTT(GTH), VMGTYAVTT(GTY)	12	C220	Sync Buck HC	V_{IN}	12	1.2	2.5-10	ARD_X_ZUM_D2_IC3
14	VMGTAVCC(GTH), VMGTAVCC(GTY)	13	C200	Sync Buck	V_{IN}	12	0.9	6	ARD_X_ZUM_D2_IC3
15	VMGTVCCAUX(GTH), VMGTYVCCAUX(GTY)	14	C750	Load Switch	VCC_PSAUX	1.8	1.8	0.3	ARD_X_ZUM_D2_IC3
16	HDIO_VCCO	14	C150	Async Buck	V_{IN}	12	1.2-3.3	0.5	ARD_X_ZUM_D2_IC3
17	HPIO_VCCO	11	C150	Async Buck	V_{IN}	12	1-1.8	1	ARD_X_ZUM_D2_IC2

*Only required for EV devices

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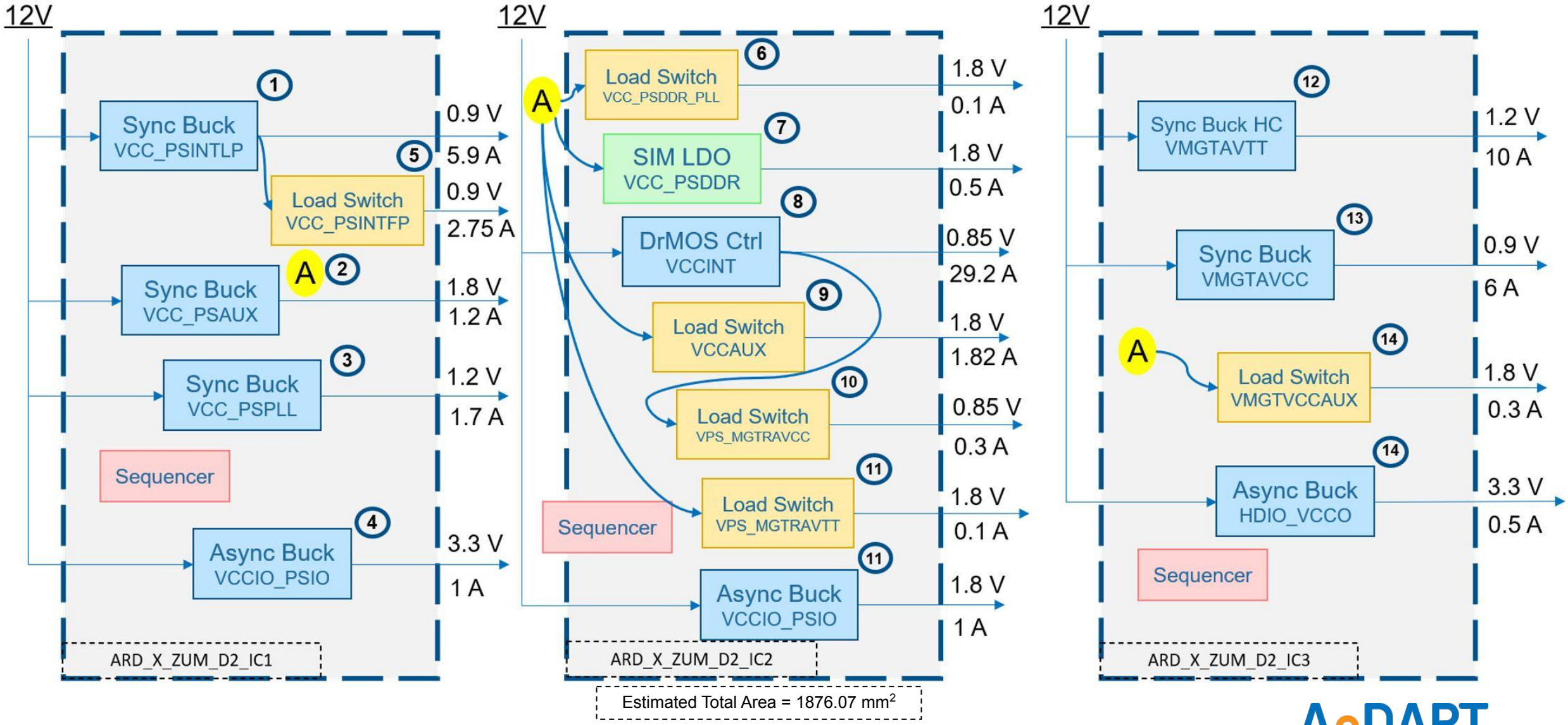
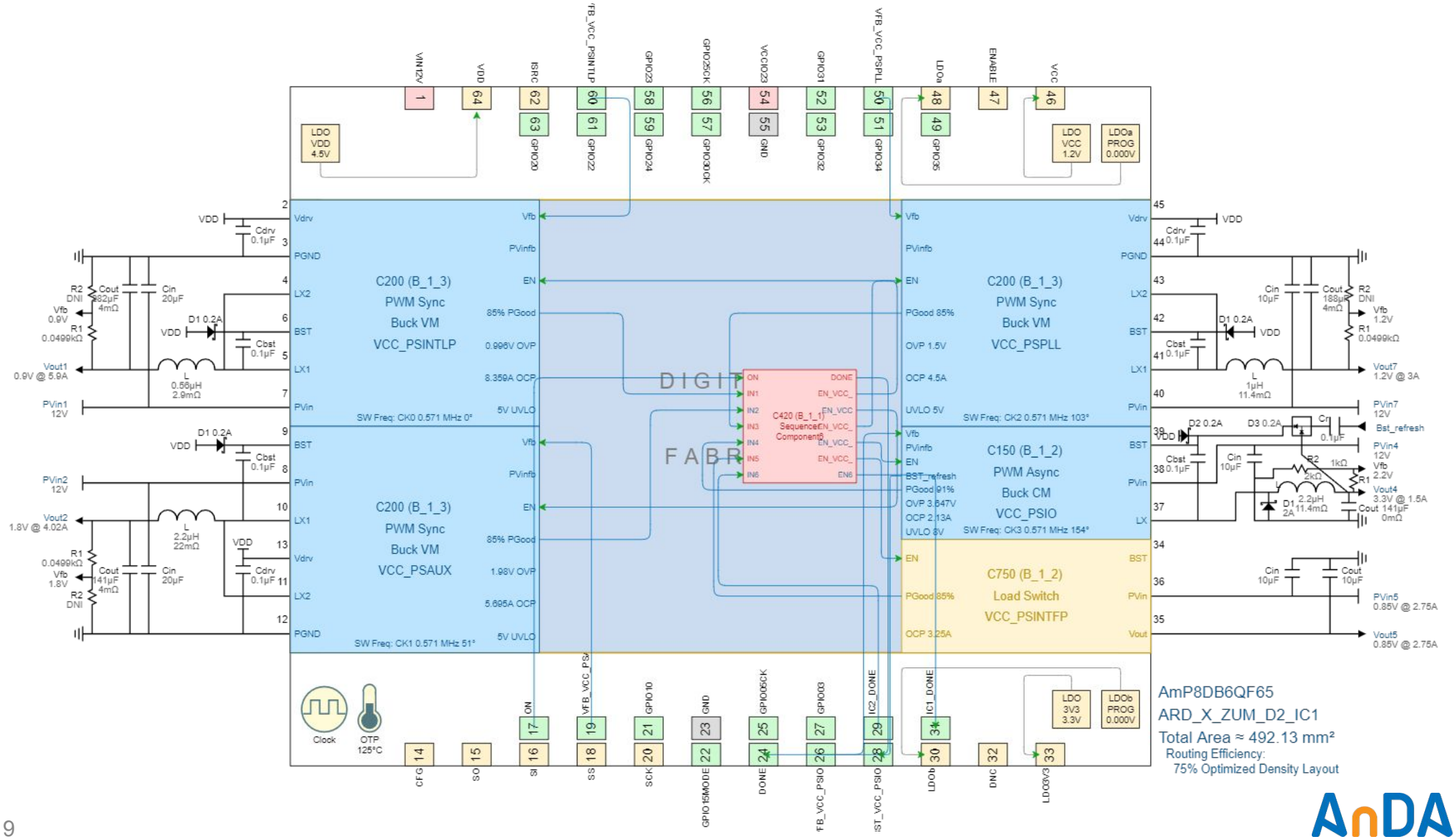
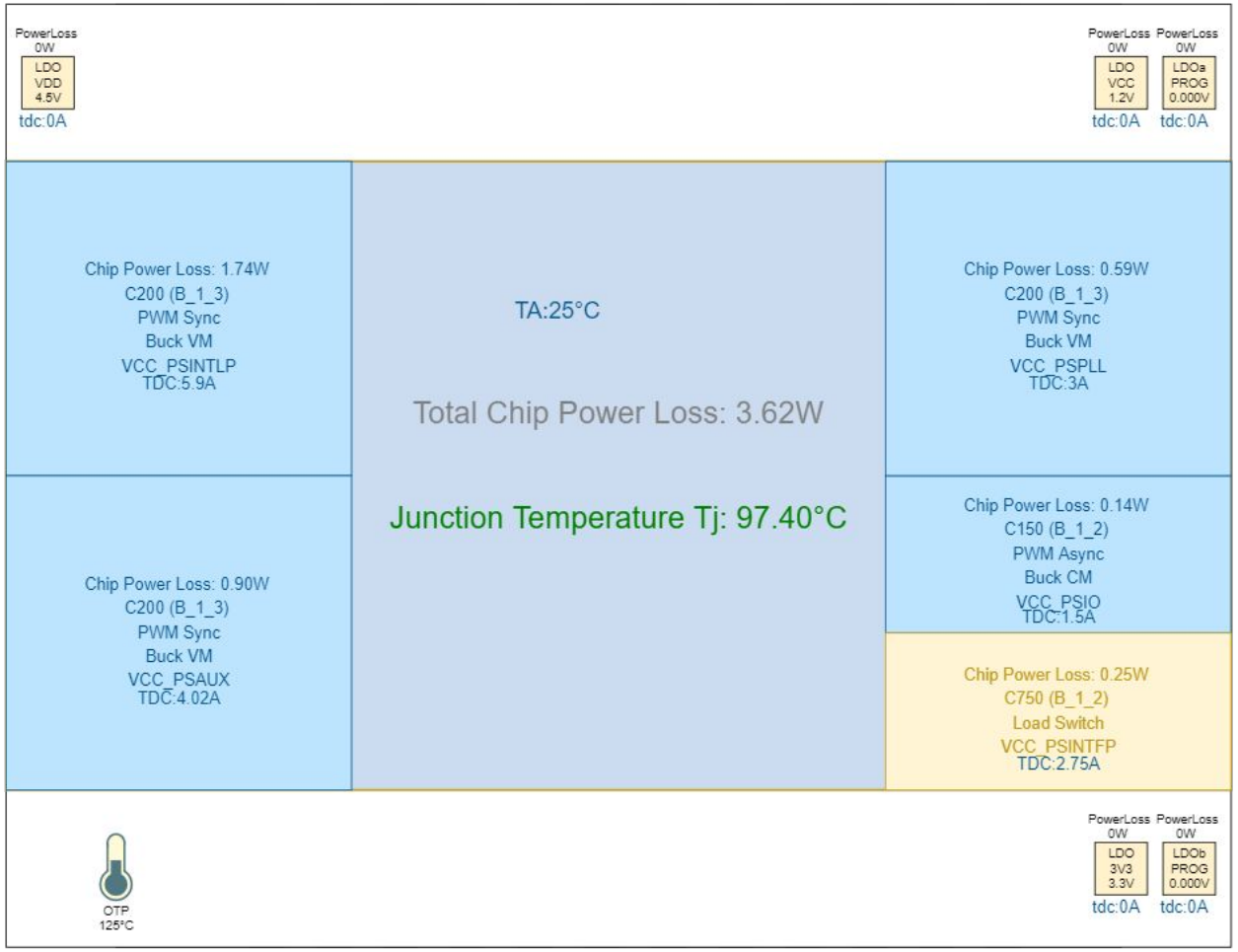
Proposed Solution (3xPMICs)
Use-Case D2



Mapping IC1 (WebAmP View)
Use-Case D2



Thermal Design View (IC1)
Use-Case D2



AmP8DB6QF65
ARD_X_ZUM_D2_IC1
Total Area ≈ 492.13 mm²
Routing Efficiency:
75% Optimized Density Layout

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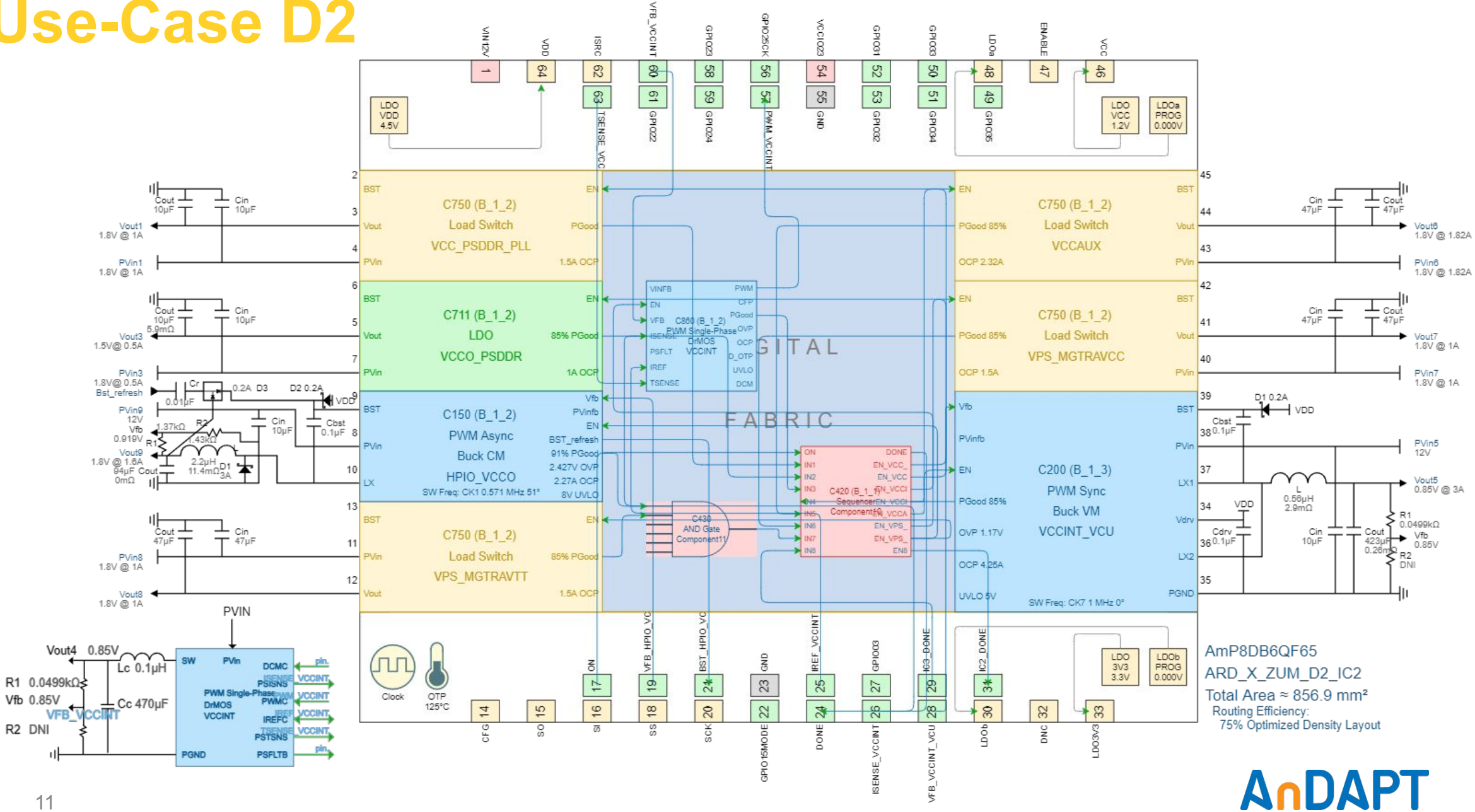
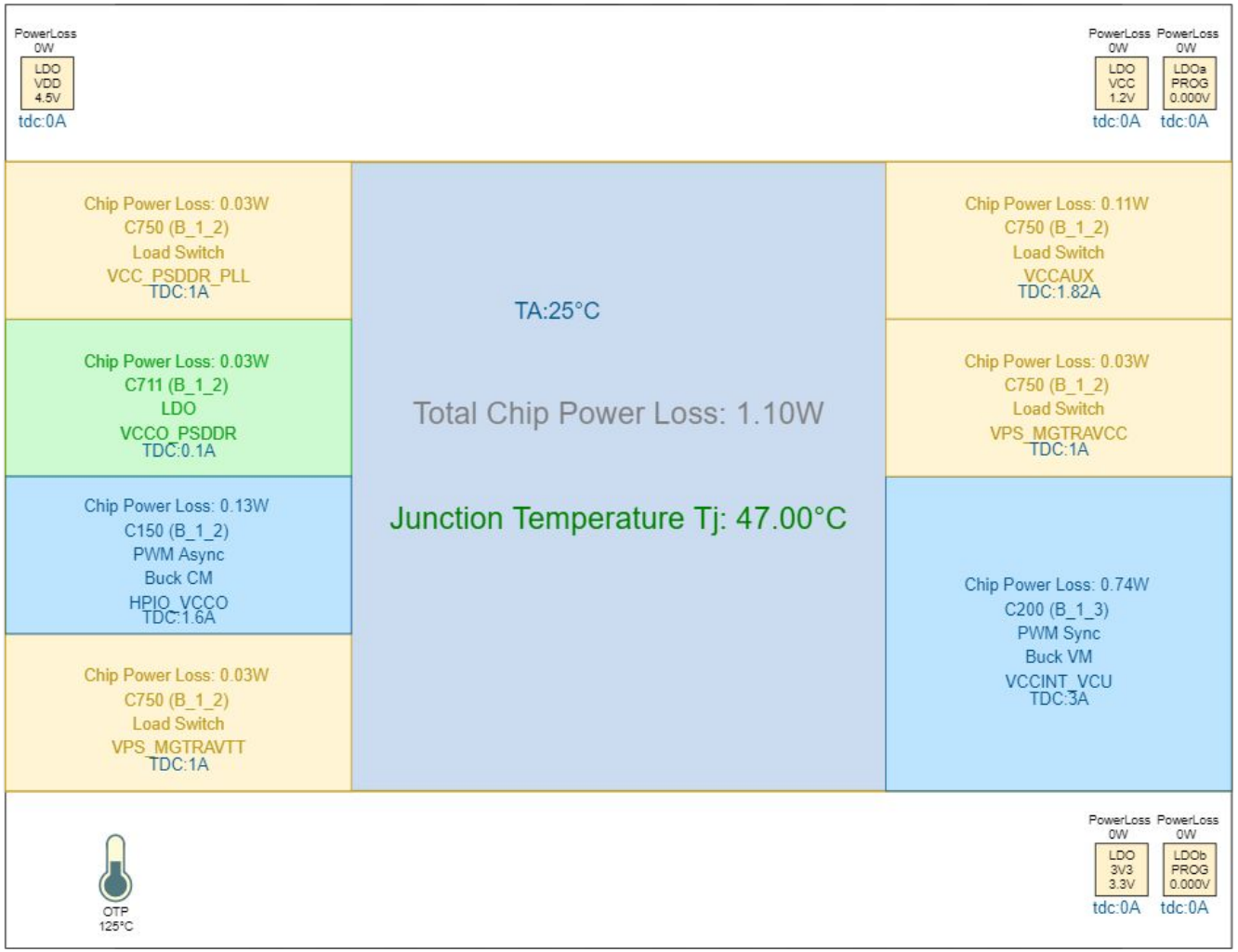
Mapping IC2 (WebAmP View)

Use-Case D2



Thermal Design View (IC2)
Use-Case D2



AmP8DB6QF65
ARD_X_ZUM_D2_IC2
Total Area ≈ 856.9 mm²
Routing Efficiency:
75% Optimized Density Layout

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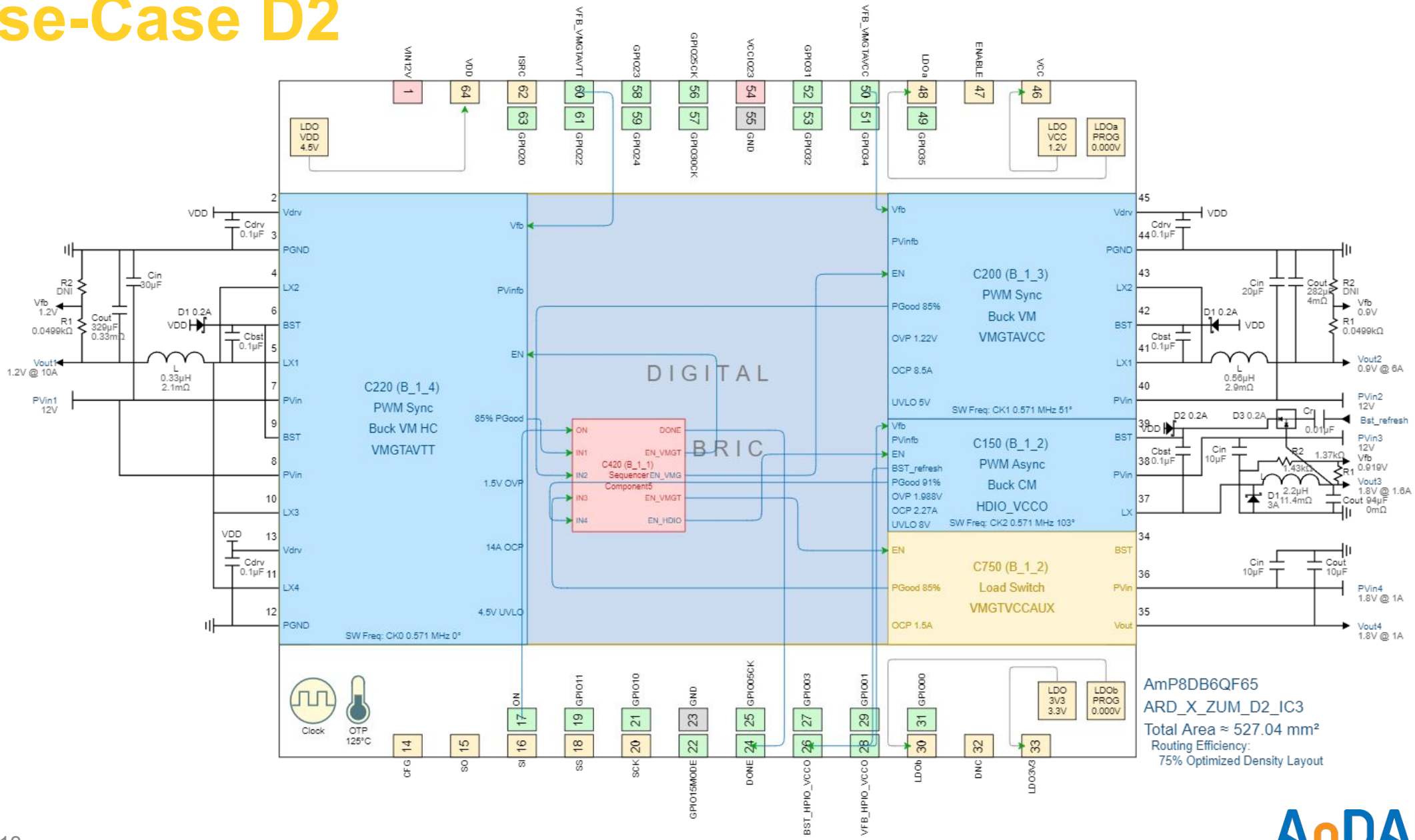
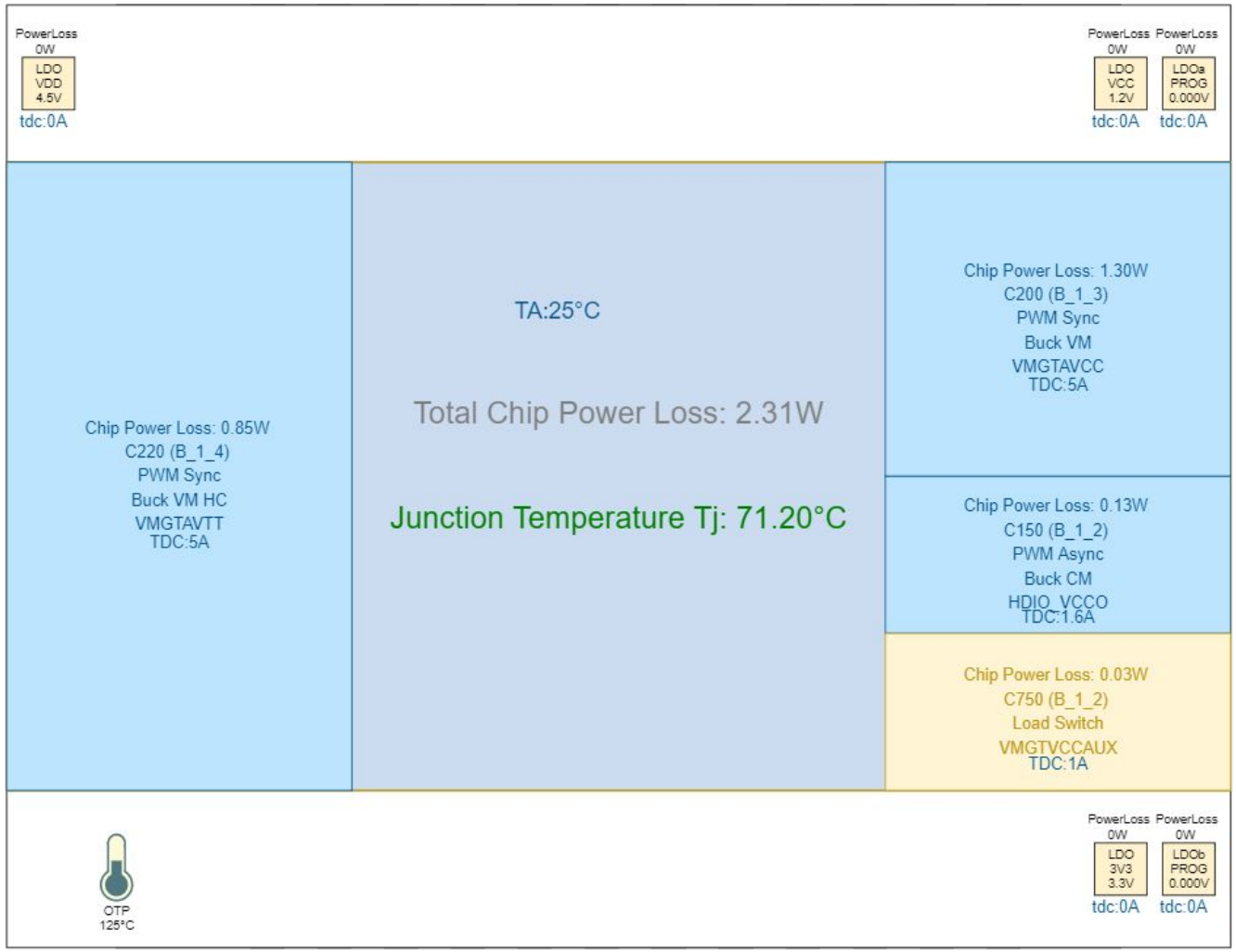
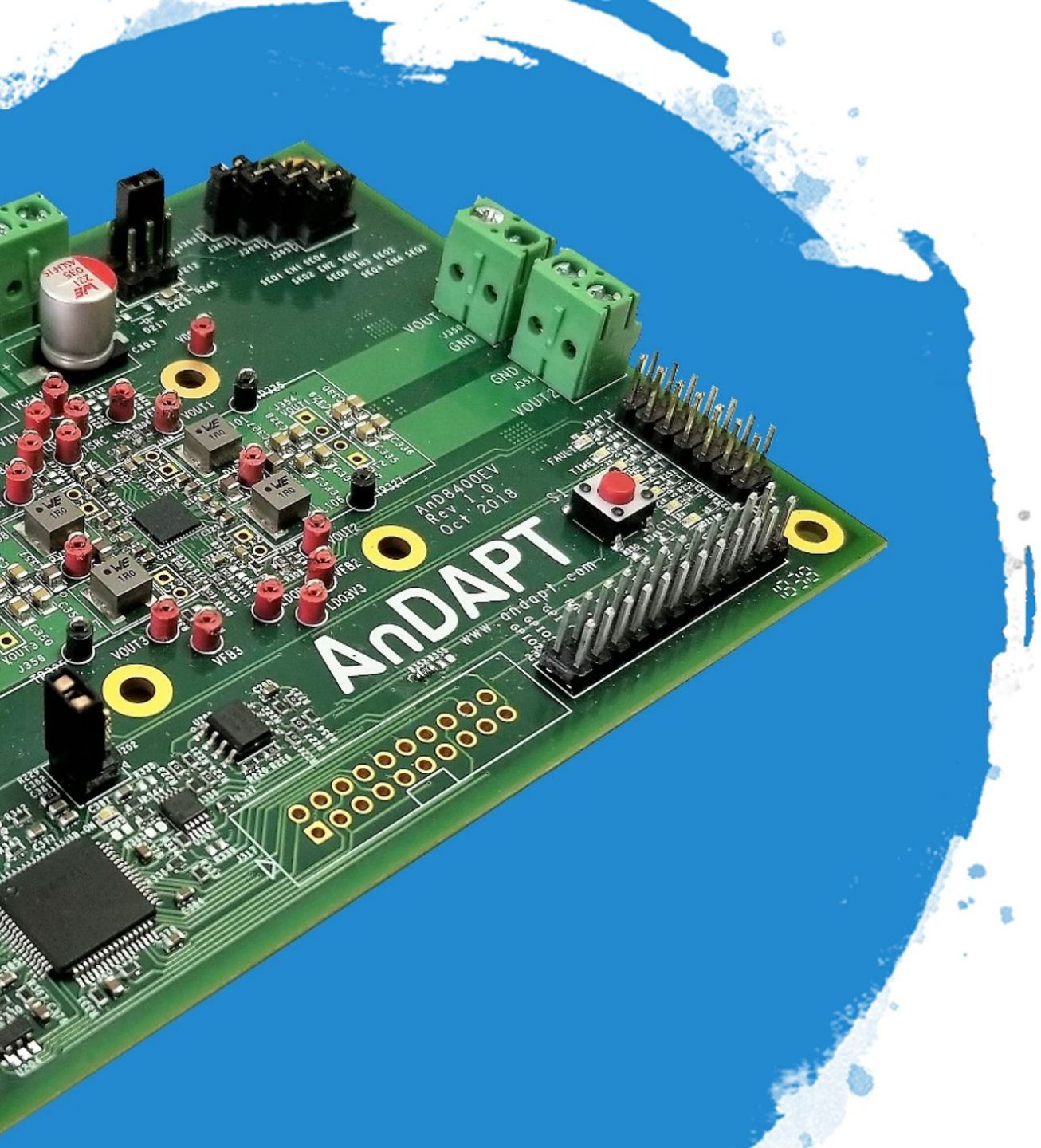
Mapping IC3 (WebAmP View)
Use-Case D2



Thermal Design View (IC3)
Use-Case D2



AmP8DB6QF65
ARD_X_ZUM_D2_IC3
Total Area ≈ 527.04 mm²
Routing Efficiency:
75% Optimized Density Layout



Bench Data

Use-Case D2

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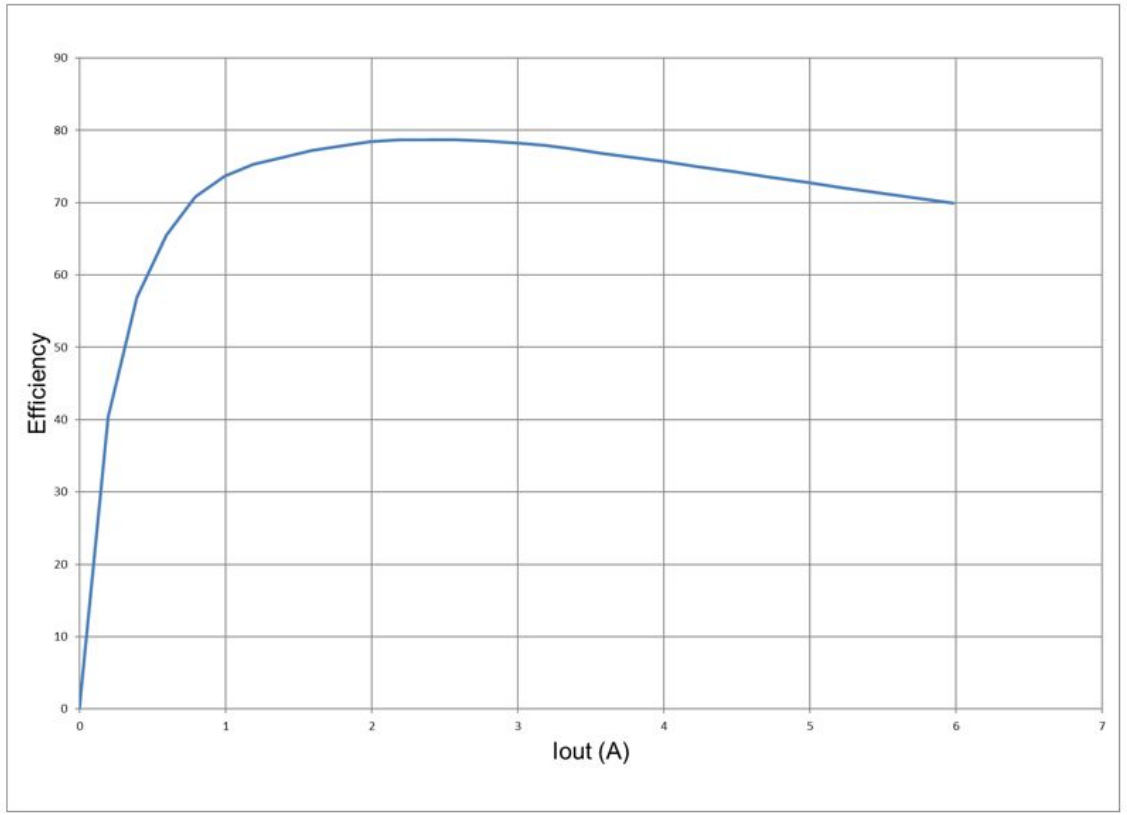
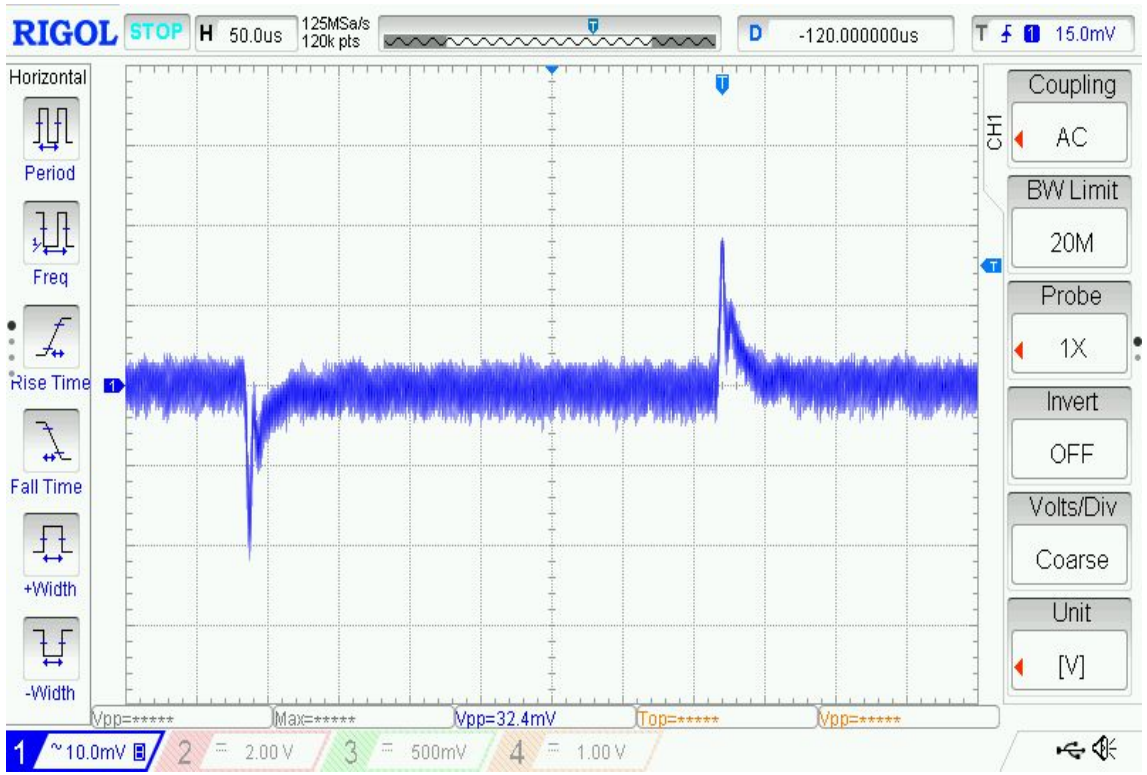
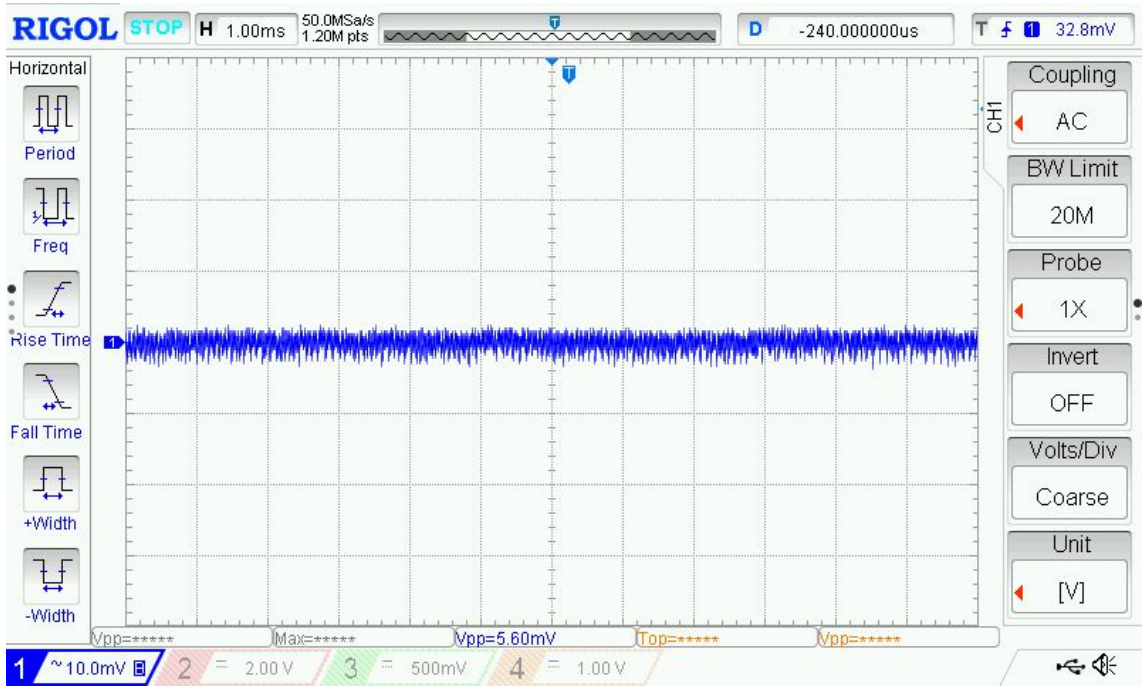
VCCPSINTLP: Efficiency & Transient



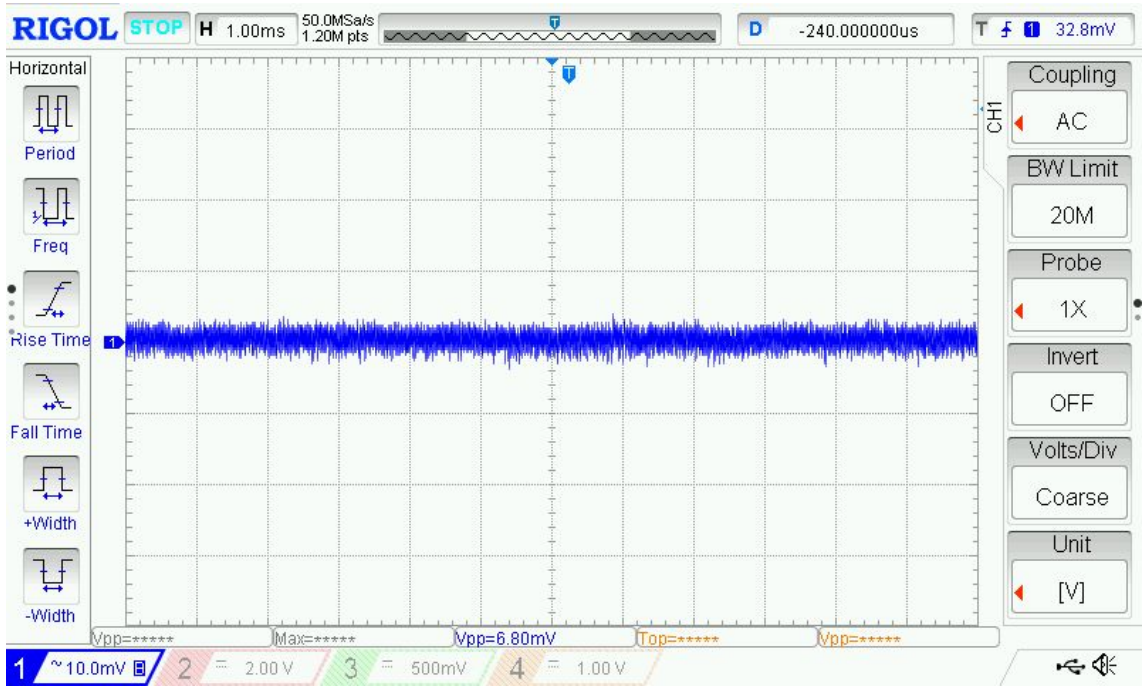


Vout = 0.9 V
Transient 4.5 A – 6 A
V_{PP} = 32.4mV
Lout = 0.56 nH, Cout = 3 x 47 µF

VCCPSINTLP: Ripple



No Load
V_{PP} = 5.6 mV



Full Load
V_{PP} = 6.8 mV

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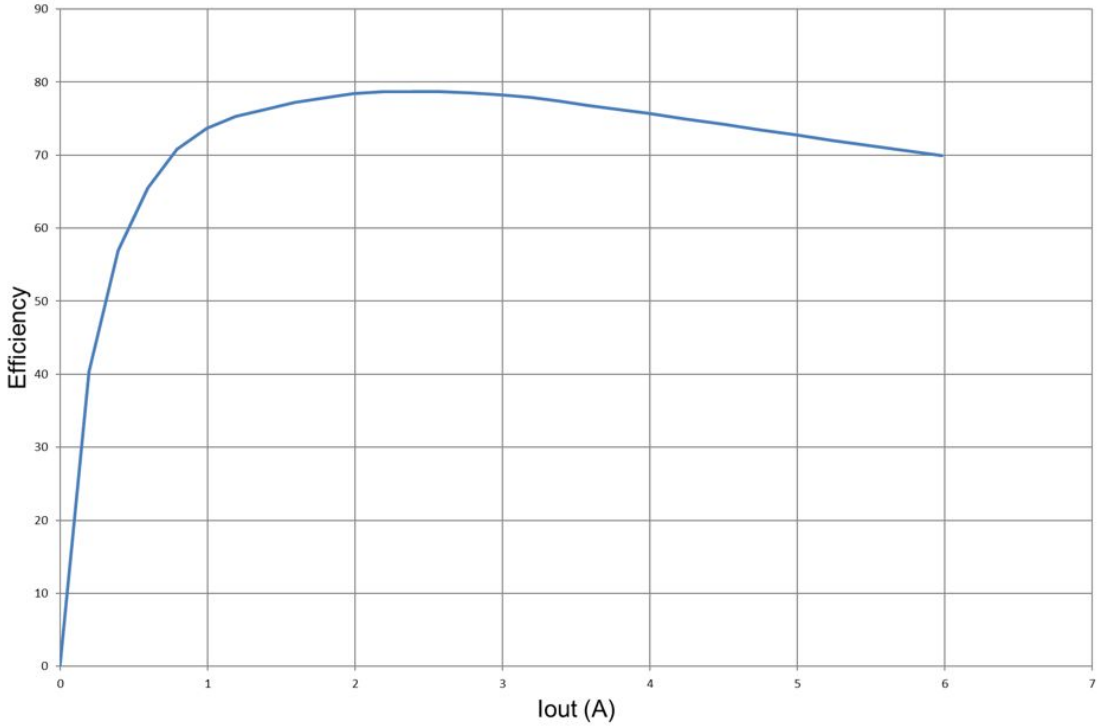
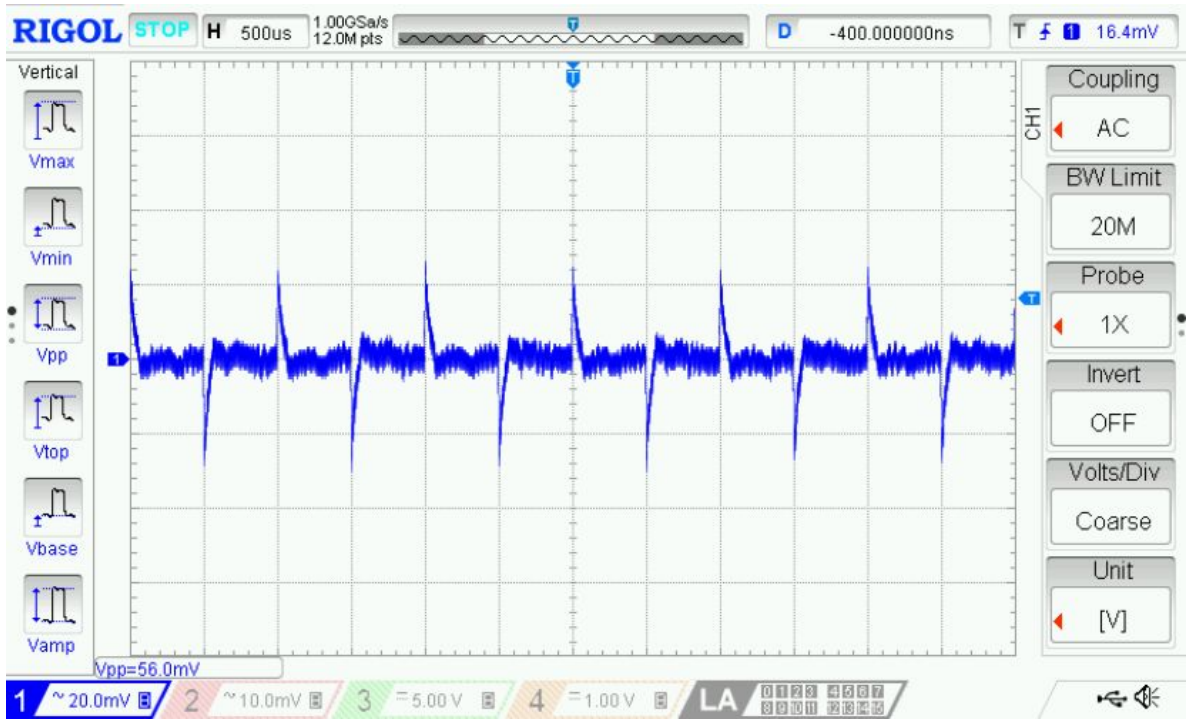
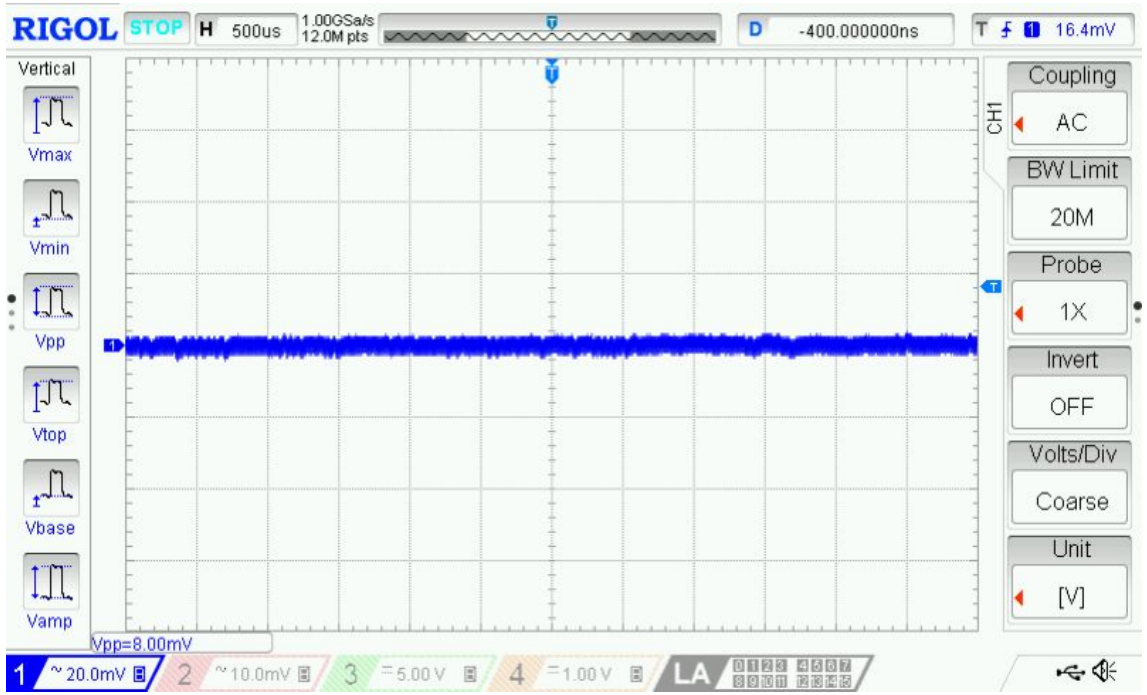
VCC_PSAUX: Efficiency & Transient



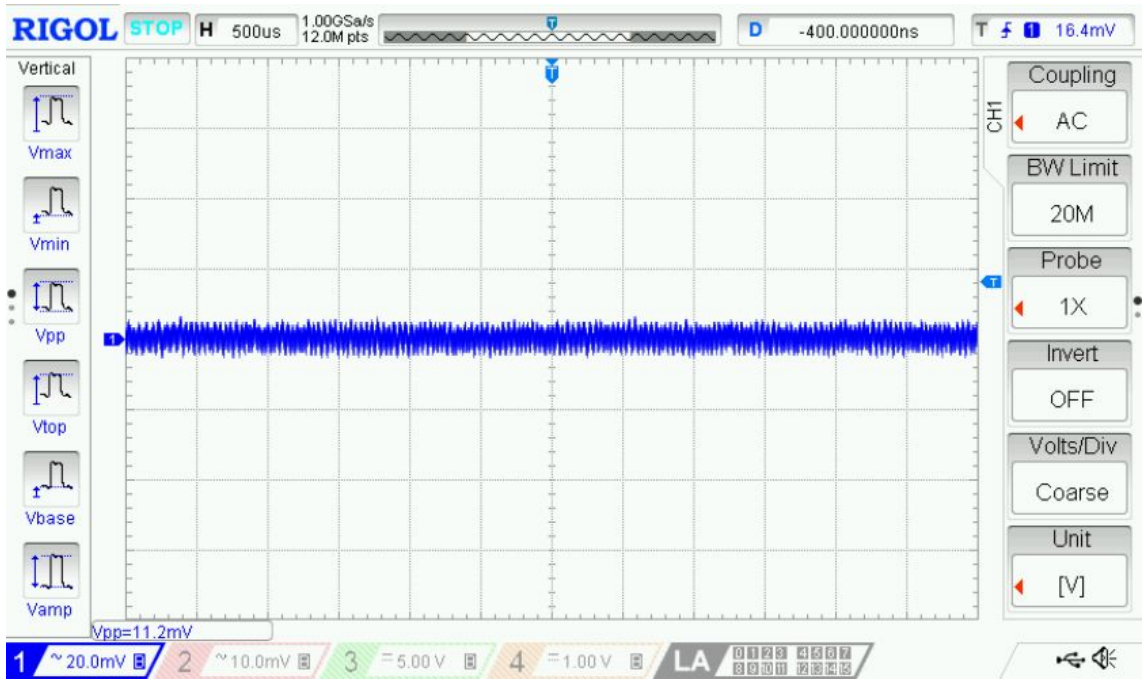


Vout = 0.9 V
Transient 3 A – 4.02 A
V_{PP} = 56mV
Lout = 2.2 nH, Cout = 3 x 47 µF

VCC_PSAUX: Ripple



No Load
V_{PP} = 8 mV



Full Load
V_{PP} = 11.2 mV

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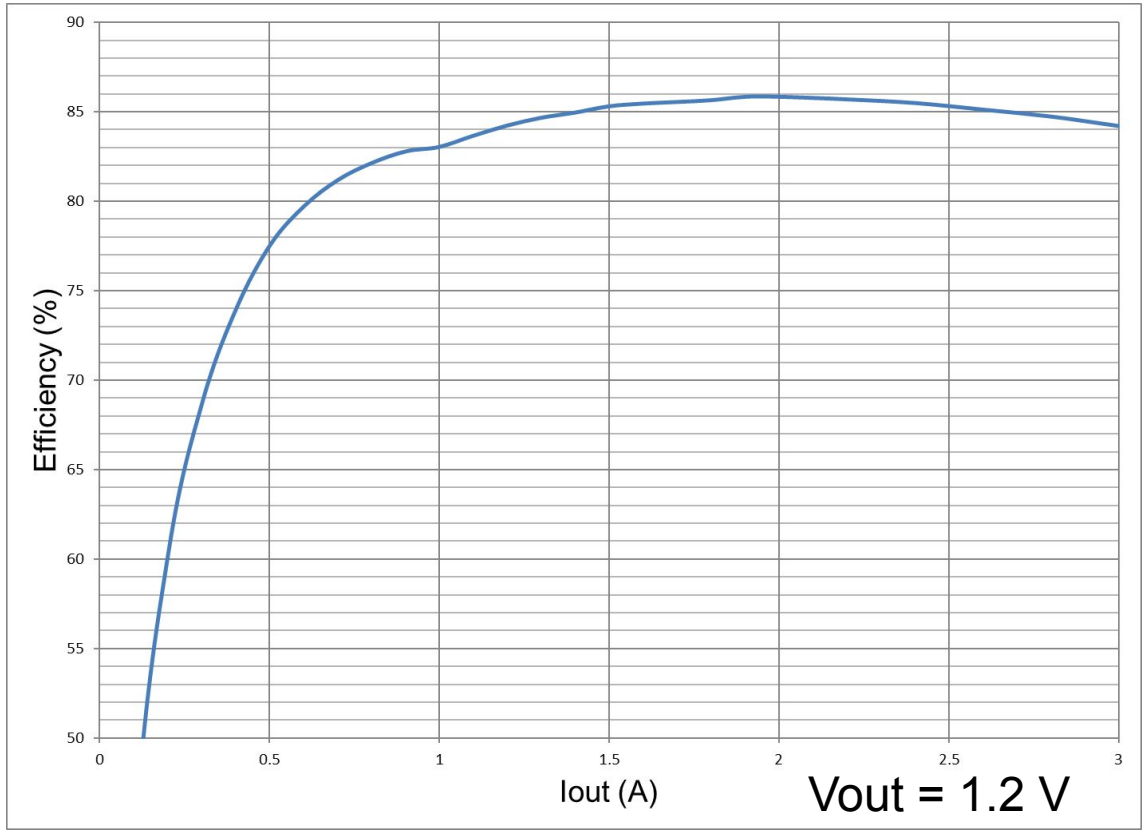
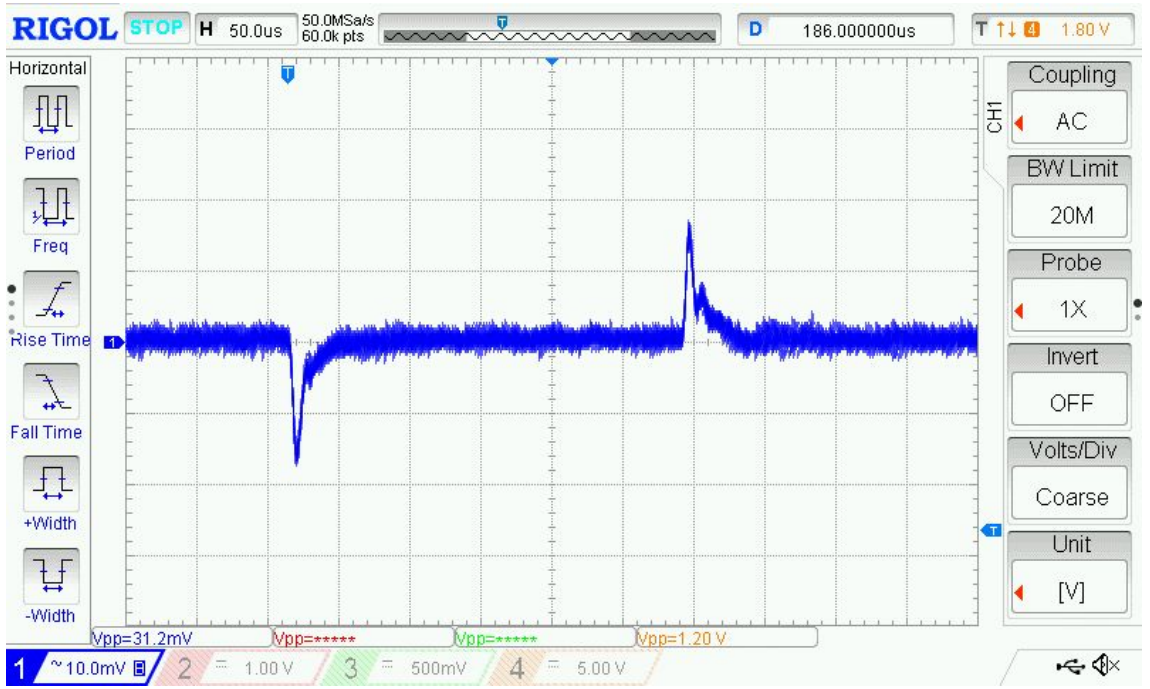
VCC_PSPLL: Efficiency & Transient





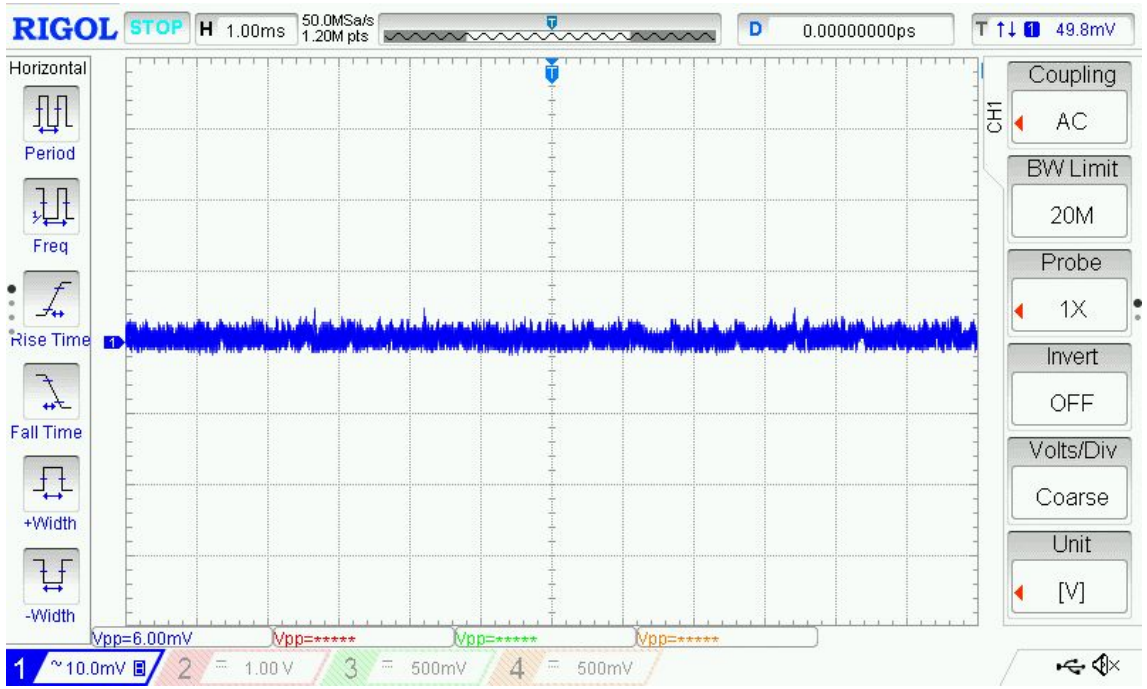
Vout = 1.2 V

Transient 2.25A to 3A @ 10 A/us

V_{PP} = 31.2 mV

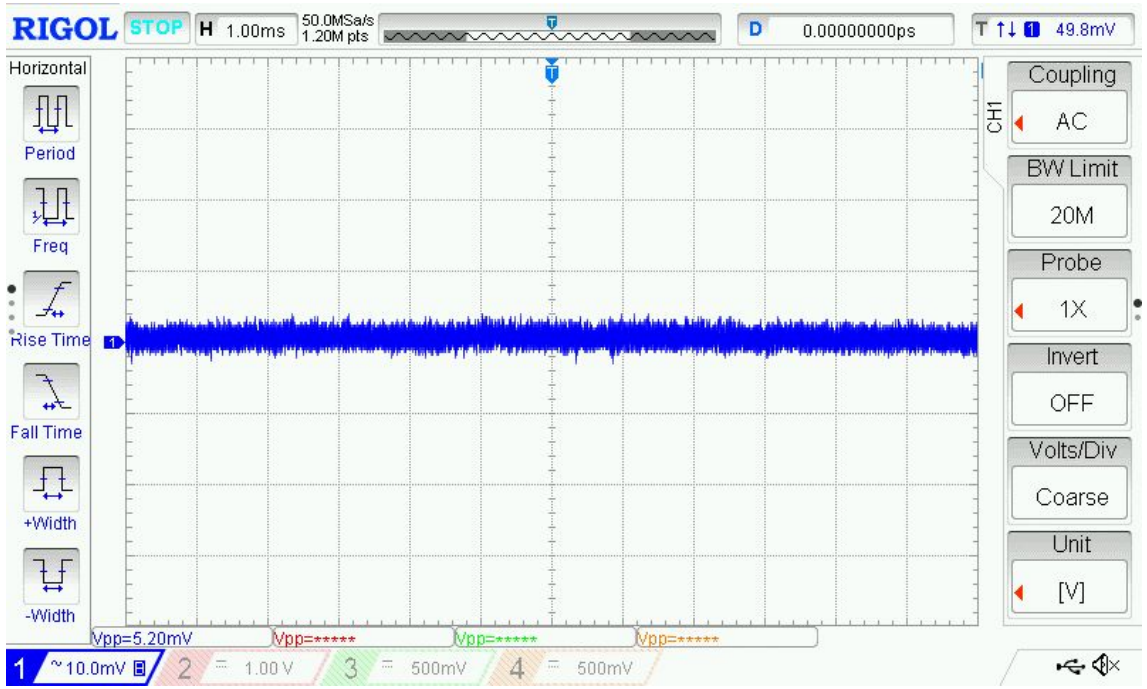
Lout = 1 µH, Cout = 4 x 47 µF

VCC_PSPLL: Ripple



No Load

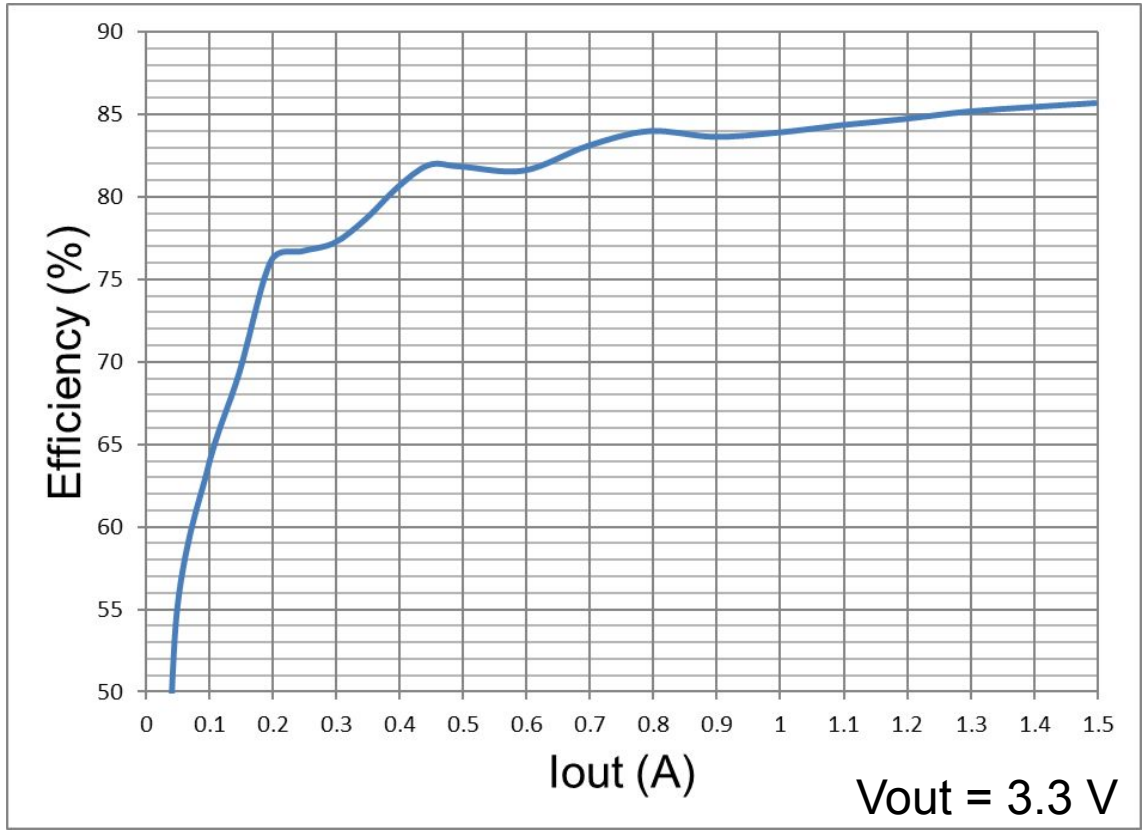
V_{PP} = 6 mV

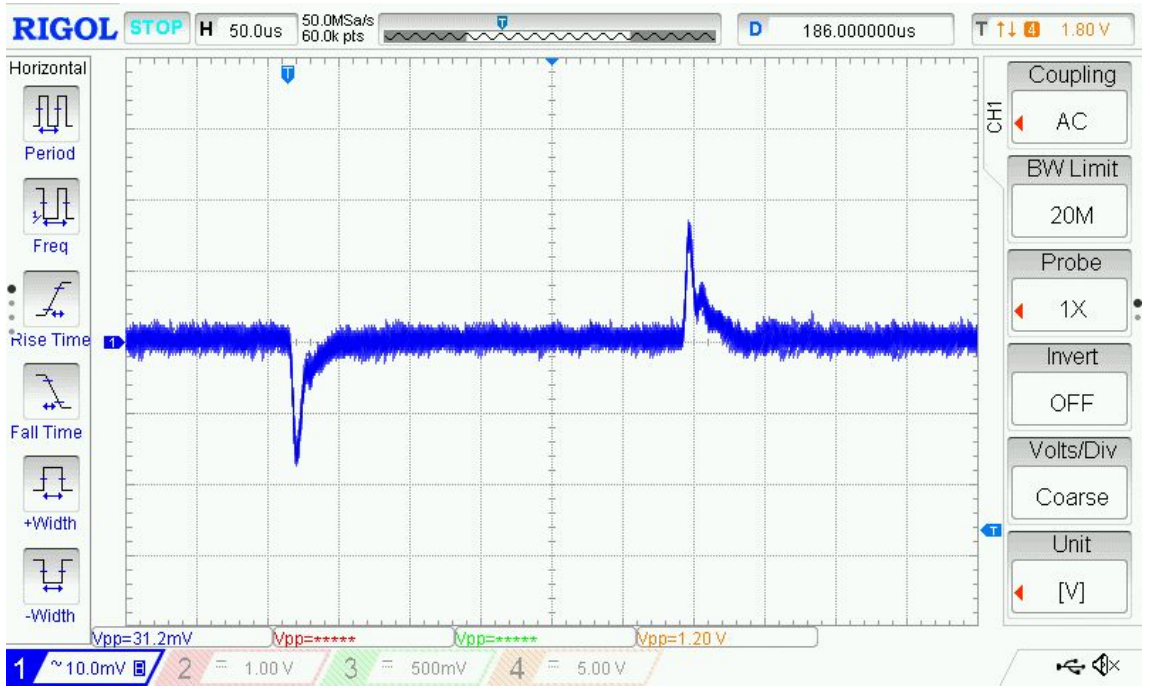


Full Load

V_{PP} = 5.2 mV

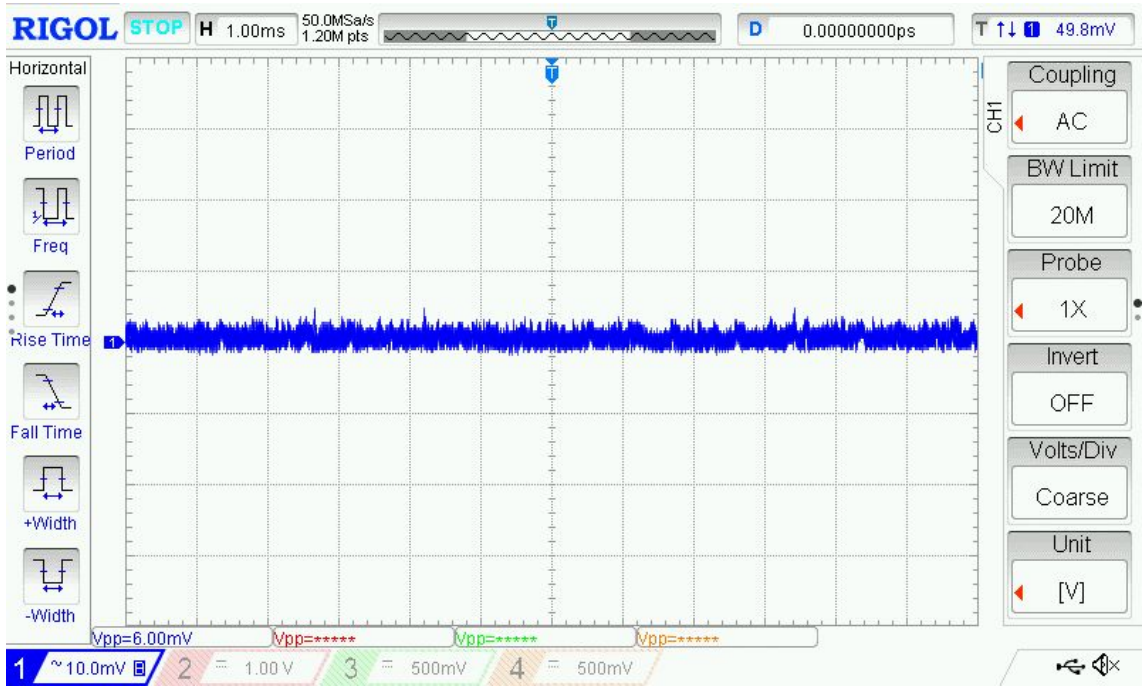
VCCO_PSIO: Efficiency & Transient



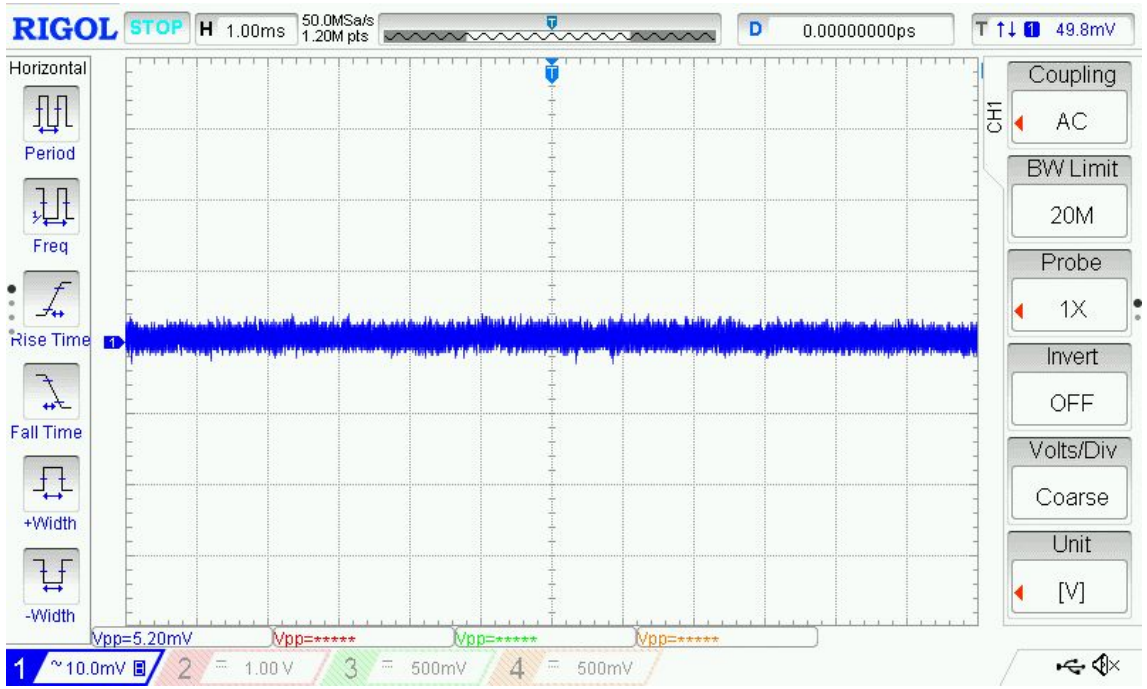


Vout = 3.3 V
Transient 0.15 A to 1.5 A @ 10 A/us
V_{PP} = 94 mV
Lout = 2.2 µH, Cout = 2 x 47 µF

VCCO_PSIO: Ripple

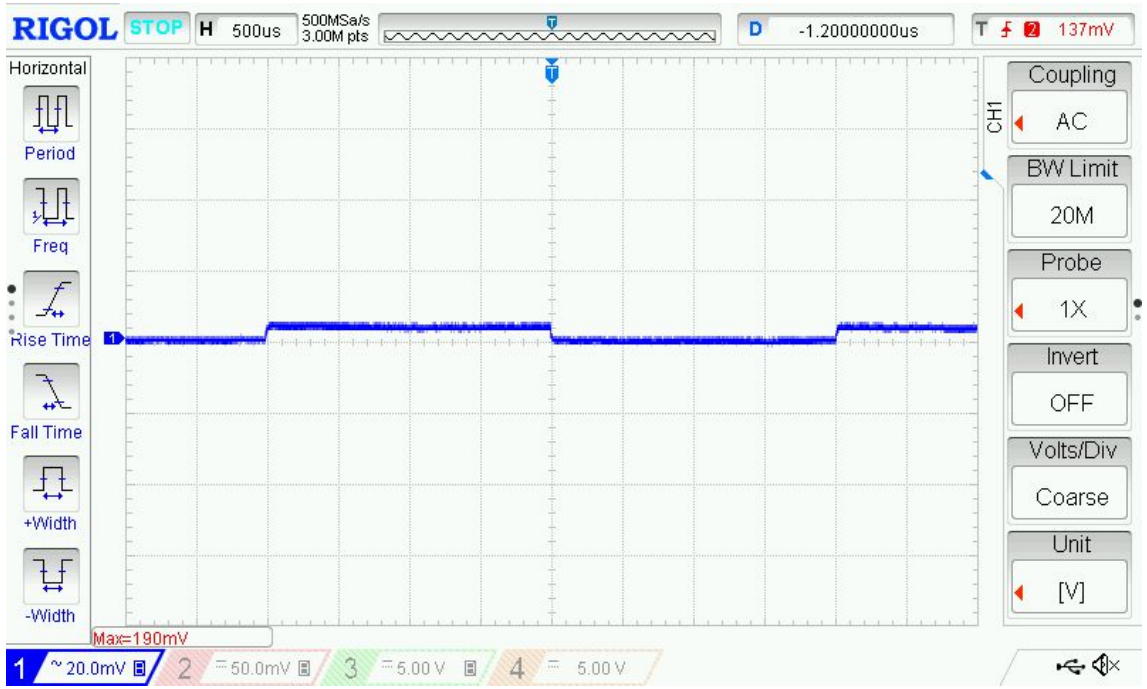


No Load
V_{PP} = 6 mV

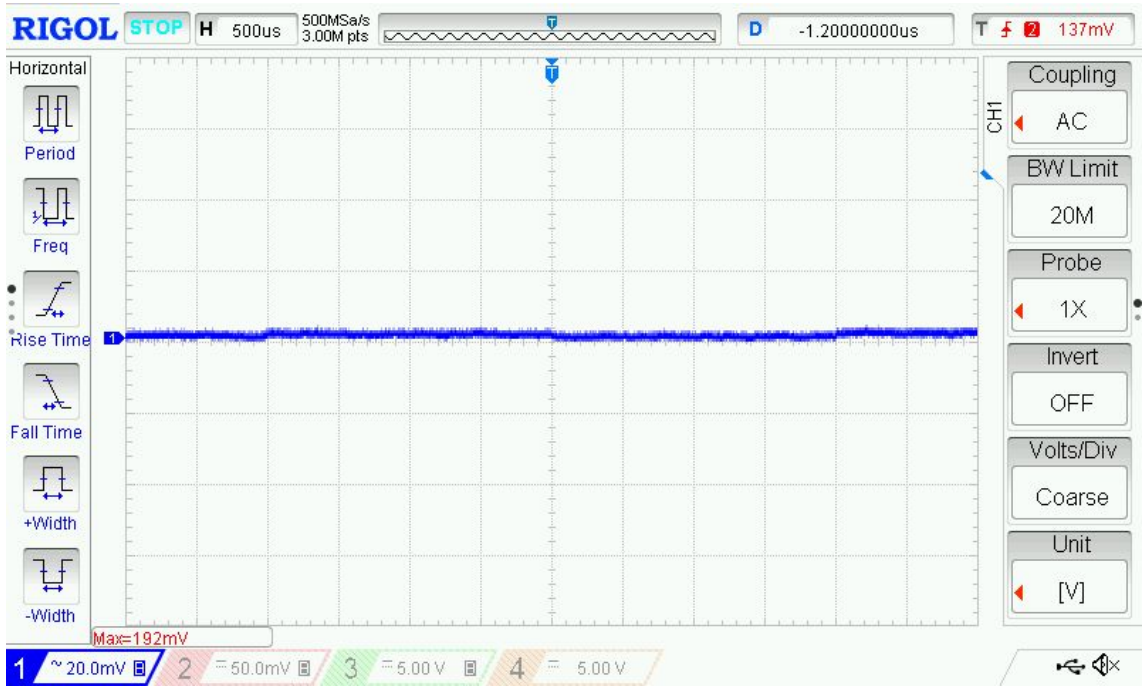


Full Load
V_{PP} = 5.2 mV

VCCO_PSDDR: Transient



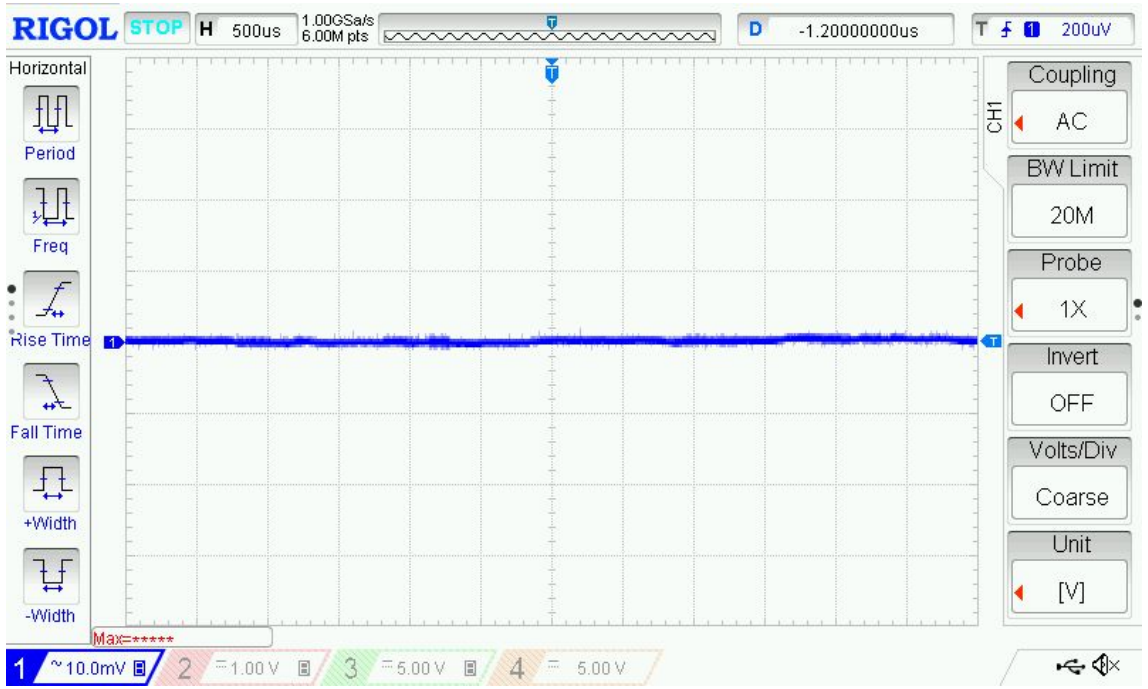
Internal

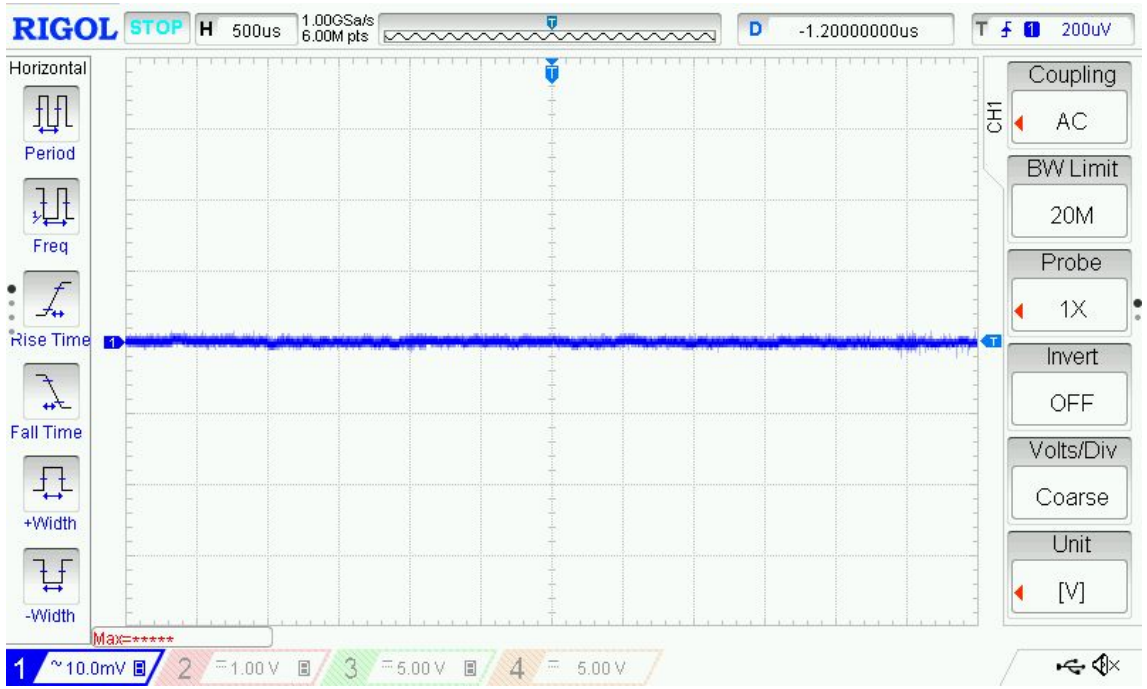


External

Vout = 1.5 V
Transient 0.25 A to 0.5 A
V_{PP} = 17.2 mV
Cout = 22uF

VCCO_PSDDR: Ripple





No Load

Cout = 22uF

0.5 A Load

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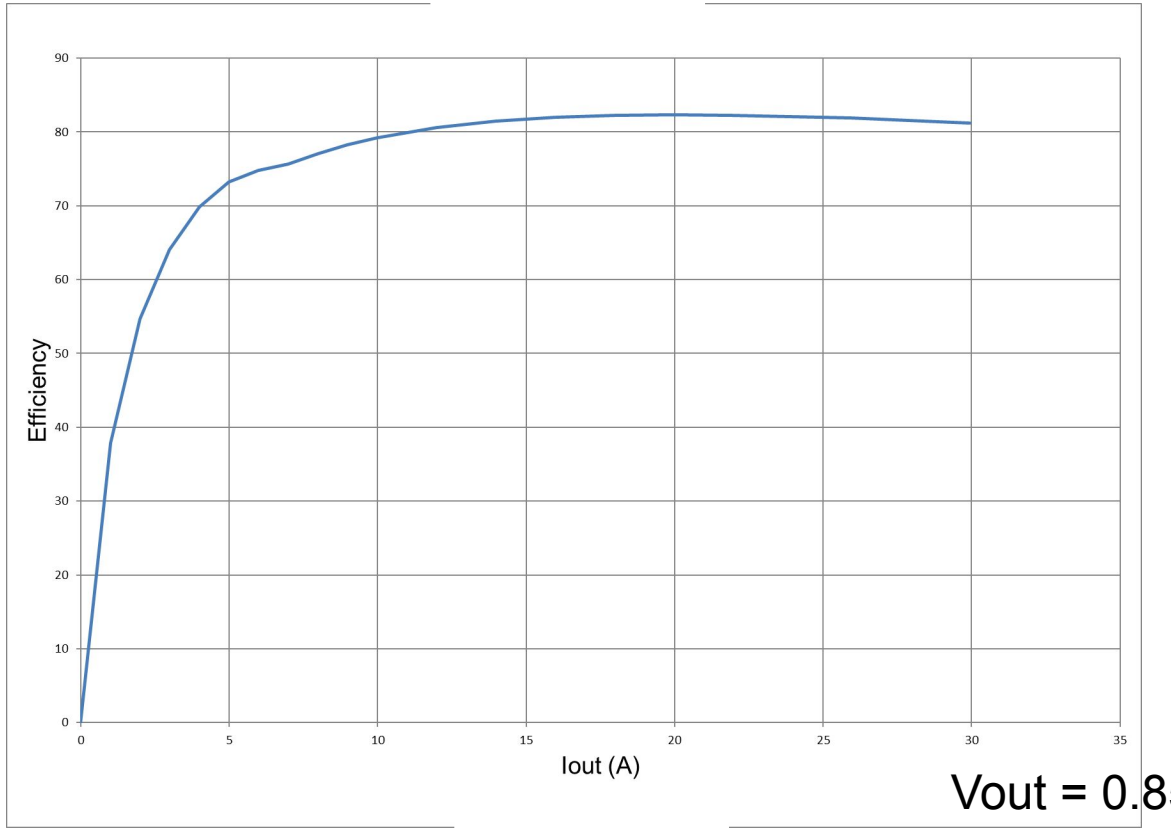
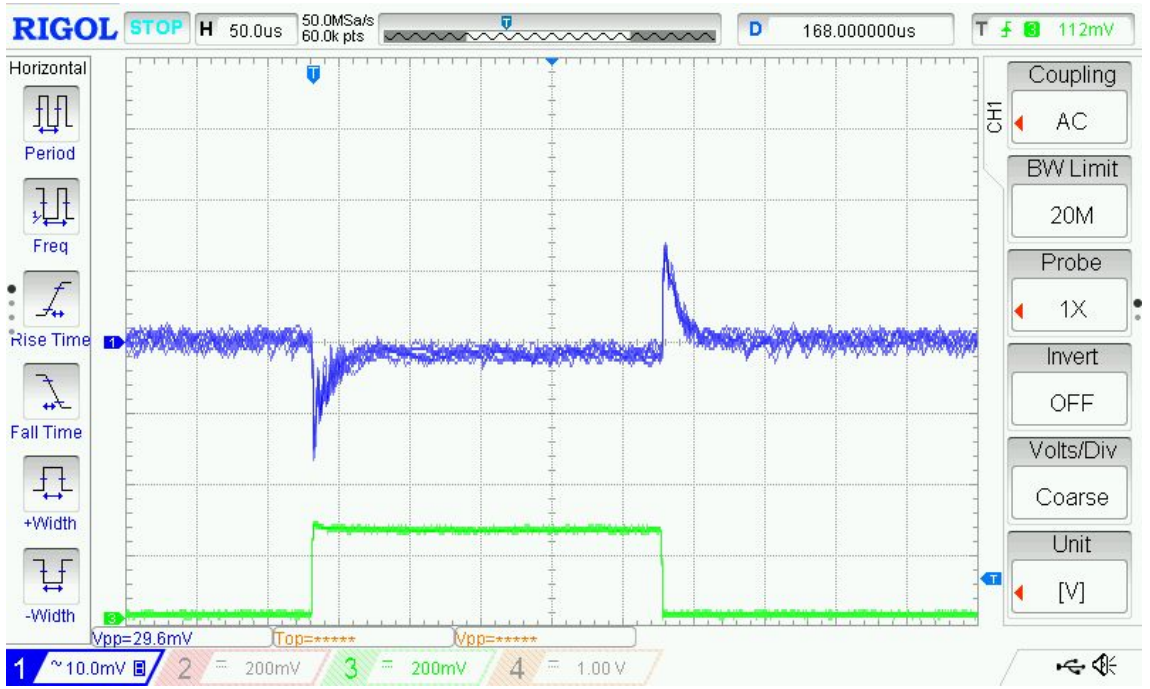
VCCINT: Efficiency & Transient





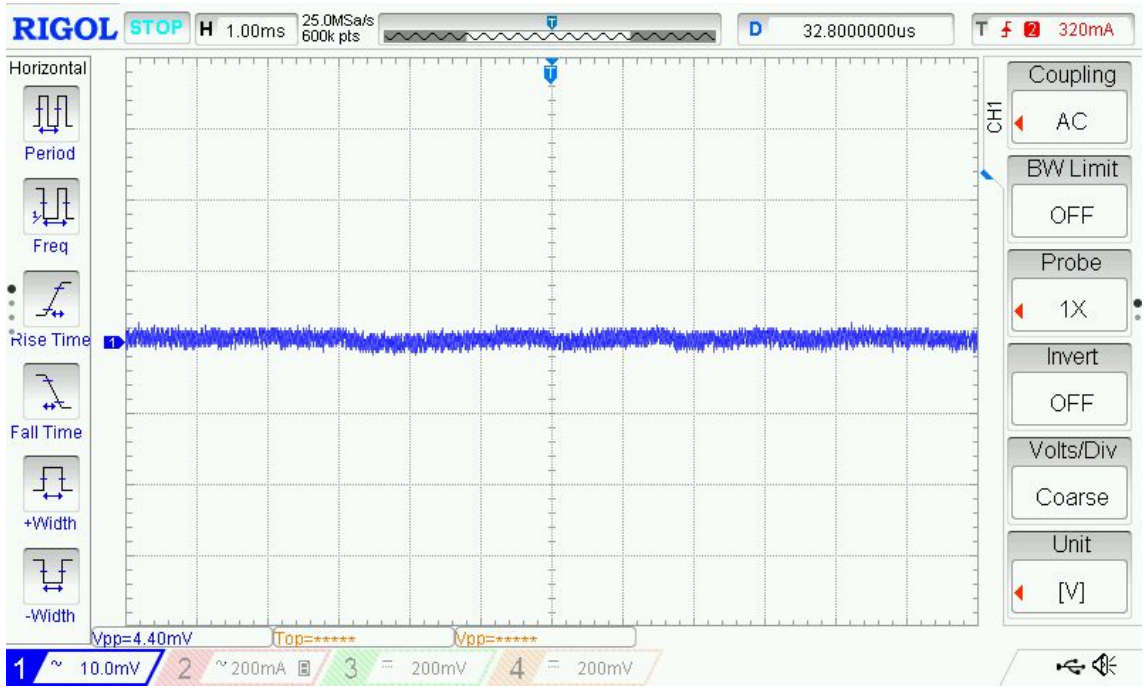
Vout = 0.85 V

Transient 22.5A to 30 A

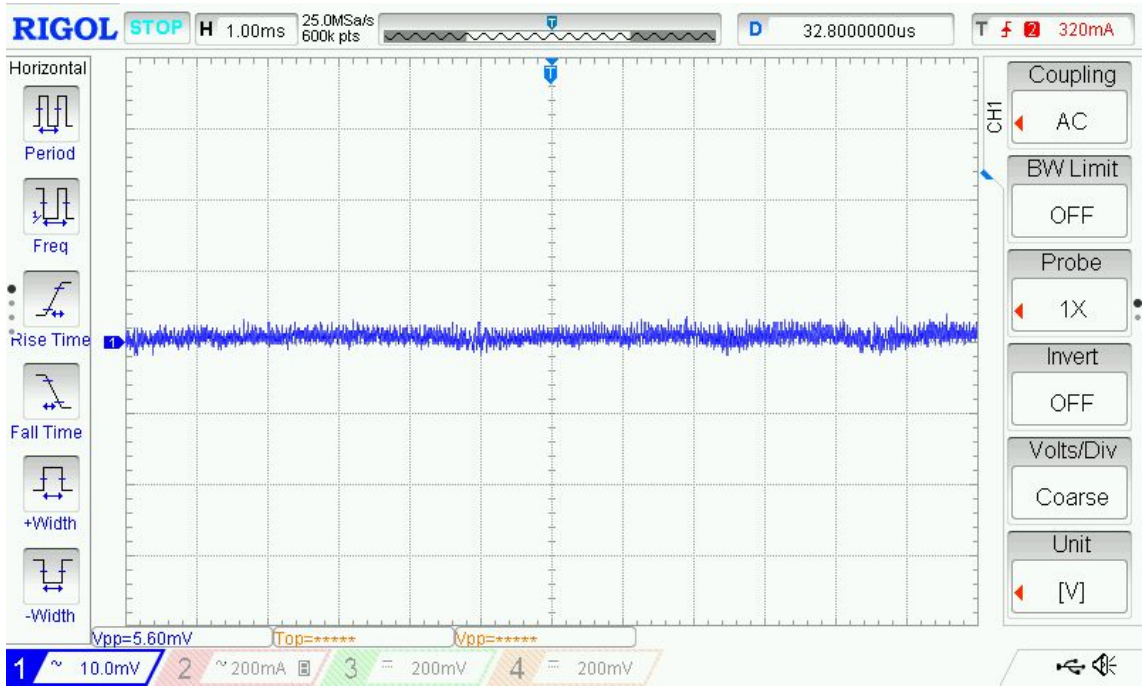
V_{PP} = 29.6 mV

Cout = 910 uF

VCCINT: Ripple



No Load
V_{PP} = 4.4 mV



Full Load
V_{PP} = 5.6 mV

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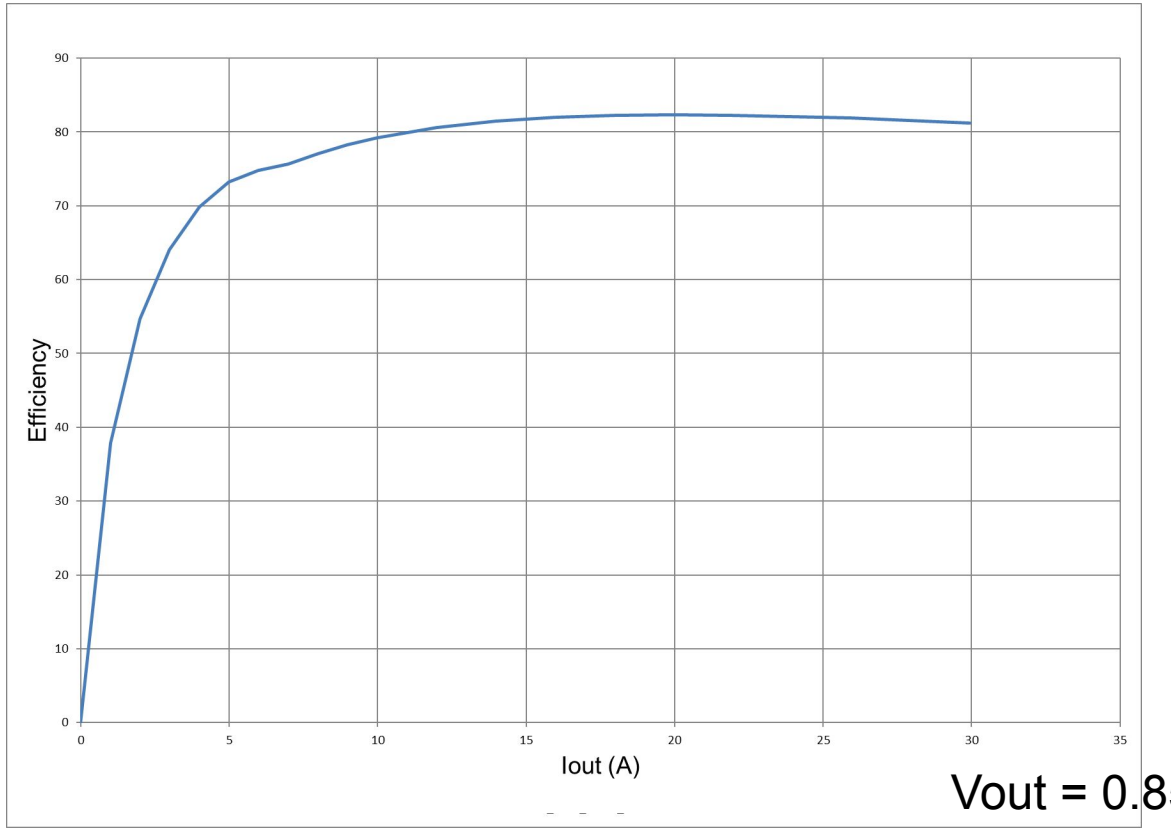
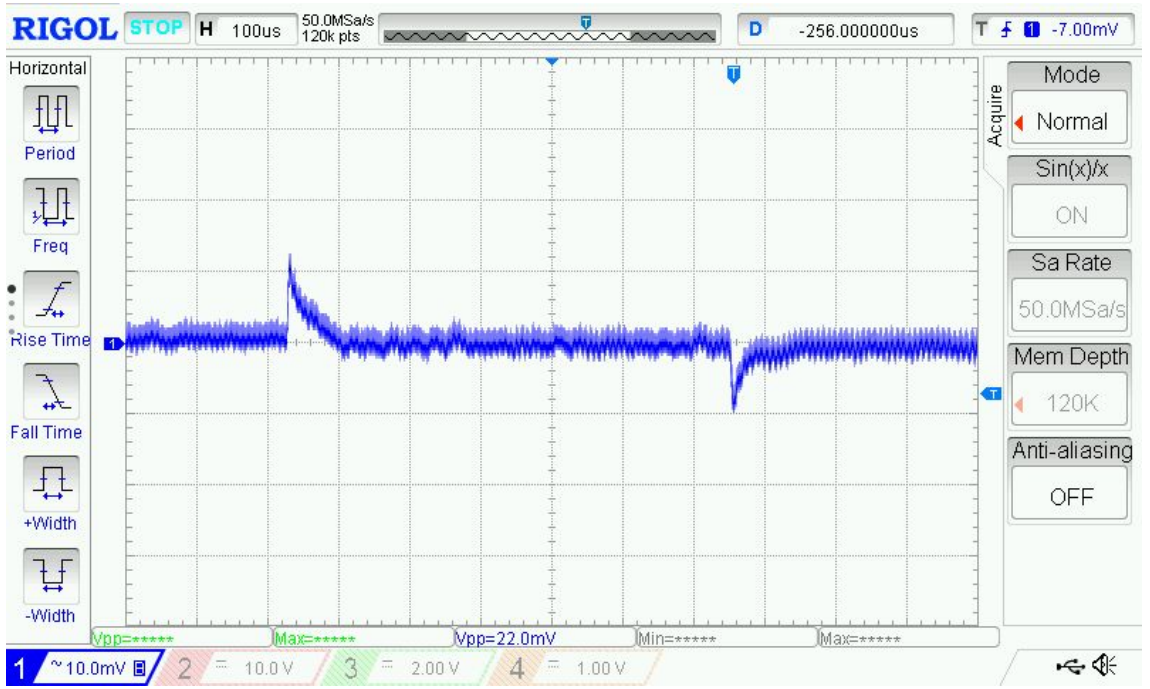
VCCINT_VCU: Efficiency & Transient





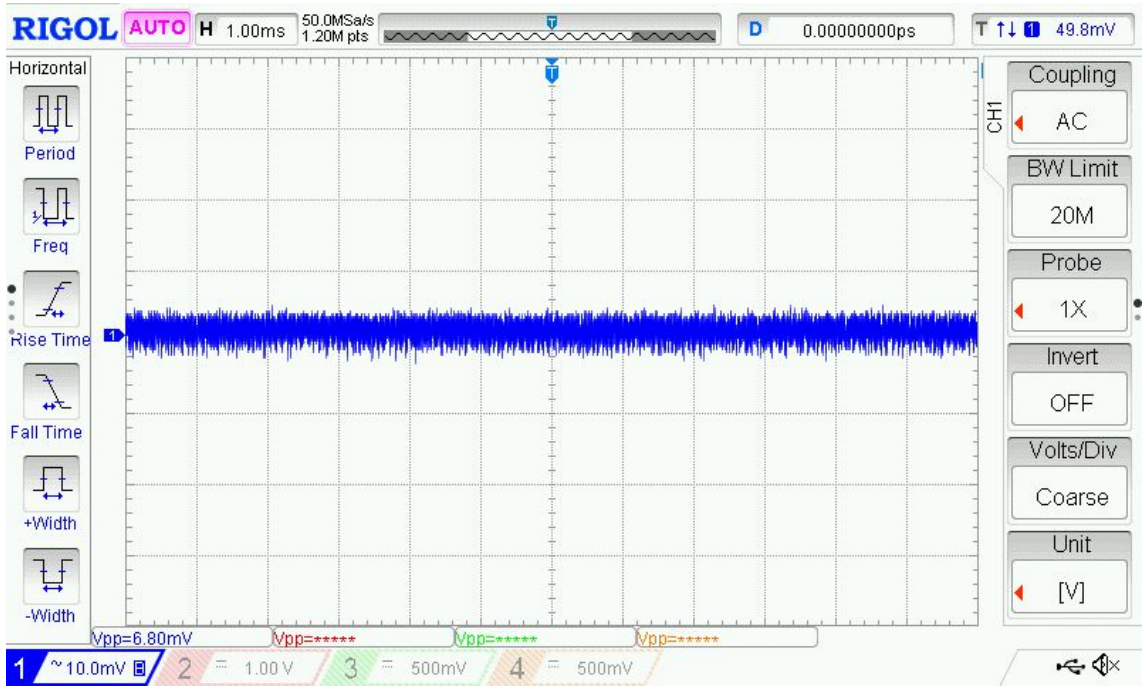
Vout = 0.85 V

Transient 2.625 A to 3.5 A

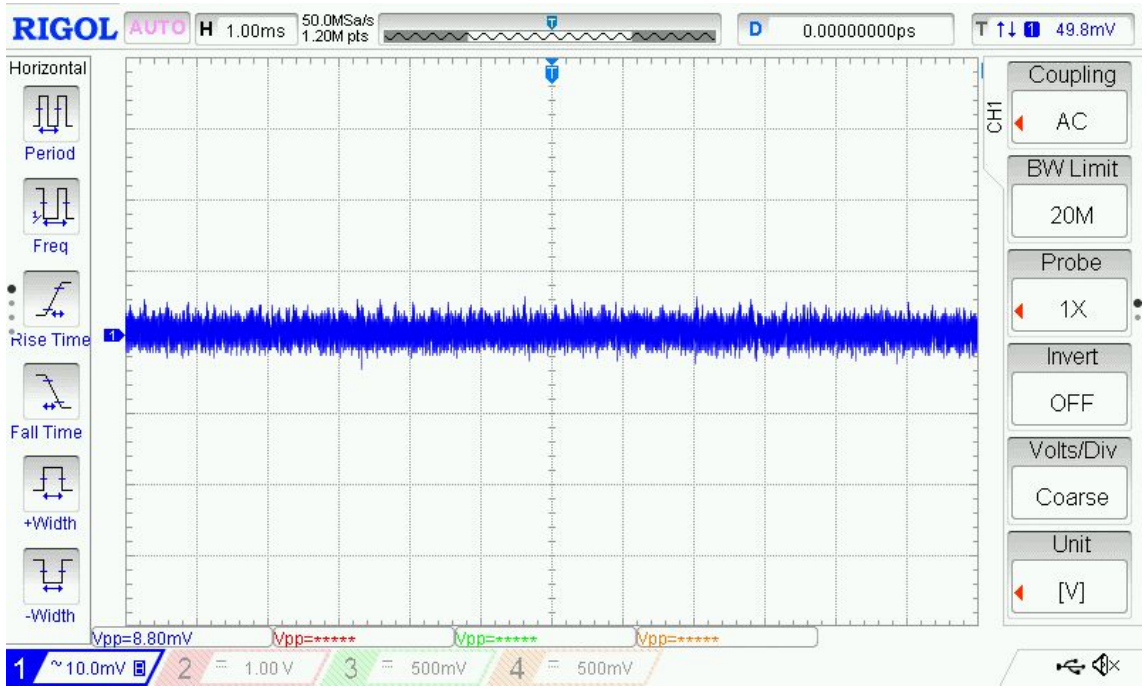
V_{PP} = 22 mV

Cout = 9 x 47 uF

VCCINT_VCU: Ripple

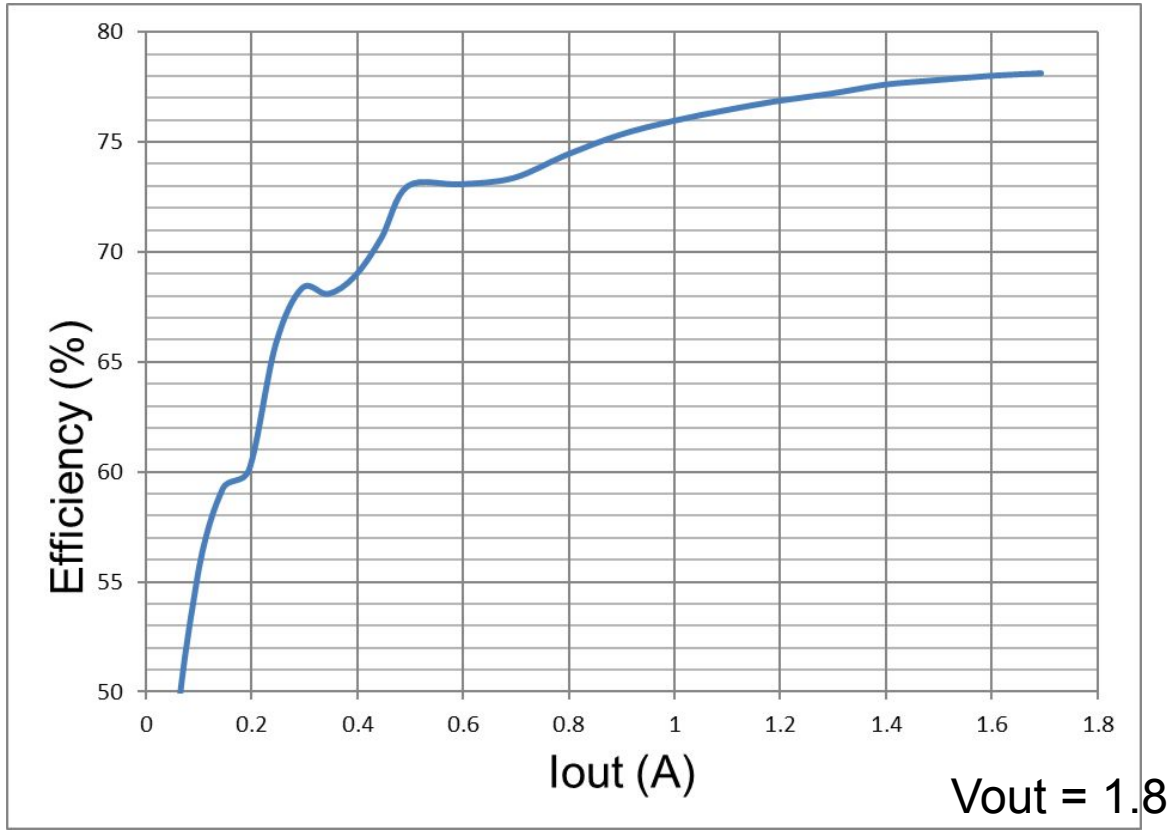


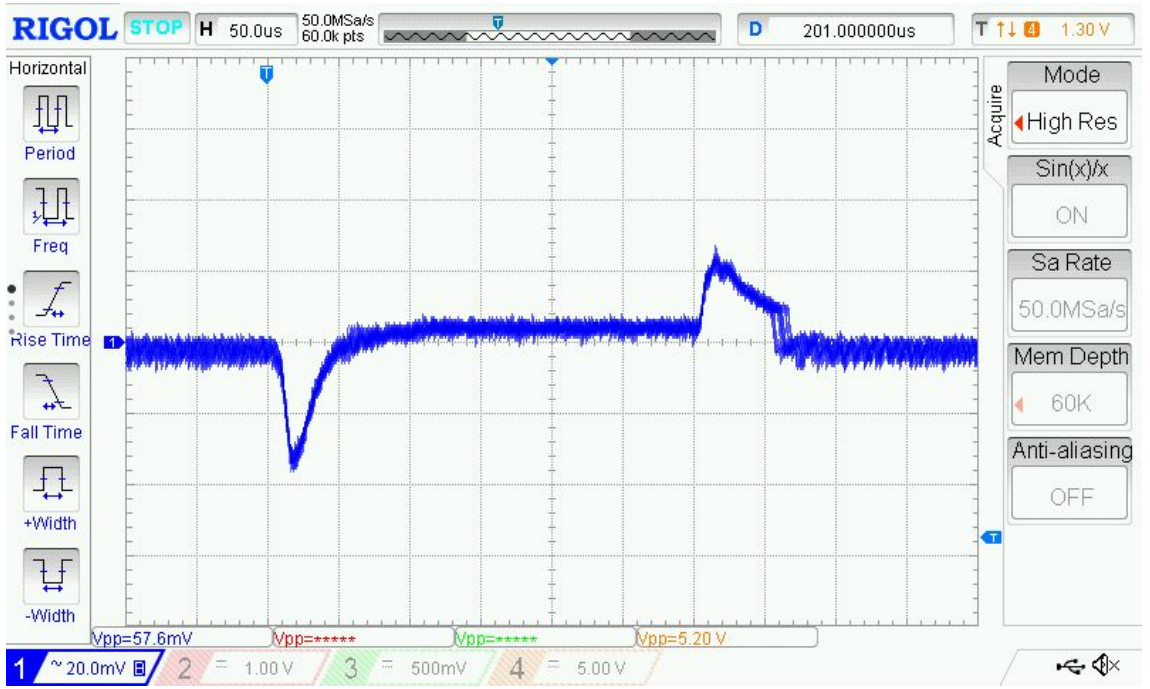
No Load
V_{PP} = 6.8 mV



Full Load
V_{PP} = 8.8 mV

HPIO_VCCO: Efficiency & Transient

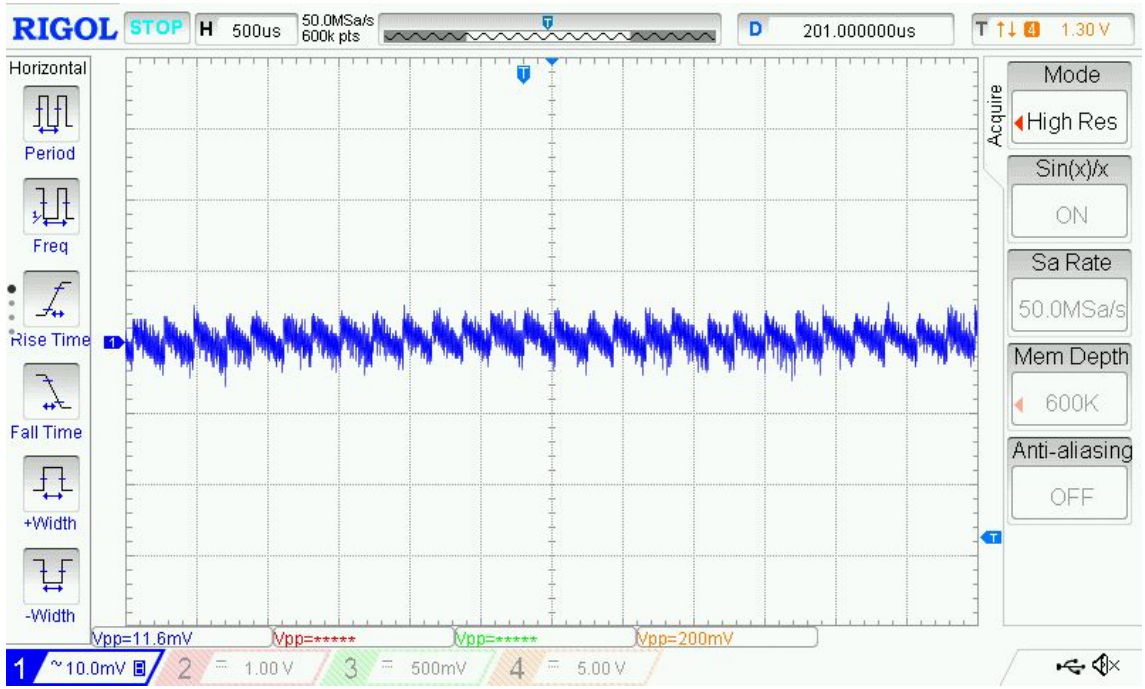




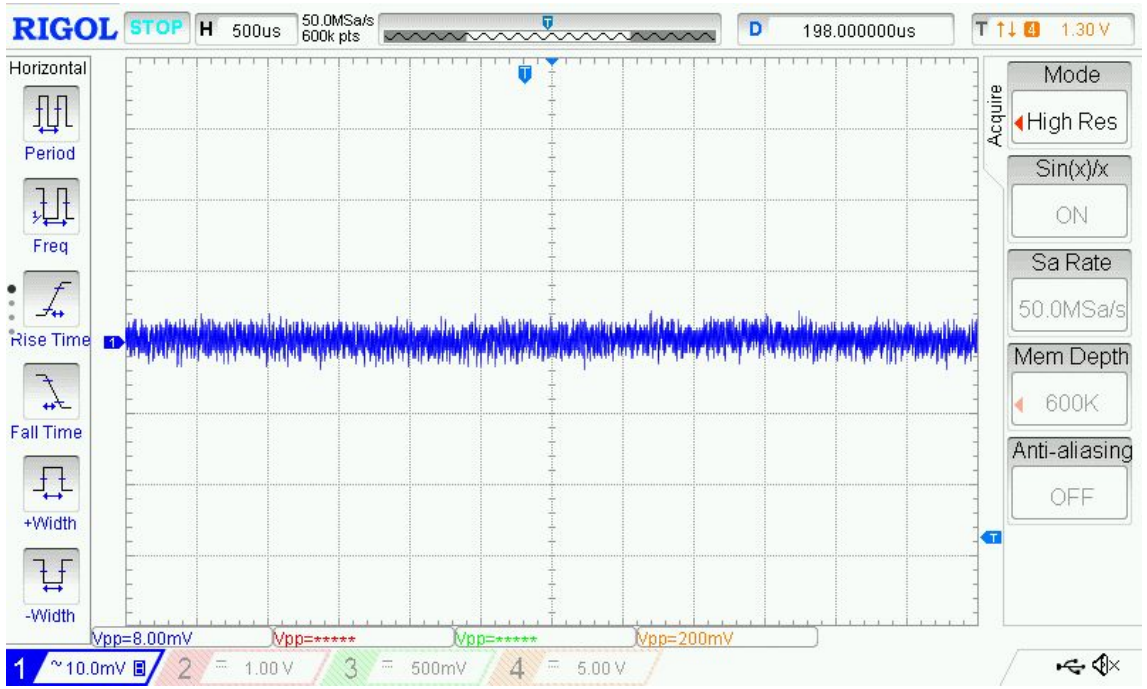
Vout = 1.8 V
Transient 0.16 A to 1.8 A
V_{PP} = 57.6 mV
Cout = 2 x 47 uF

AnDAPT

HPIO_VCCO: Ripple

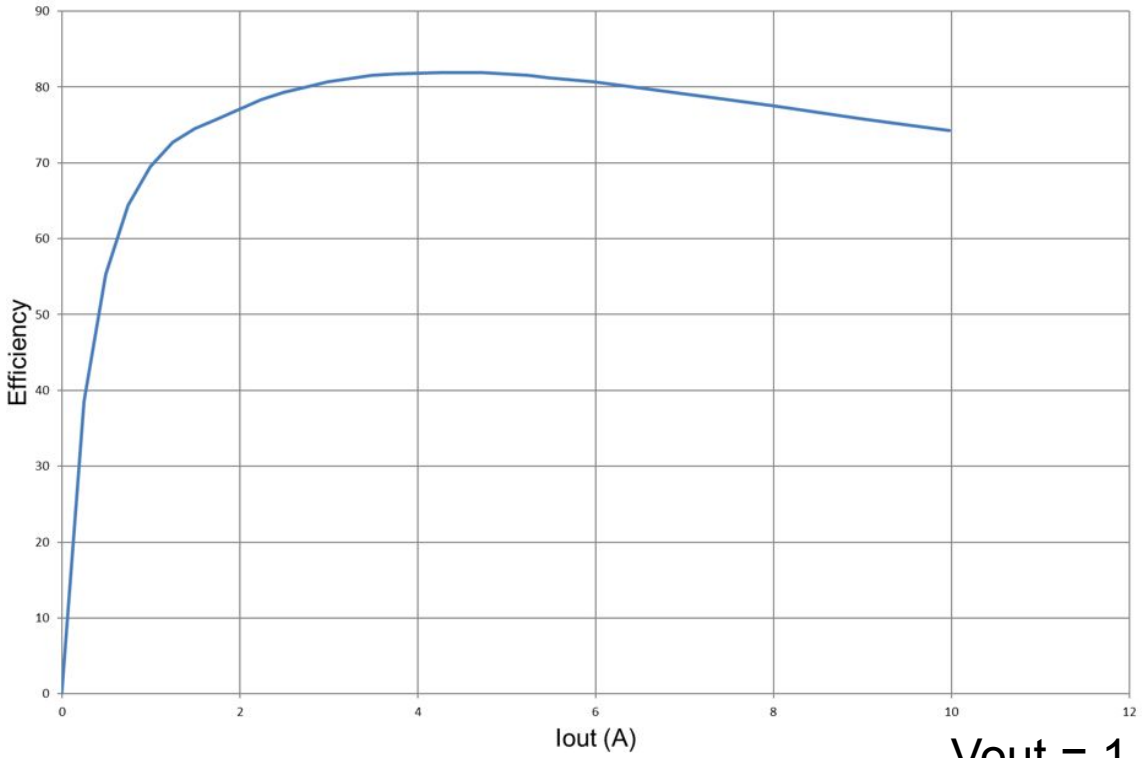


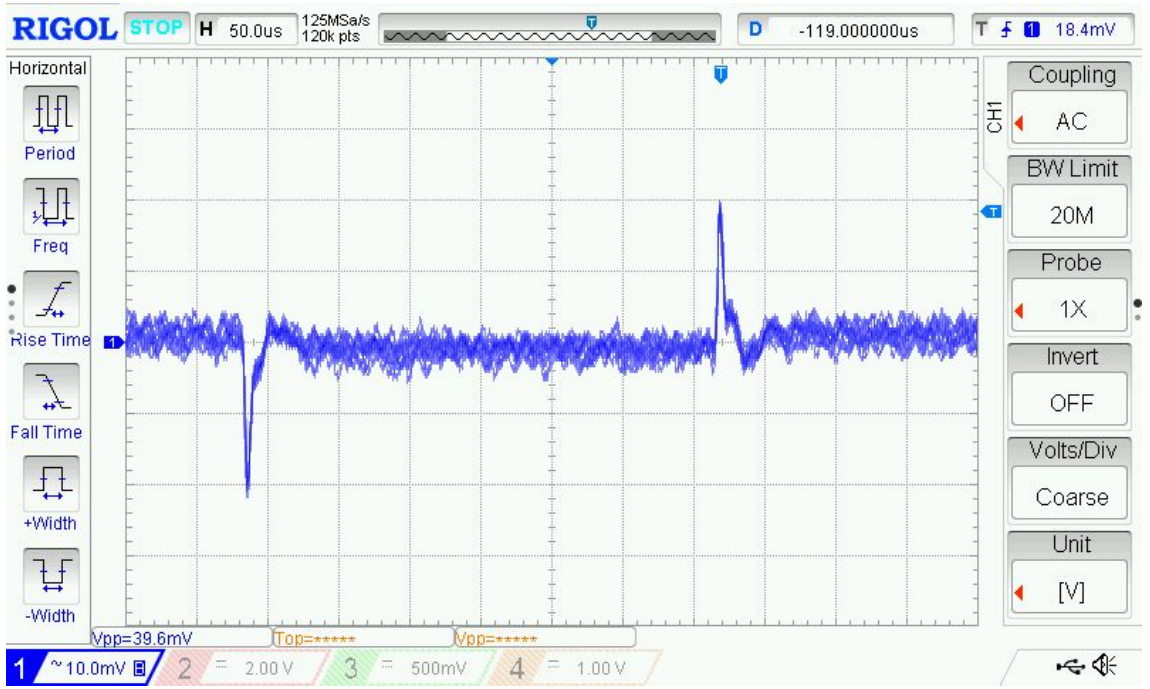
No Load
V_{PP} = 11.6 mV



Full Load
V_{PP} = 8 mV

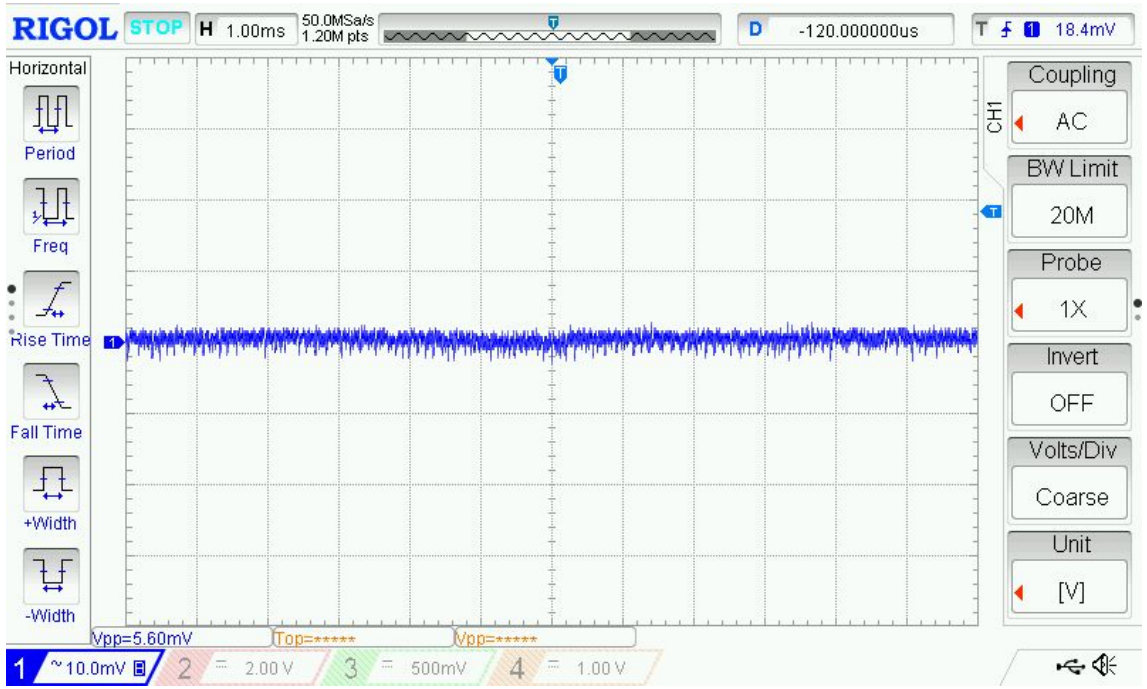
VMGTAVTT: Efficiency & Transient



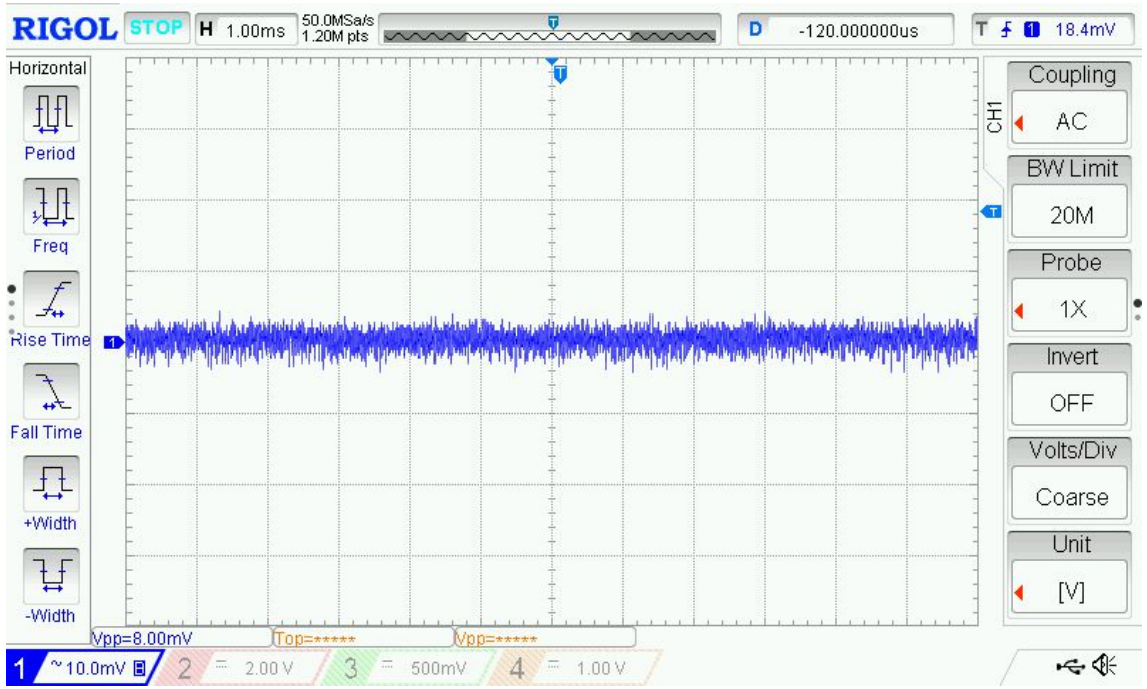


Vout = 1.2 V
Transient 7.5 A to 10 A
V_{PP} = 39.8 mV
Cout = 7 x 47 uF

VMGTAVTT: Ripple

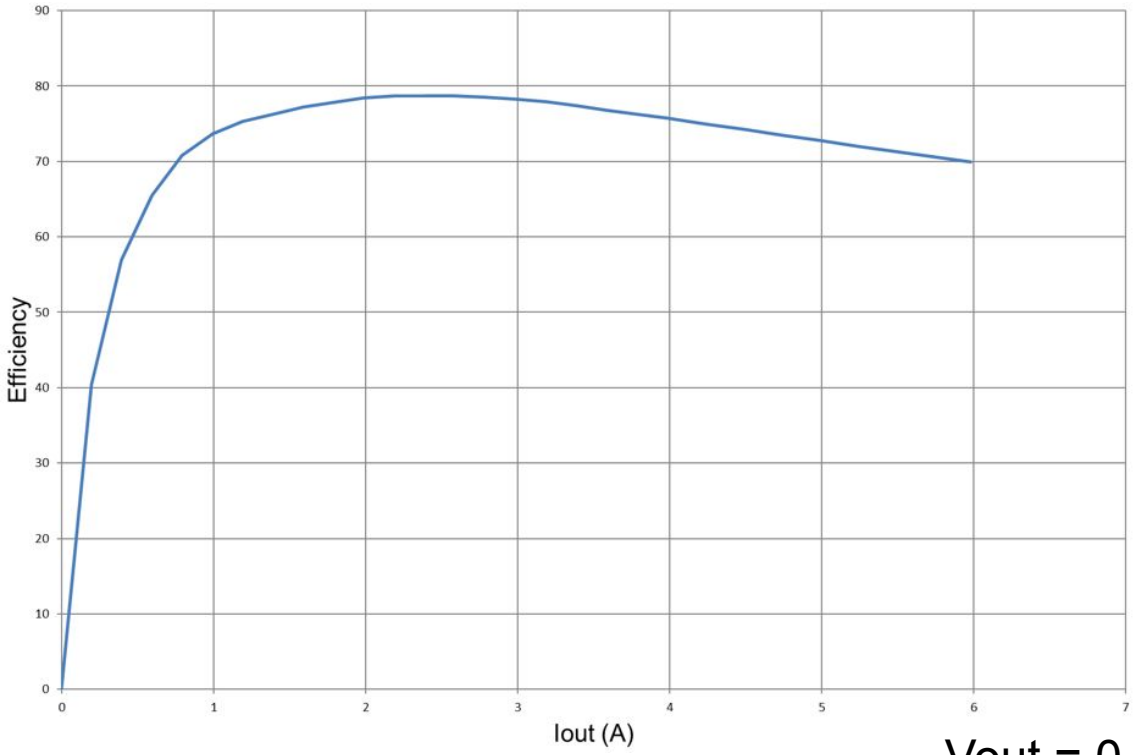


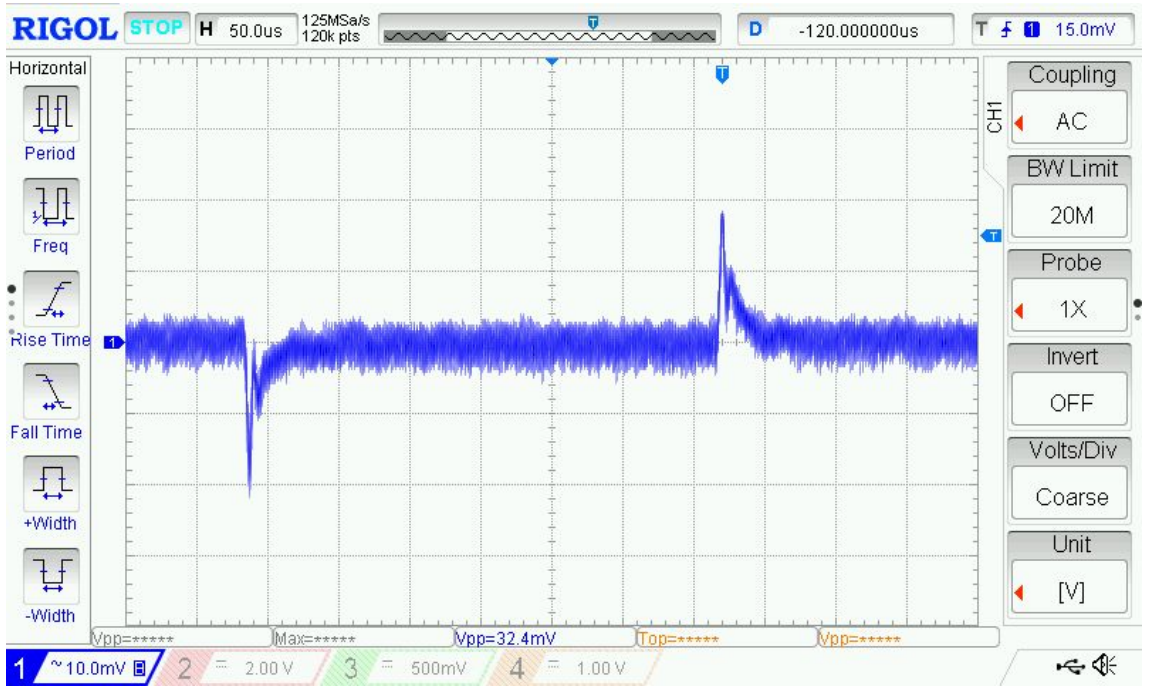
No Load
V_{PP} = 5.6 mV



Full Load
V_{PP} = 8 mV

VMGTAVCC: Efficiency & Transient





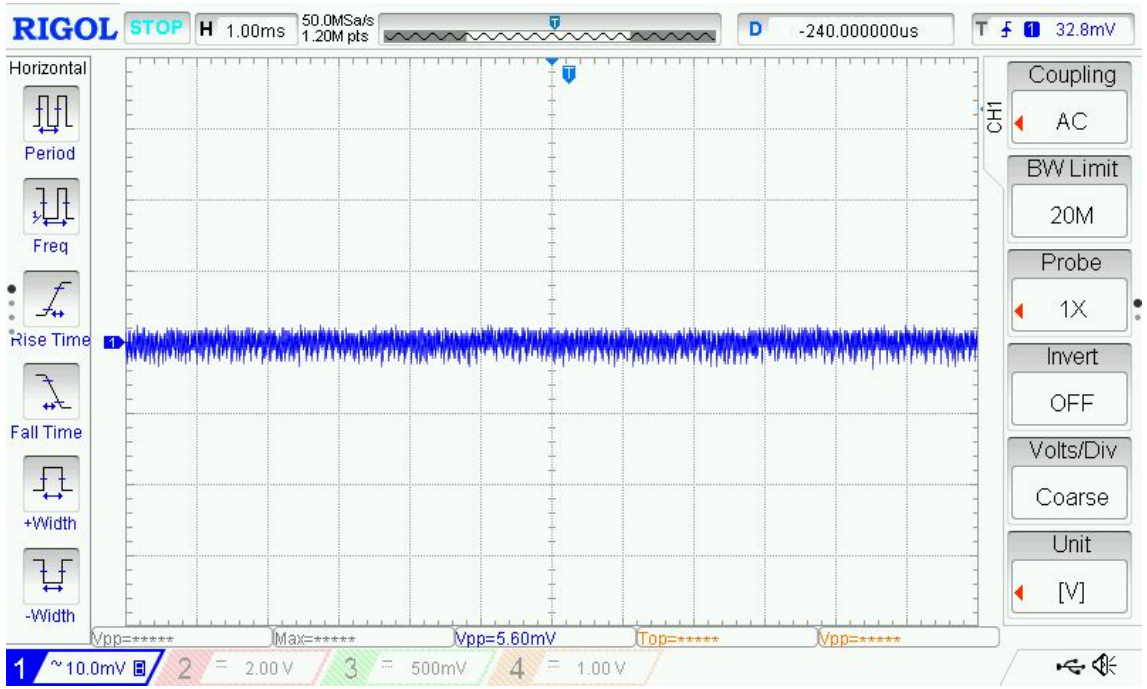
Vout = 0.9 V

Transient 4.5 A to 6 A

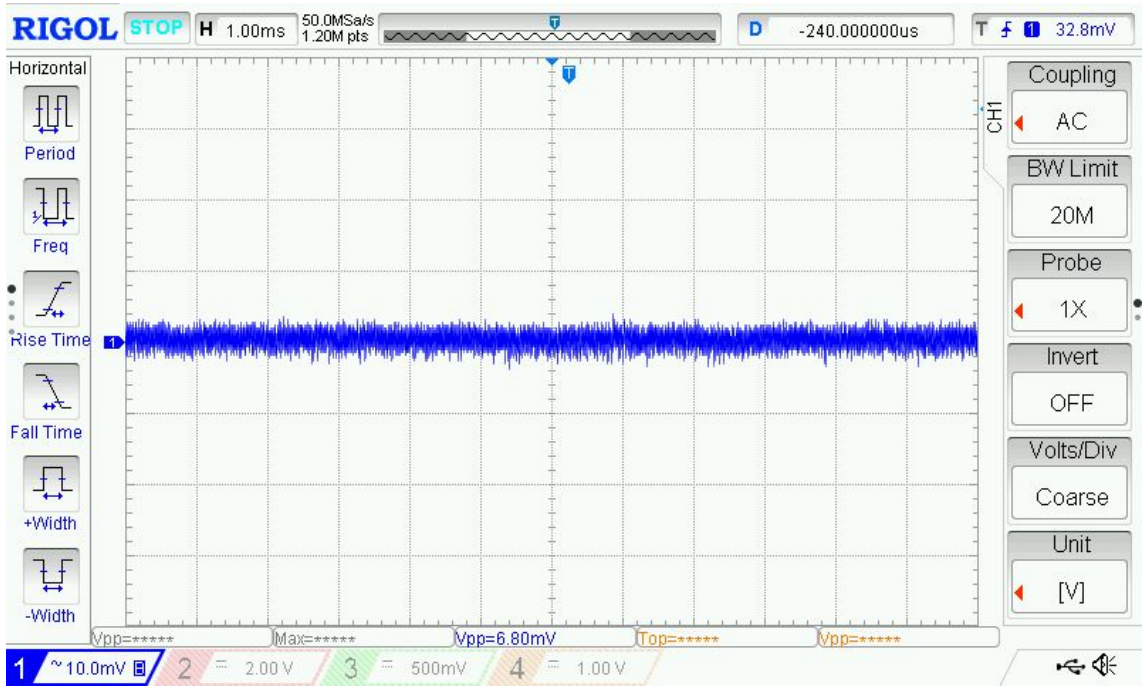
V_{PP} = 32.4 mV

Cout = 6 x 47 uF

VMGTAVCC: Ripple



No Load
V_{PP} = 5.6 mV



Full Load
V_{PP} = 6.8 mV

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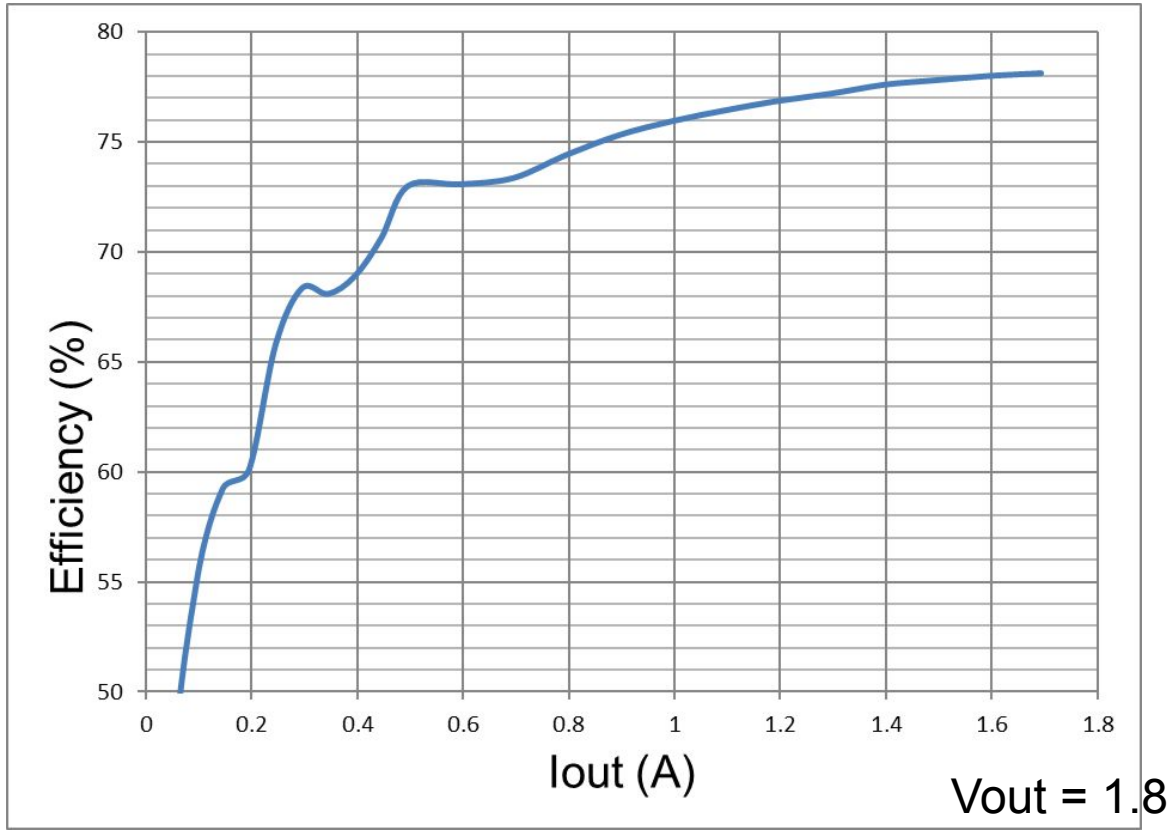
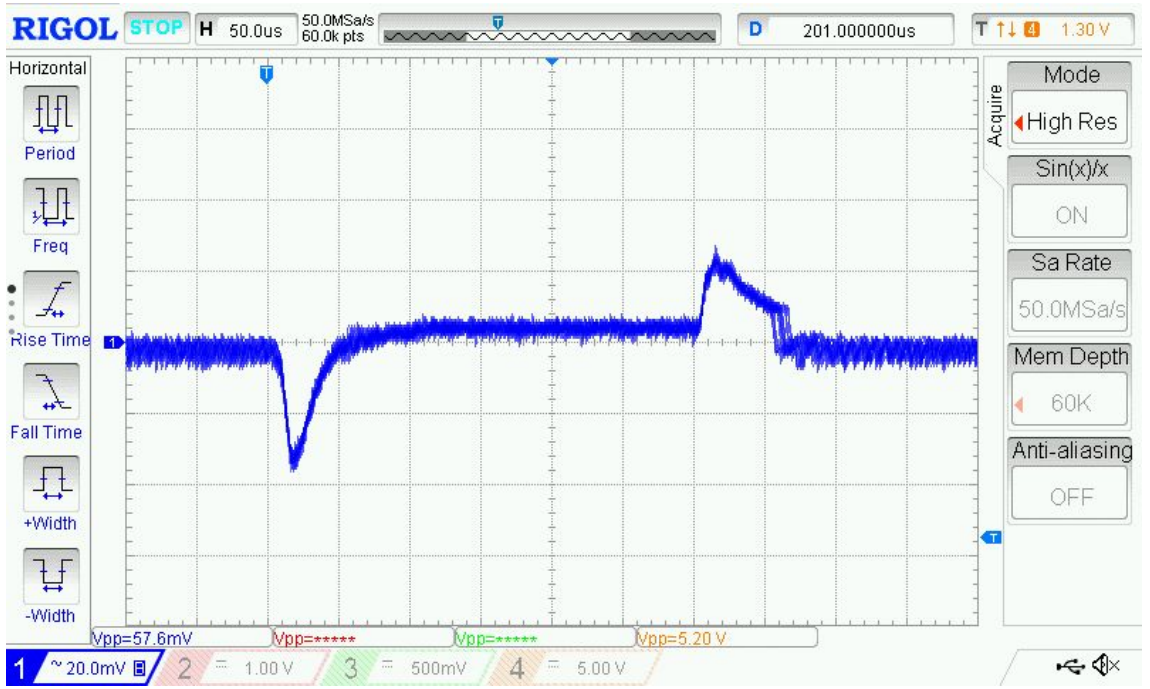
HDIO_VCCO: Efficiency & Transient

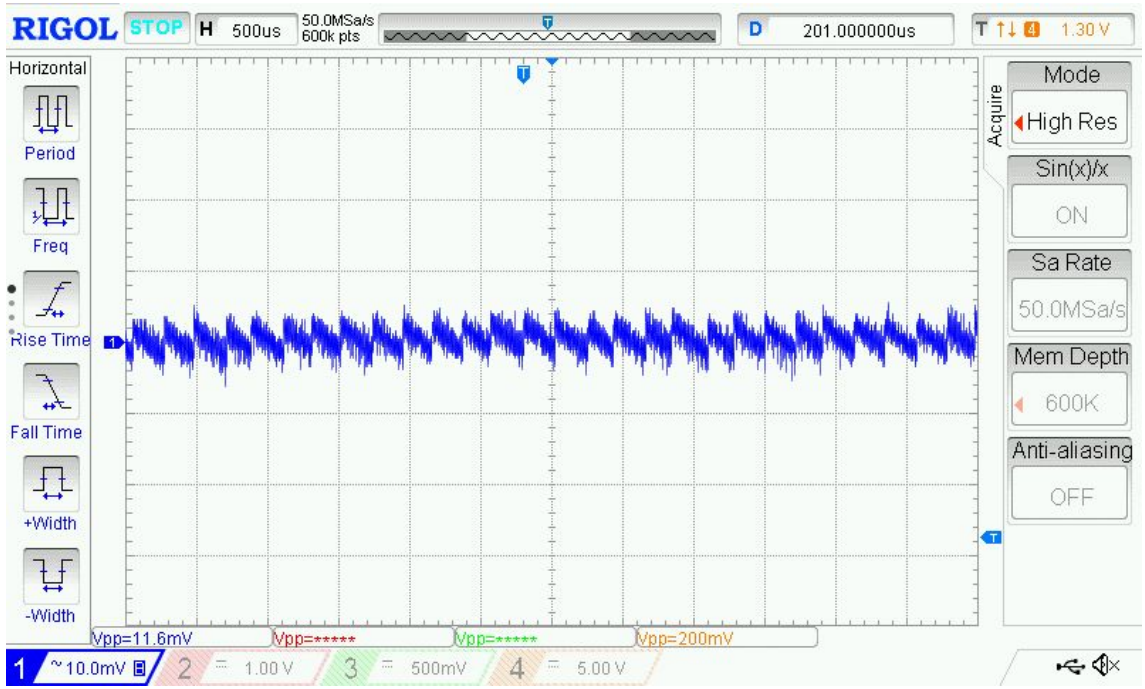




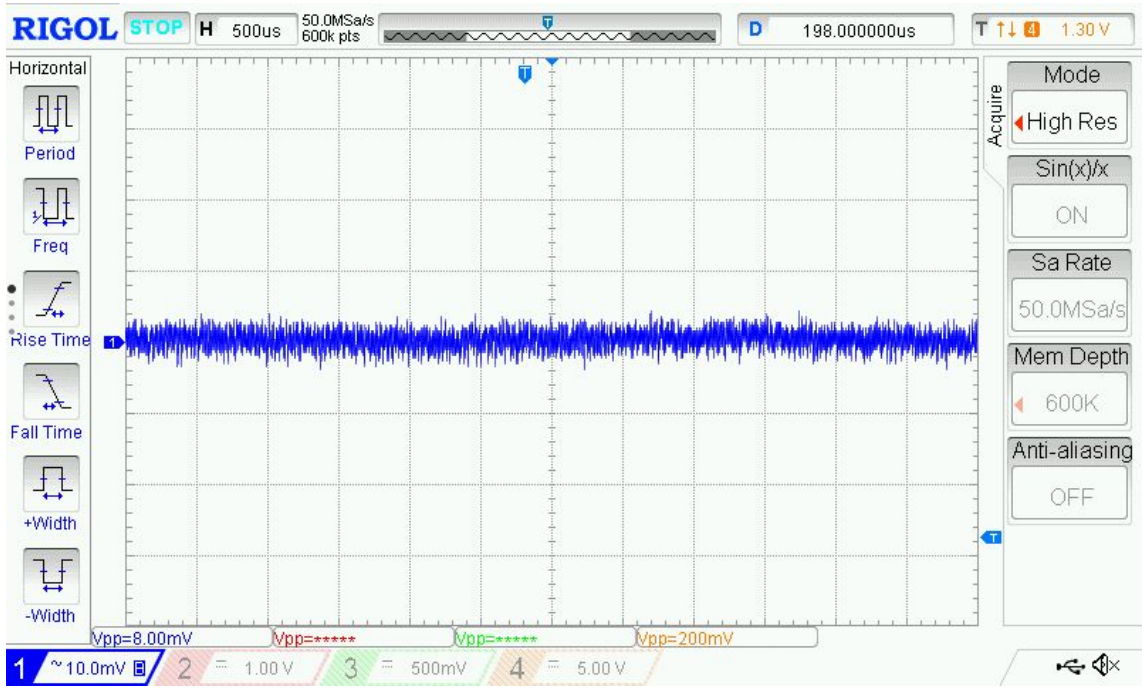
Vout = 1.8 V
Transient 0.18 A to 1.6 A
V_{PP} = 57.6 mV
Cout = 2 x 47 uF

AnDAPT

HDIO_VCCO: Ripple



No Load
V_{PP} = 11.6 mV



Full Load
V_{PP} = 8 mV

AnDAPT

Thank You

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