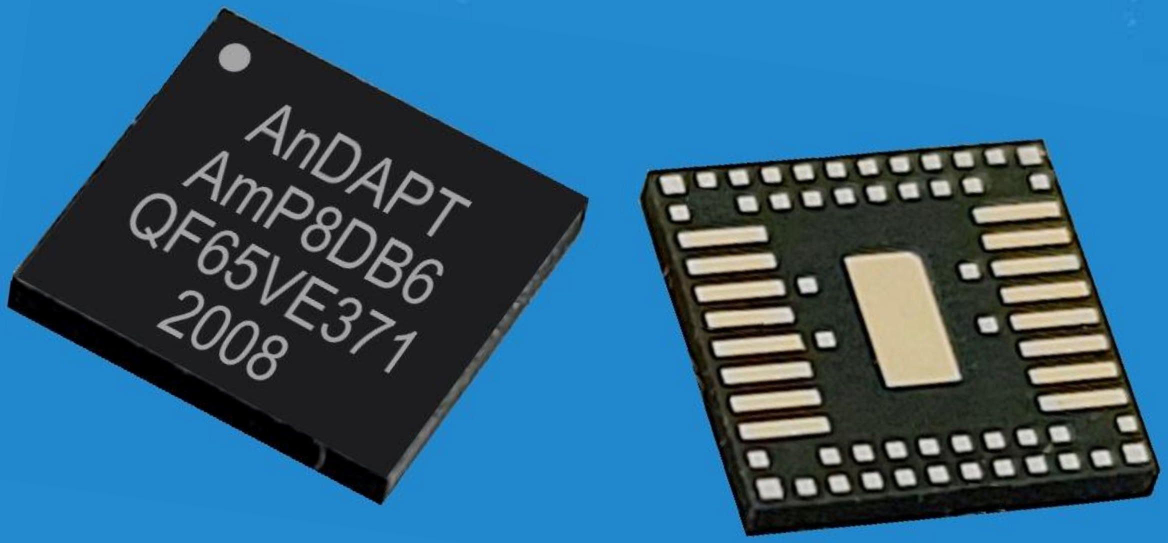

AnDAPT Power Solutions for Xilinx

Zynq Ultrascale+ RFSoC Mapping & Lab Data

Use-Case A1, B1, B2

AnDAPT Marketing Team

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Contents

- Xilinx Zynq Ultrascale+ (ZU+) family of RFSoC devices’ use-cases
- AnDAPT integrated power supply reference design availability for ZU+ RFSOC SKUs
- Lab data for each power rail for Full Power Domain (A2) use-case using AnDAPT PMICs

Use-Cases (RFSoC Devices)

SKU	USE CASE	USE CASE
ZU21DR ZU25DR ZU27DR ZU28DR ZU29DR	GEN 1 MANDATORY POWER	GEN 1 FULL POWER
ZU39DR	GEN 2 MANDATORY POWER	GEN 2 FULL POWER
ZU42DR ZU43DR ZU46DR ZU47DR ZU48DR ZU49DR	GEN 3 MANDATORY POWER	GEN 3 FULL POWER

Power Tree- Use-Case: A1

V_{IN} = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC
1	VCCINT	1	C870	DrMOS Ctrl 2-ph	V_{IN}	12	0.72/0.85	45	ARD_X_ZUR_A1_IC1
2	VCCBRAM, INT_IO, INT_AMS, SDFEC	2	C860	DrMOS Ctrl 1-ph	V_{IN}	12	0.85	28	ARD_X_ZUR_A1_IC1
3	VMGTAVTT, VCC_PSPLL, VCU_PLL	2	C200	Sync Buck	V_{IN}	12	1.2	4	ARD_X_ZUR_A1_IC1
4	MGTAVCC	2	C200	Sync Buck	V_{IN}	12	0.9	2	ARD_X_ZUR_A1_IC1
5	VPS_MGTRAVCC	3	C710	SIM LDO	MGTAVCC	0.9	0.85	0.3	ARD_X_ZUR_A1_IC1
6	VCCO_PSDDR, DDR_VDDQ	6	C200	Sync Buck	V_{IN}	12	1.1-1.5	6	ARD_X_ZUR_A1_IC2
7	VCCAUX, ADC, IO, VCCPSAUX, DDR_PLL, ADC	5	C200	Sync Buck	V_{IN}	12	1.8	2-3	ARD_X_ZUR_A1_IC2
8	VCCO	6	C200	Sync Buck	V_{IN}	12	3.3/5	4	ARD_X_ZUR_A1_IC2
9	VPS_MGTAVTT, VMGTVAUX	4	C200	Sync Buck	V_{IN}	12	1.8	0.5	ARD_X_ZUR_A1_IC2

Power Tree- Use-Case: B2

V_{IN} = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC	Comment
1	VCCINT	1	C870	DrMOS Ctrl 2-ph	V_{IN}	12	0.72/0.85	45	ARD_X_ZUR_B1_IC1	
2	VCCBRAM, INT_IO, INT_AMS, SDFEC	2	C860	DrMOS Ctrl 1-ph	V_{IN}	12	0.85	28	ARD_X_ZUR_B1_IC1	
3	VMGTAVTT, VCC_PSPLL, VCU_PLL	2	C200	Sync Buck	V_{IN}	12	1.2	4	ARD_X_ZUR_B1_IC1	
4	MGTAVCC	2	C200	Sync Buck	V_{IN}	12	0.9	2	ARD_X_ZUR_B1_IC1	
5	VPS_MGTRAVCC	3	C710	SIM LDO	MGTAVCC	0.9	0.85	0.3	ARD_X_ZUR_B1_IC1	
6	VCCO_PSDDR, DDR_VDDQ	6	C200	Sync Buck	V_{IN}	12	1.1-1.5	6	ARD_X_ZUR_B1_IC2	
7	VCCAUX, ADC, IO, VCCPSAUX, DDR_PLL, ADC	5	C200	Sync Buck	V_{IN}	12	1.8	2-3	ARD_X_ZUR_B1_IC2	
8	VCCO	6	C200	Sync Buck	V_{IN}	12	3.3/5	4	ARD_X_ZUR_B1_IC2	
9	VPS_MGTAVTT, VMGTVAUX	4	C200	Sync Buck	V_{IN}	12	1.8	0.5	ARD_X_ZUR_B1_IC2	
10	ADC_AVCC	8	C200	Sync Buck	V_{IN}	12	0.925/0.98	3.2	ARD_X_ZUR_B1_IC3	Optional for Gen1/Gen2/Gen3
11	DAC_AVCC	9	C200	Sync Buck	V_{IN}	12	0.925	6	ARD_X_ZUR_B1_IC3	
12	ADC_AVCCAUX	7	C150	Async Buck	V_{IN}	12	1.8	1.5	ARD_X_ZUR_B1_IC3	
13	DAC_AVCCAUX	11	C710	SIM LDO	DAC_AVTT	2.5	1.8	0.72	ARD_X_ZUR_B1_IC3	
14	DAC_AVTT	10	C200	Sync Buck	V_{IN}	12	2.5/3/3.3	0.9	ARD_X_ZUR_B1_IC3	

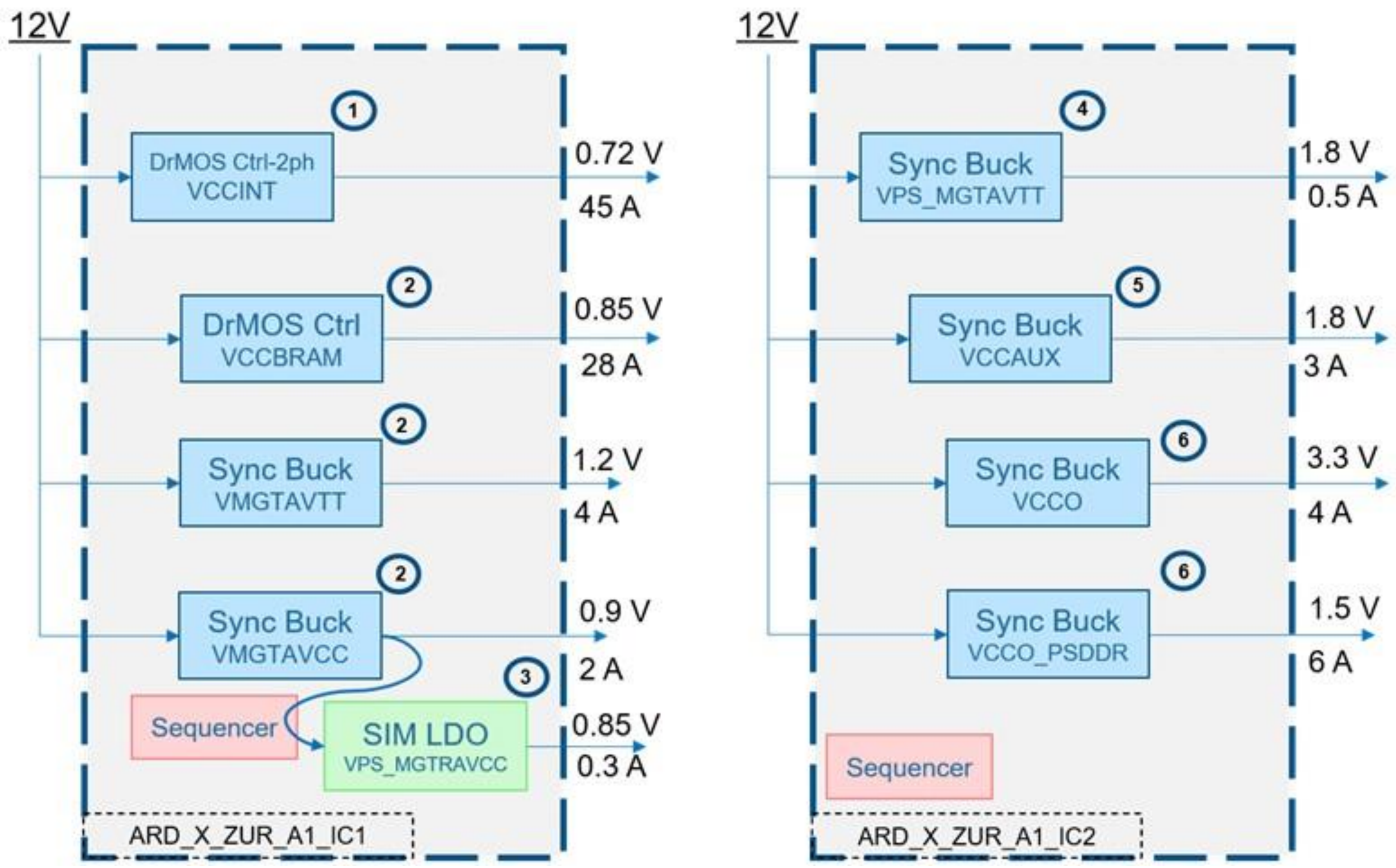
Power Tree- Use-Case: B2

V_{IN} = 12 V

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	IC	Comment
1	VCCINT	1	C870	DrMOS Ctrl 2-ph	V_{IN}	12	0.72/0.85	45	ARD_X_ZUR_B2_IC1	
2	VCCBRAM, INT_IO, INT_AMS, SDFEC	2	C860	DrMOS Ctrl 1-ph	V_{IN}	12	0.85	28	ARD_X_ZUR_B2_IC1	
3	VMGTAVTT, VCC_PSPLL, VCU_PLL	2	C200	Sync Buck	V_{IN}	12	1.2	4	ARD_X_ZUR_B2_IC1	
4	MGTAVCC	2	C200	Sync Buck	V_{IN}	12	0.9	2	ARD_X_ZUR_B2_IC1	
5	VPS_MGTRAVCC	3	C710	SIM LDO	MGTAVCC	0.9	0.85	0.3	ARD_X_ZUR_B2_IC1	
6	VCCO_PSDDR, DDR_VDDQ	6	C200	Sync Buck	V_{IN}	12	1.1-1.5	6	ARD_X_ZUR_B2_IC2	
7	VCCAUX, ADC, IO, VCCPSAUX, DDR_PLL, ADC	5	C200	Sync Buck	V_{IN}	12	1.8	2-3	ARD_X_ZUR_B2_IC2	
8	VCCO	6	C200	Sync Buck	V_{IN}	12	3.3/5	4	ARD_X_ZUR_B2_IC2	
9	VPS_MGTAVTT, VMGTVAUX	4	C200	Sync Buck	V_{IN}	12	1.8	0.5	ARD_X_ZUR_B2_IC2	
10	ADC_AVCC	8	C200	Sync Buck	V_{IN}	12	0.925/0.98	3.2	ARD_X_ZUR_B2_IC3	Optional for Gen1/Gen2/Gen3
11	DAC_AVCC	9	C200	Sync Buck	V_{IN}	12	0.925	6	ARD_X_ZUR_B2_IC3	
12	ADC_AVCCAUX	7	C150	Async Buck	V_{IN}	12	1.8	1.5	ARD_X_ZUR_B2_IC3	
13	DAC_AVCCAUX	11	C710	SIM LDO	DAC_AVTT	2.5	1.8	0.72	ARD_X_ZUR_B2_IC3	
14	DAC_AVTT	10	C200	Sync Buck	V_{IN}	12	2.5/3/3.3	0.9	ARD_X_ZUR_B2_IC3	
15	PL_DDR4_VTT1	12	C210	Sync Buck	V_{IN}	12	0.6	3	ARD_X_ZUR_B2_IC4	Optional for Gen2/Gen3
16	PL_DDR4_VTT2	13	C210	Sync Buck	V_{IN}	12	0.6	3	ARD_X_ZUR_B2_IC4	
17	PS_DDR4_VTT	14	C210	VTT Terminator	C200	1.2	0.6	1	ARD_X_ZUR_B2_IC4	

Proposed Solution (4xPMICs)

Use-Case A1



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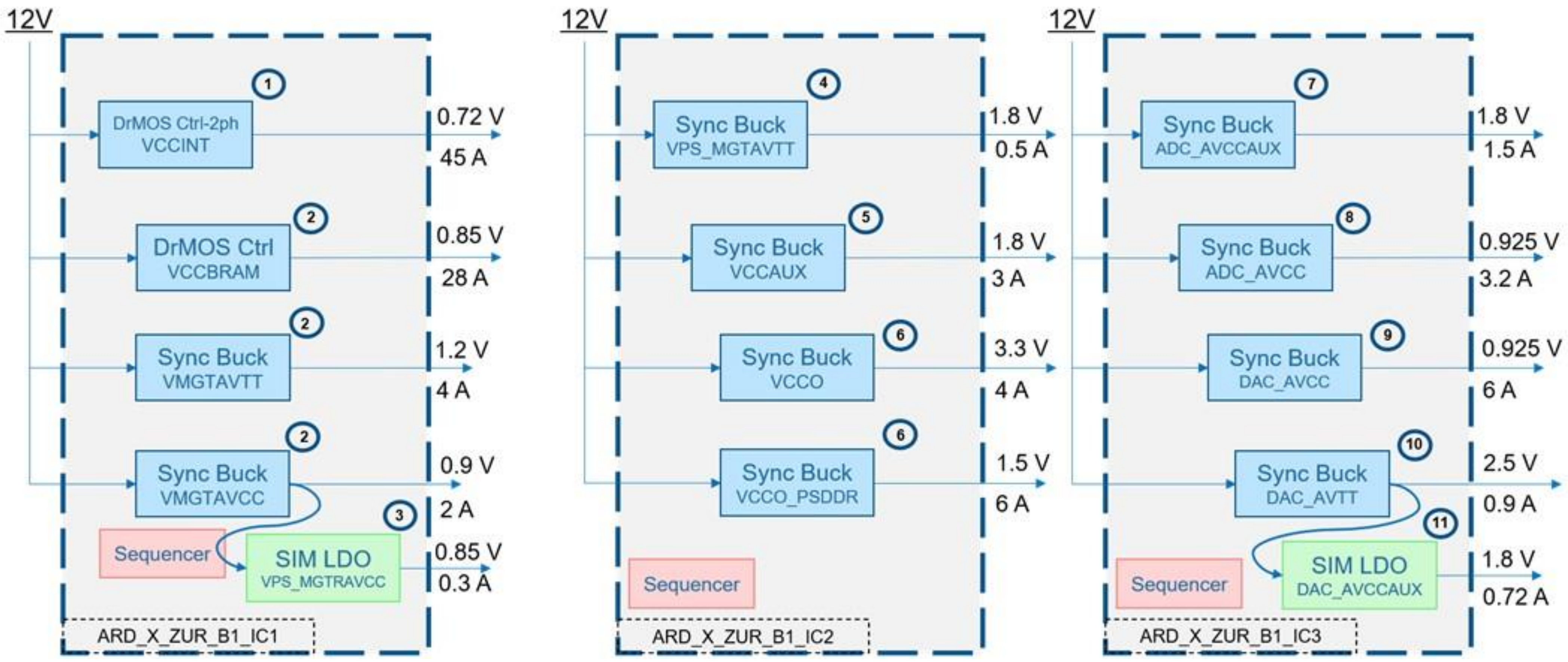
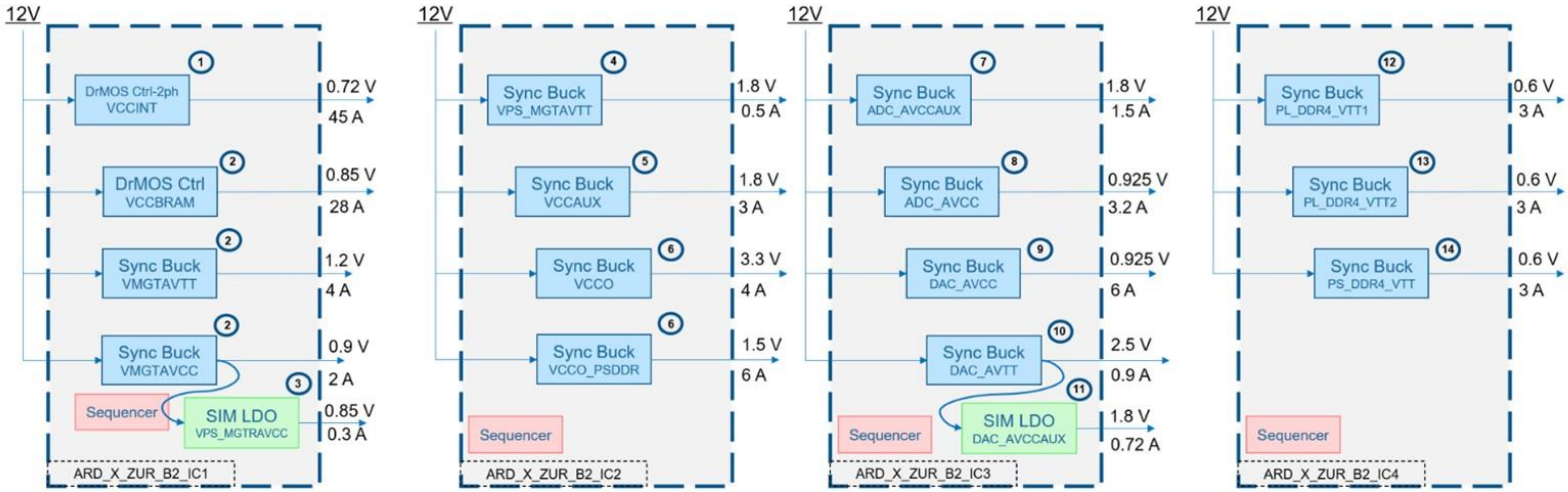
Proposed Solution (4xPMICs)
Use-Case B1



Proposed Solution (4xPMICs)
Use-Case B2



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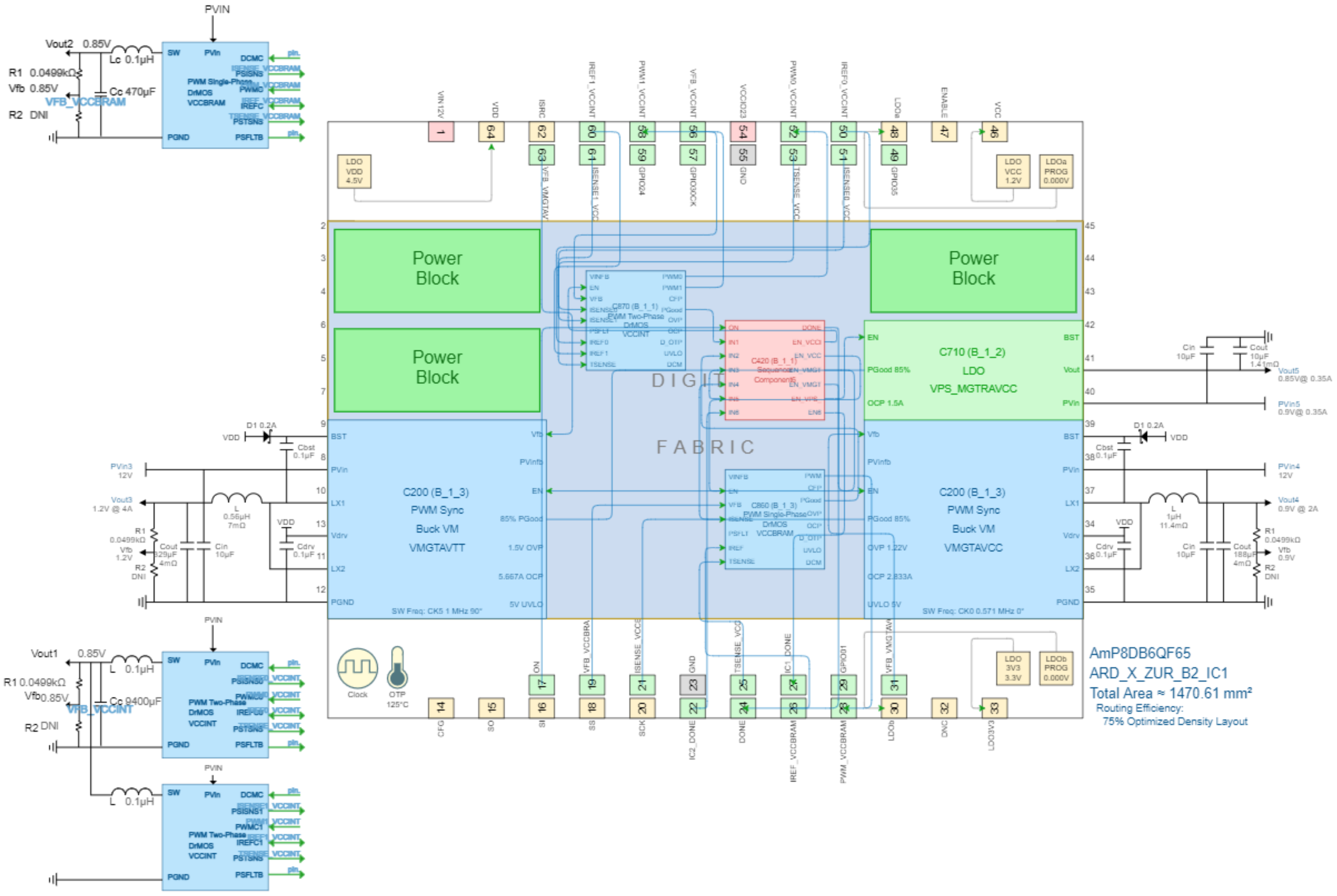
Mapping IC1 (WebAmp View)

Use-Case A1, B1, B2



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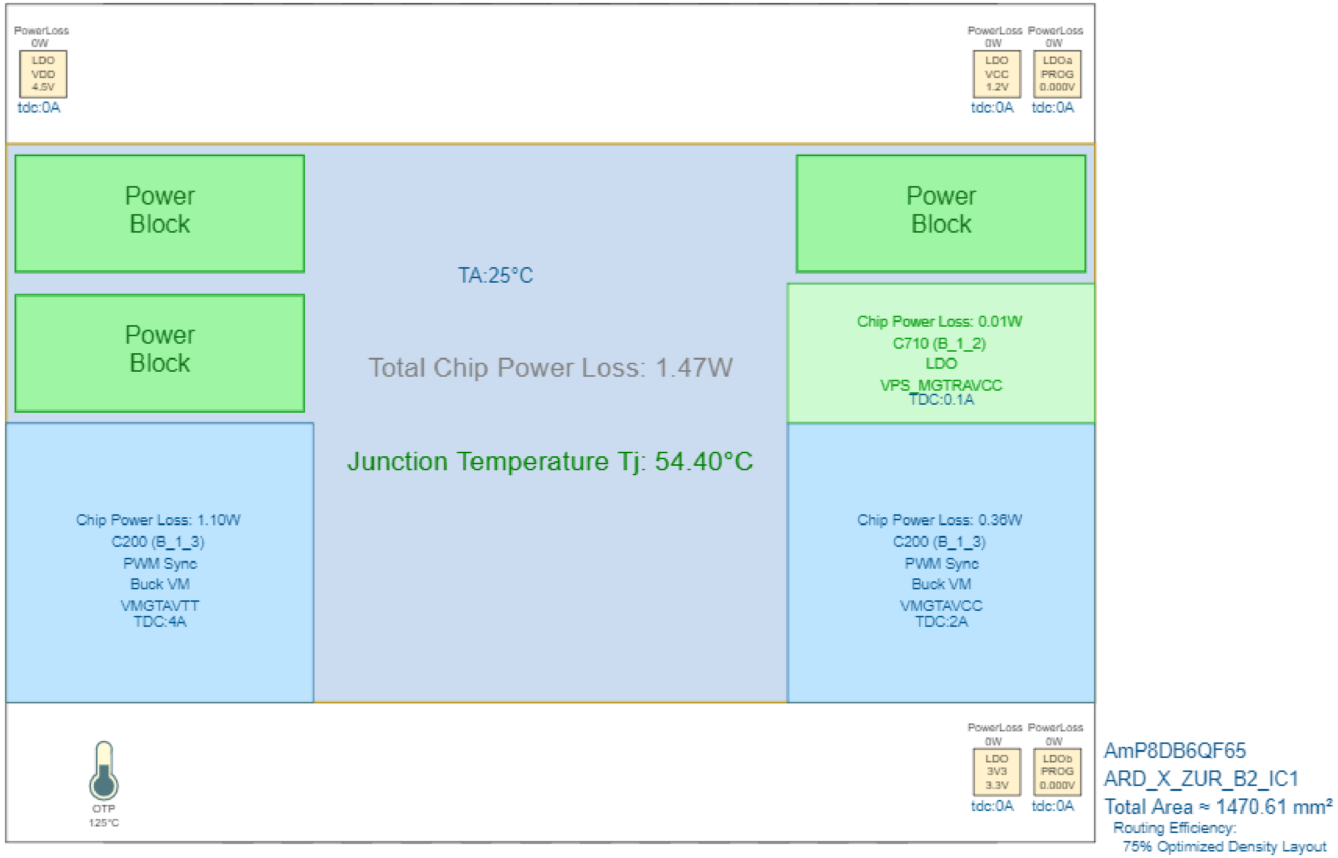
Thermal Design View (IC1)
Use-Case A1, B1, B2



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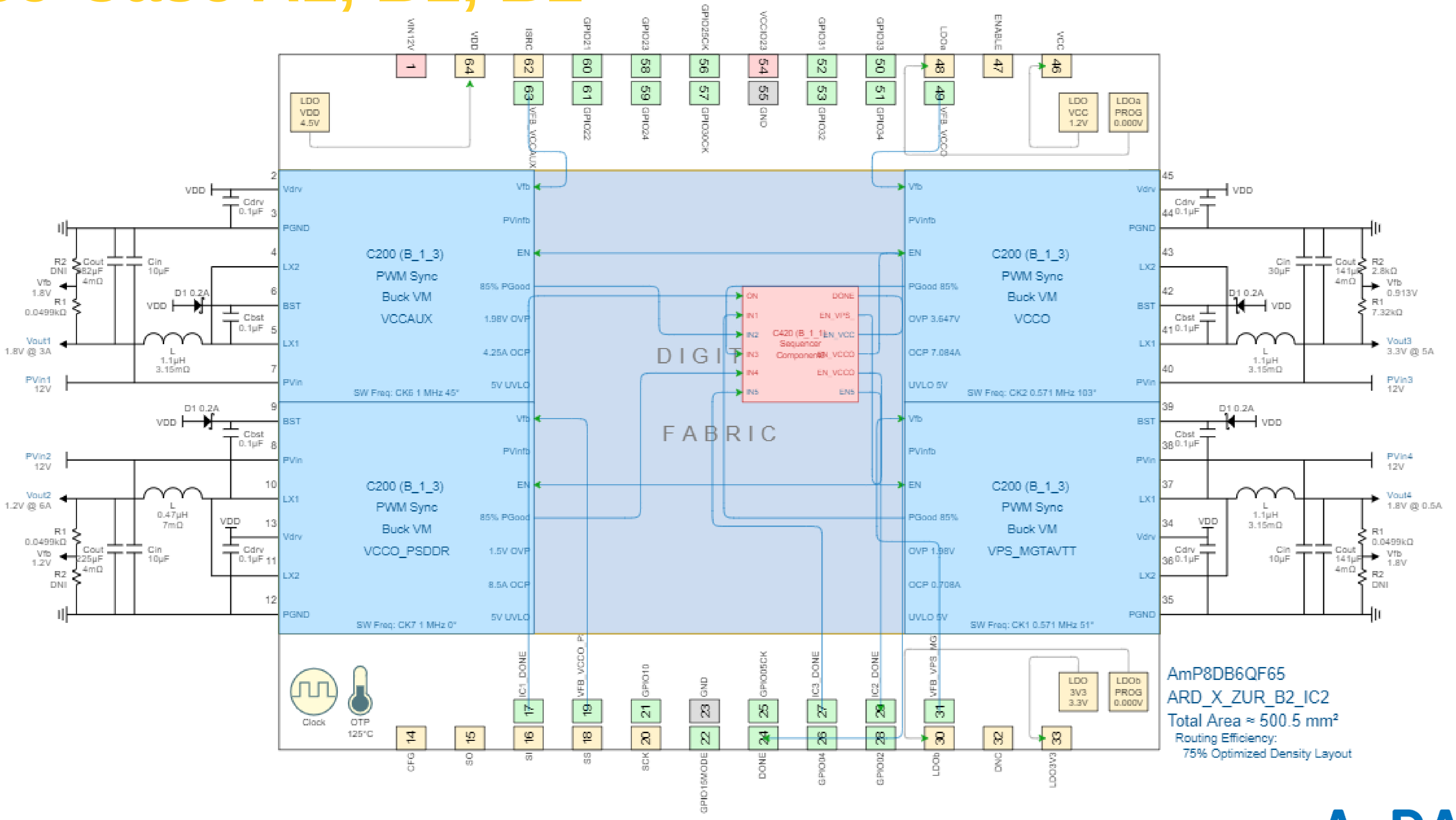
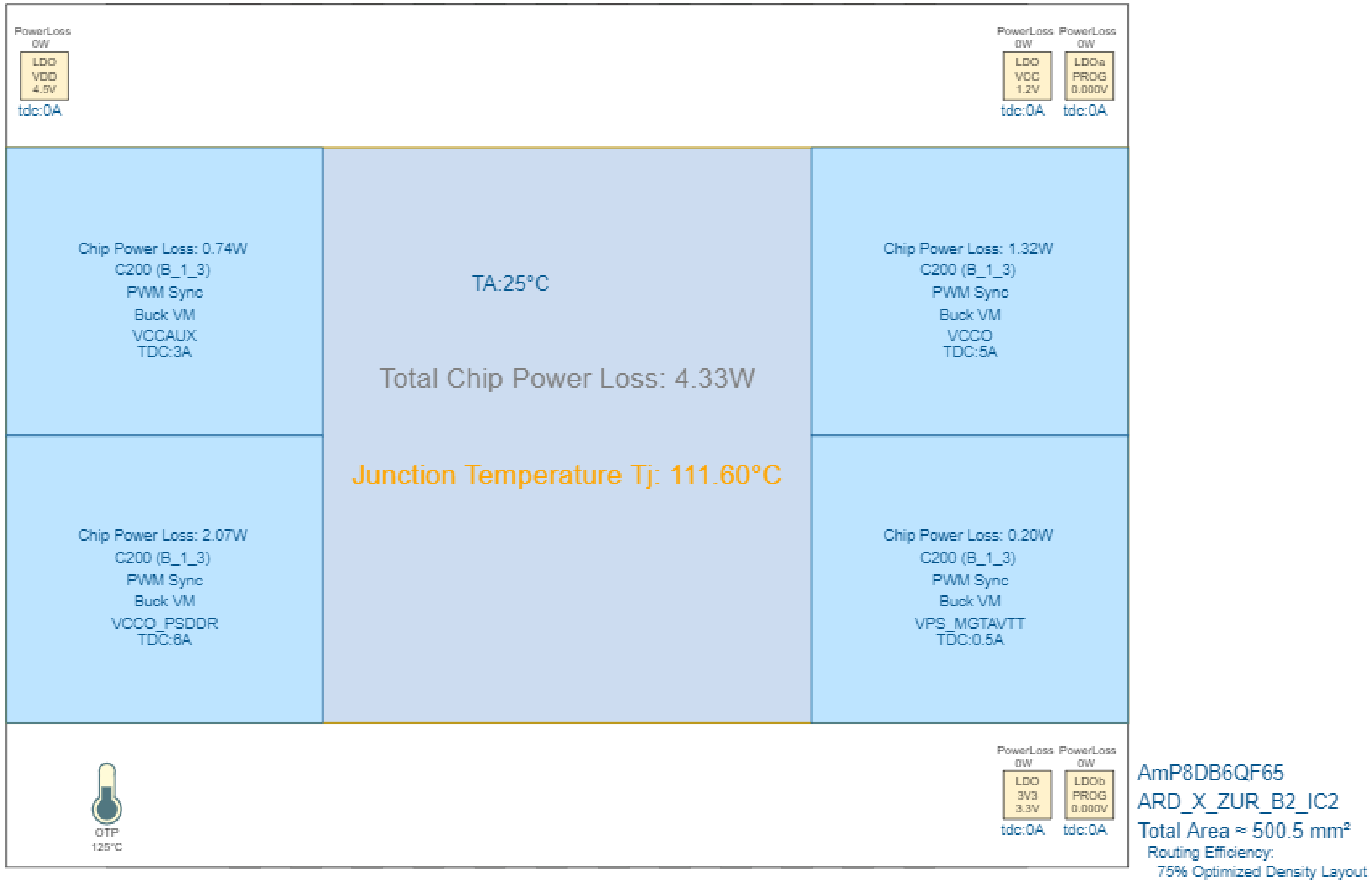
Mapping IC2 (WebAmp View)

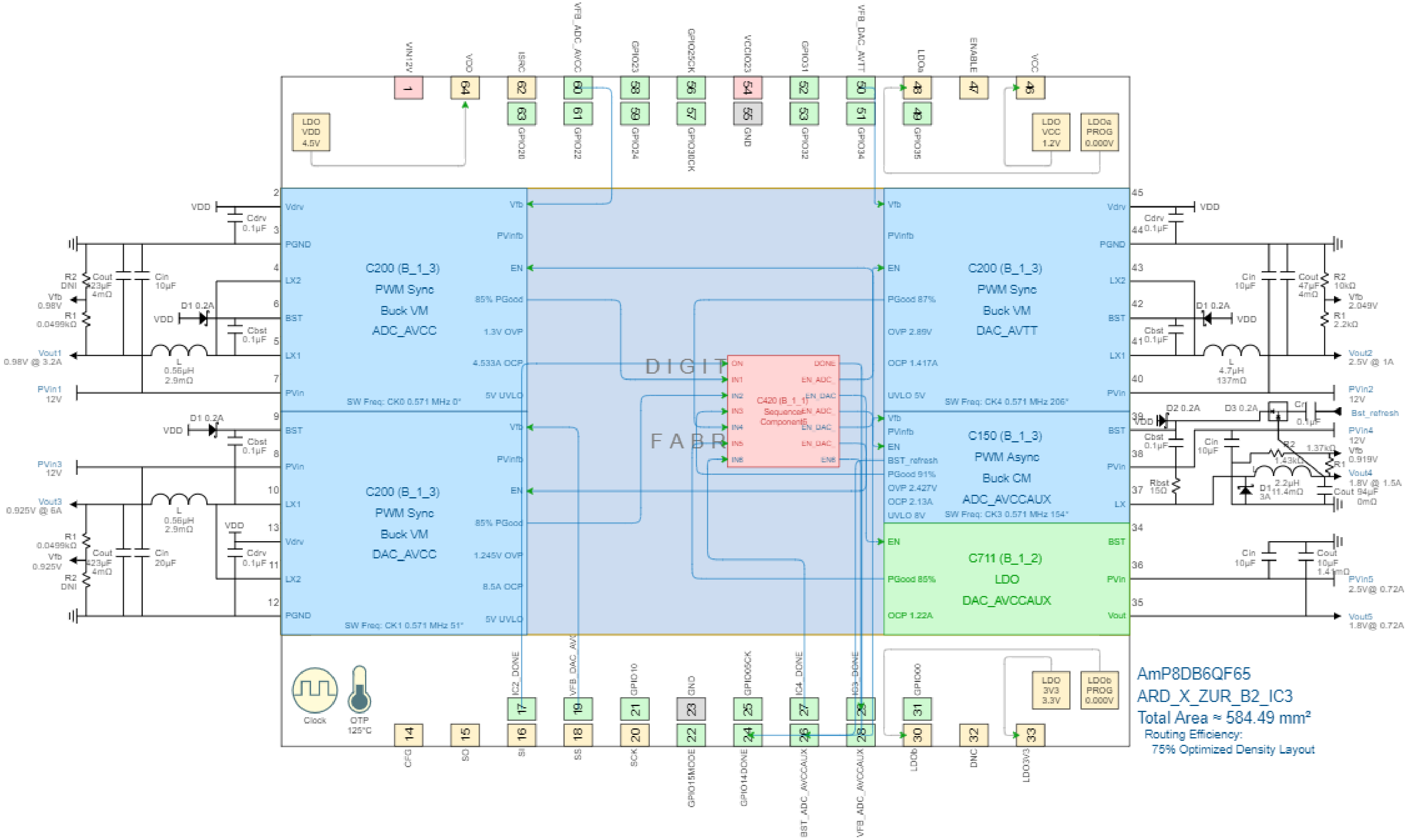
Use-Case A1, B1, B2



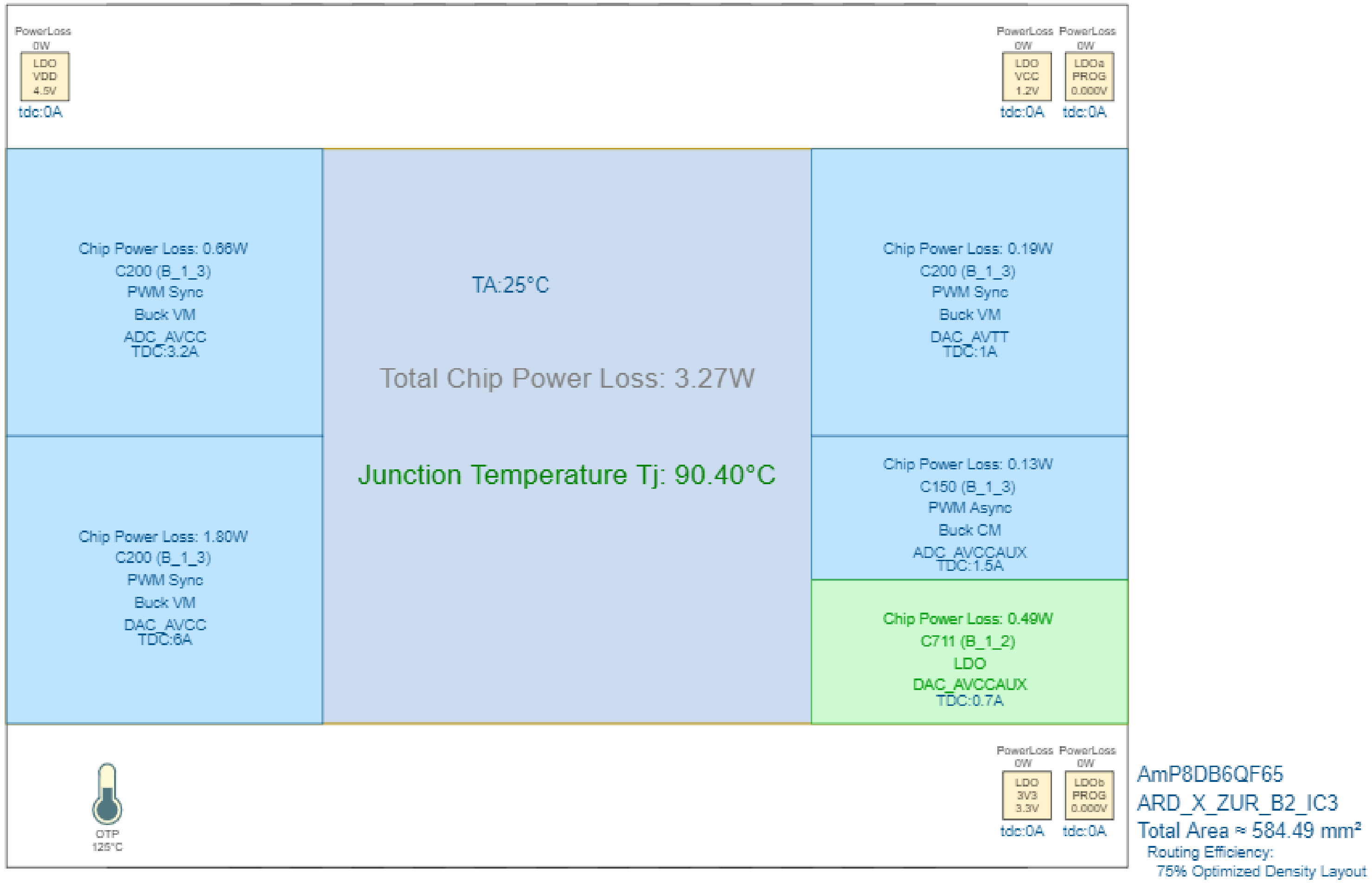
Thermal Design View (IC2)
Use-Case A1, B1, B2



Mapping IC3 (WebAmp View)
Use-Case B1, B2

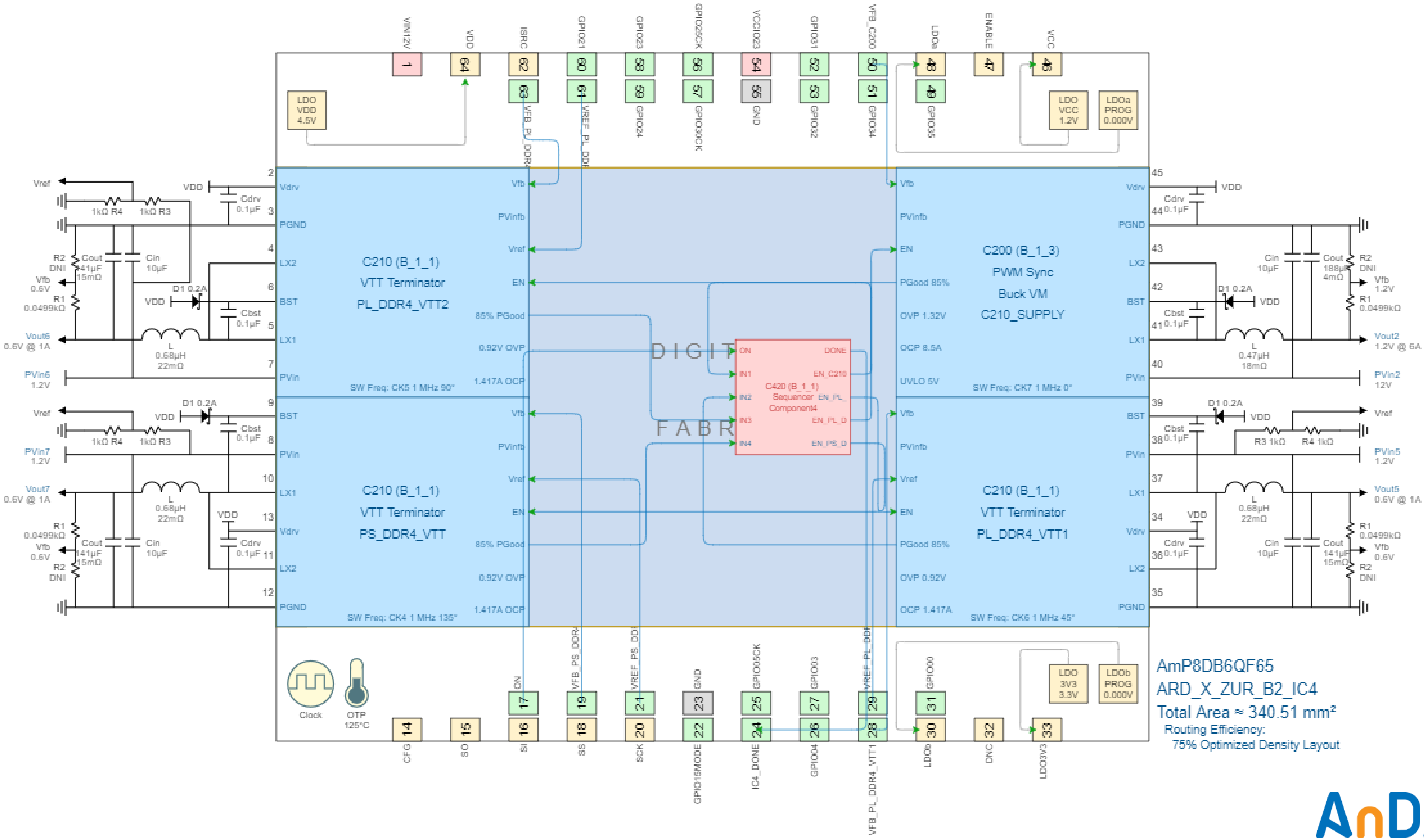


Thermal Design View (IC3)
Use-Case B1, B2



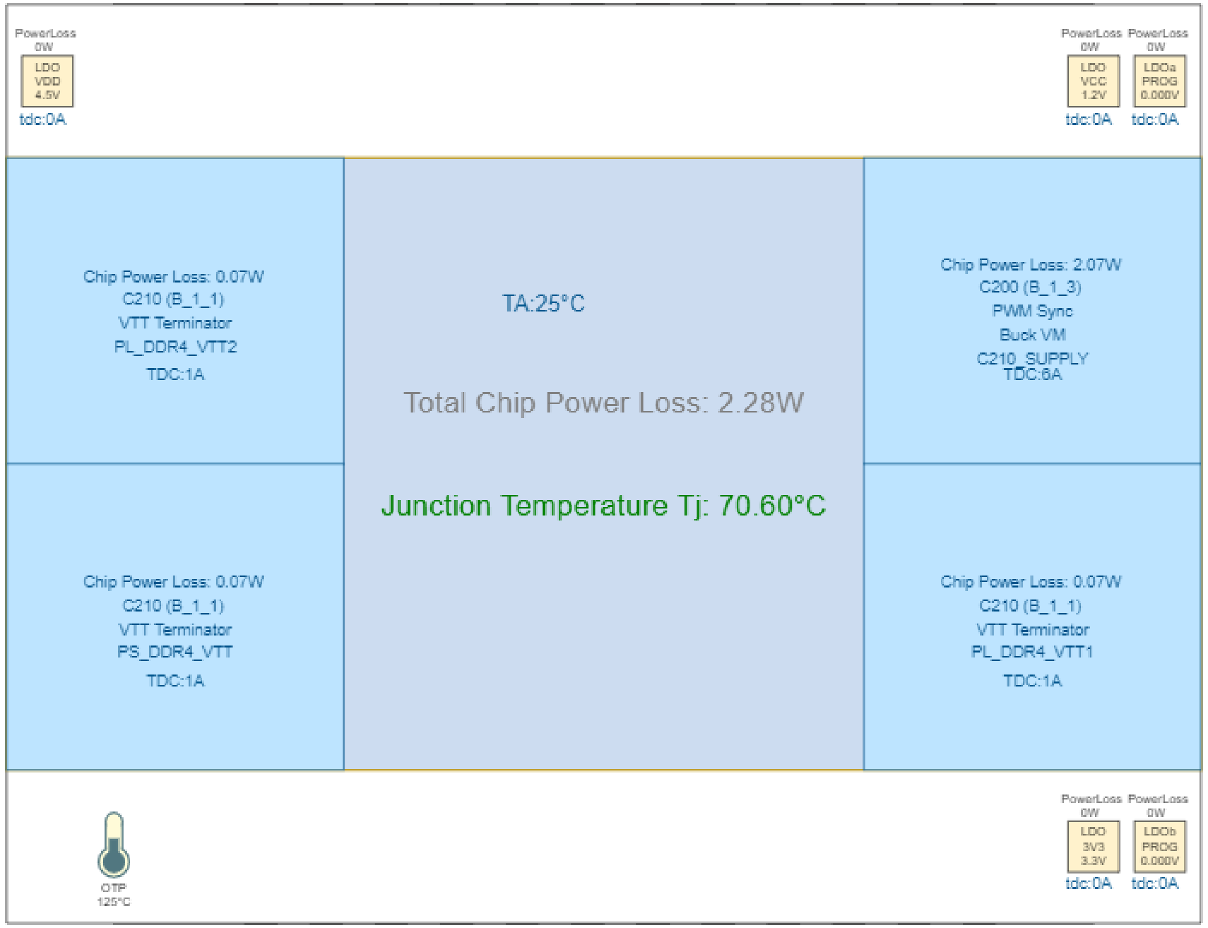
Mapping IC4 (WebAmp View)

Use-Case B2

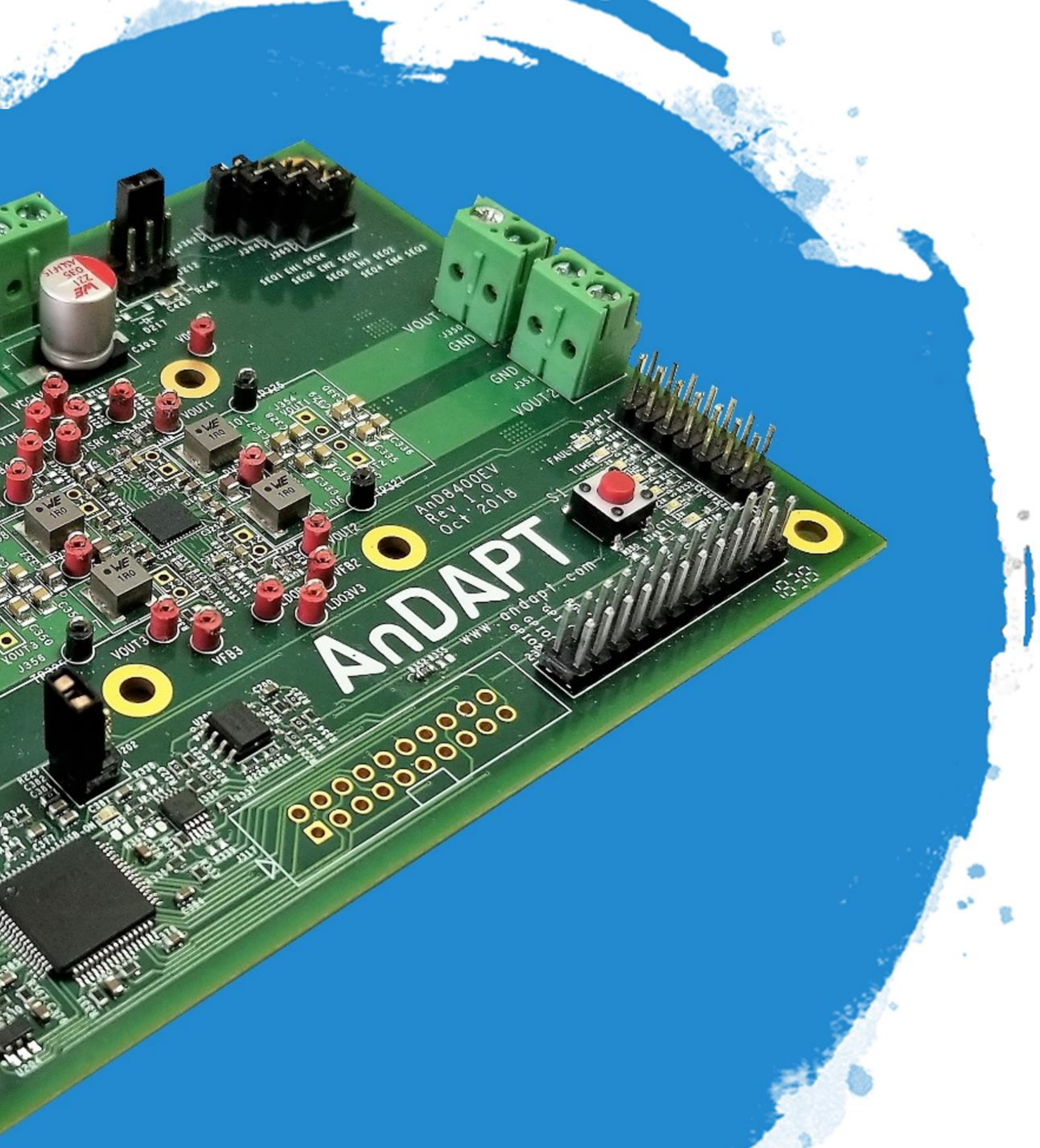


AmP8DB6QF65
ARD_X_ZUR_B2_IC4
Total Area ≈ 340.51 mm²
Routing Efficiency:
75% Optimized Density Layout

Thermal Design View (IC4)
Use-Case B2



AmP8DB6QF65
ARD_X_ZUR_B2_IC4
Total Area ≈ 340.51 mm²
Routing Efficiency:
75% Optimized Density Layout



Bench Data

Use-Case B2

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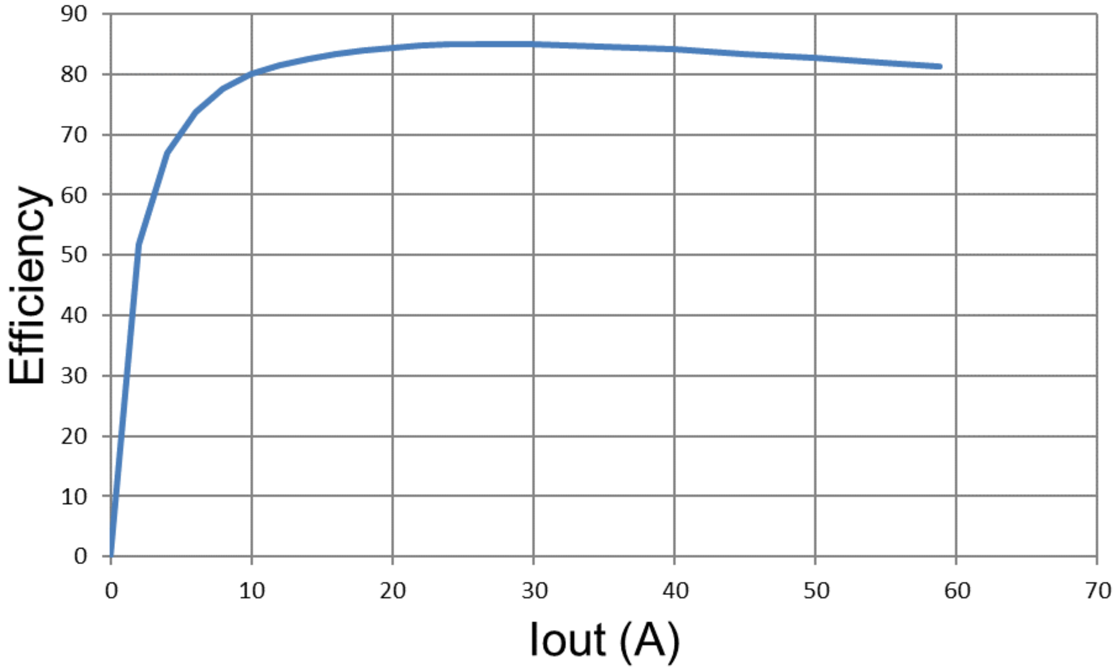
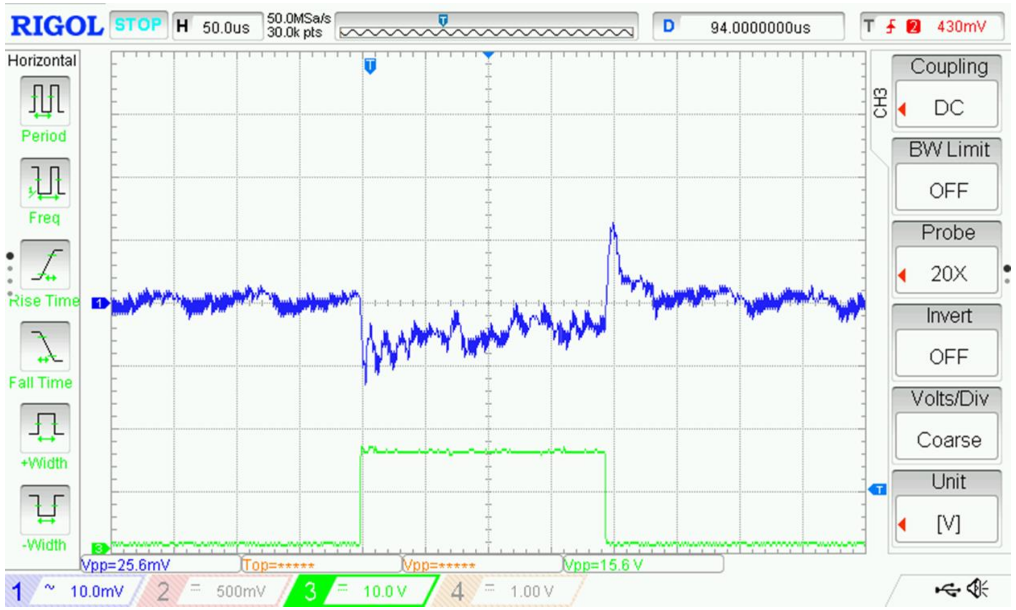
VCCINT: Efficiency & Transient





Vout = 0.72 V

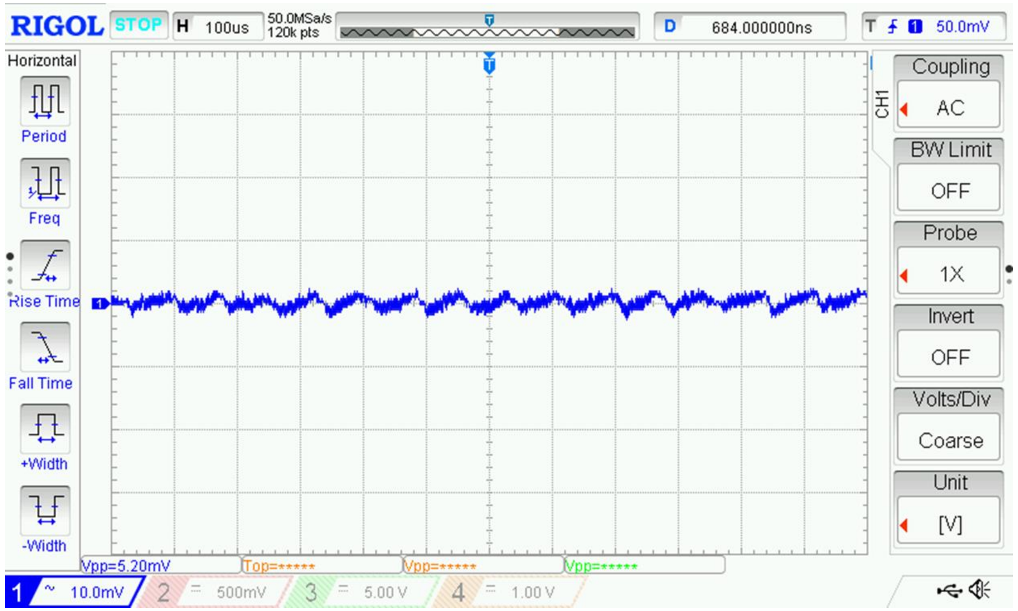
Transient 45A – 60A @ 100 A/µs

V_{PP} = 25.6 mV

Fsw = 1 MHz

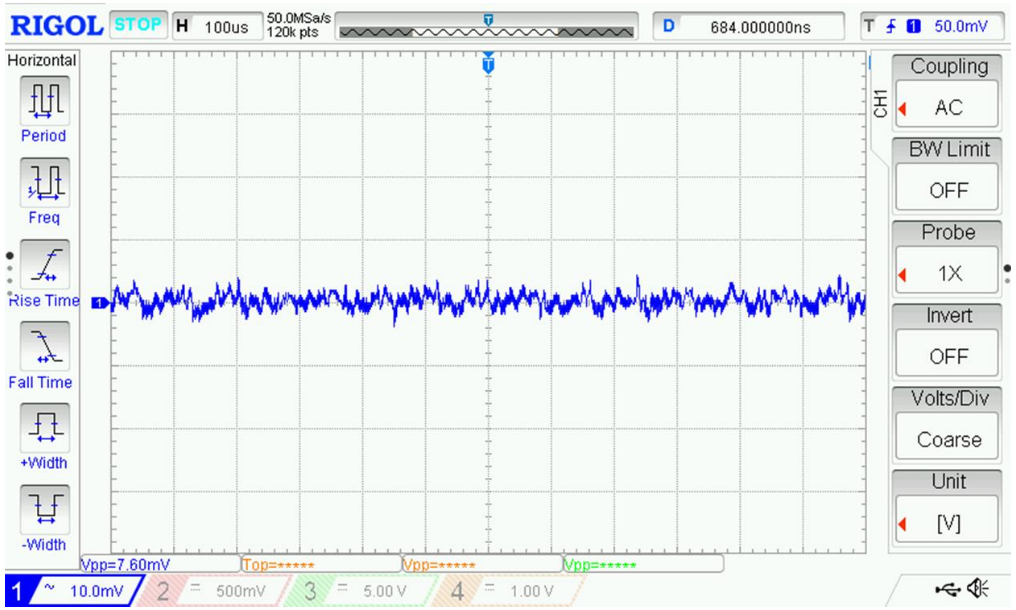
Lout = 0.1 µH, Cout = 1,900 µF

Ripple



No Load

V_{PP} = 5.2 mV



Full Load

V_{PP} = 7.6 mV

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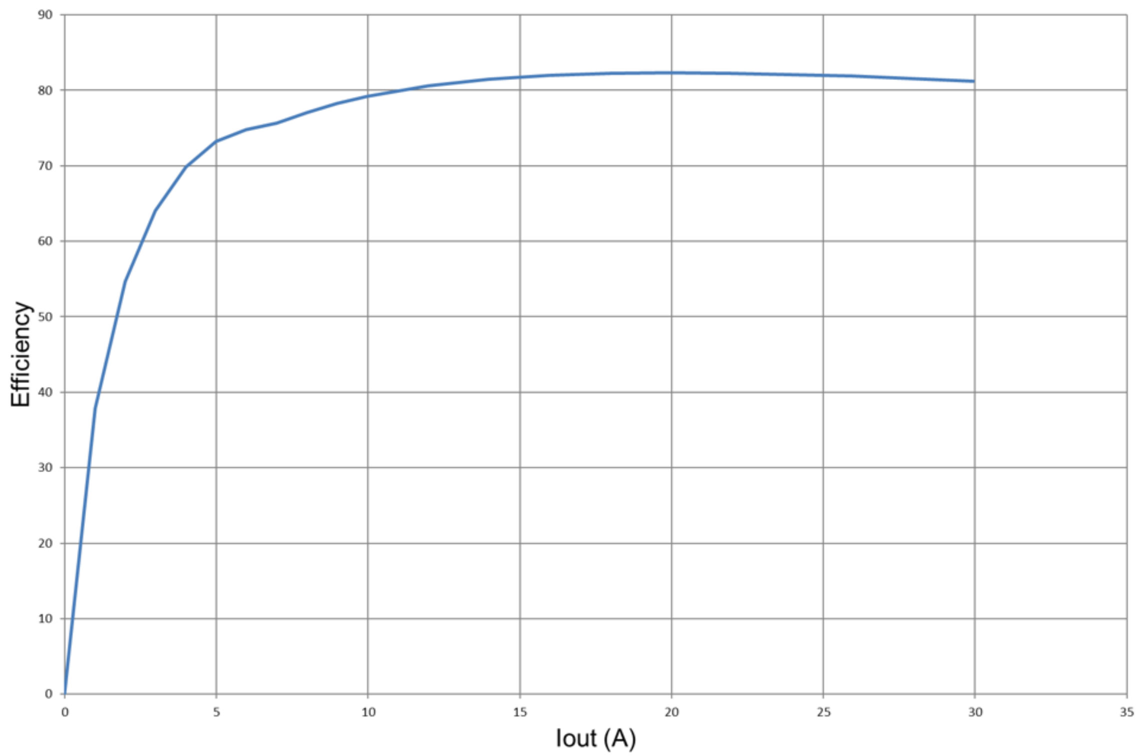
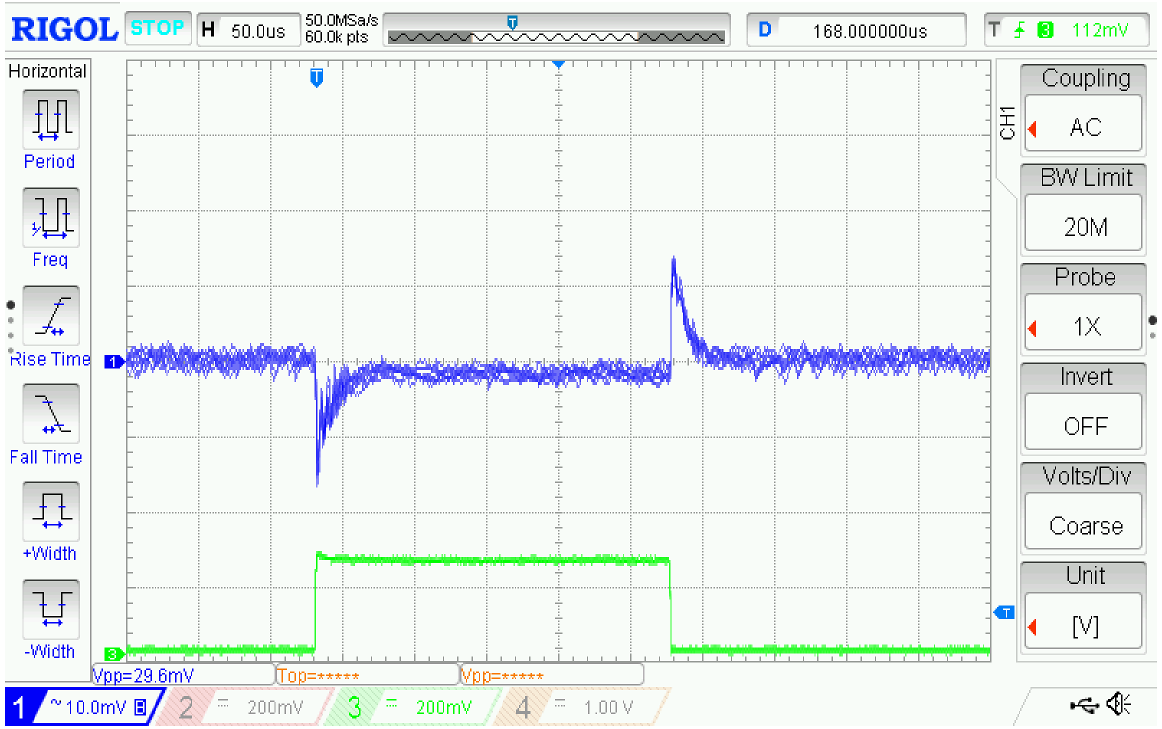
VCCBRAM: Efficiency & Transient





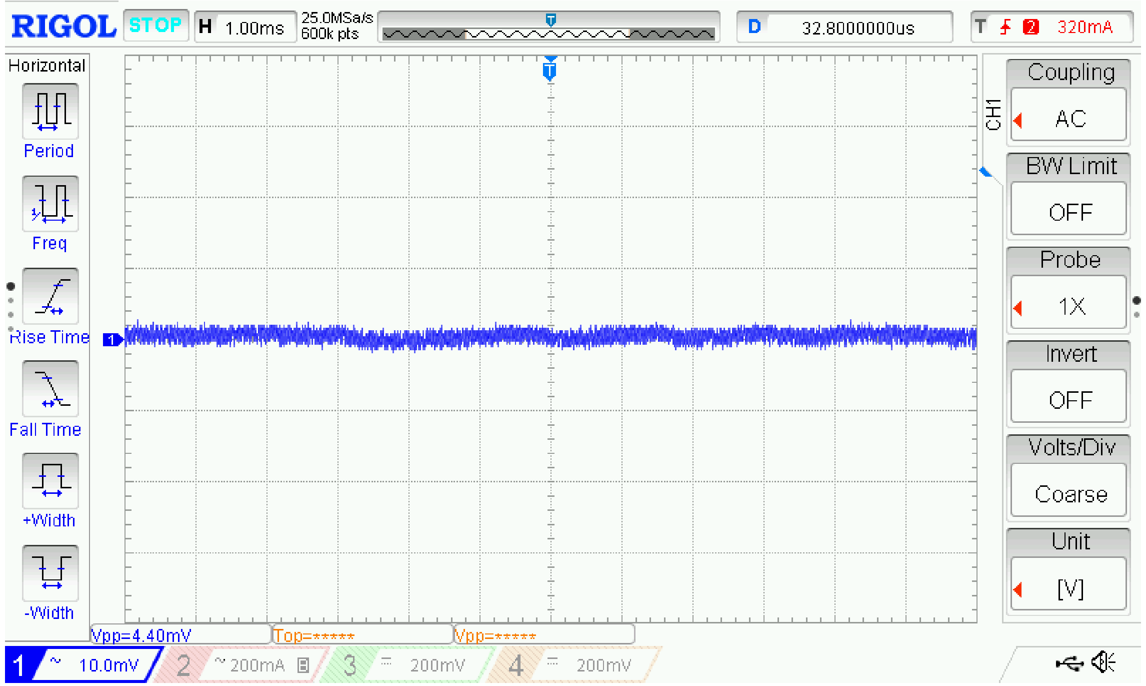
Vout = 0.85 V

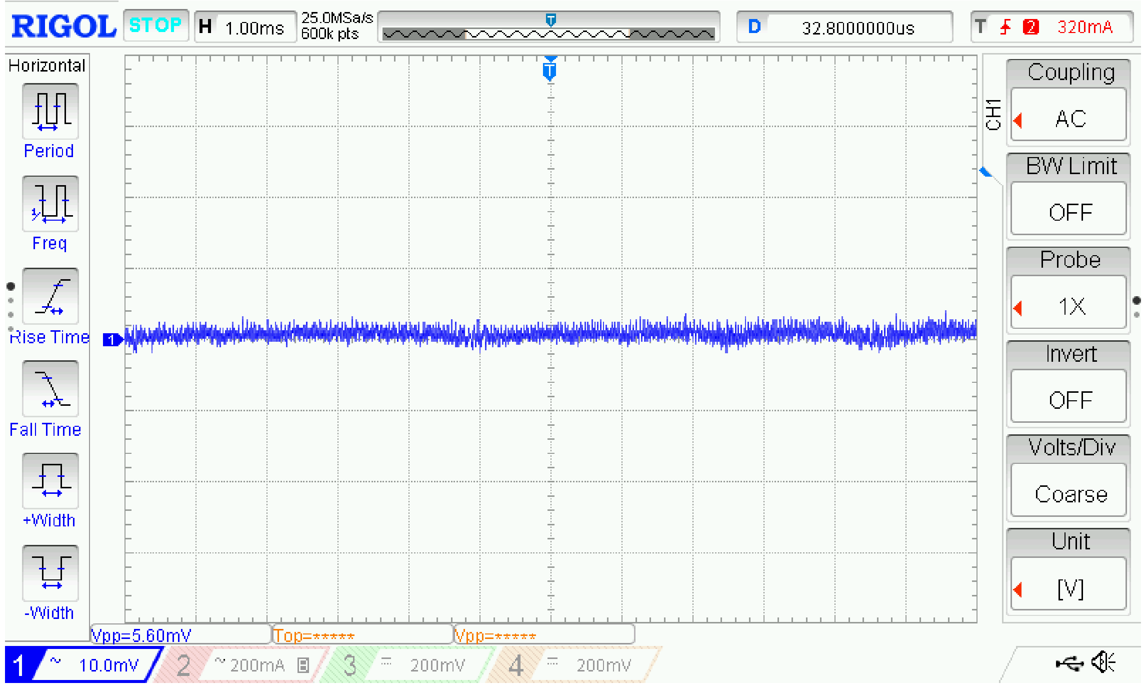
Transient: 22.5 A – 30A @ 100 A/us

V_{PP} = 29.6 mV

Lout = 0.1 µH, Cout = 910 µF

VCCBRAM: Ripple

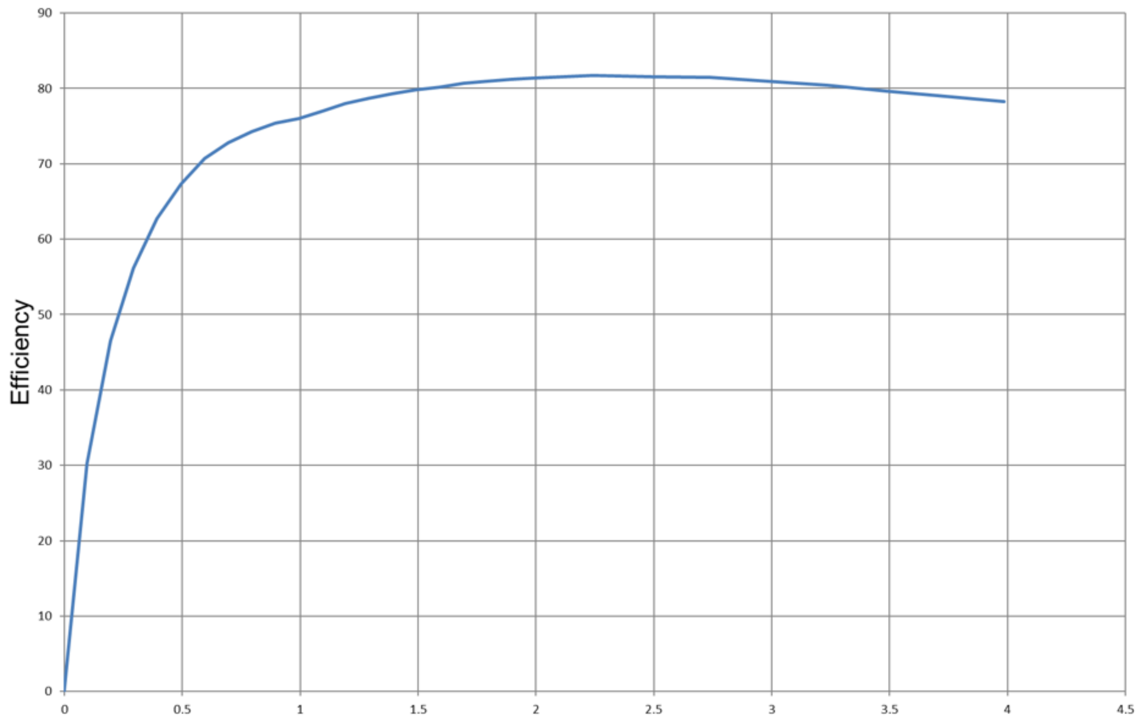


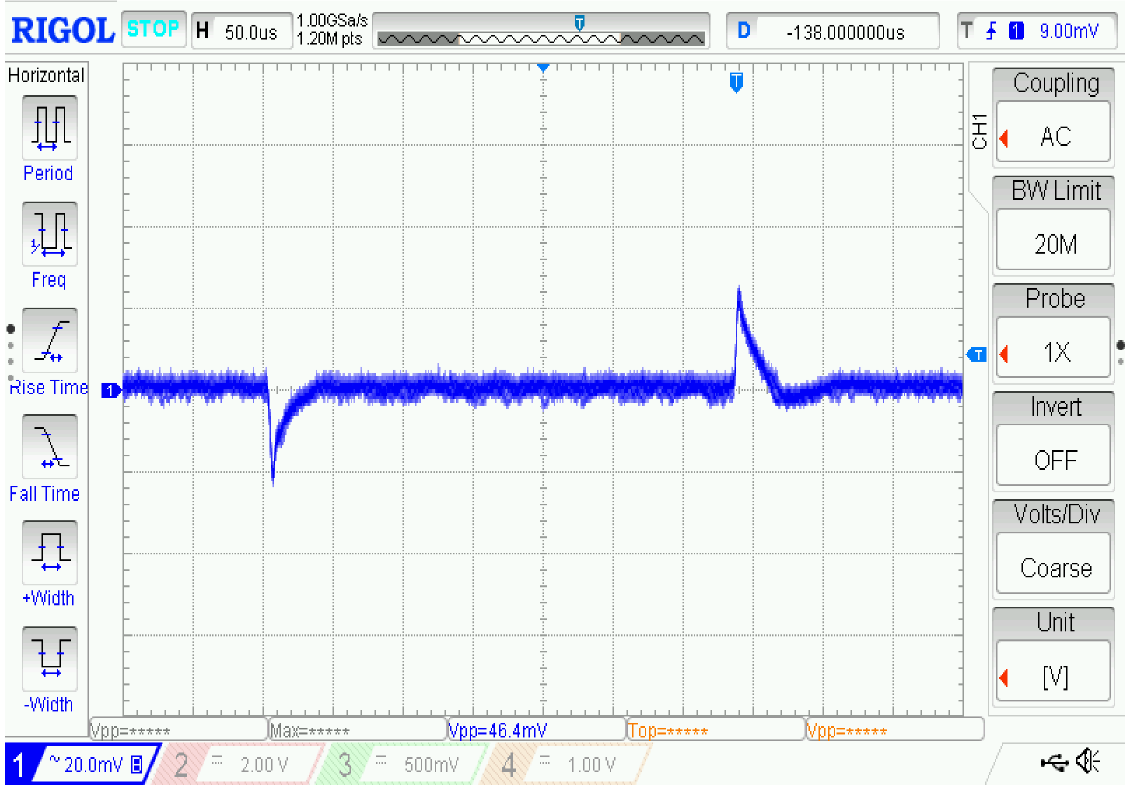


No Load Ripple
V_{PP} = 8 mV

Full Load Ripple
V_{PP} = 11.2 mV

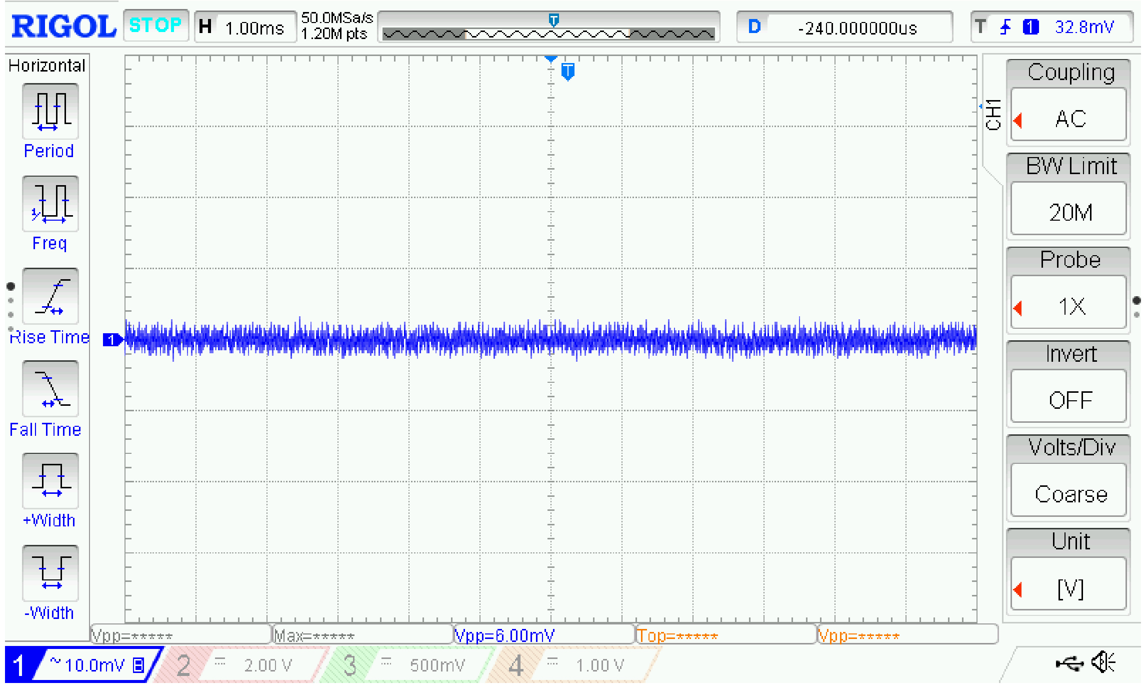
VMGTAVTT: Efficiency & Transient



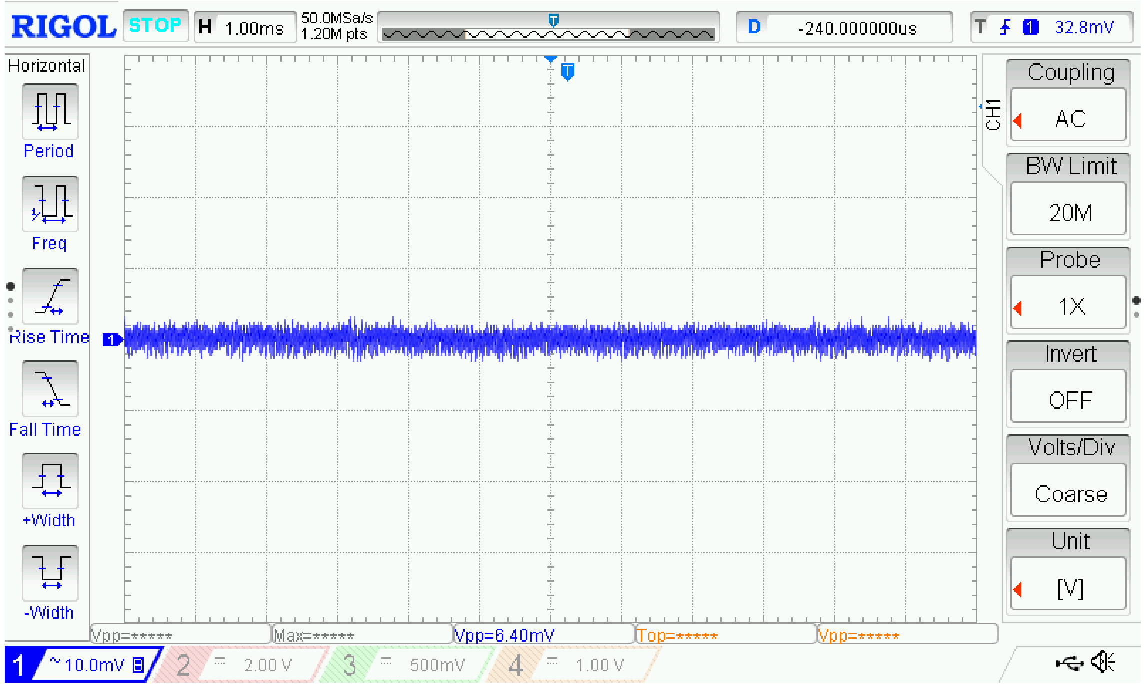


Vout = 1.2 V
Transient: 0.8A – 4A @ 10 A/us
V_{PP} = 46.4 mV
Lout = 0.56 µH, Cout = 329 µF

VMGTAVTT: Ripple

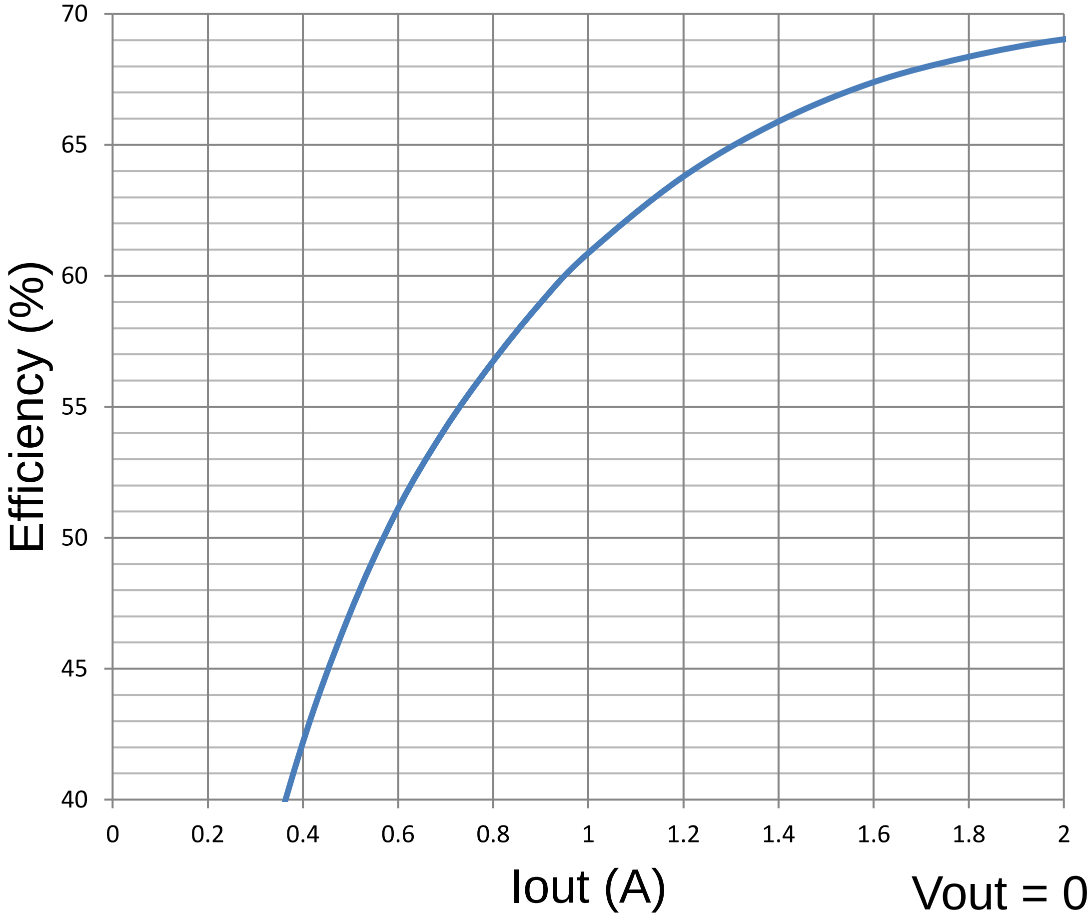


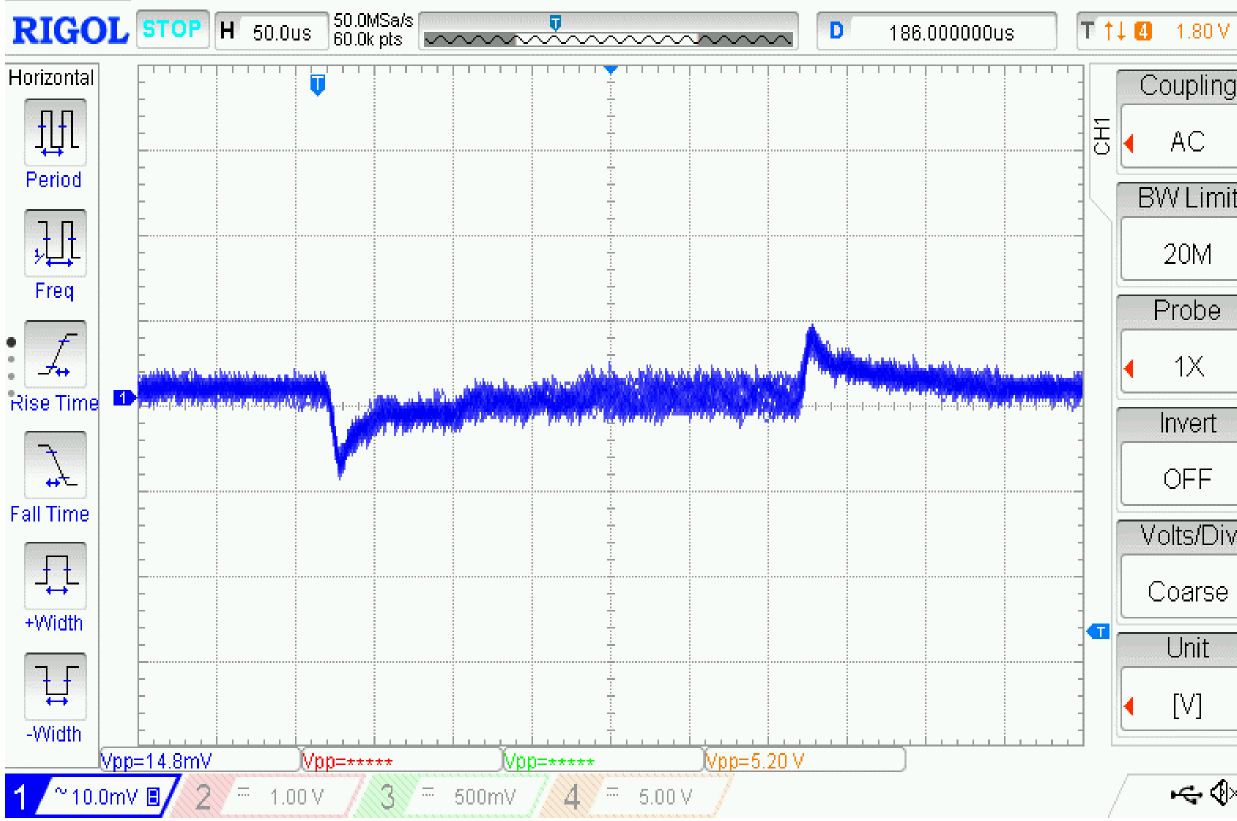
No Load Ripple
V_{PP} = 6 mV



Full Load Ripple
V_{PP} = 6.4 mV

VMGTAVCC: Efficiency & Transient





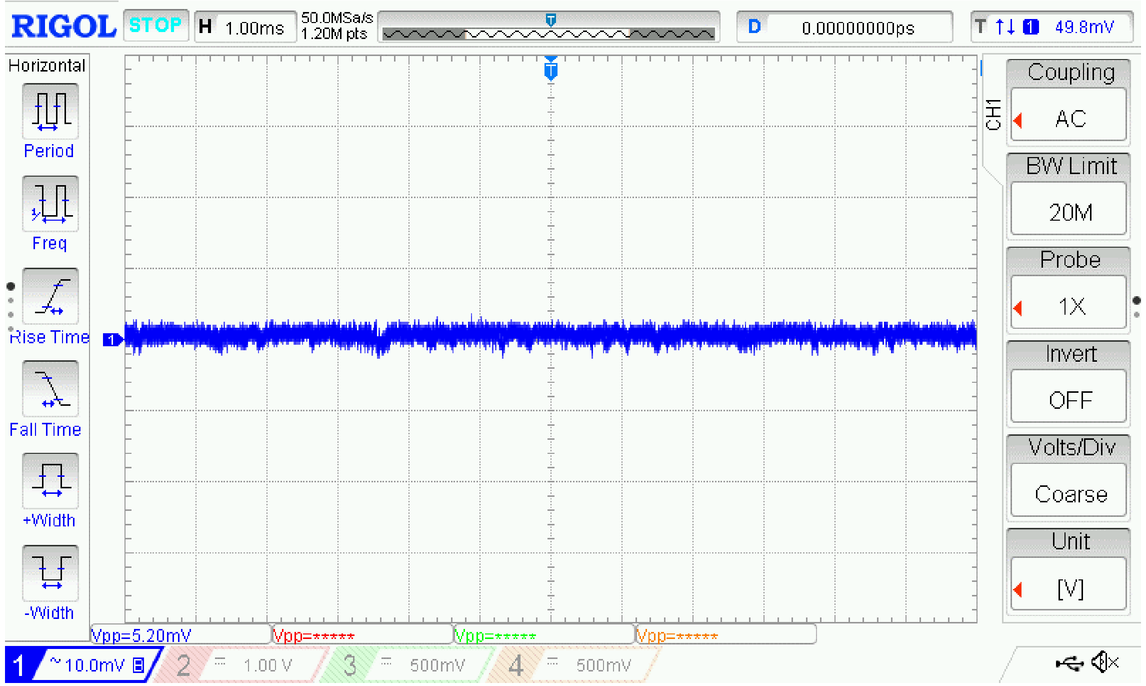
Vout = 0.9 V

Transient: 1.5 A – 2A @ 10 A/us

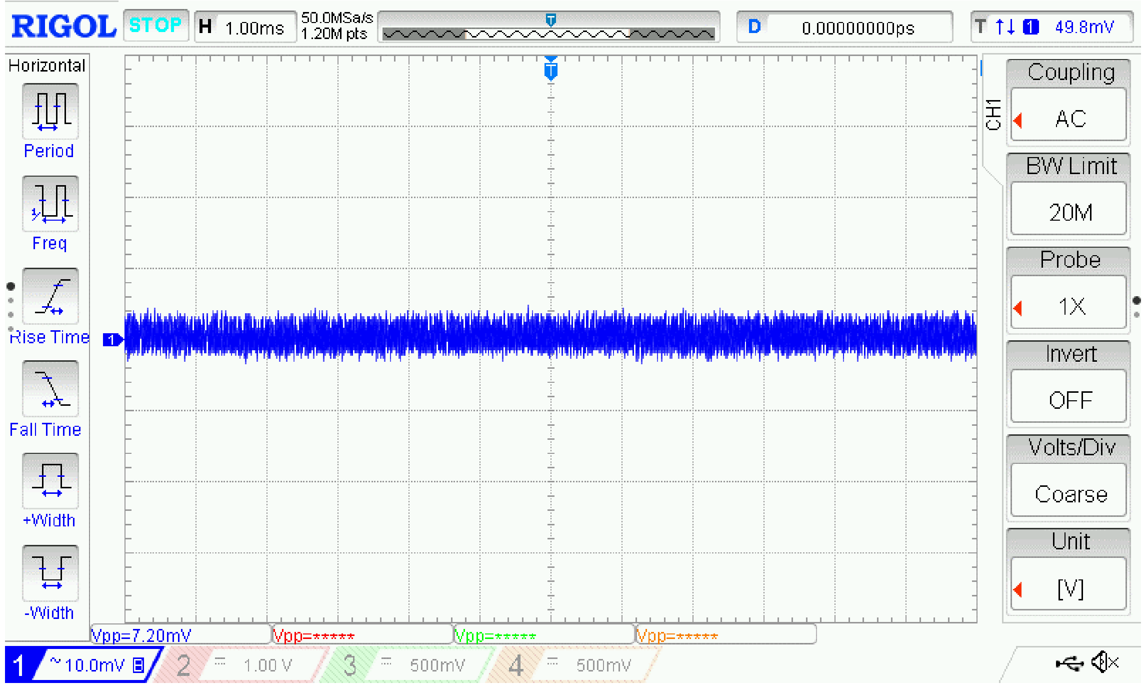
V_{PP} = 14.8 mV

Lout = 1 µH, Cout = 188 µF

VMGTAVCC: Ripple

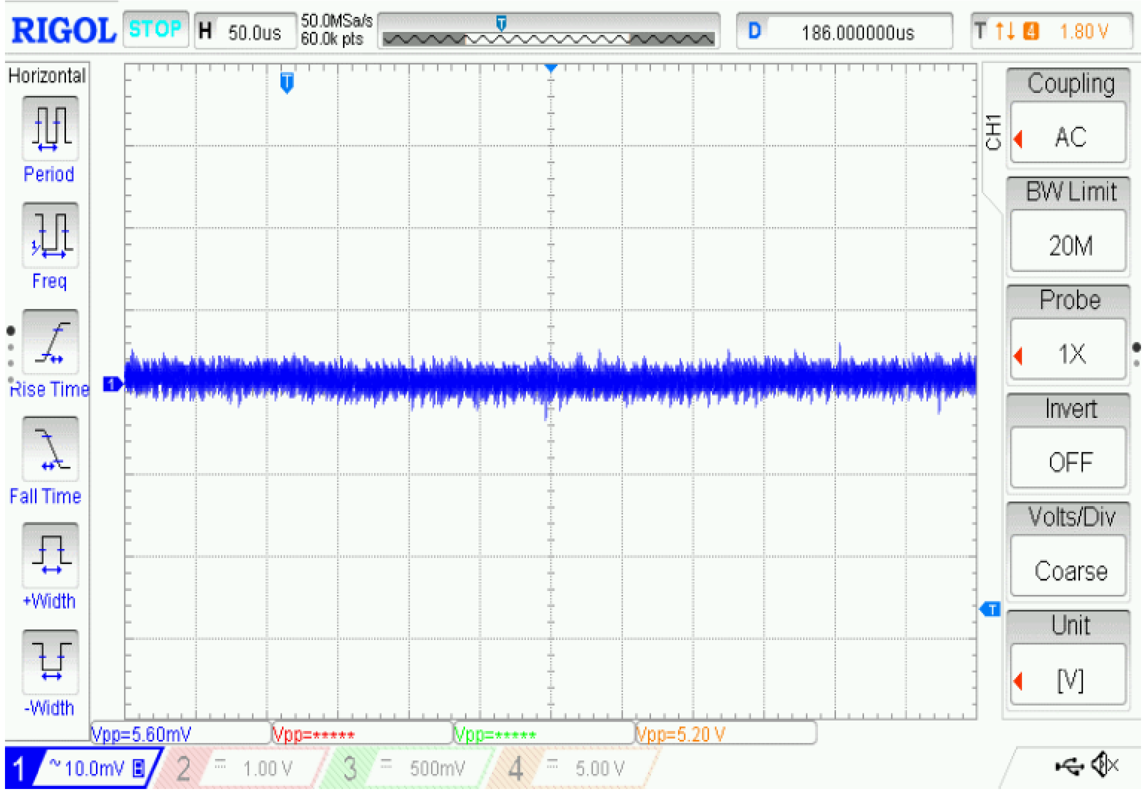


No Load Ripple
V_{PP} = 5.2 mV



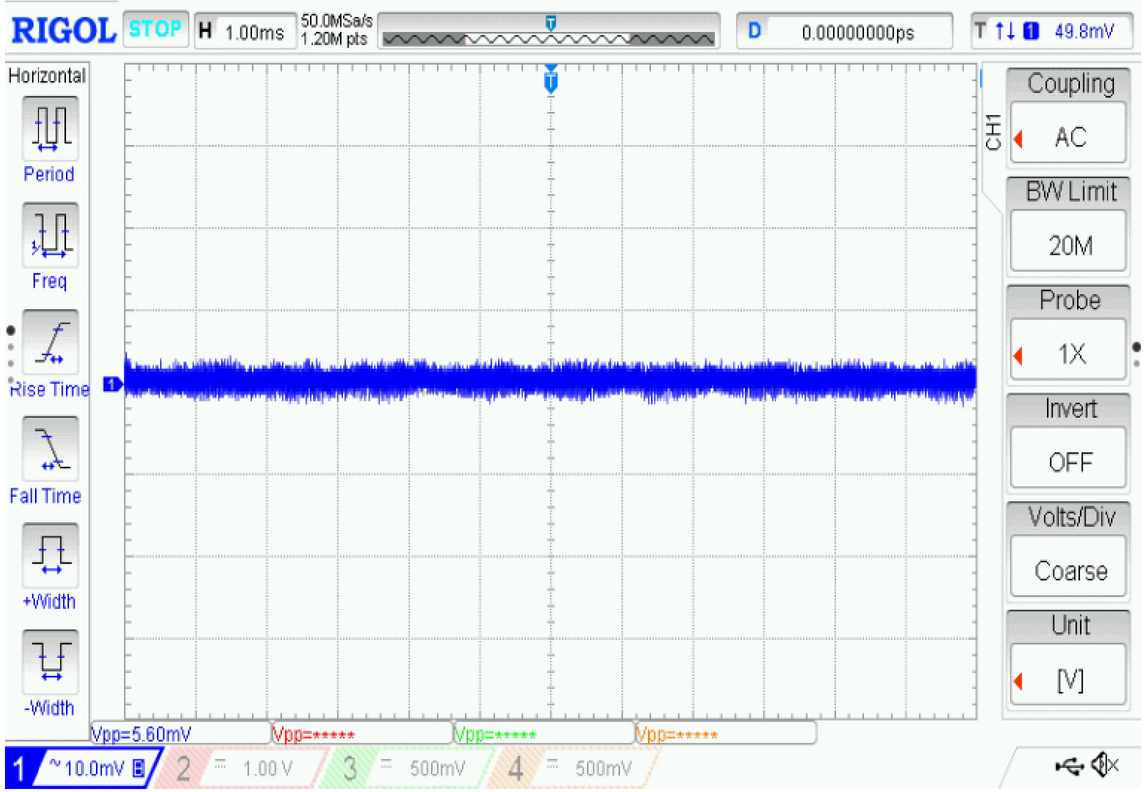
Full Load Ripple
V_{PP} = 7.2 mV

VPS_MGTRAVCC: Transient

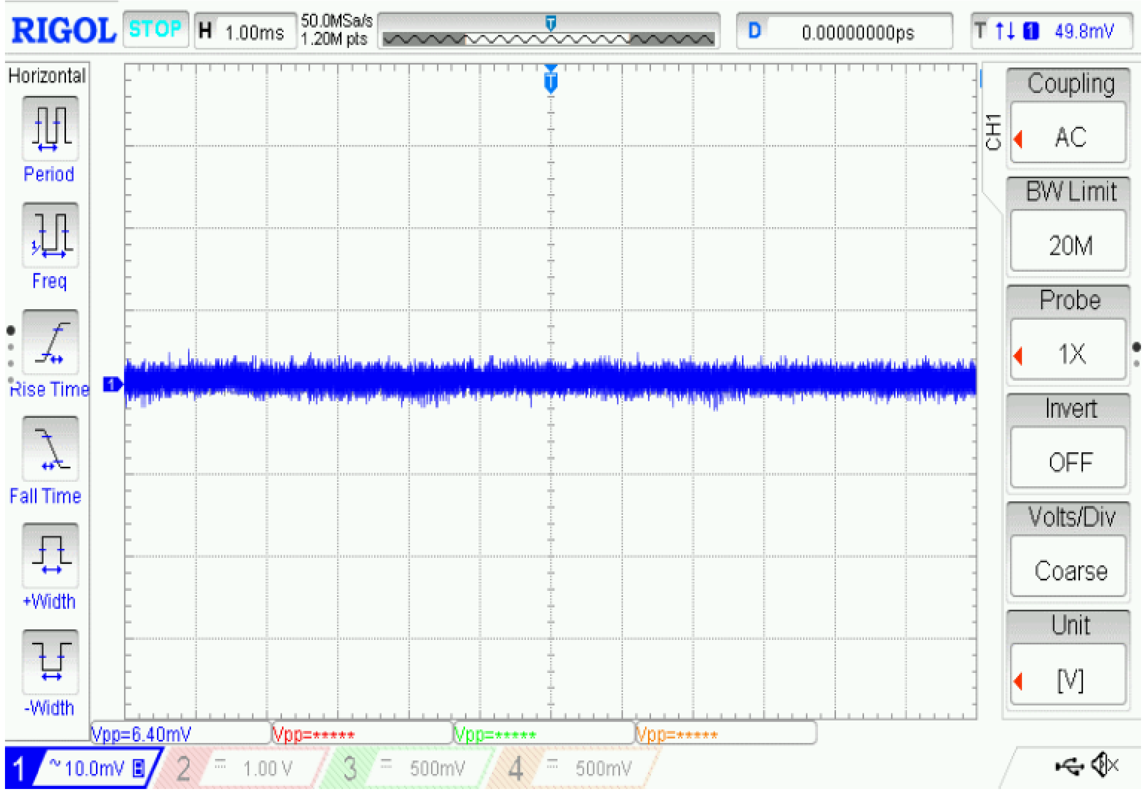


Vout = 0.85 V
Transient: 0.21A – 0.35 A @ 2.5 A/us
V_{PP} = 5.6 mV

VPS_MGTRAVCC: Ripple

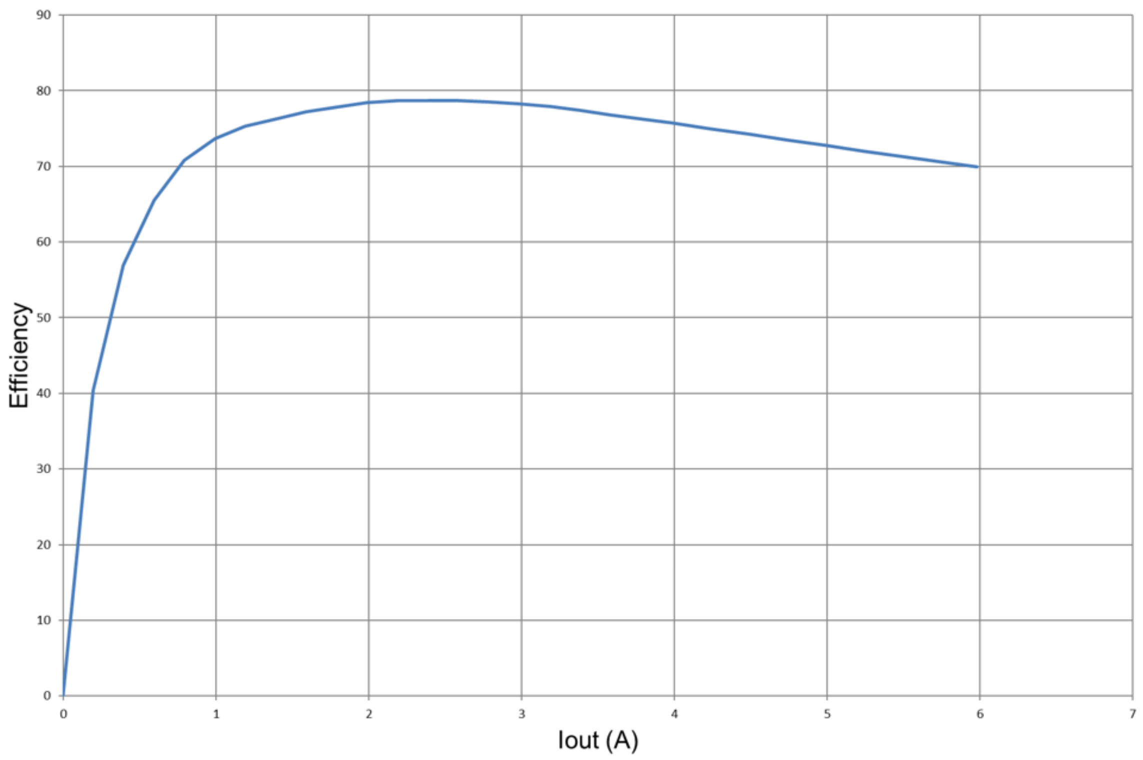


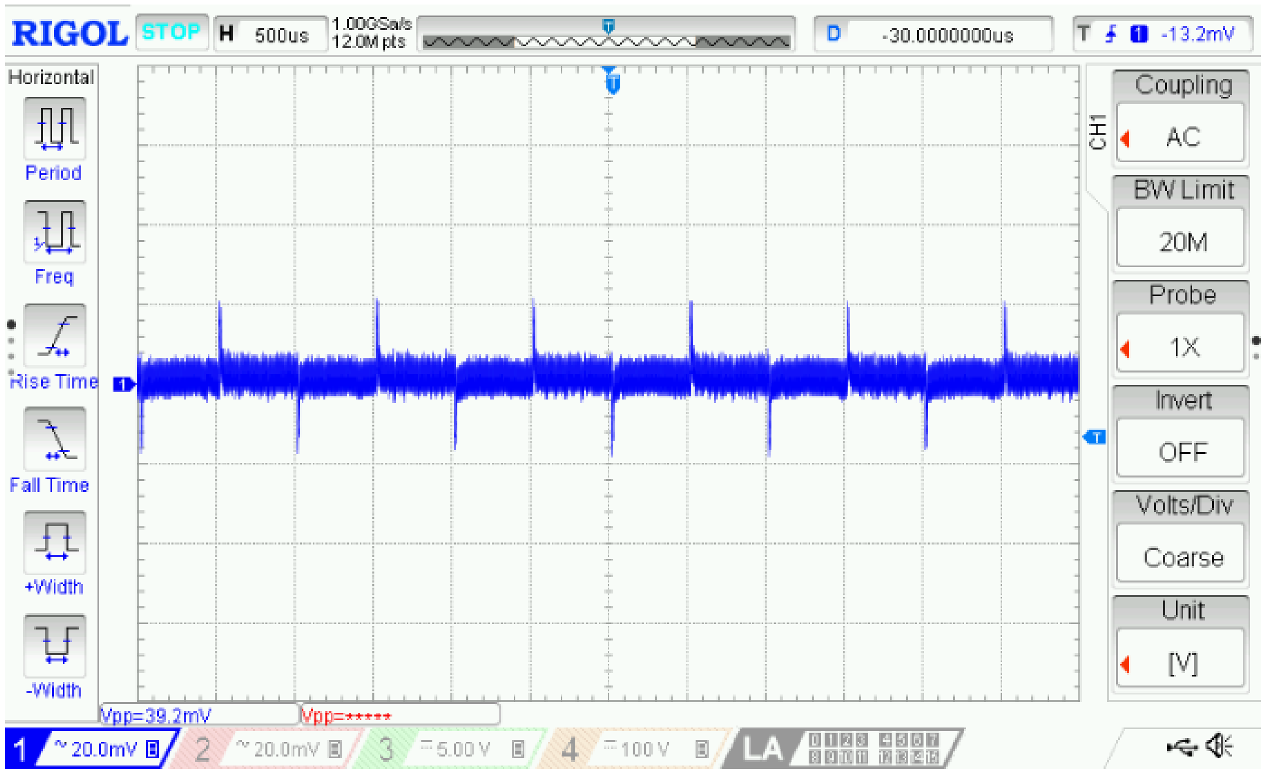
No Load Ripple
V_{PP} = 5.6 mV



Full Load Ripple
V_{PP} = 6.4 mV

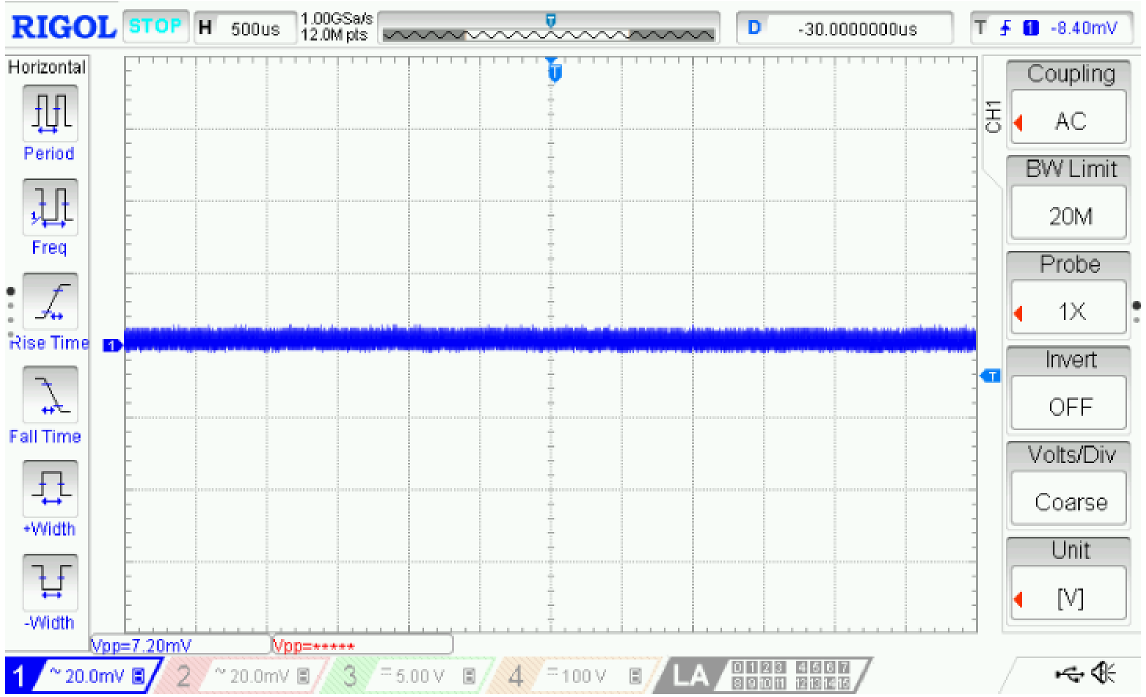
VCCO_PSDDR: Efficiency & Transient

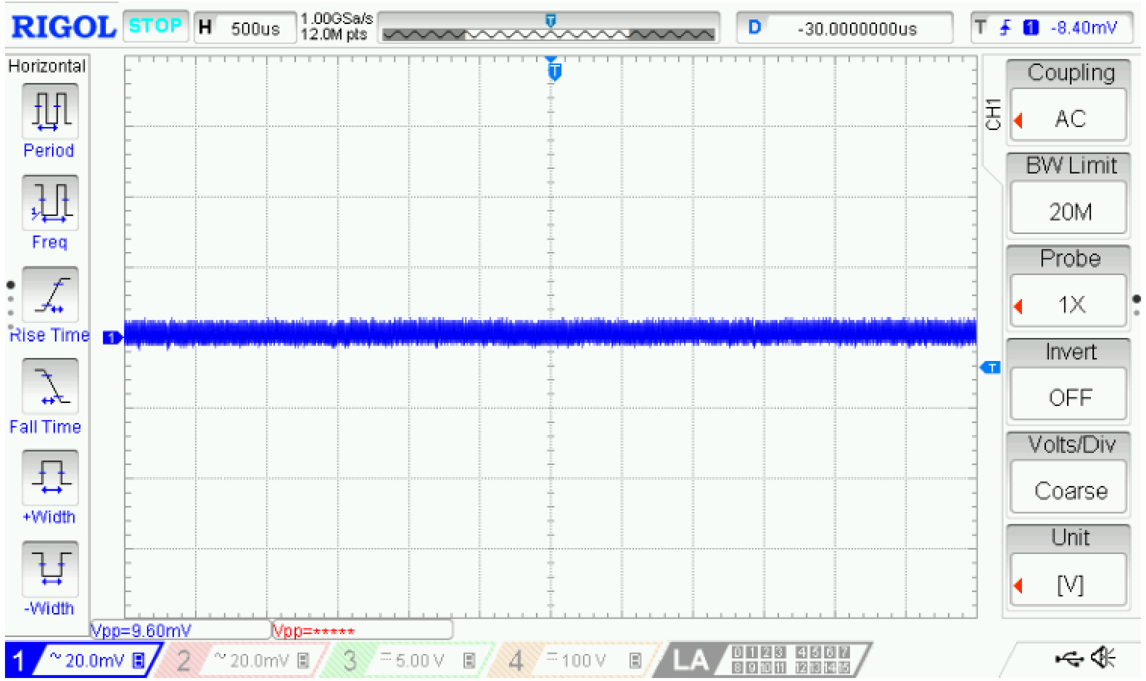




Vout = 1.2 V
Transient: 4.5 A – 6A @ 10 A/us
V_{PP} = 39.2 mV
Lout = 0.47 µH, Cout = 4 x 47 µF

VCCO_PSDDR: Ripple

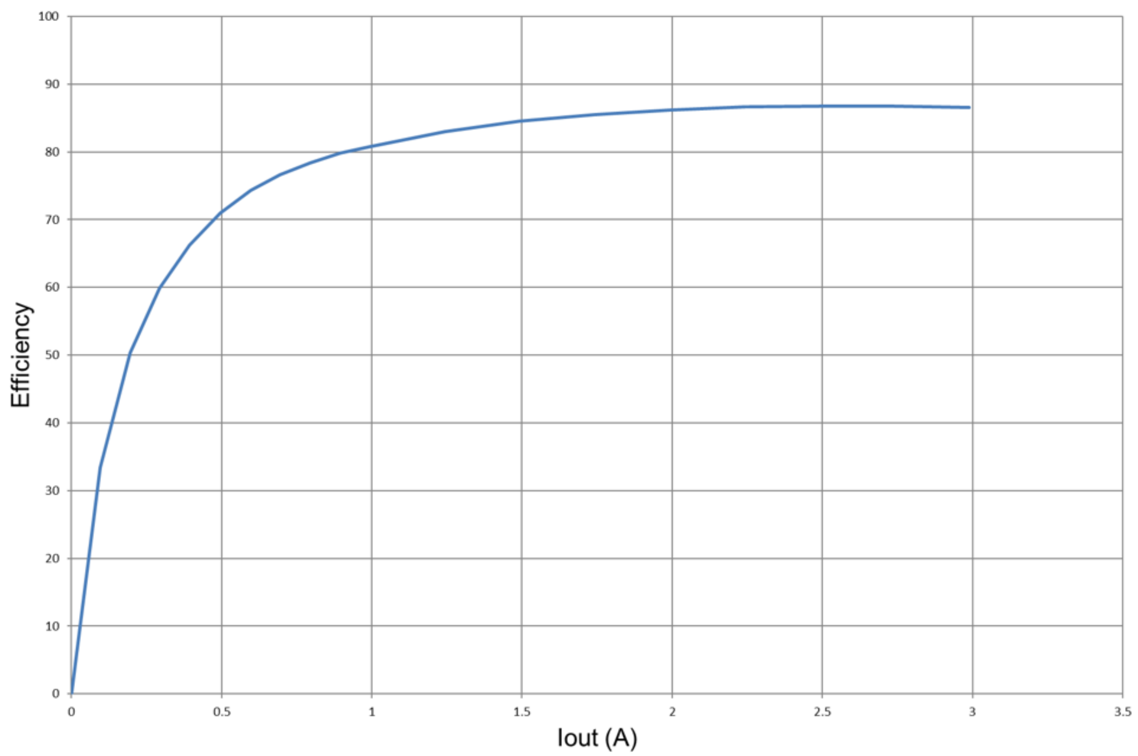


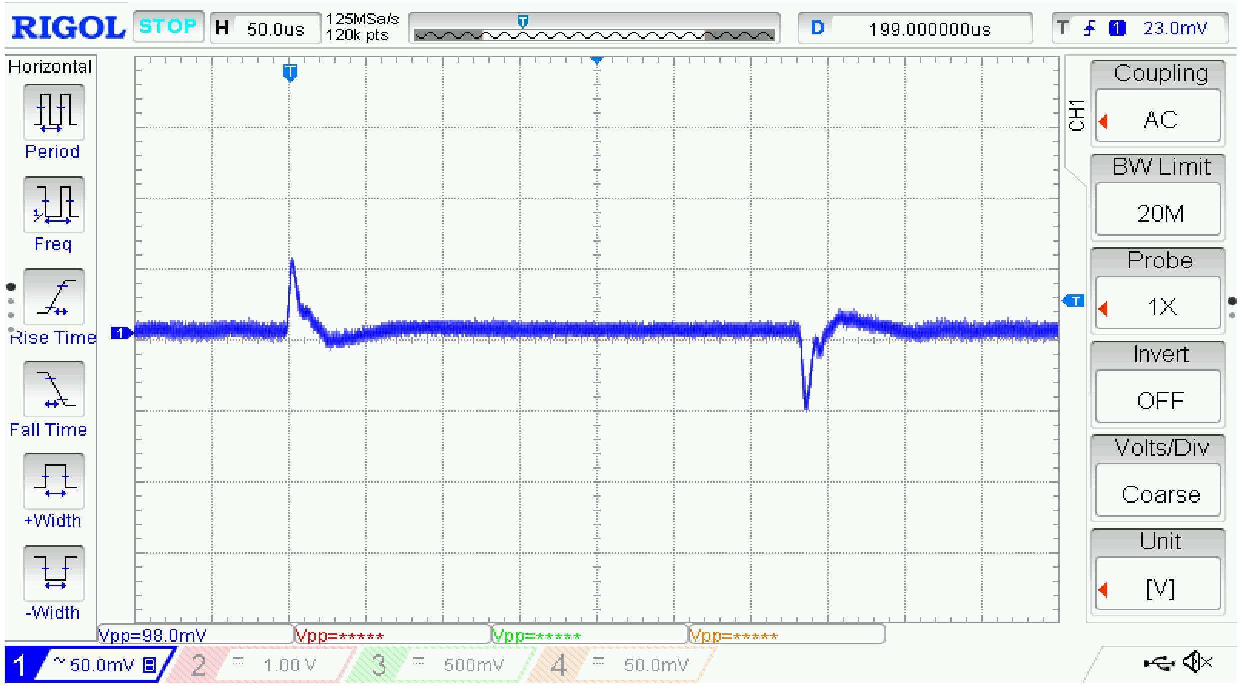


No Load Ripple
V_{PP} = 7.2 mV

Full Load Ripple
V_{PP} = 11.2 mV

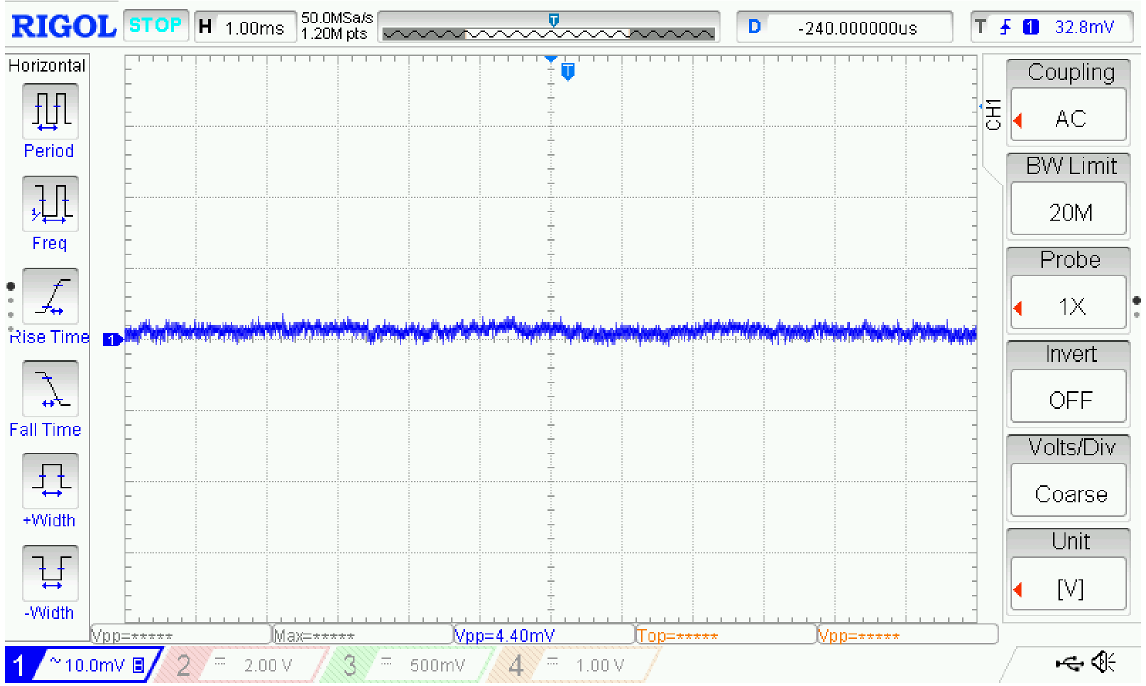
VCCAUX: Efficiency & Transient



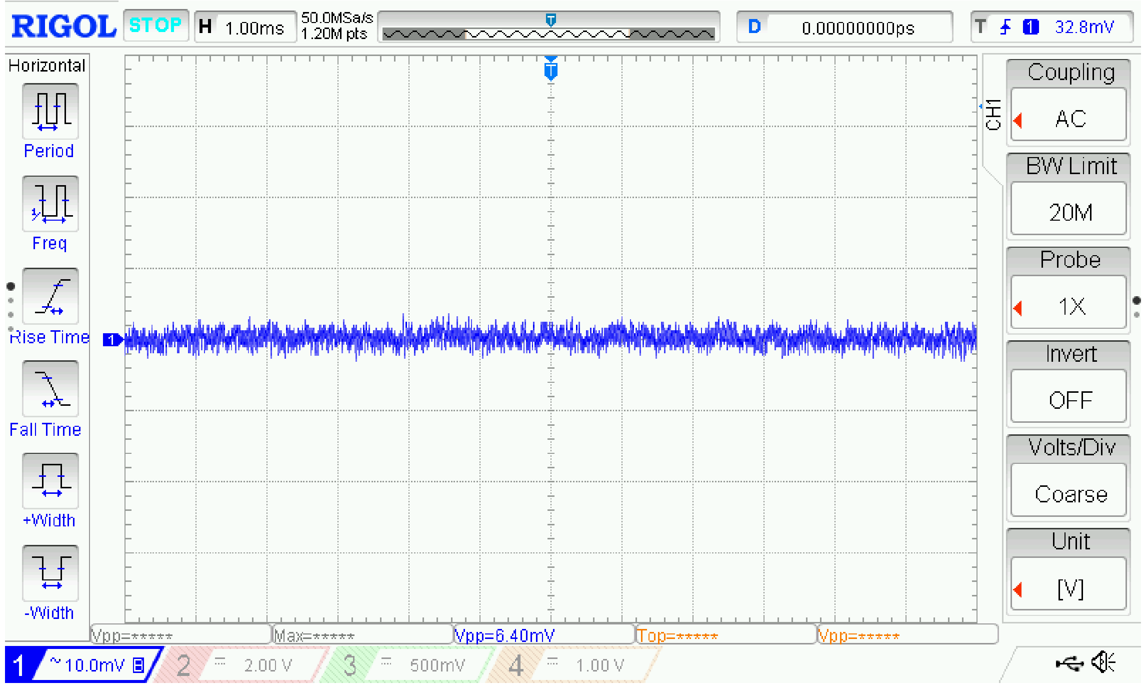


Vout = 1.8 V
Transient: 0.3 A – 3A @ 10 A/us
V_{PP} = 98 mV
Lout = 1.1 µH, Cout = 910 µF

VCCAUX: Ripple



No Load Ripple
V_{PP} = 4.4 mV



Full Load Ripple
V_{PP} = 6.4 mV

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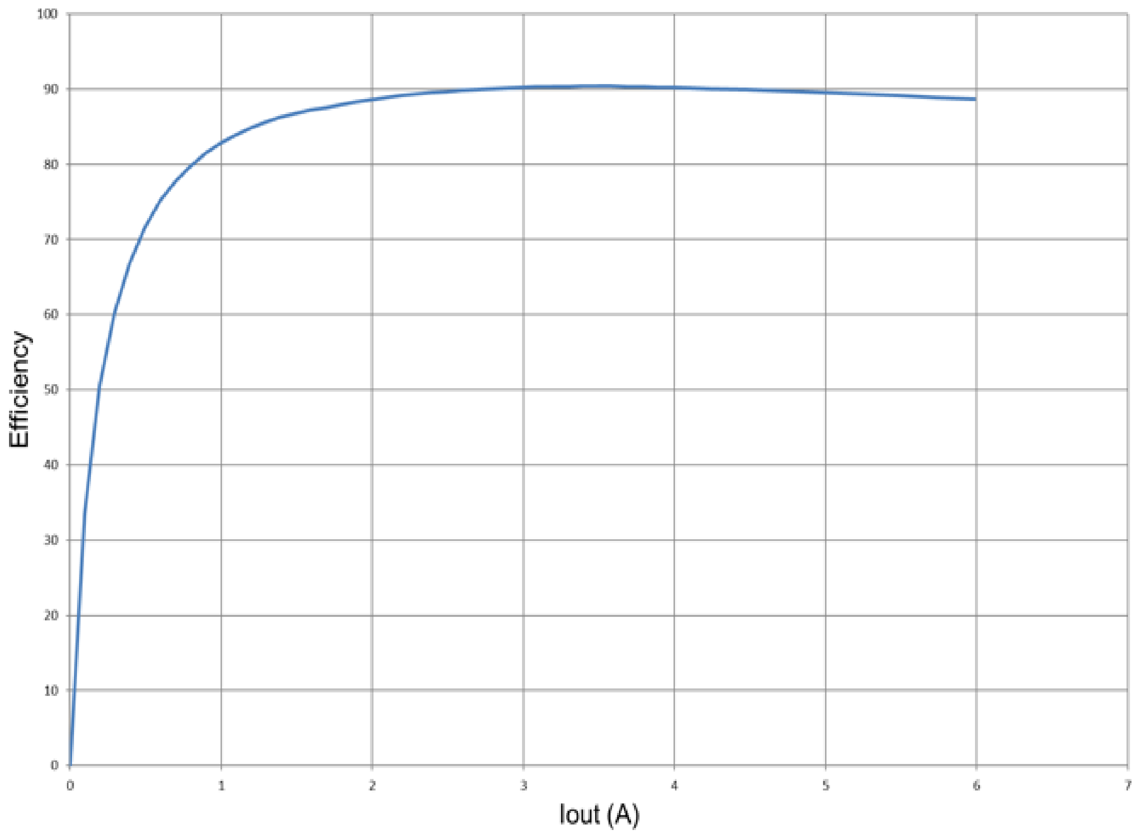
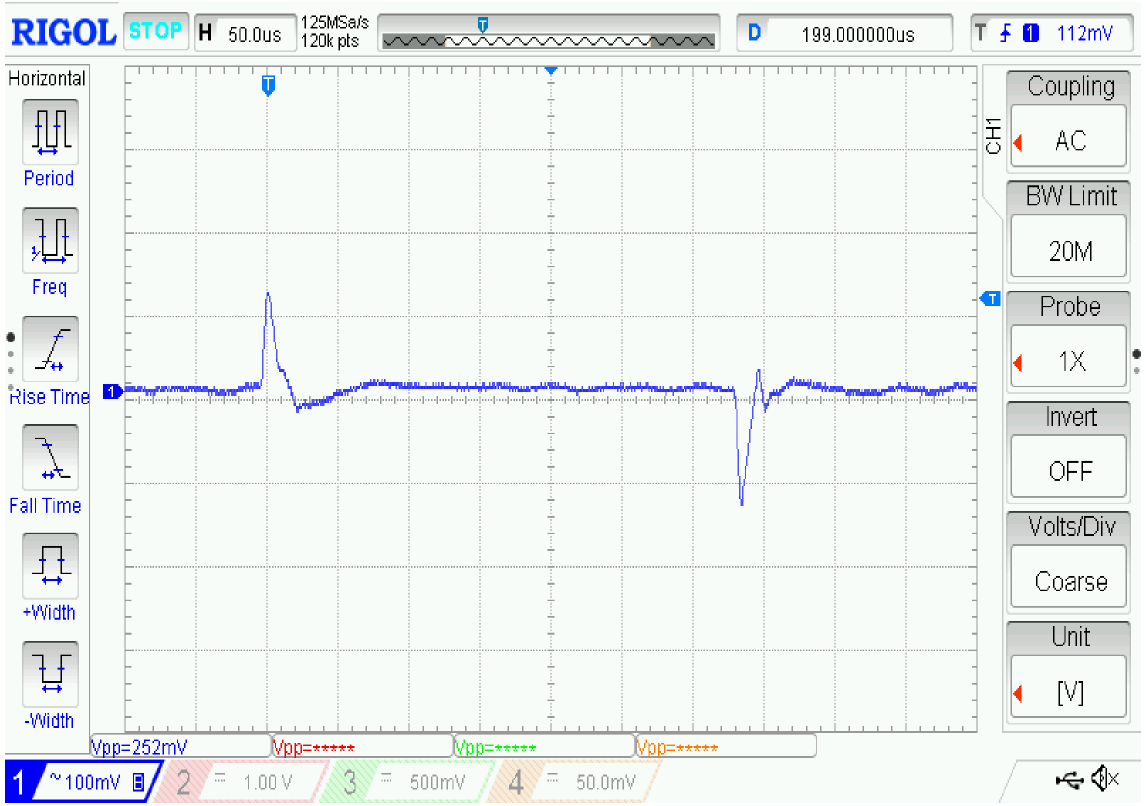
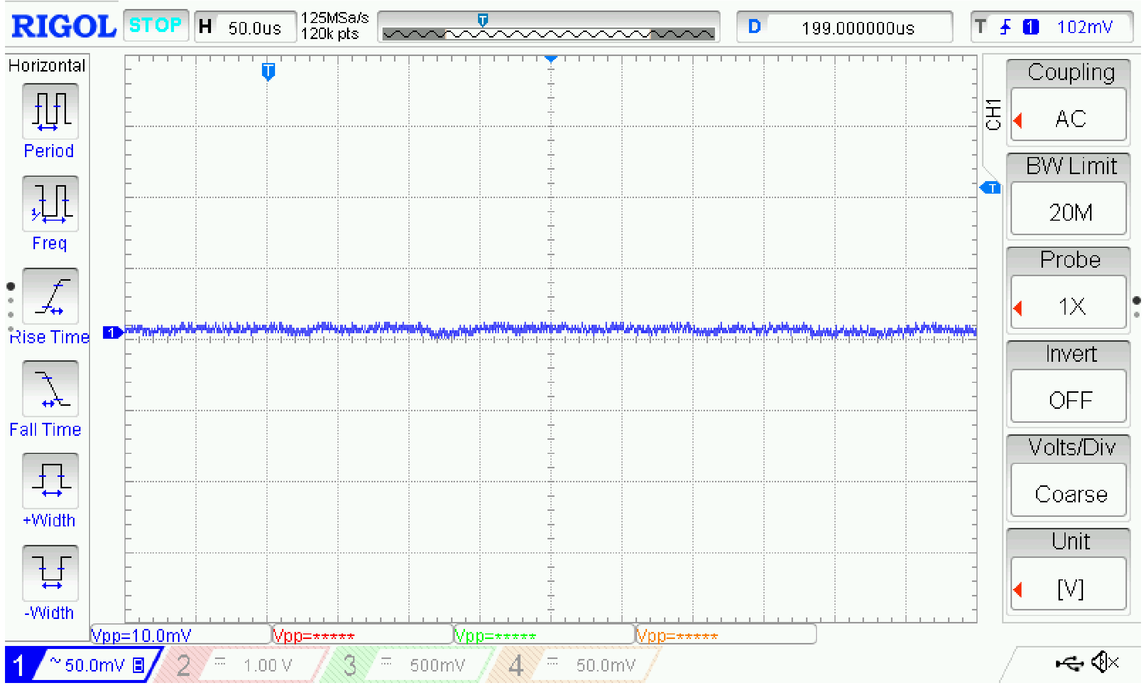
VCCO: Efficiency & Transient





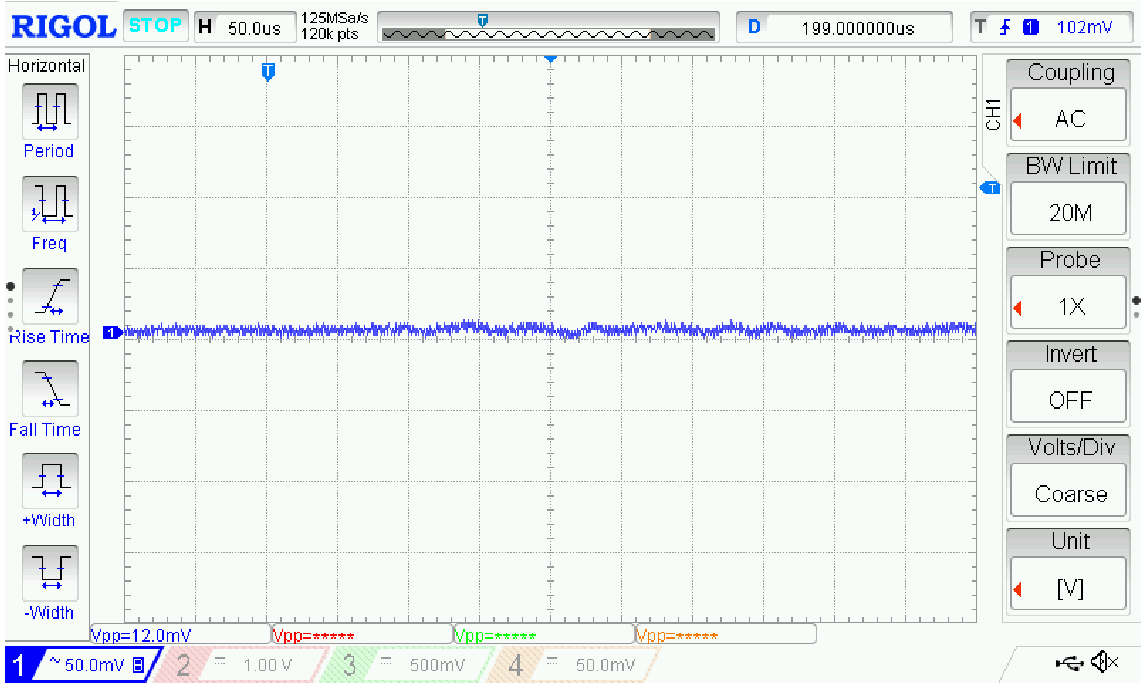
Vout = 3.3 V
Transient: 0.6 A – 6A @ 10 A/us
V_{PP} = 28 mV
Lout = 1.1 µH, Cout = 3 x 47 µF

VCCO: Ripple



No Load Ripple

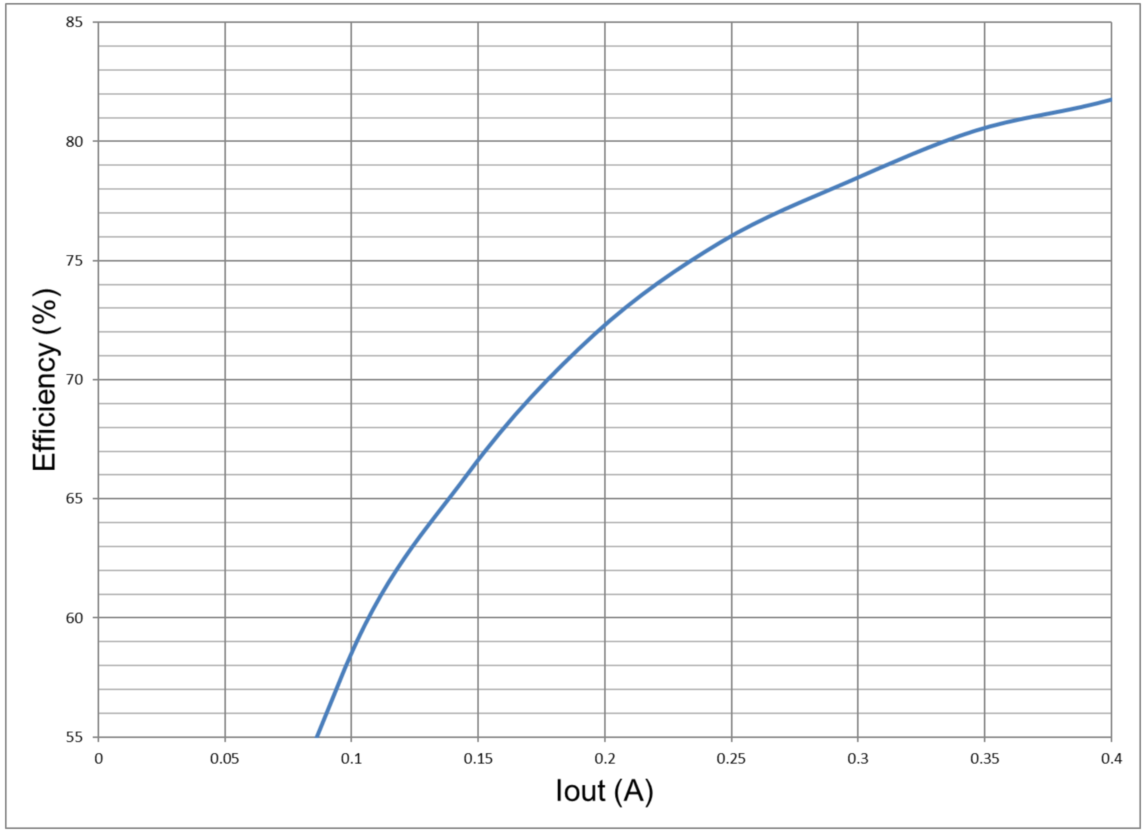
V_{PP} = 10 mV

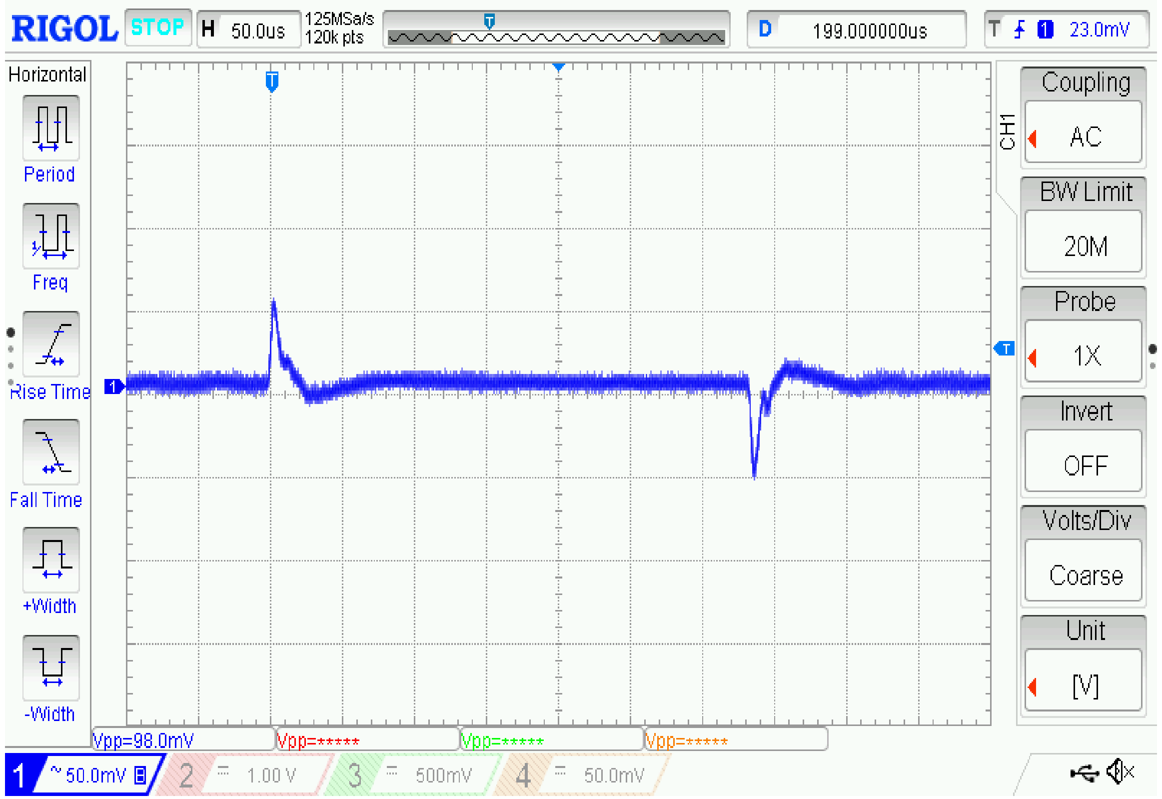


Full Load Ripple

V_{PP} = 12 mV

VPS_MGTAVTT: Efficiency & Transient





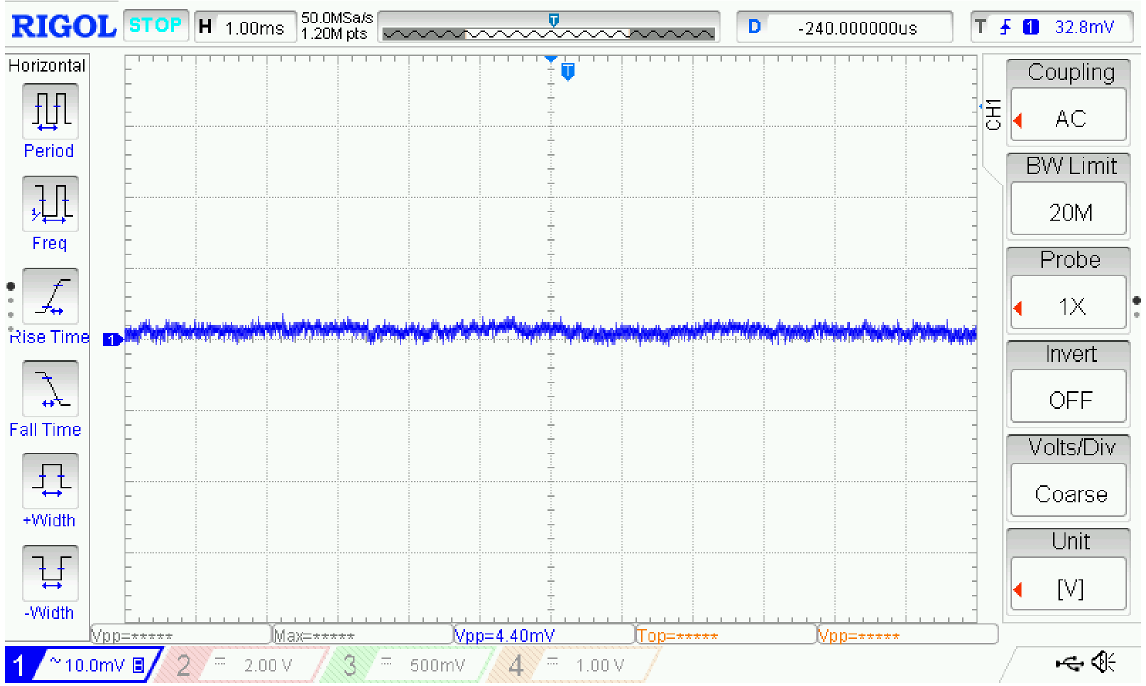
Vout = 1.8 V

Transient: 0.3 A – 3A @ 10 A/us

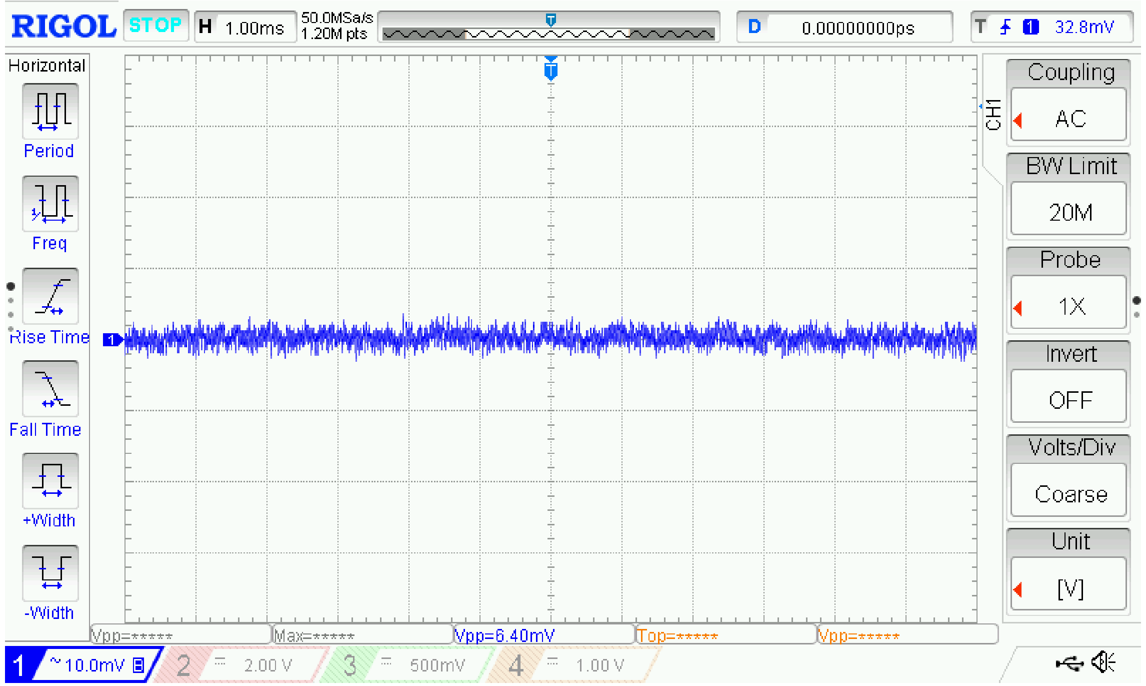
V_{PP} = 98 mV

Lout = 1.1 µH, Cout = 3 x 47 µF

VPS_MGTAVTT : Ripple

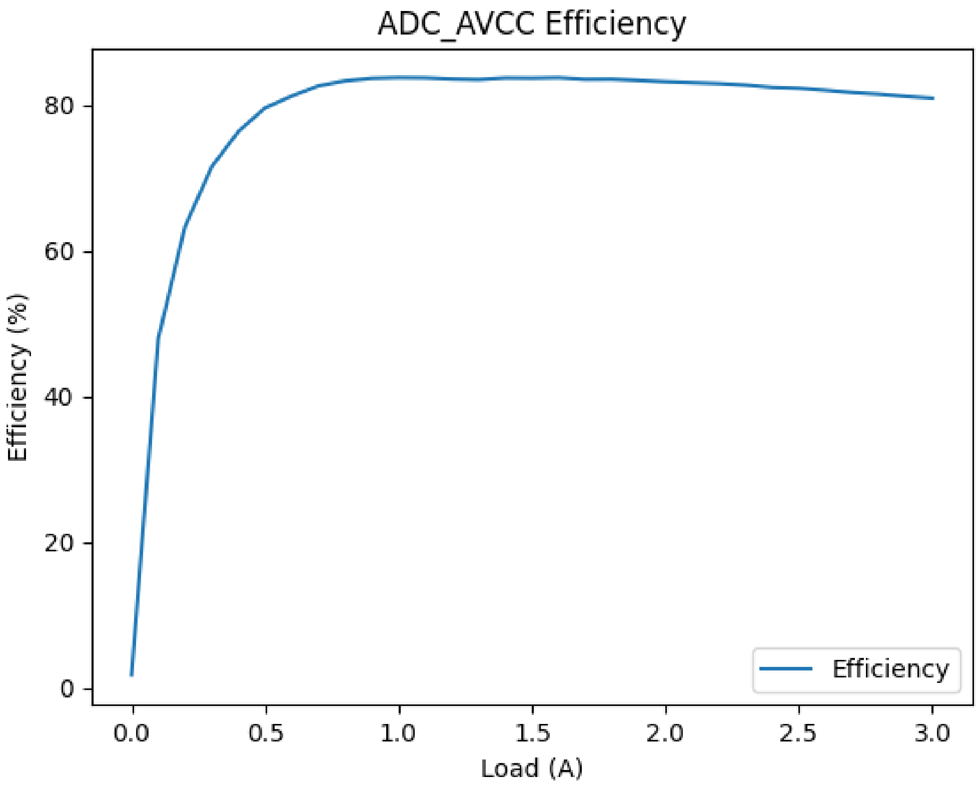


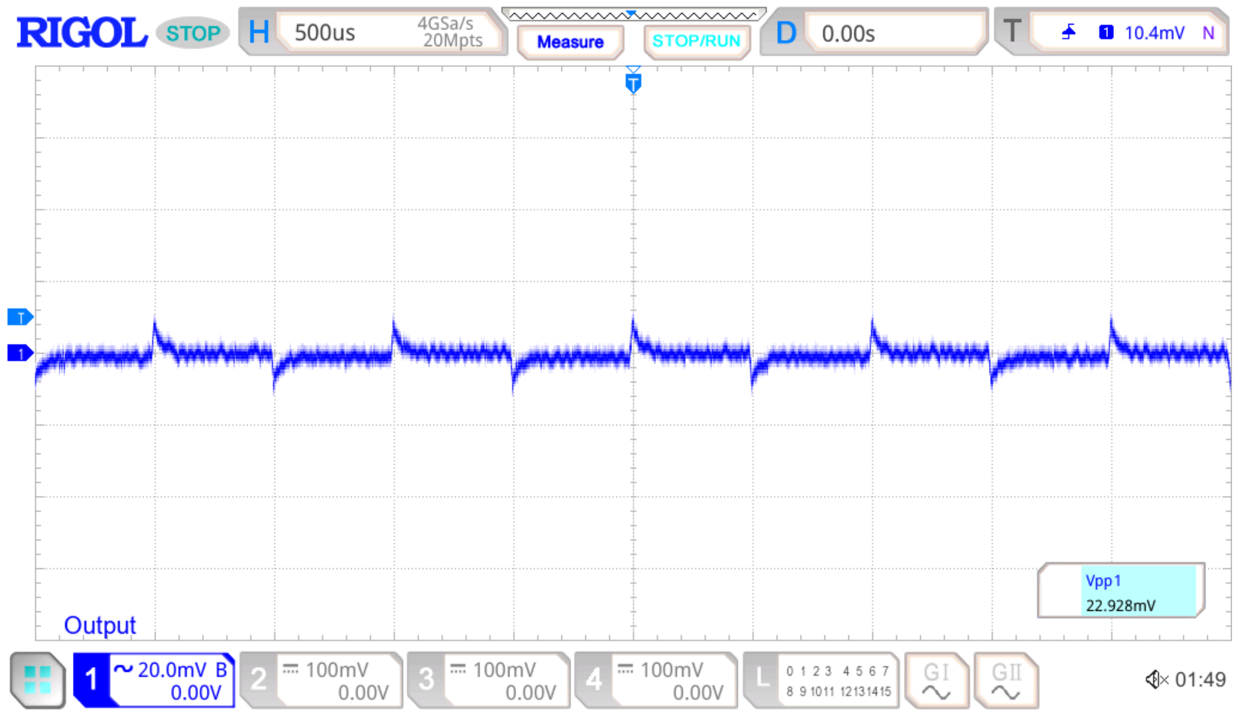
No Load Ripple
V_{PP} = 4.4 mV



Full Load Ripple
V_{PP} = 6.4 mV

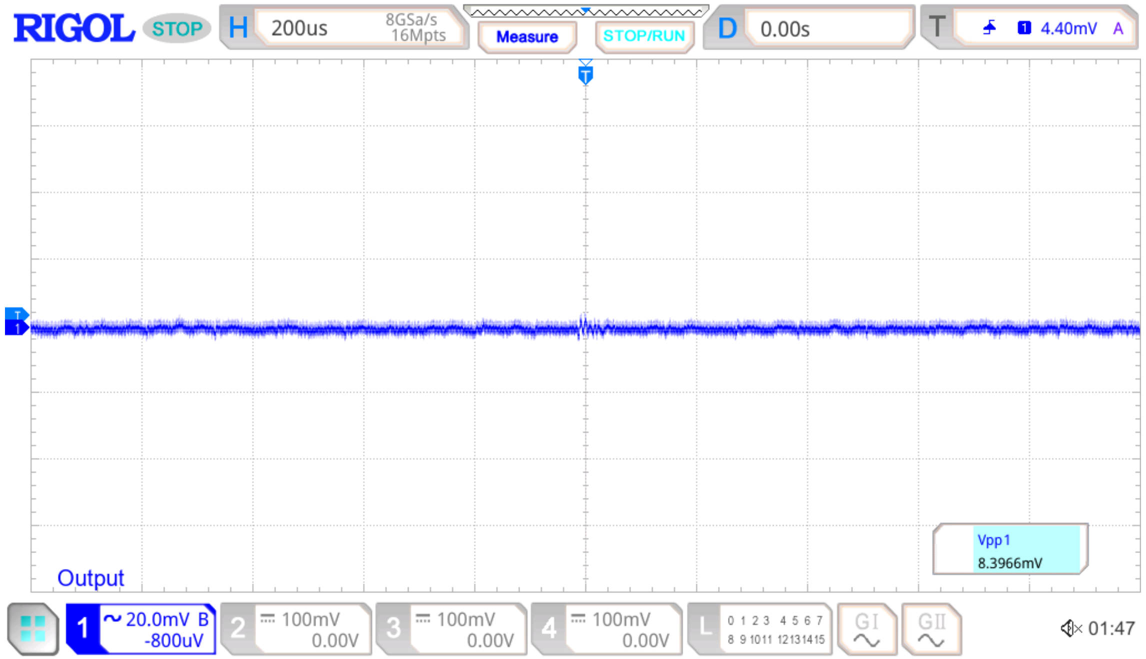
ADC_AVCC: Efficiency & Transient



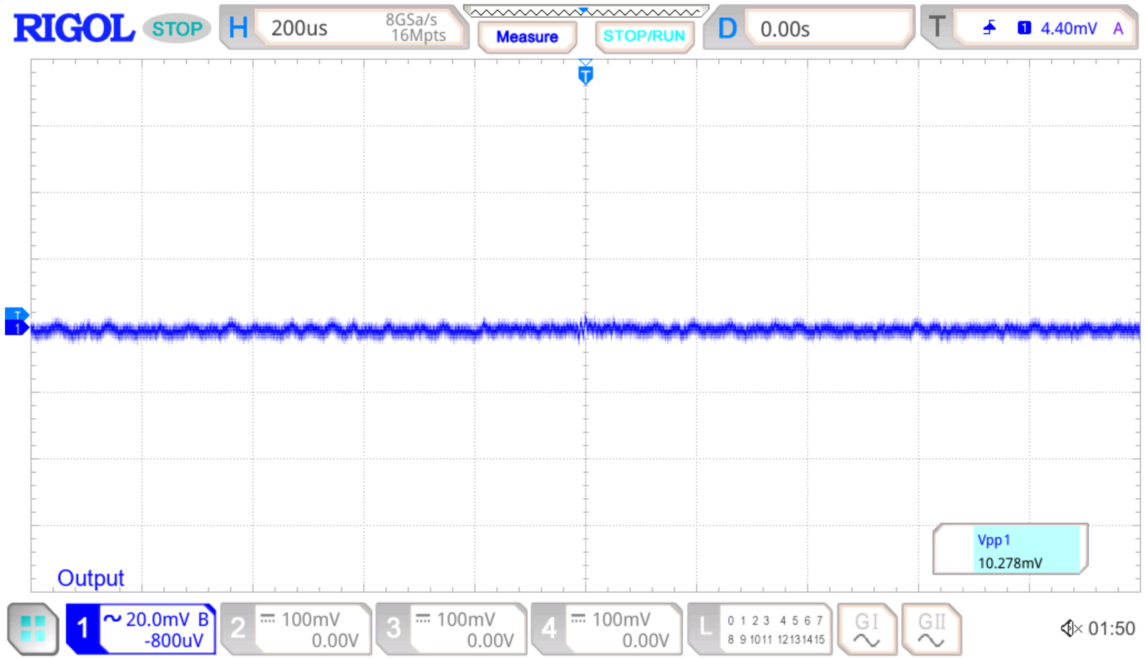


Vout = 0.925 V
Transient: 6.525 A – 8.7A @ 2.5 A/us
V_{PP} = 22.9 mV
Lout = 0.56 µH, Cout = 9 x 47 µF

ADC_AVCC: Ripple

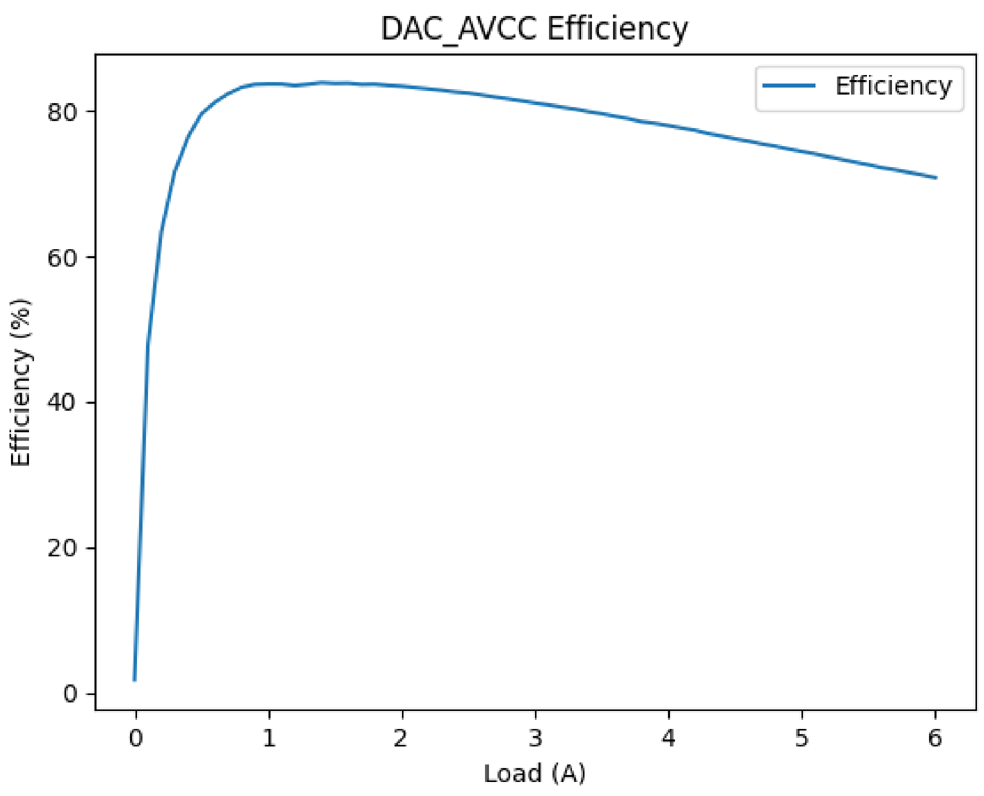


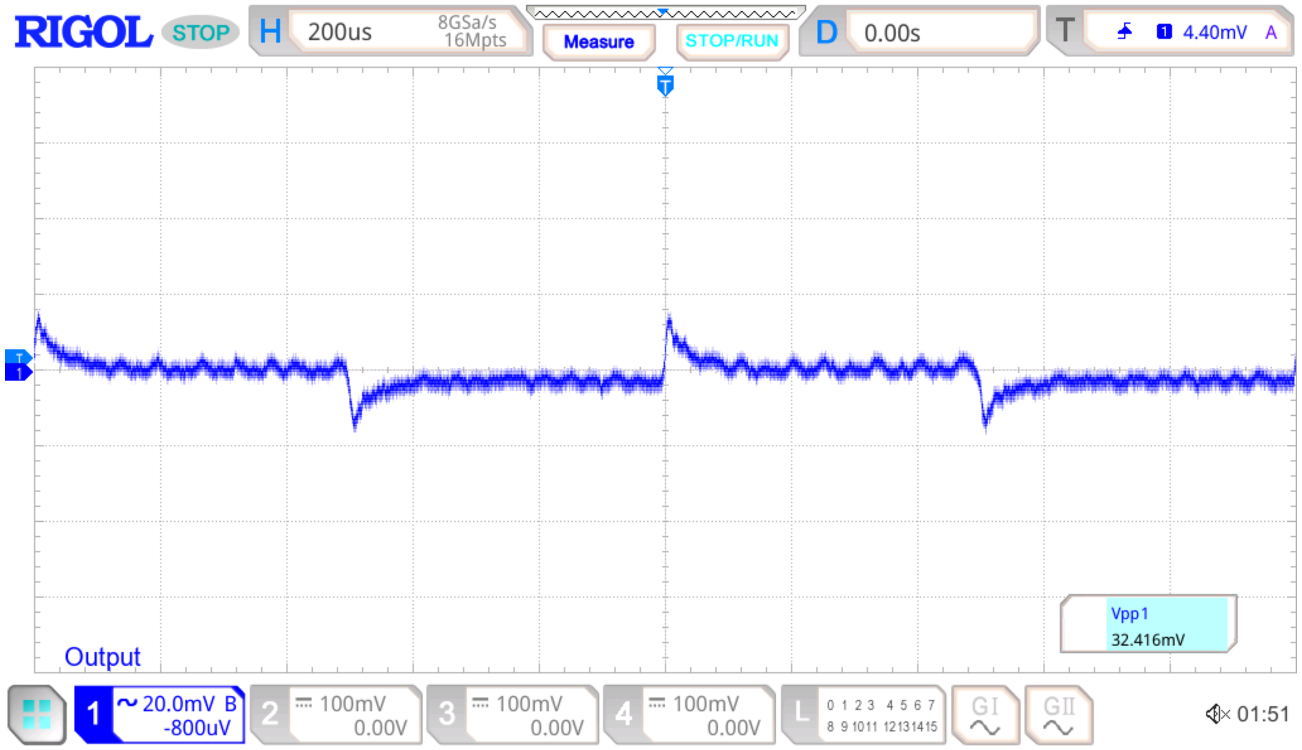
No Load Ripple
V_{PP} = 8.3 mV



Full Load Ripple
V_{PP} = 10.3 mV

DAC_AVCC: Efficiency & Transient





Vout = 0.925 V

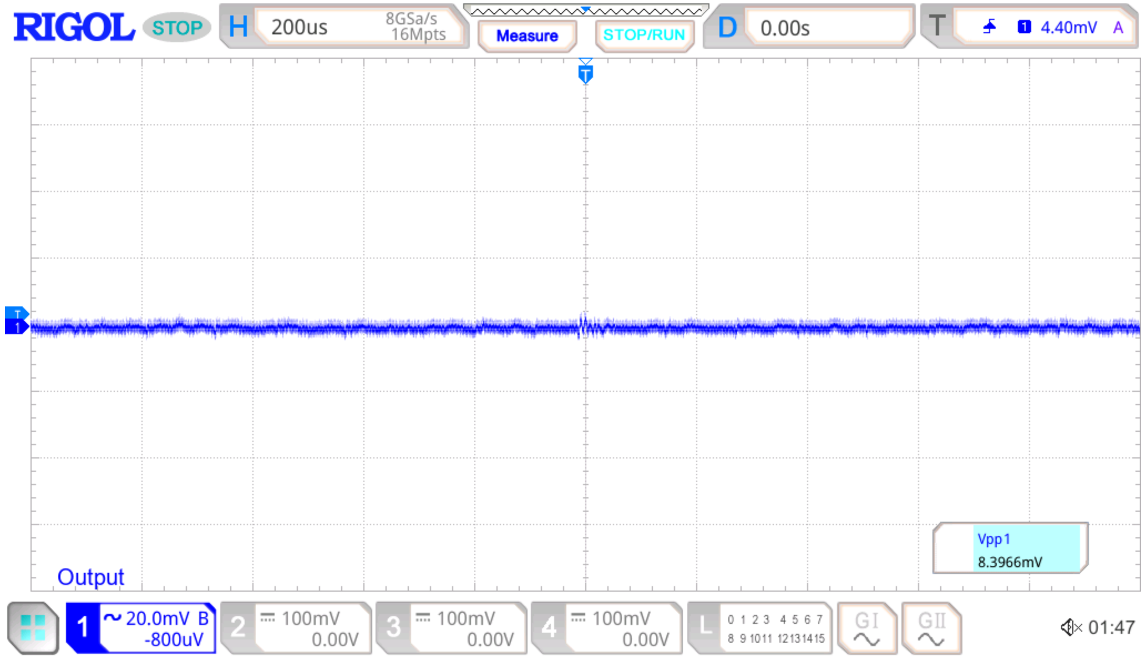
Transient: 4.5 A – 6A @ 2.5 A/us

V_{PP} = 32.4 mV

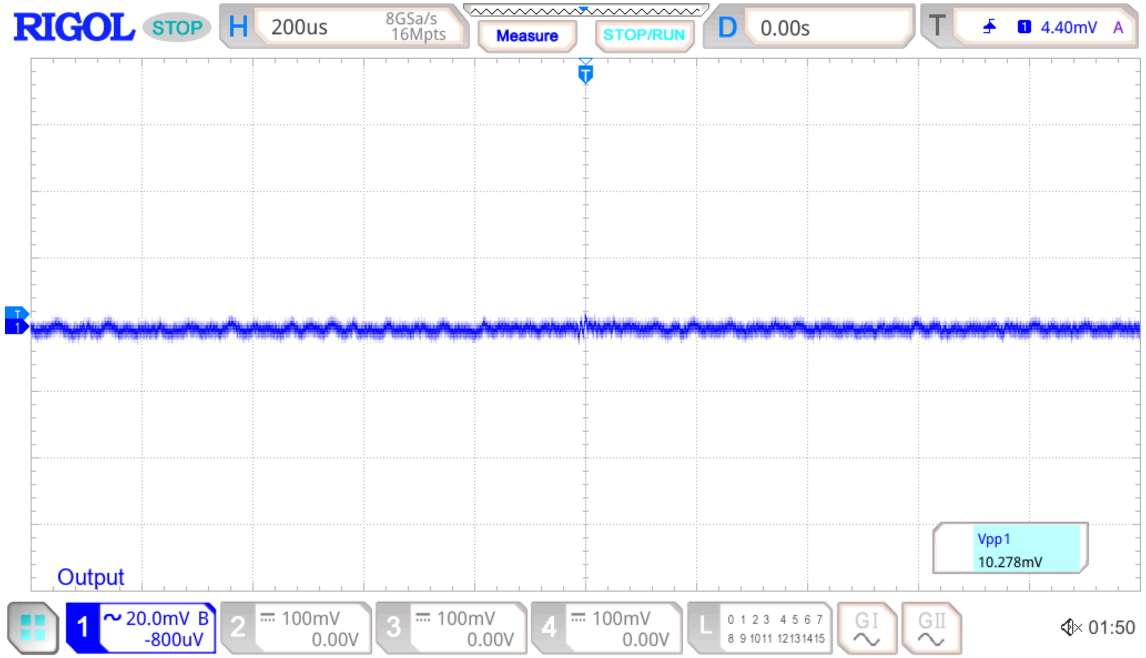
Lout = 0.56 µH, Cout = 9 x 47 µF

AnDAPT

DAC_AVCC: Ripple



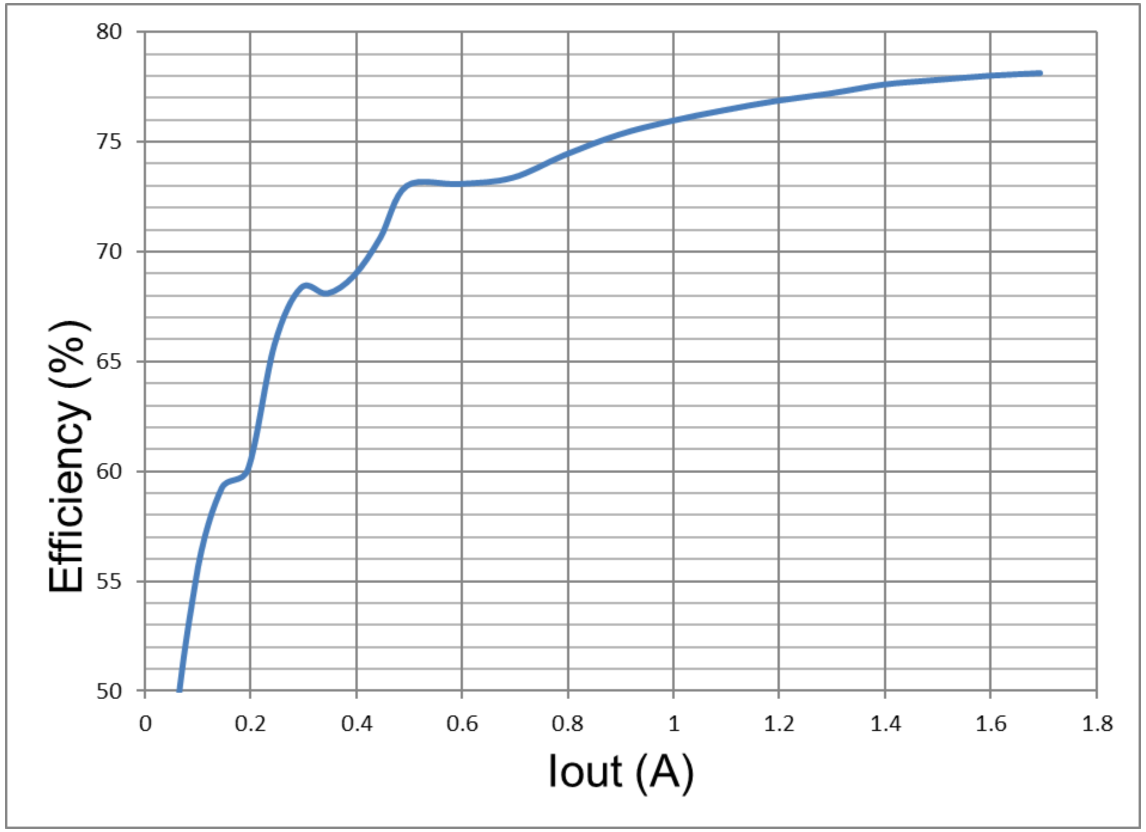
No Load Ripple
V_{PP} = 8.3 mV

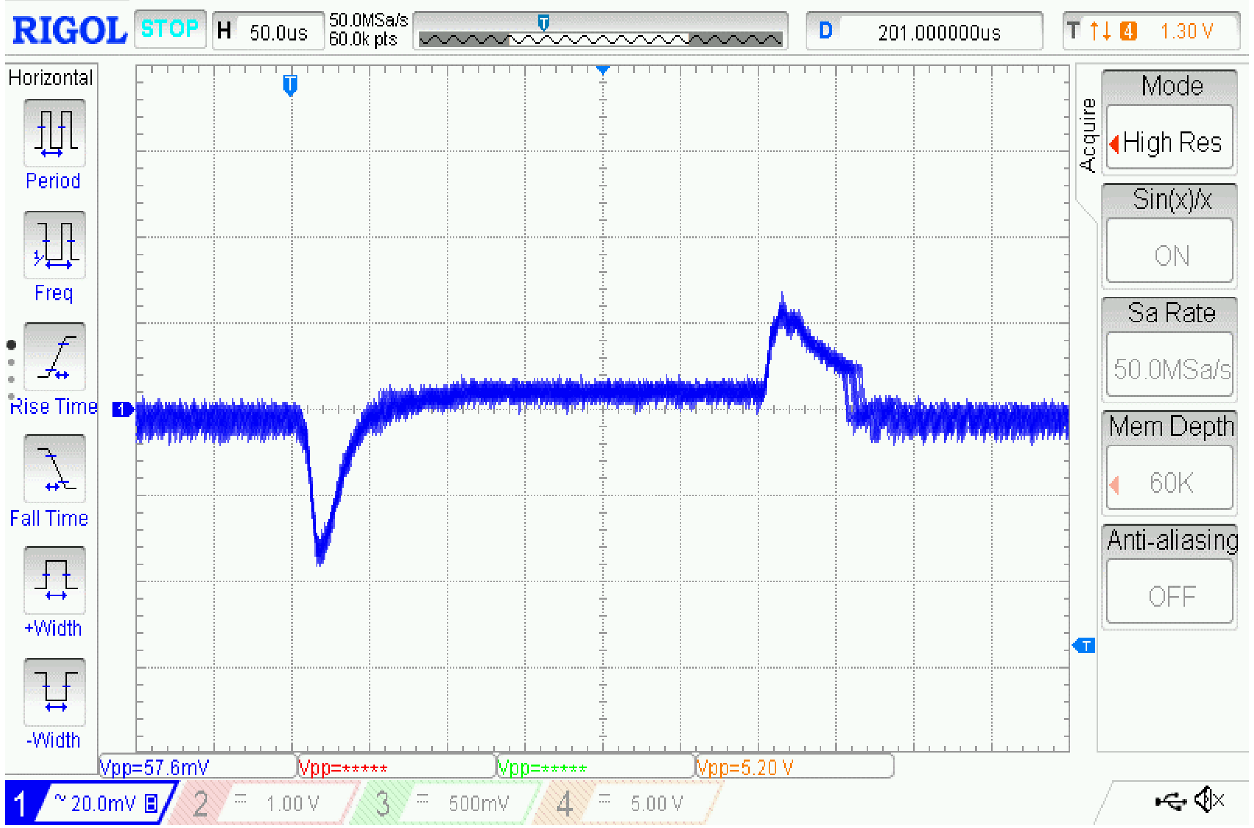


Full Load Ripple
V_{PP} = 10.3 mV

AnDAPT

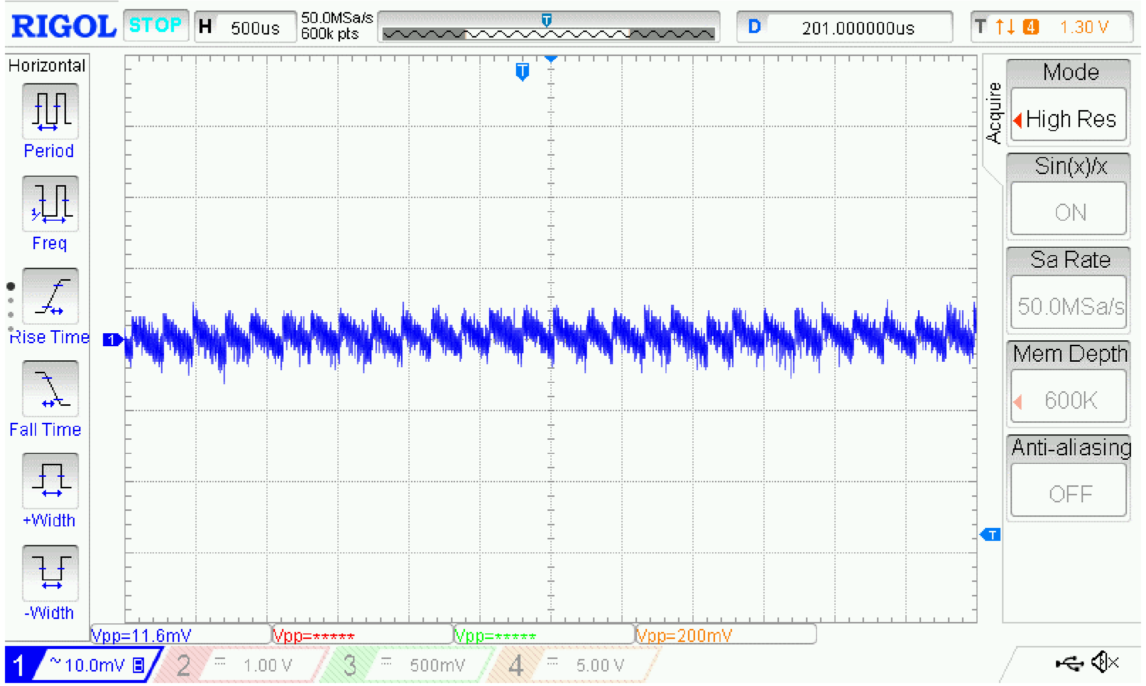
ADC_AVCCAUX: Efficiency & Transient



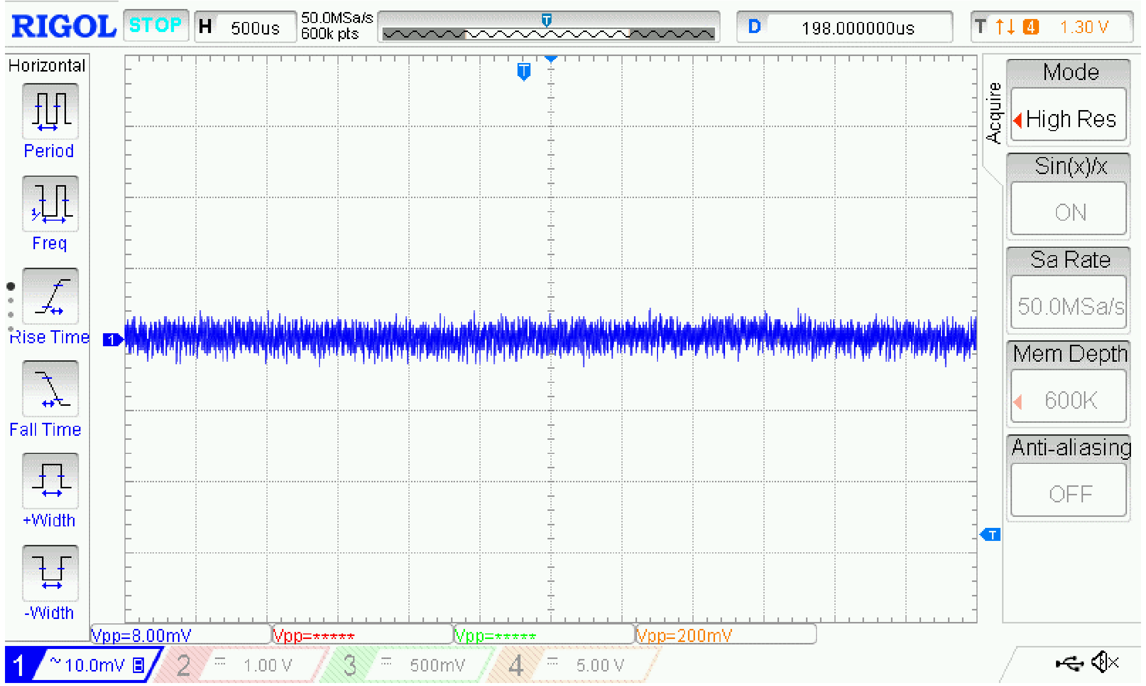


Vout = 1.8 V
Transient: 0.16A – 1.6A @ 2.5 A/us
V_{PP} = 57.8 mV
Lout = 2.2 µH, Cout = 94 µF

ADC_AVCCAUX: : Ripple

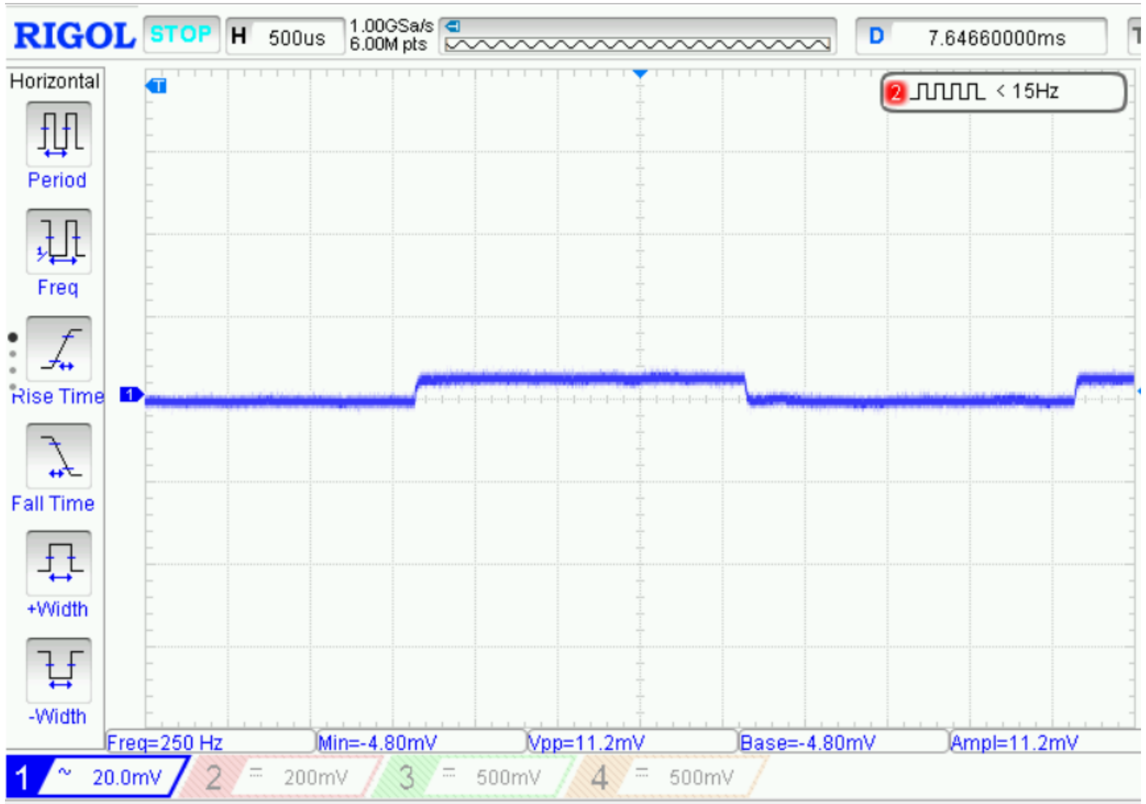


No Load Ripple
V_{PP} = 11.6 mV



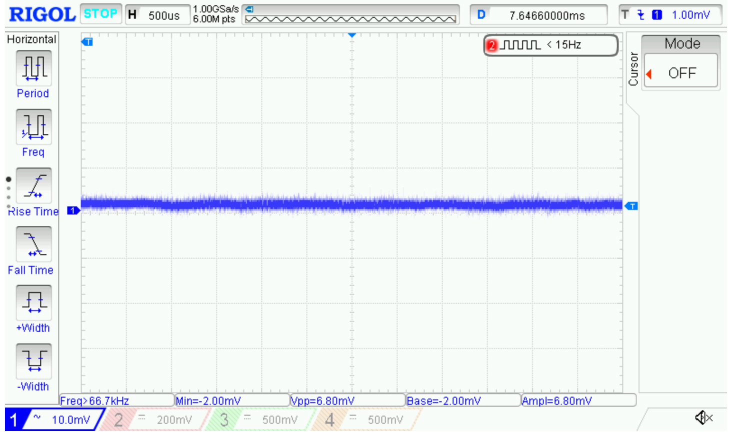
Full Load Ripple
V_{PP} = 8 mV

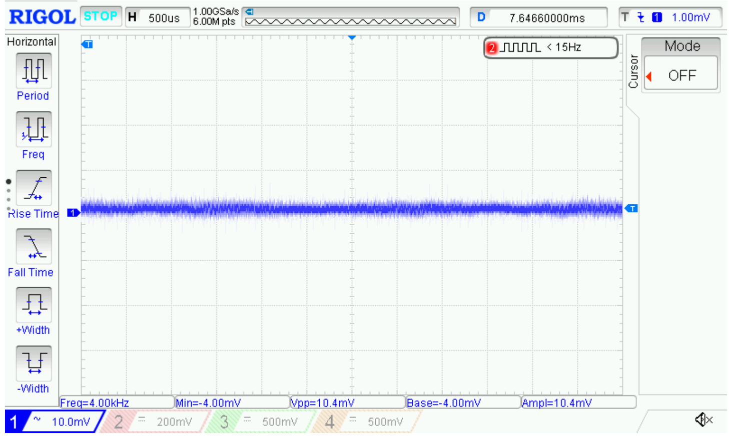
DAC_AVCCAUX: Transient

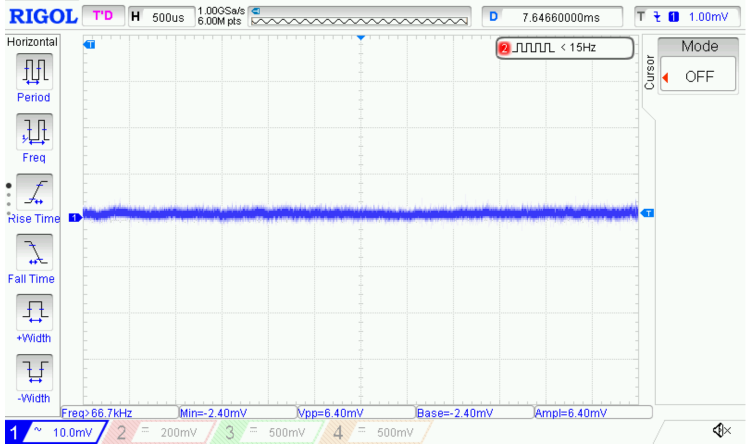


Vin = 2.5V Vout = 1.8 V
Transient: 0.36A - 0.72A @ 2.5 A/us
V_{PP} = 11.2 mV
Cout = 22 µF
Internal Feedback

DAC_AVCCAUX: Ripple







No Load Ripple
V_{PP} = 6.8 mV

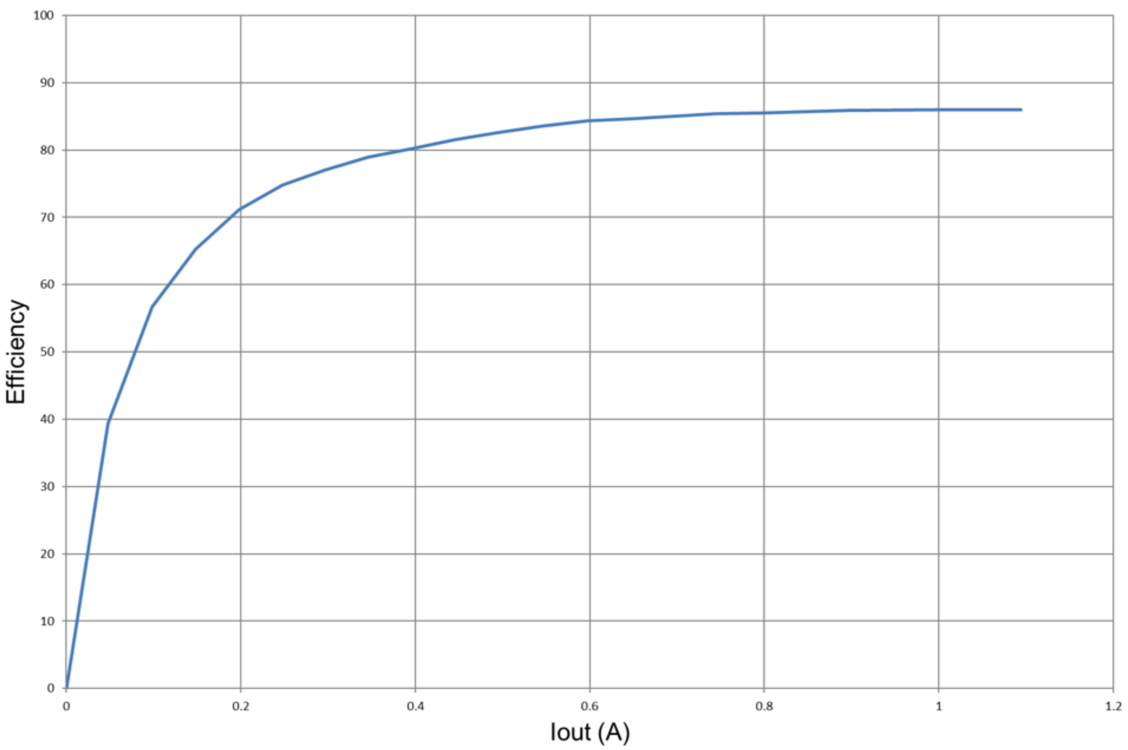
200mA Ripple
V_{PP} = 10.4 mV

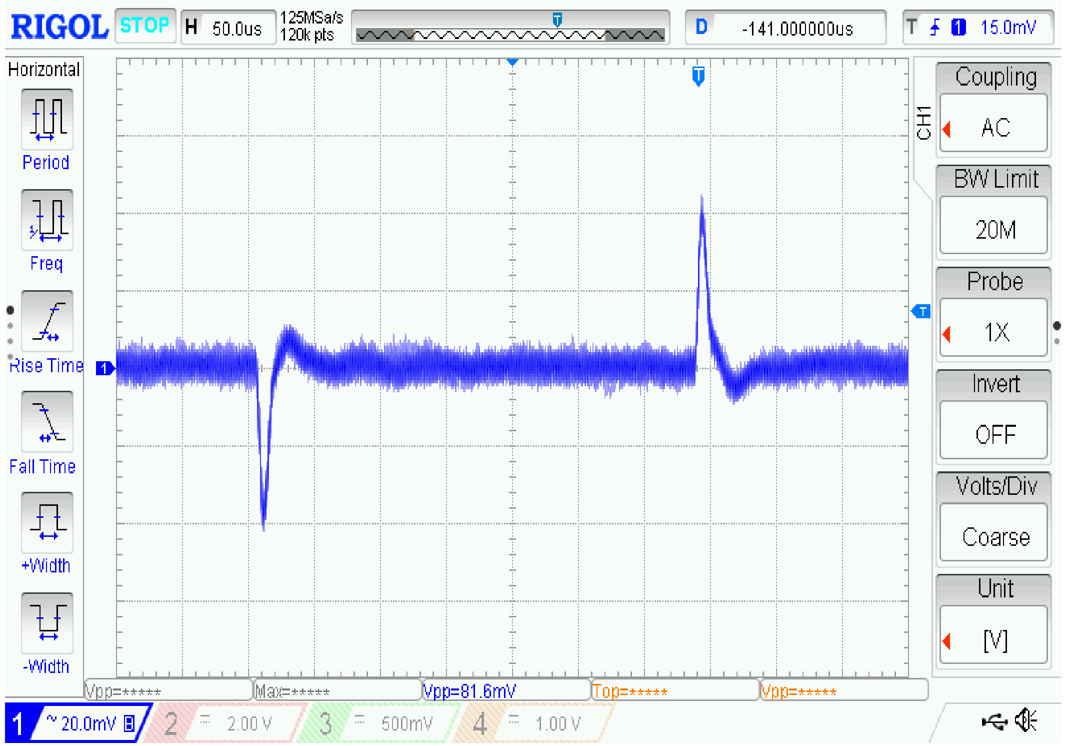
Full Load Ripple
V_{PP} = 6.4 mV

Internal Feedback

AnDAPT

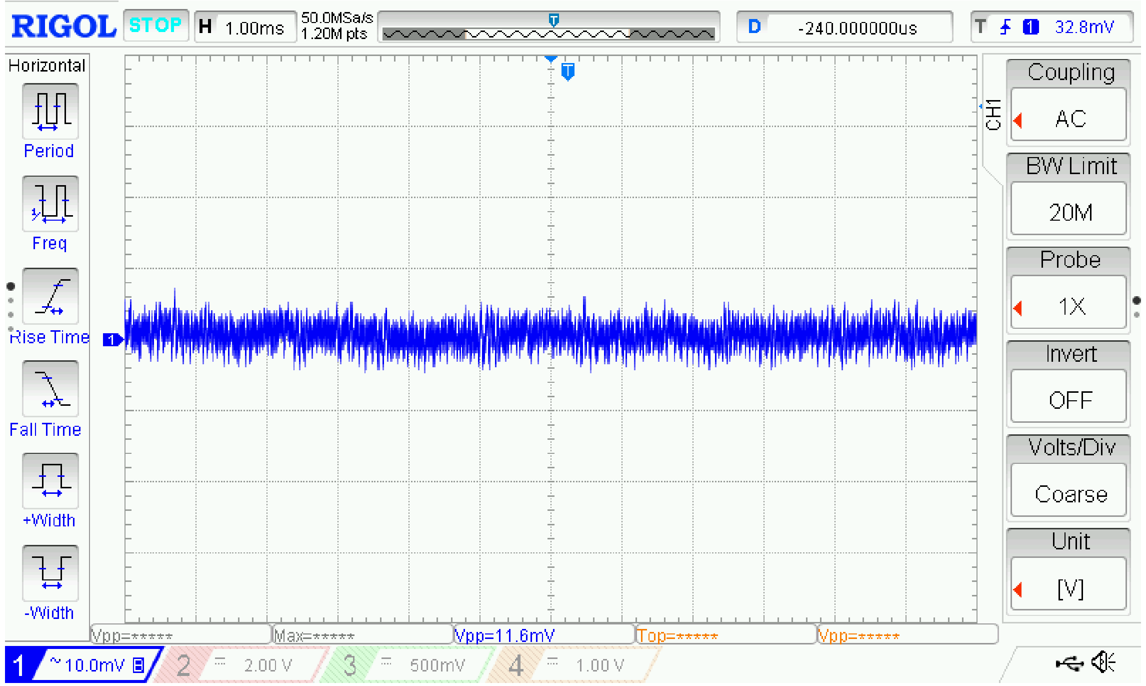
DAC_AVTT: Efficiency & Transient



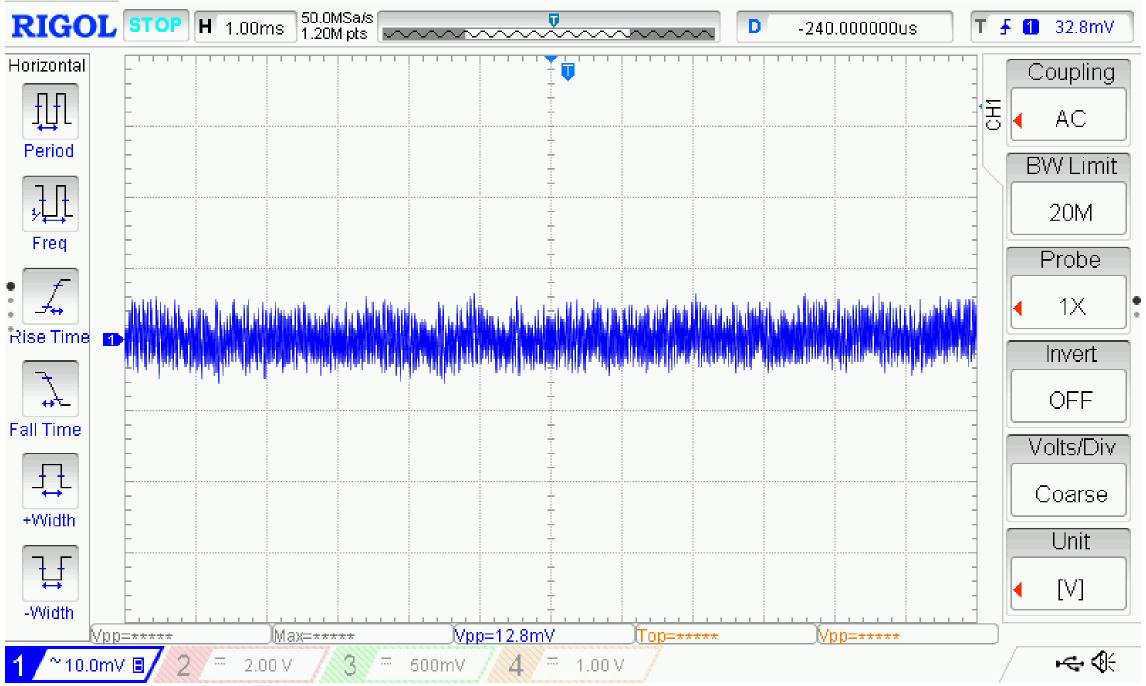


Vout = 2.5 V
Transient: 0.2 A – 1A @ 10 A/us
V_{PP} = 81.6 mV
Lout = 4.7 µH, Cout = 47 µF

DAC_AVTT: Ripple



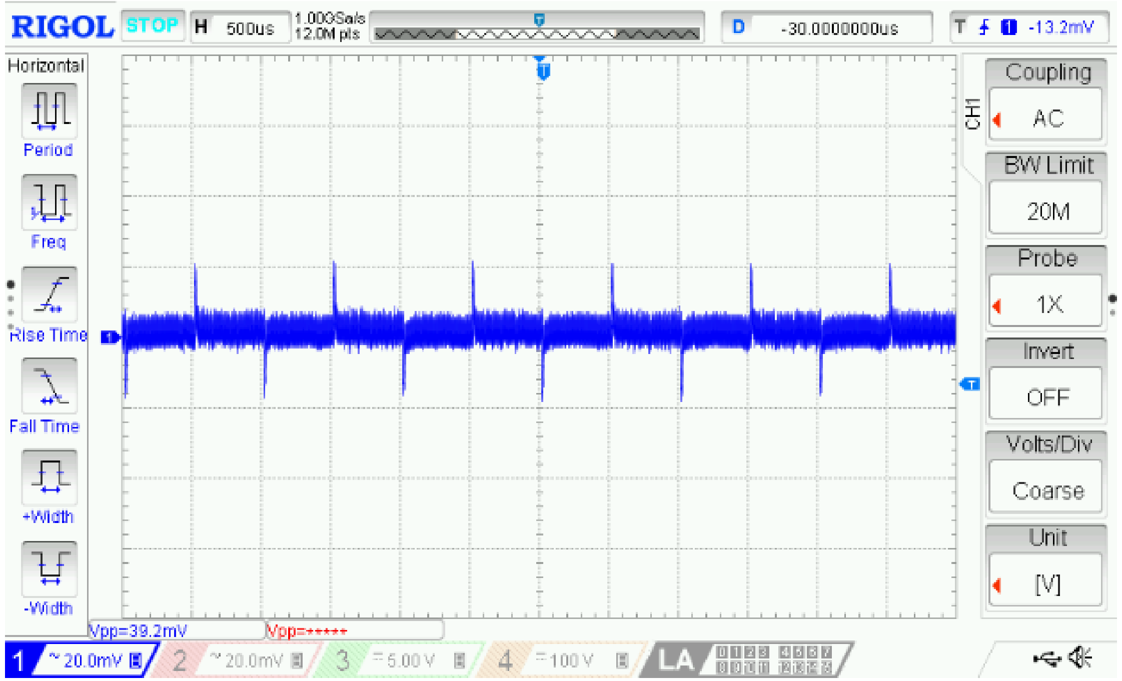
No Load Ripple
V_{PP} = 11.6 mV



Full Load Ripple
V_{PP} = 12.8 mV

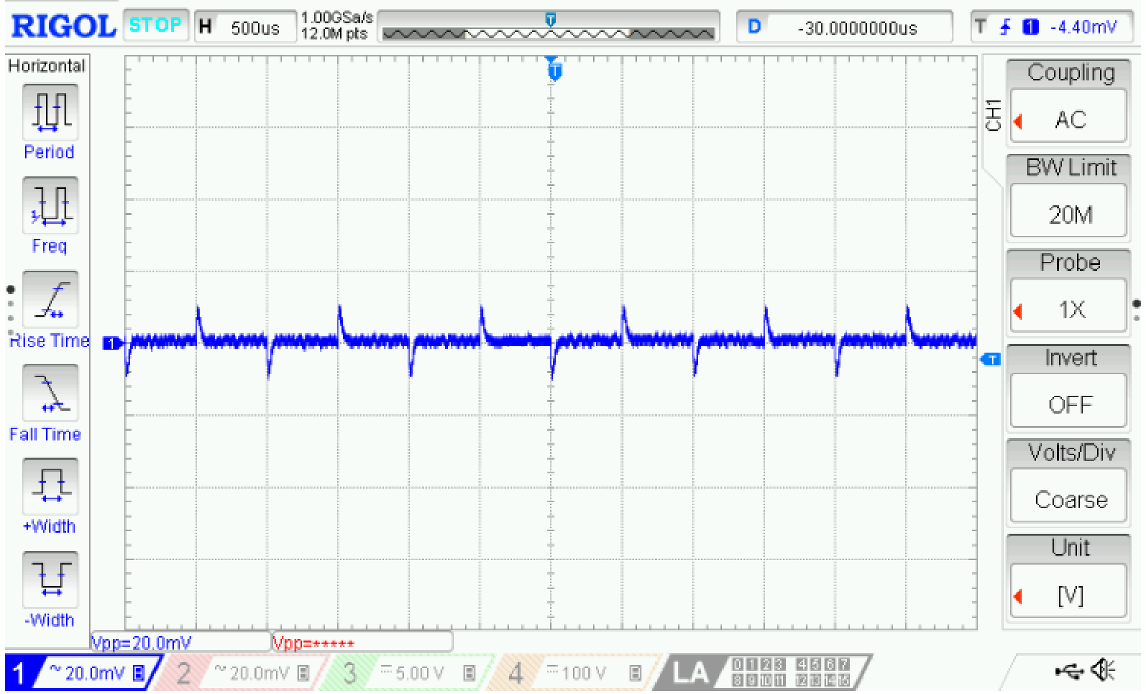
DDR4 Rails - Transient

C200



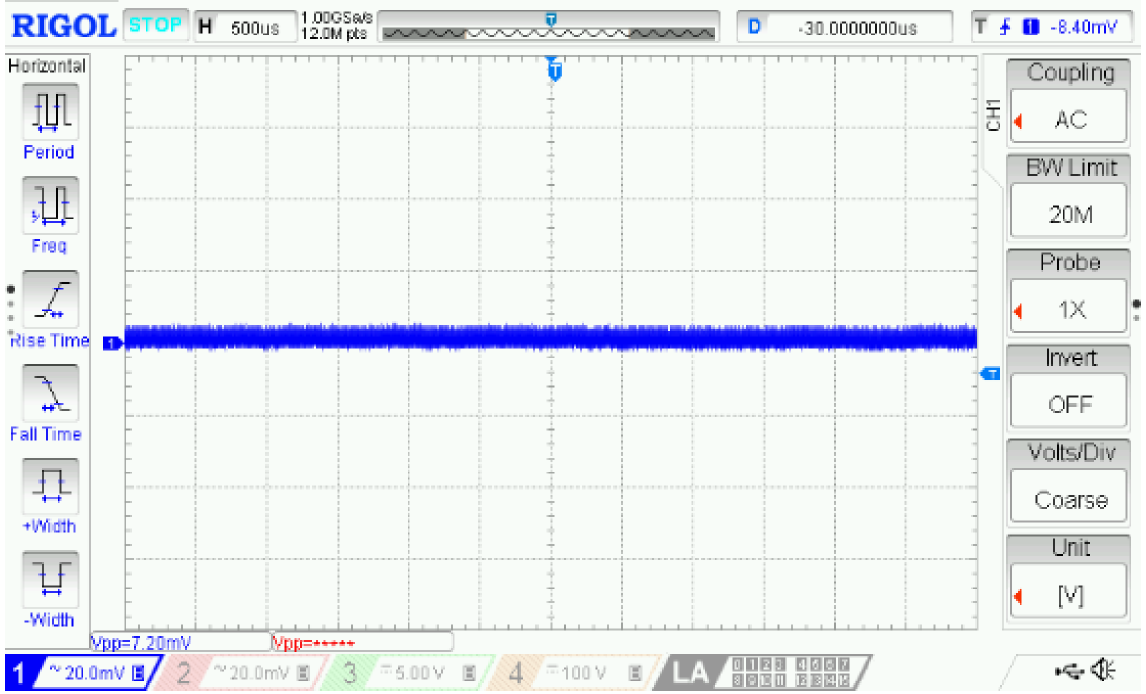
Vout = 1.2 V
Transient: 0.2 A – 1A @ 2.5 A/us
V_{PP} = 39.2 mV
Lout = 0.47 µH, Cout = 4 x 47 µF

C210

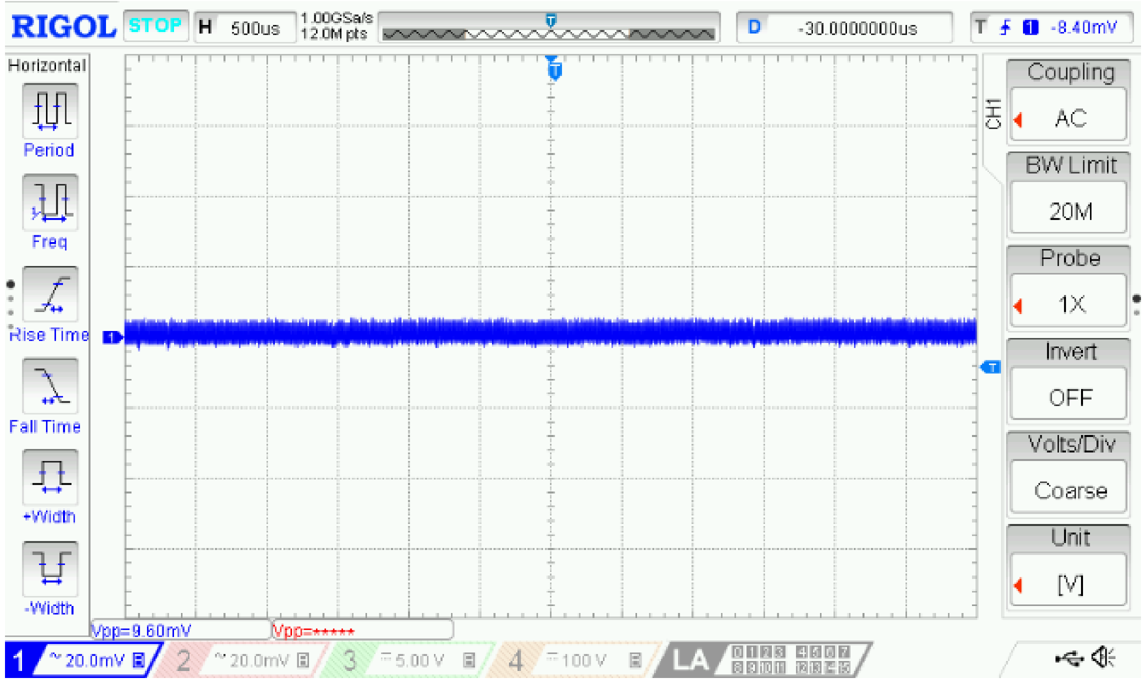


Vout = 0.6 V
Transient: 0.2 A – 1A @ 2.5 A/us
V_{PP} = 20 mV
Lout = 0.68 µH, Cout = 3 x 47 µF

DDR4 Rails: Ripple (C200)

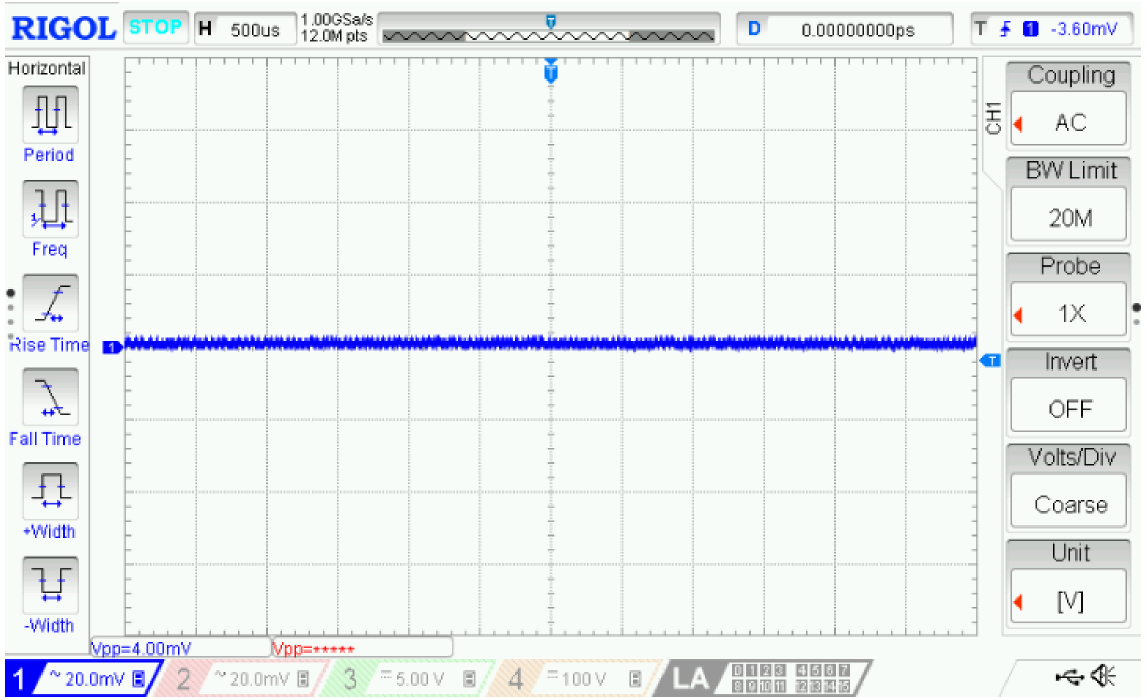


No Load Ripple
V_{PP} = 7.2 mV



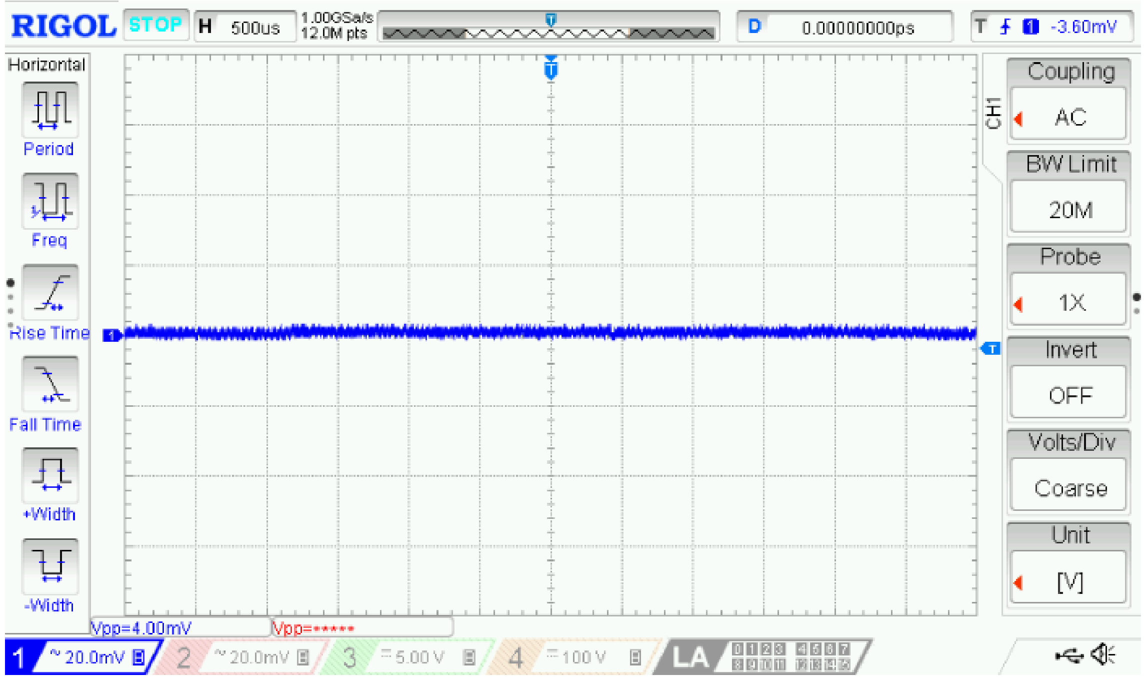
Full Load Ripple
V_{PP} = 9.6 mV

DDR4 Rails: Ripple (C210)



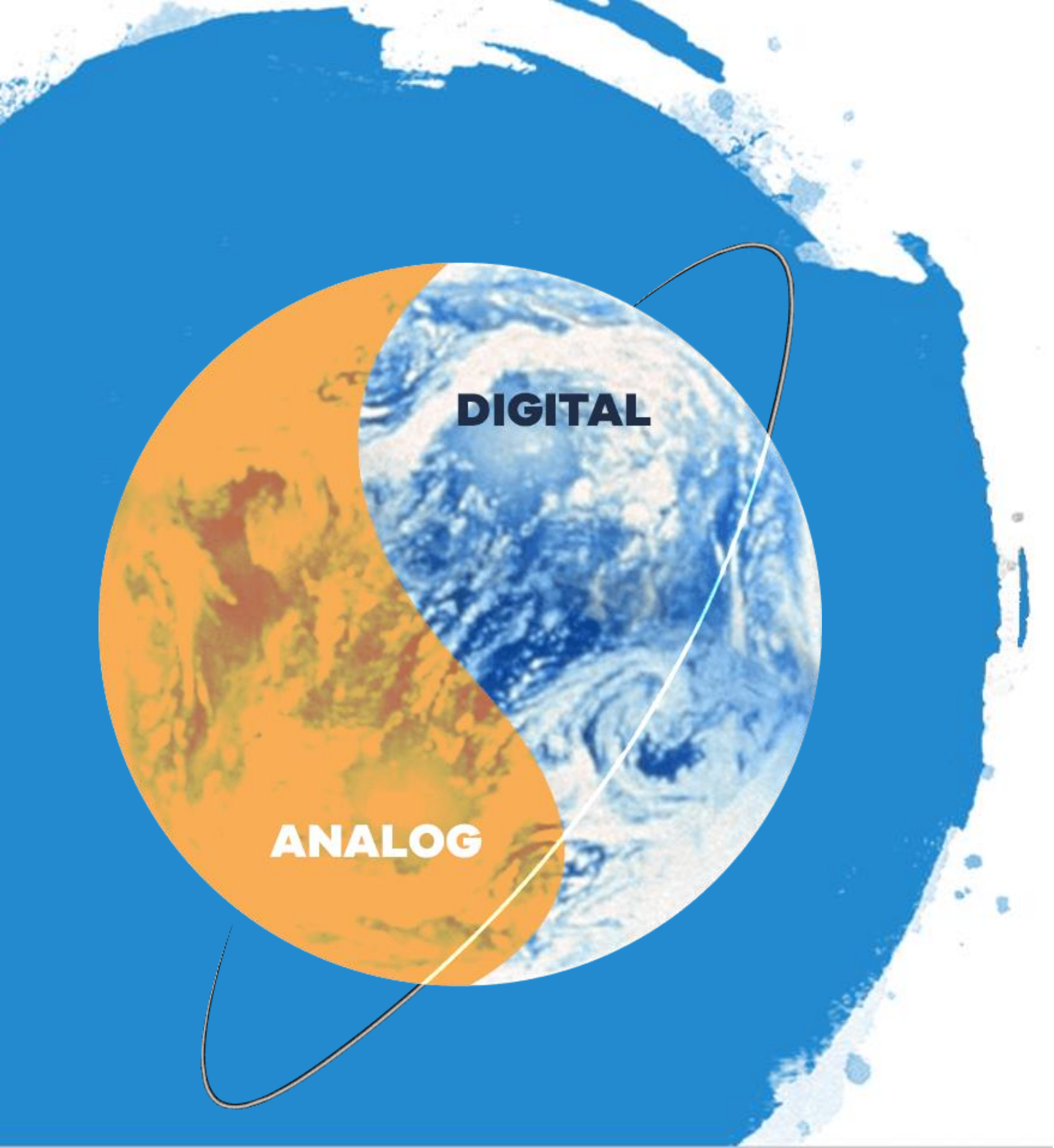
No Load Ripple

V_{PP} = 4 mV



Full Load Ripple

V_{PP} = 4 mV



Thank You