

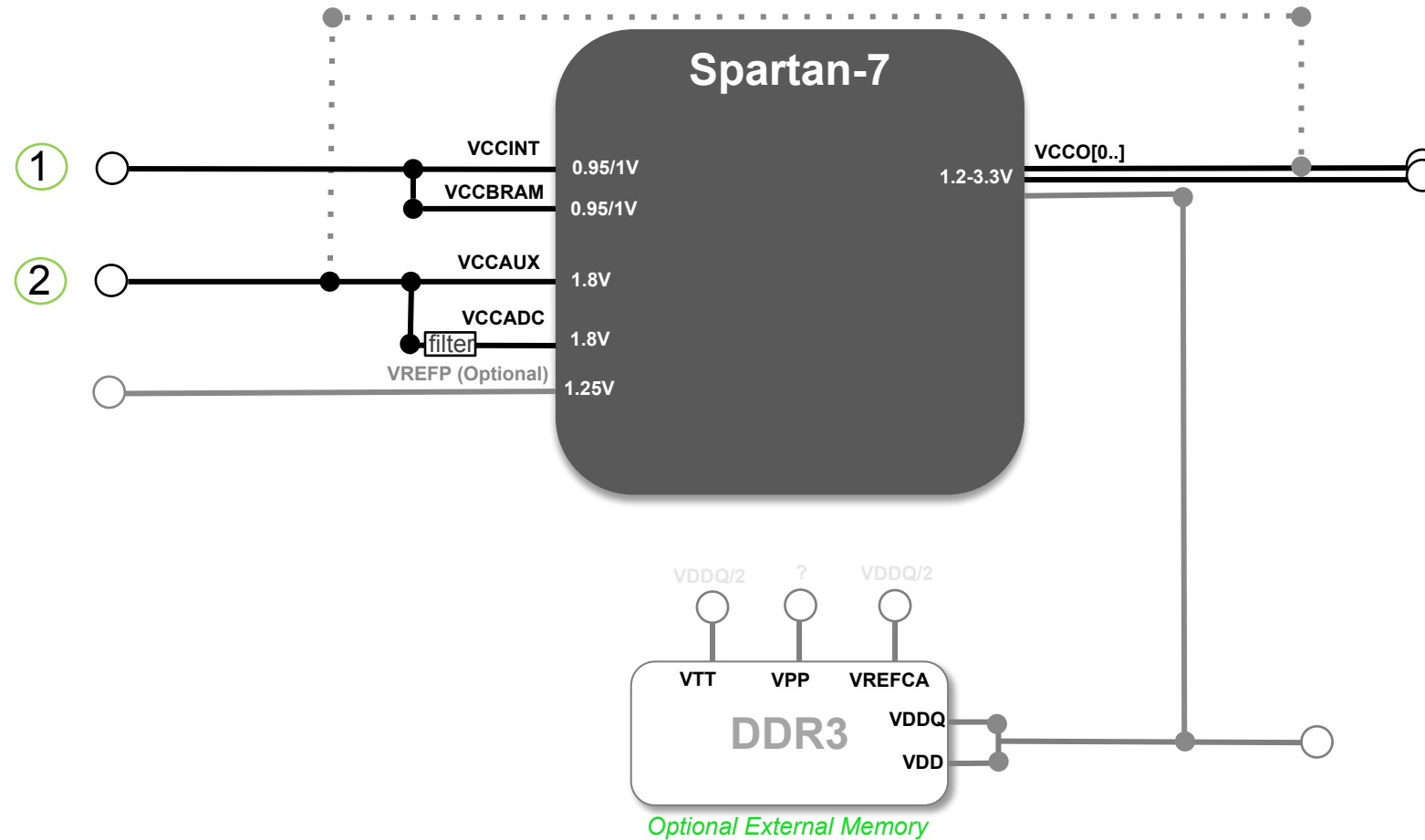
Spartan 7 (Full Power Management)

Mapping & Test Data

Contents

- Power tree mappings completed per data received from Xilinx Power Management team.
- Total 7 power rails covered by 2x AmP ICs including memory and termination rails.
- Data gathered and bench tested by applications team at AnDAPT
 - Data meets or exceeds Xilinx power and timing specifications
- Total solution area is 1128.43 mm².
- Presentation contains thermal views of both ICs.

Spartan-7 (Full Power Management)



Spartan-7 Rails (Full Power Management)

	Rail	Voltage	Load	Comment
1	VIN	12V		
2	VCCINT	0.95/1V \pm 5%	0.3-2.5A	
3	VCCBRAM	0.95/1V \pm 5%	0.1A	Normally tied to VCCINT
3	VCCAUX & VCCADC	1.8V \pm 5%	0.15-0.35A	Additional current may be needed to support 1.8V IO
6	VCC_IO	1.8/2.5/3.3V \pm 5%	0.2-2.5A	IO current varies widely depending on application
7	VCC_DDR	1.5/1.35V \pm 5%	~2A	Some applications may use DDR3 or DDR3L
8	DDR_VTT	VCC_DDR/2		Please use your expertise to define load
9	DDR_VREF	VCC_DDR/2		Please use your expertise to define load

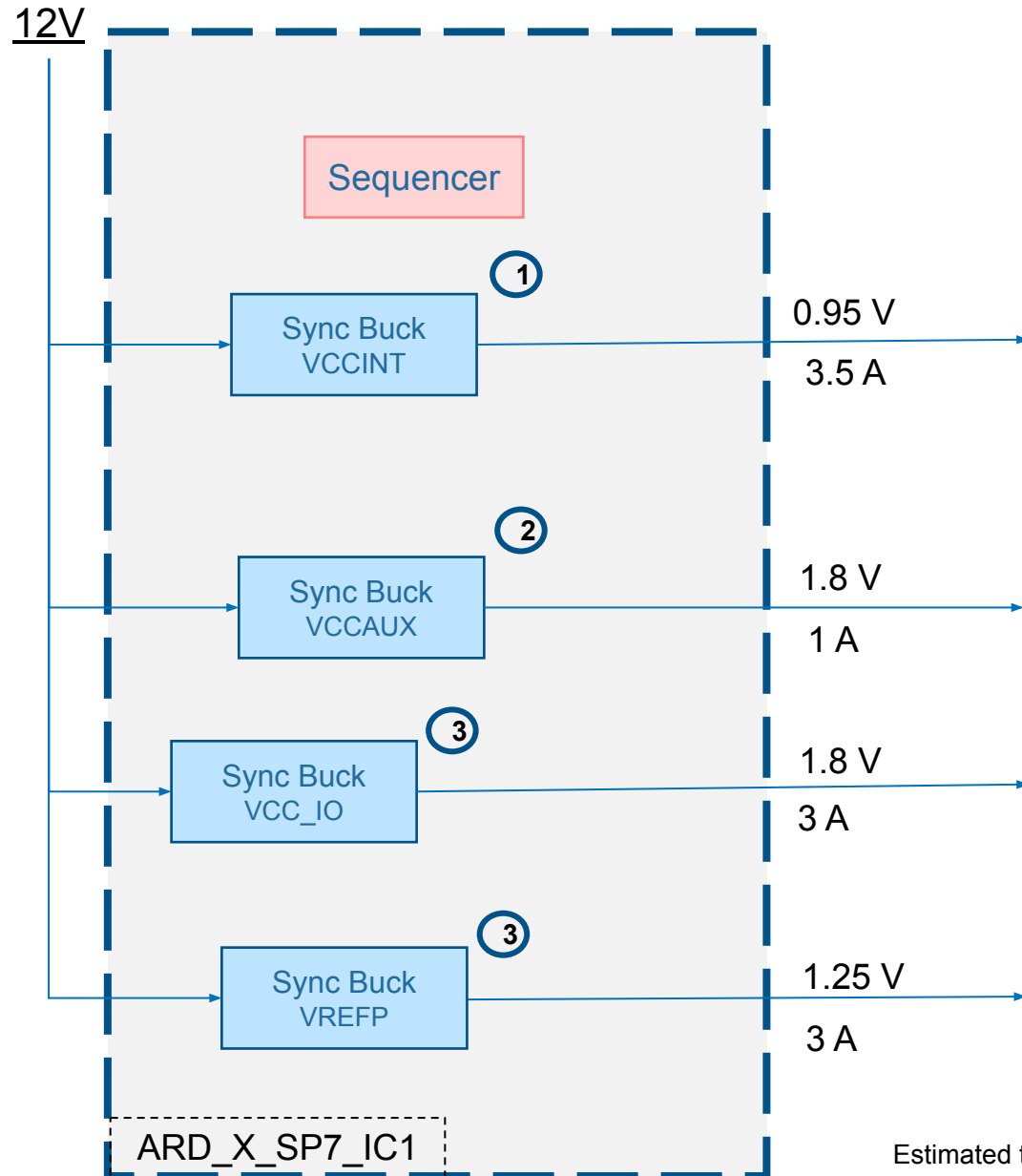
Power Tree Mapping: Spartan 7 (Full Power Management)

#	Rail	Seq	Power Component	Type	Upstream Rail	Vinput (V)	Vout (V)	Iout (A)	AnDAPT PMIC
1	VCCINT (VCCBRAM)	1	Sync Buck	C200	PVIN	12	0.95/1	3.5	ARD_X_SP7_IC1
2	VCCAUX (VCCADC)	2	Sync Buck	C200	PVIN	12	1.8	1	
3	VCC_IO	3	Sync Buck	C200	PVIN	12	1.8/2.5/3.3	3	
4	VREFP	3	Sync Buck	C200	PVIN	12	1.25	3	
5	VCC_DDR	3	HC Sync Buck	C220	PVIN	12	1.5/1.35	2 + 4 + 4	ARD_X_SP7_IC2
6	DDR_VTT	4	VTT Terminator	C210	VCC_DDR /2	1.35	0.675	4	
7	DDR_VREF	4	VTT Terminator	C210	VCC_DDR /2	1.35	0.675	4	

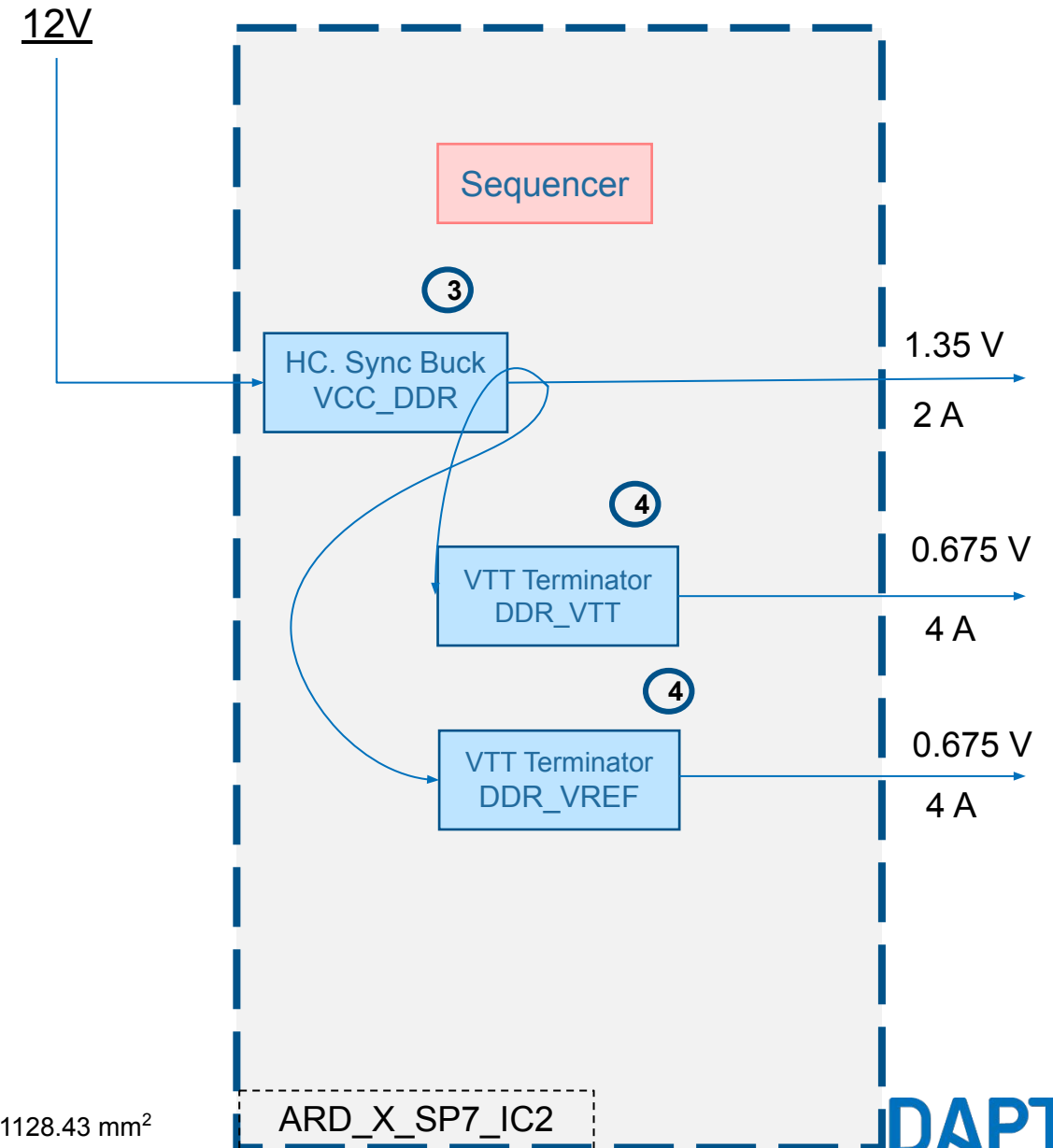
PVIN = 12V

Total estimated solution area = 1128.43 mm²

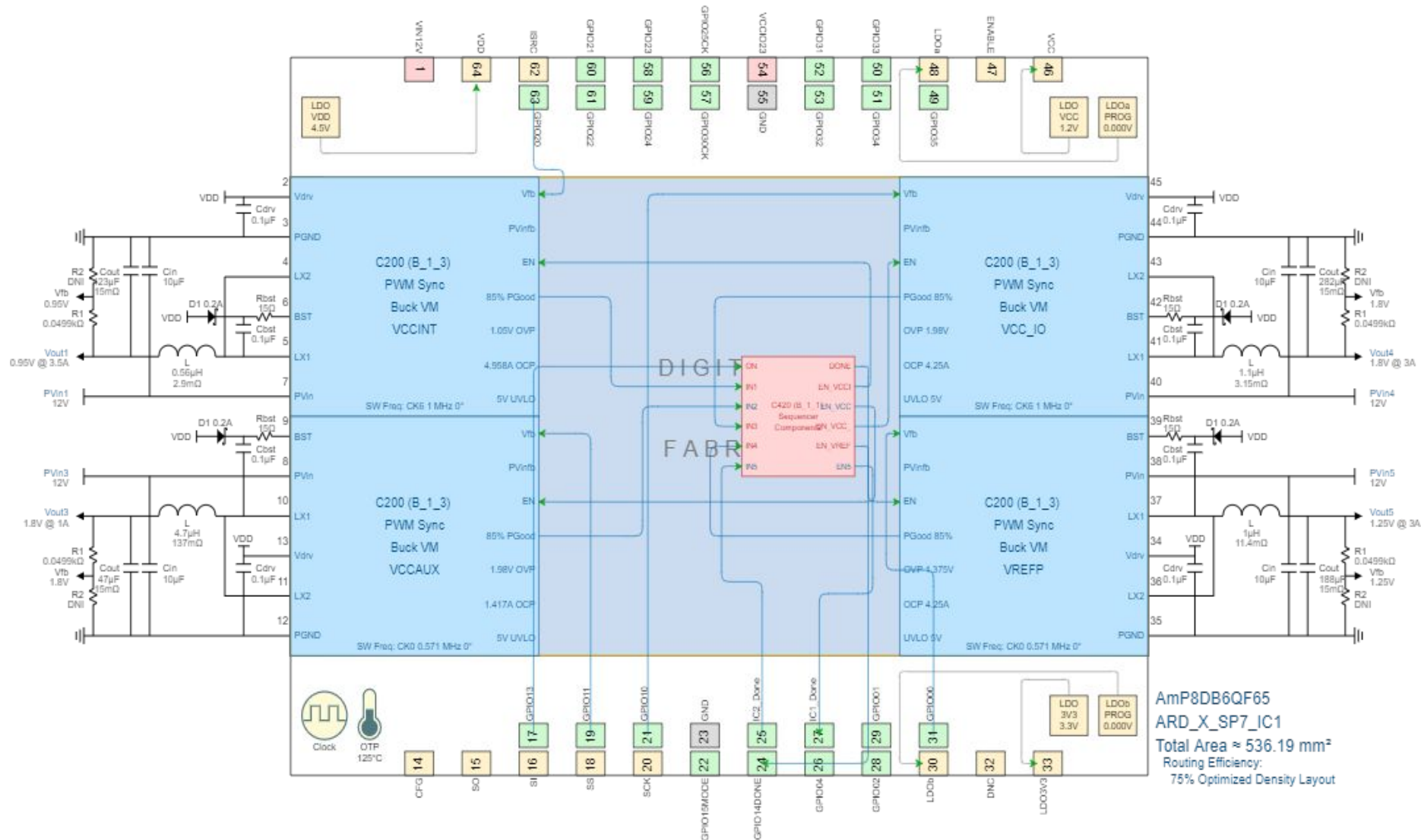
Power Tree Mapping- Spartan 7 (Full Power Management)



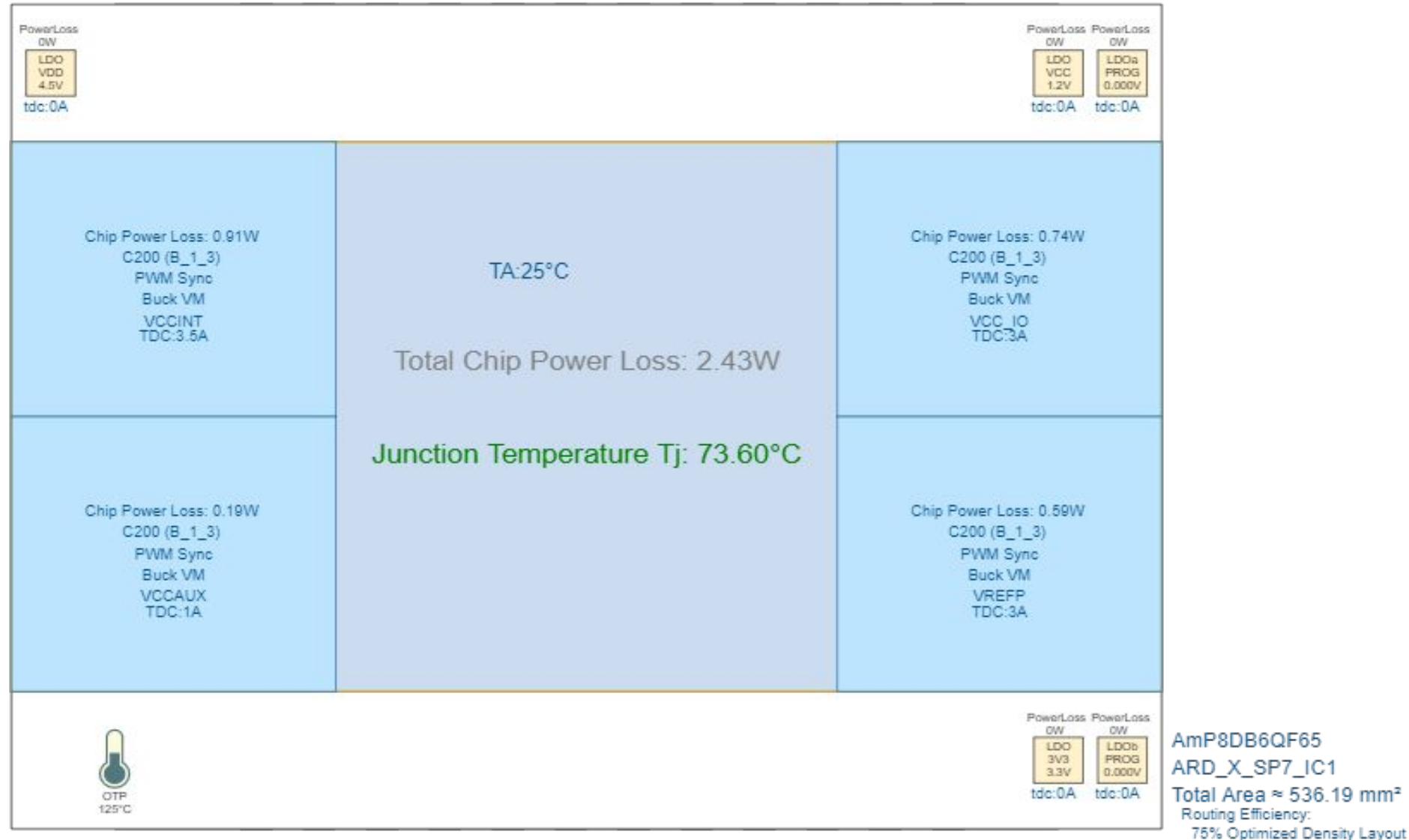
Estimated total area 1128.43 mm²



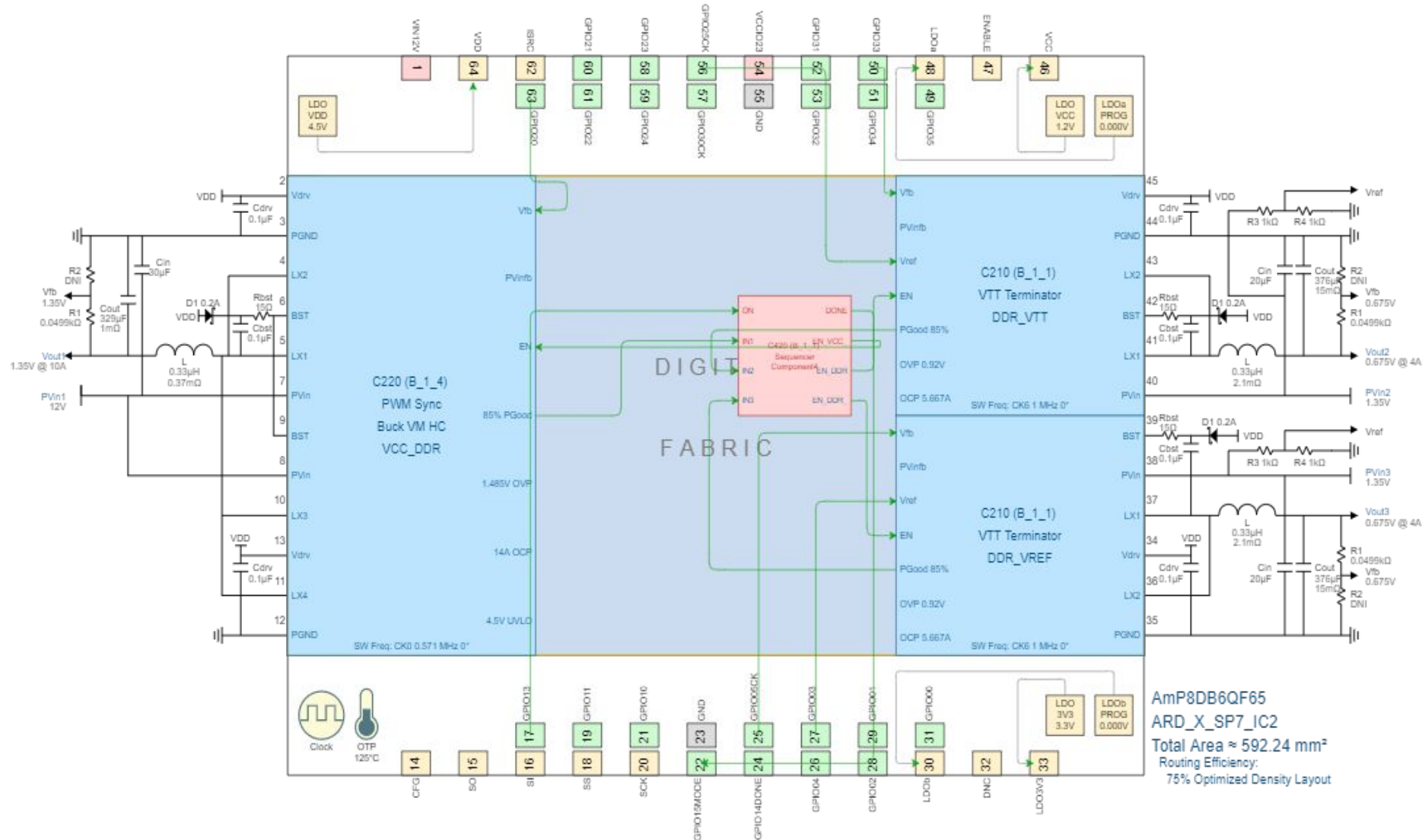
Mapping (WebAmP View) Design –IC1



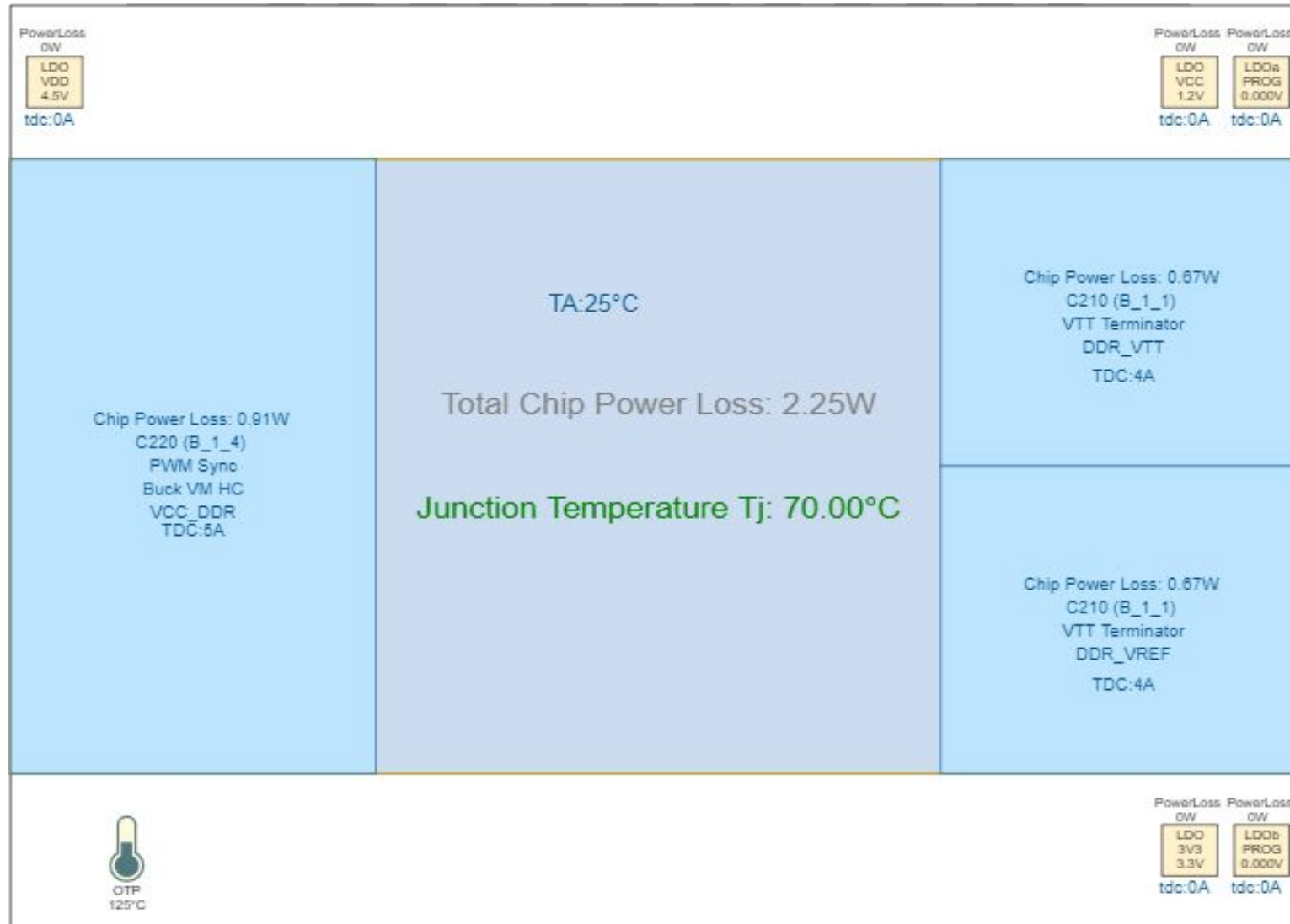
Mapping (Thermal View) –IC1



Mapping (WebAmP View) Design –IC2



Mapping (Thermal View) –IC2



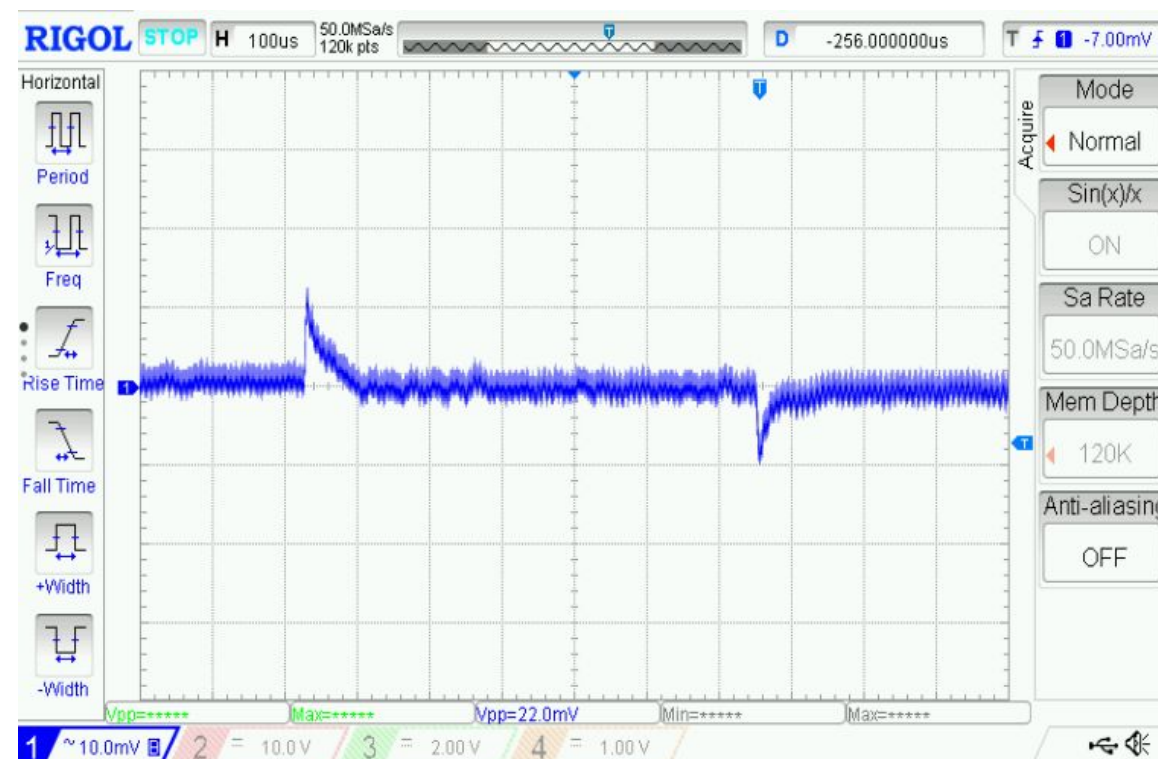
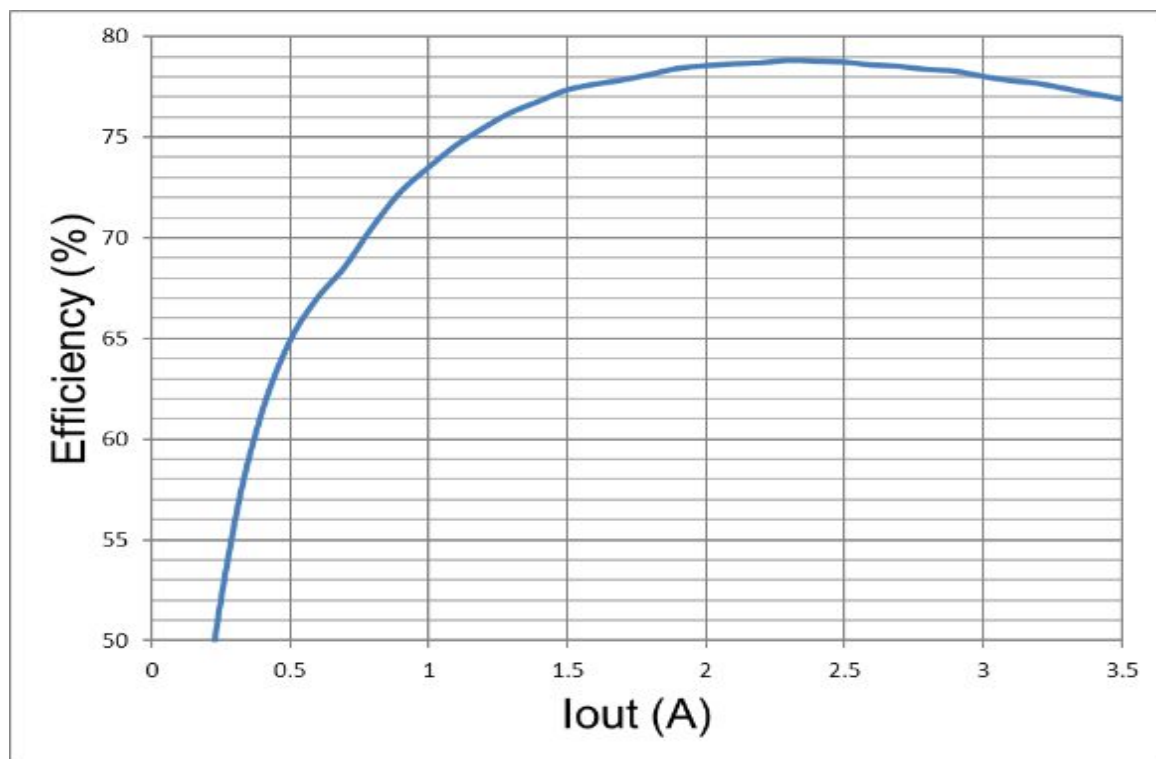
AmP8DB6QF65
ARD_X_SP7_IC2
Total Area ≈ 592.24 mm²
Routing Efficiency:
75% Optimized Density Layout

VCCINT (VCCBRAM)

0.95 V / 3.5 A

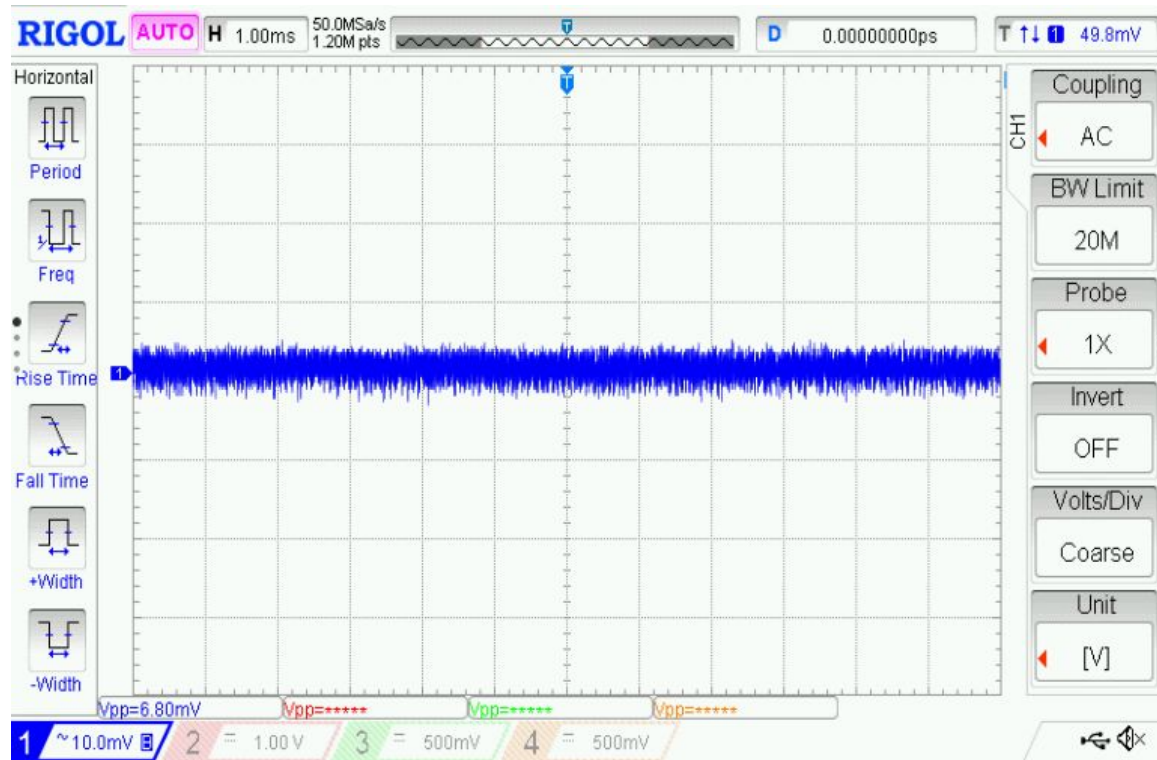
- C200 (Synchronous Buck)
- $F_{sw} = 1 \text{ MHz}$
- $L = 0.56 \text{ } \mu\text{H}$, P/N Wurth 744393440056
- $C = 9 \times 47 \text{ } \mu\text{F}$

Efficiency & Transient

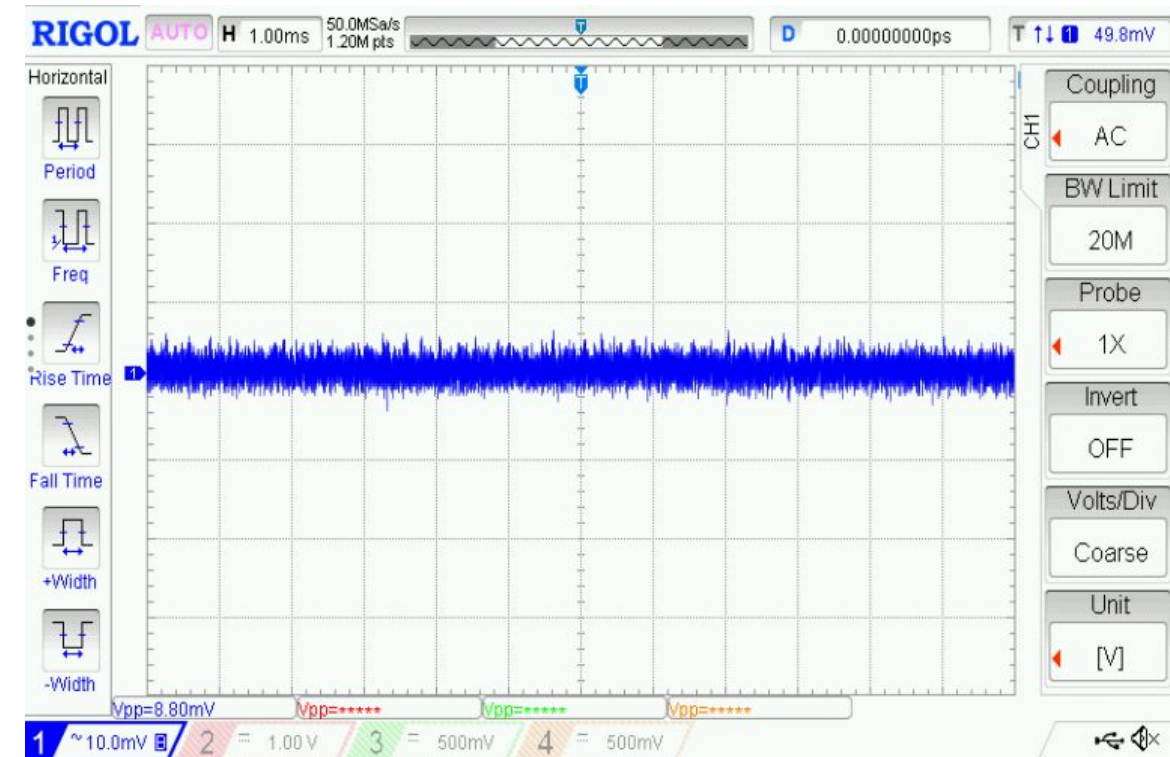


Vout = 0.95 V
Transient 2.625 – 3.5 A@100 A/μs
 $V_{PP} = 22.0$ mV
Fsw = 1 MHz
L = 0.56 μH, C = 9x47 uF

Ripple



No Load
 $V_{PP} = 6.80\text{ mV}$



3.5 A Load
 $V_{PP} = 8.80\text{ mV}$

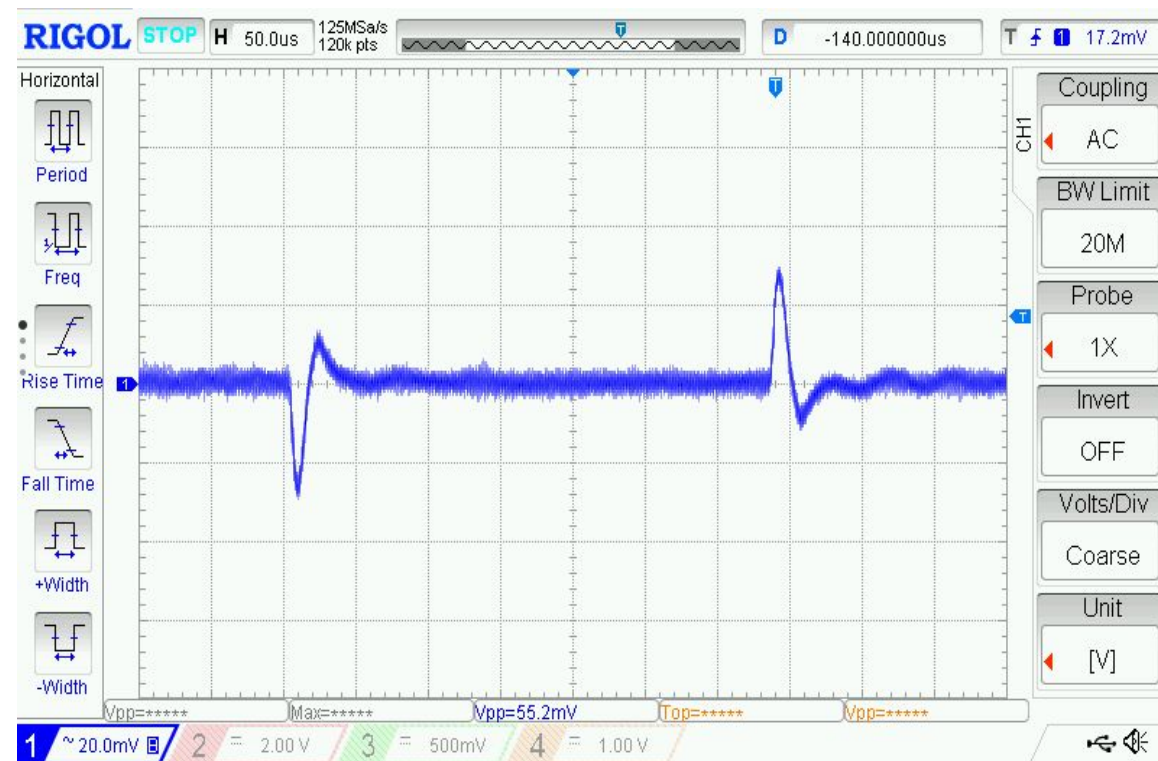
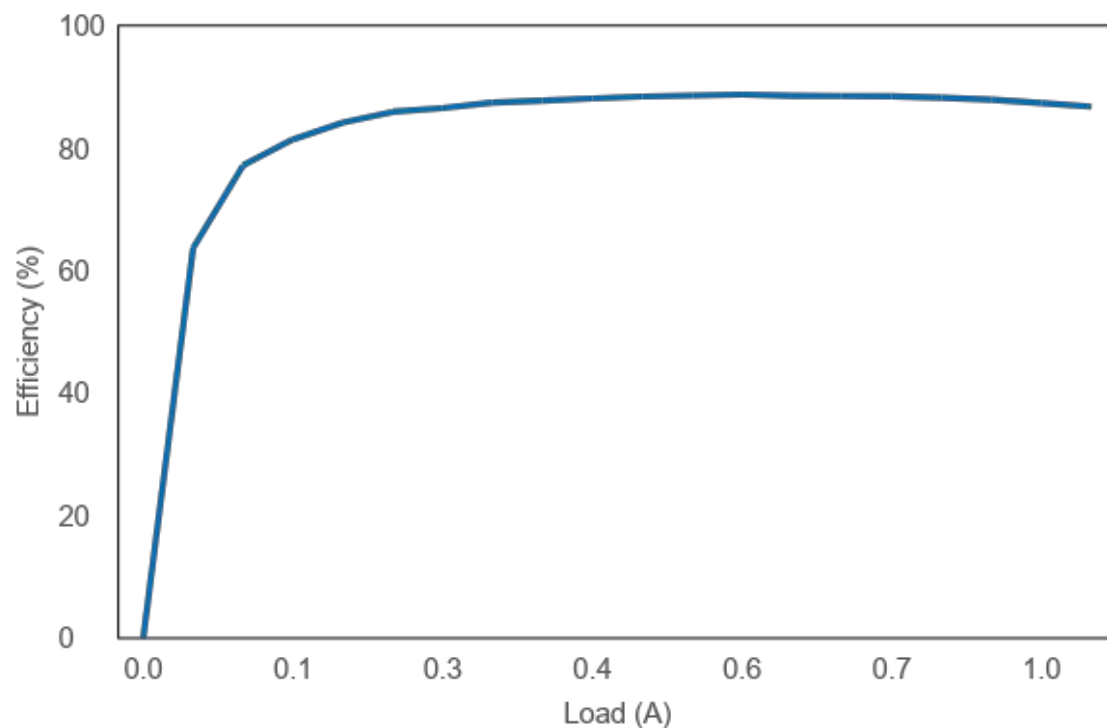
$V_{out} = 0.95\text{ V}$

VCCAUX (VCCADC)

1.8 V / 1 A

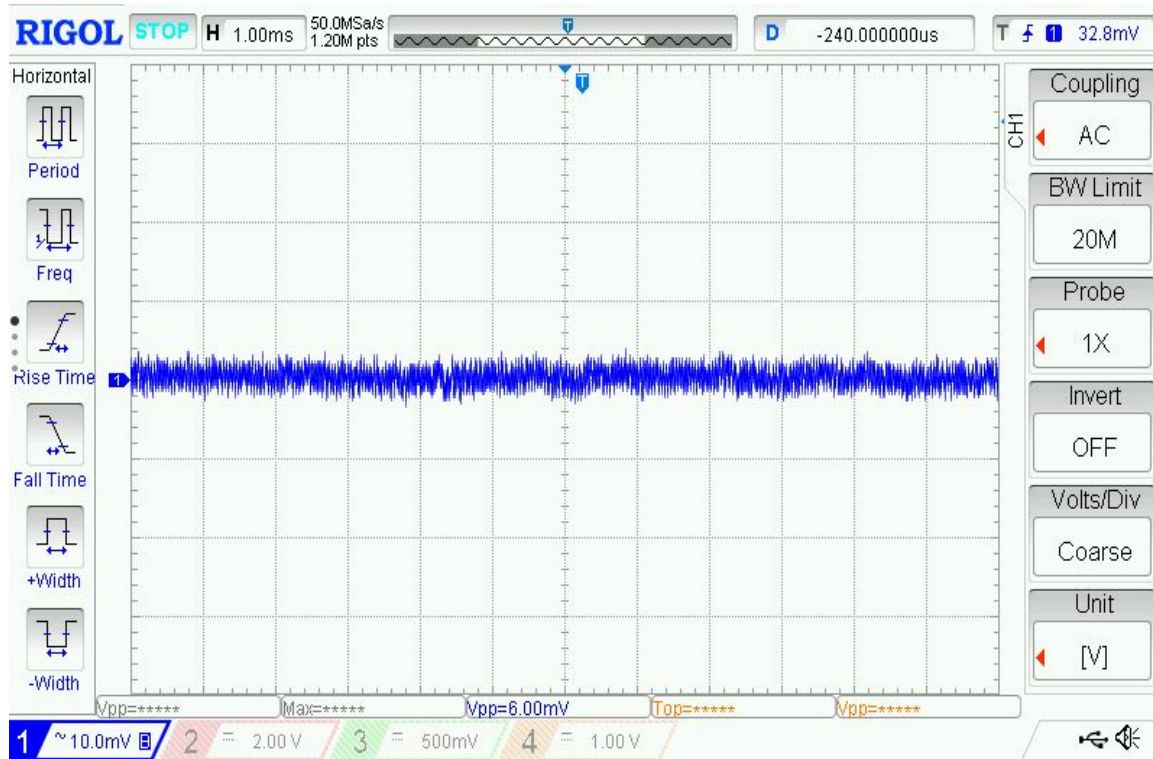
- C200 (Synchronous Buck)
- $F_{sw} = 0.571 \text{ MHz}$
- $L = 4.7 \text{ } \mu\text{H}$, P/N Wurth 74438336047
- $C = 1 \times 47 \text{ } \mu\text{F}$

Efficiency & Transient

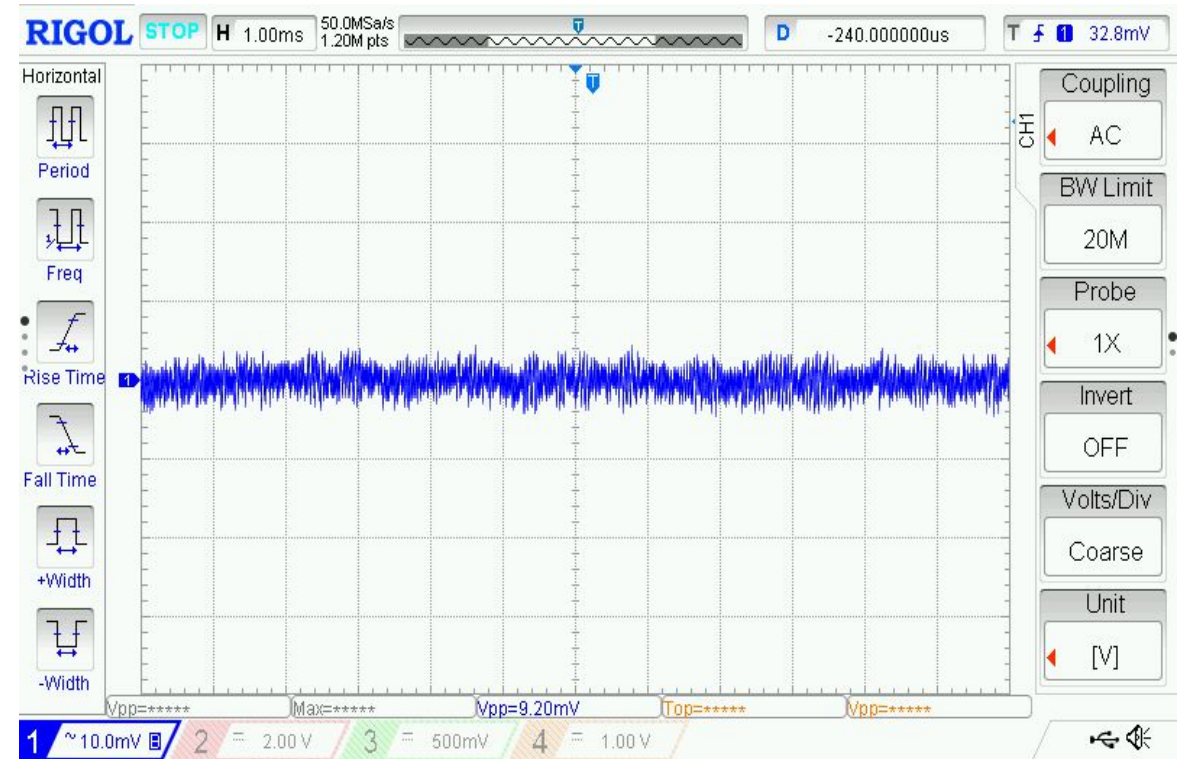


$V_{out} = 1.8 \text{ V}$
Transient $0.75 \text{ A} - 1 \text{ A} @ 10 \text{ A}/\mu\text{s}$
 $V_{pp} = 55.2 \text{ mV}$
 $F_{sw} = 0.571 \text{ MHz}$
 $L = 4.7 \mu\text{H}$, $C = 1 \times 47 \mu\text{F}$

Ripple



No Load
 $V_{PP} = 6 \text{ mV}$



$V_{out} = 1.8 \text{ V}$

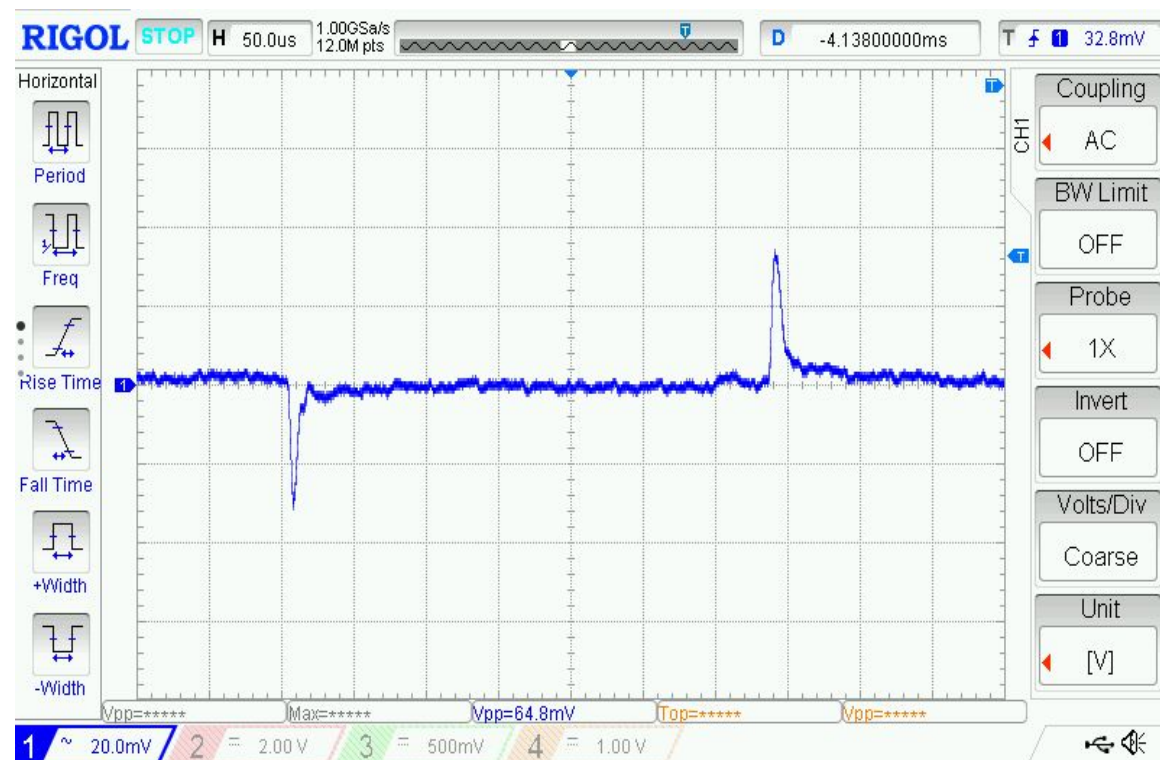
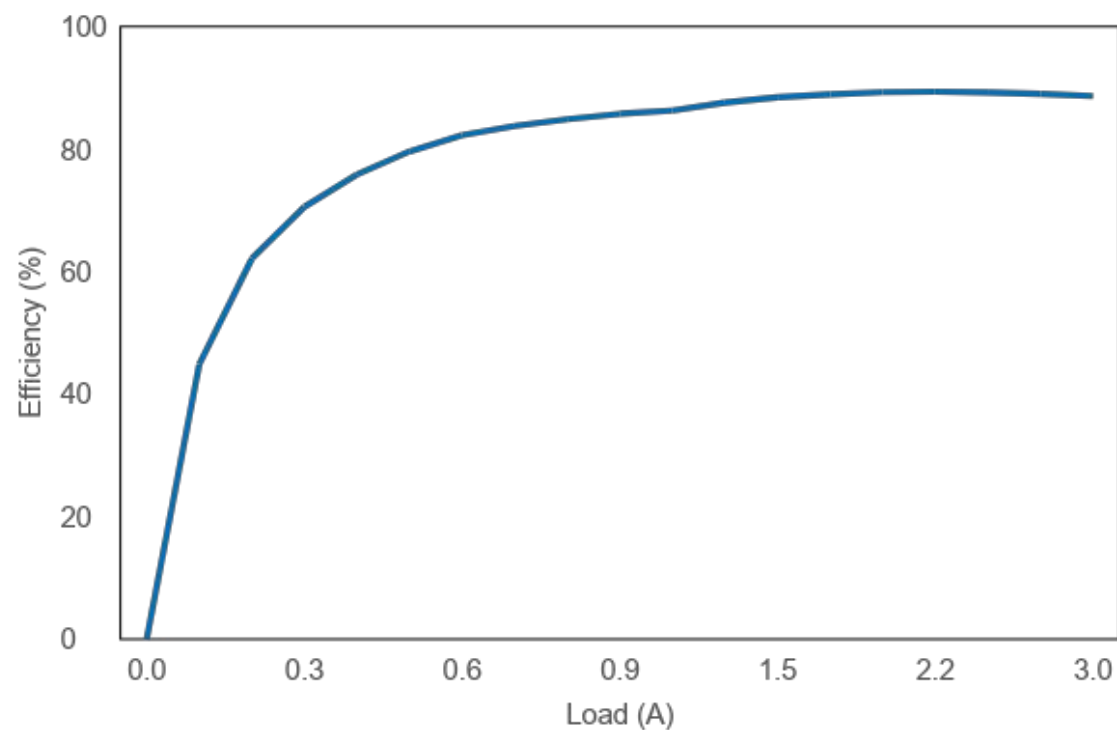
0.35 A Load
 $V_{PP} = 9.20 \text{ mV}$

VCC_IO

1.8 V / 3 A

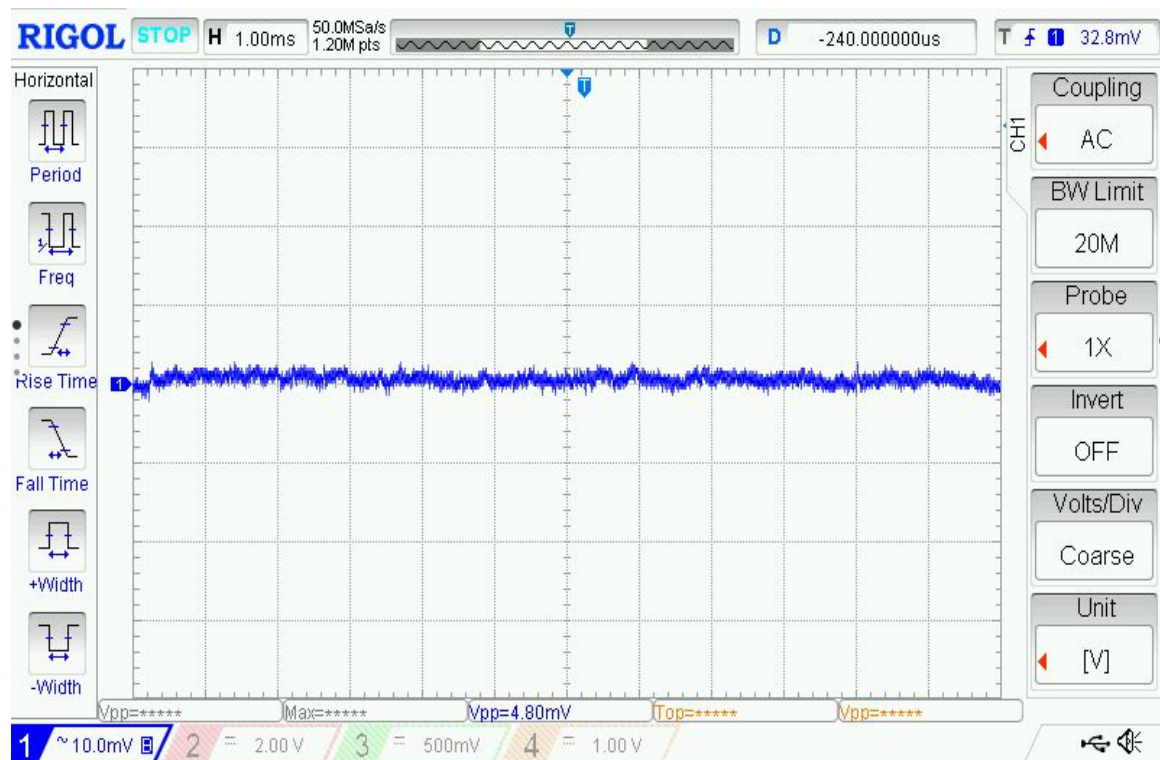
- C200 (Synchronous Buck)
- $F_{sw} = 1 \text{ MHz}$
- $L = 1.1 \mu\text{H}$, P/N Wurth 744314110
- $C = 6 \times 47 \mu\text{F}$

Efficiency & Transient

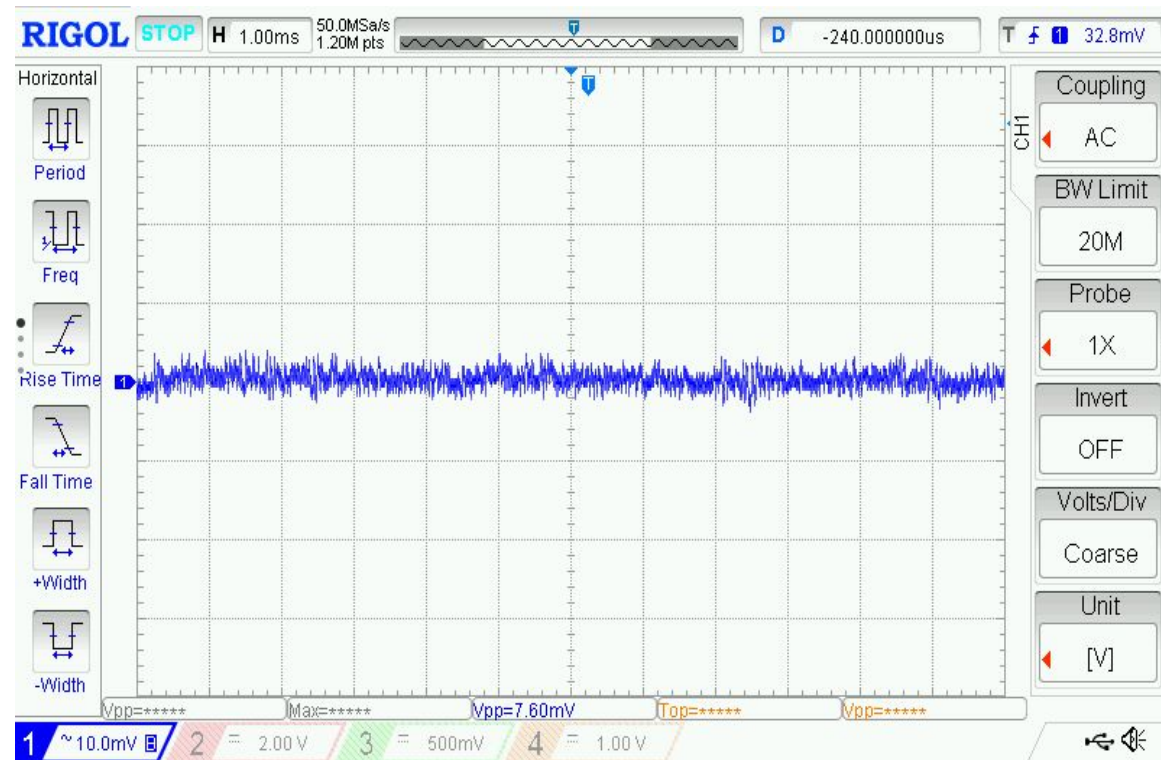


Vout = 1.8V
Transient 0.3 – 3 A@10 A/ μ s
 V_{PP} = 64.8 mV
Fsw = 1 MHz
L = 1.1 μ H, C= 6x47 μ F

Ripple



No Load
 $V_{PP} = 4.80 \text{ mV}$



6 A Load
 $V_{PP} = 7.60 \text{ mV}$

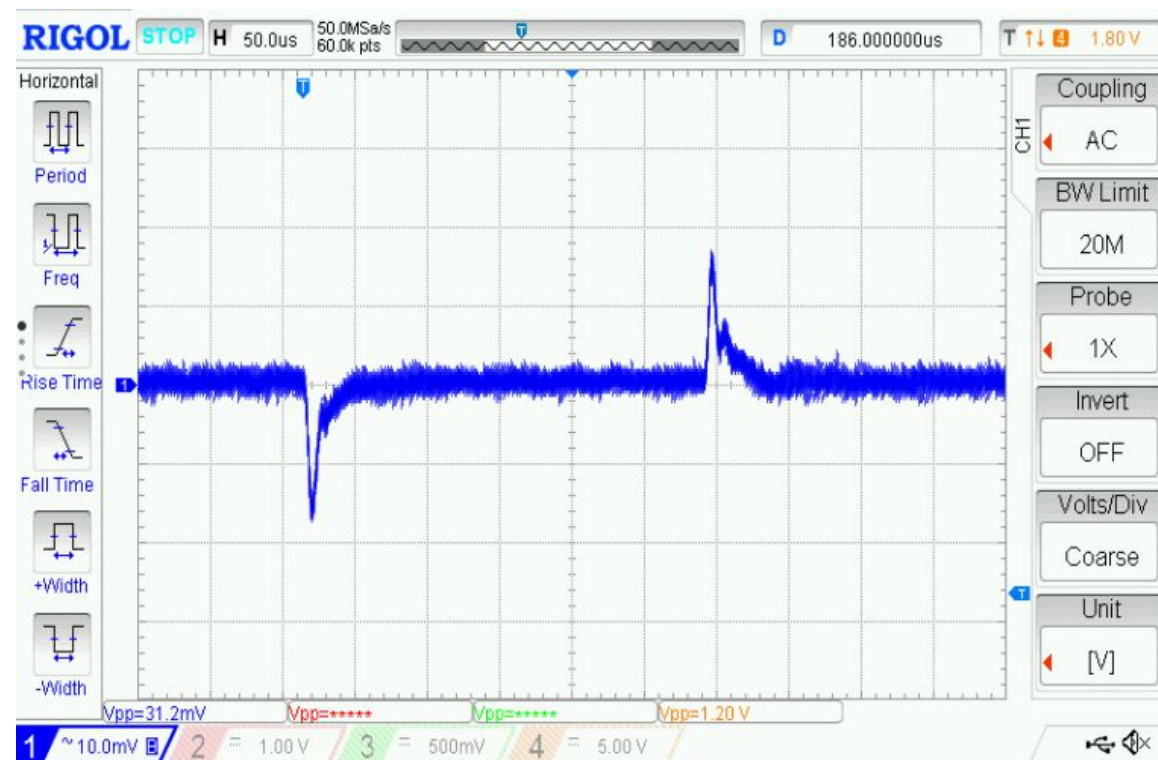
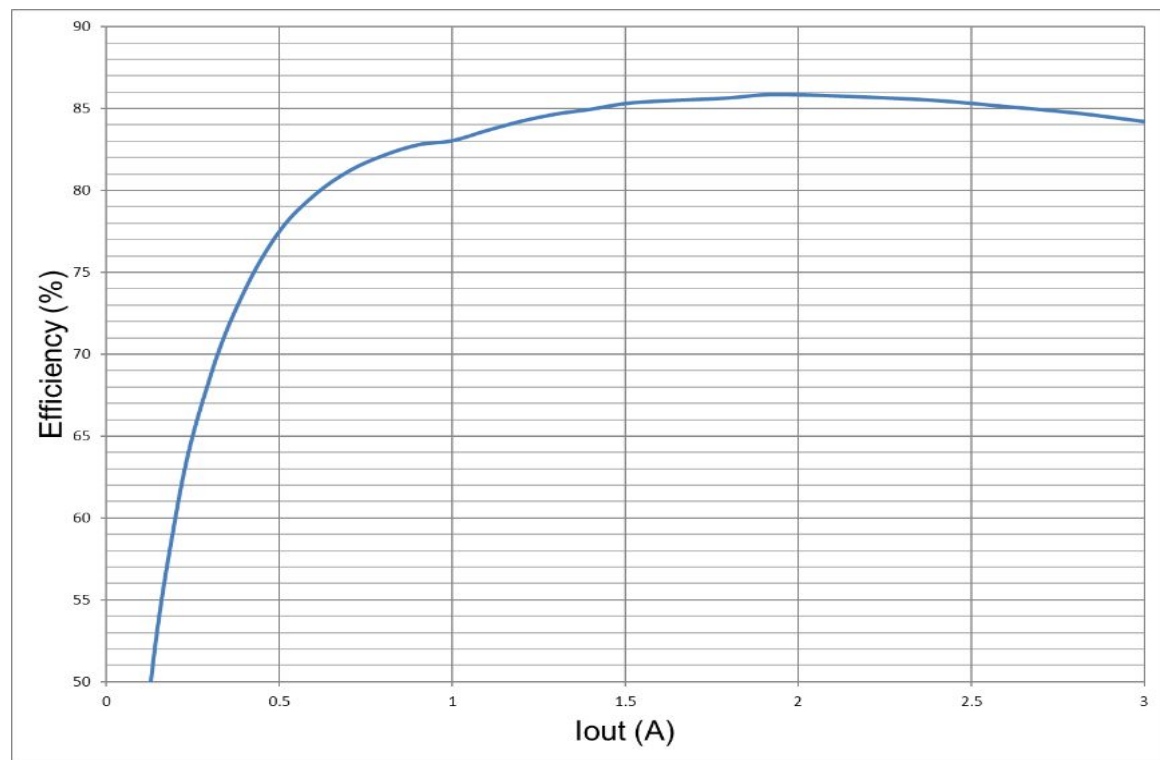
$V_{out} = 1.8 \text{ V}$

VREFP

1.25 V / 3 A

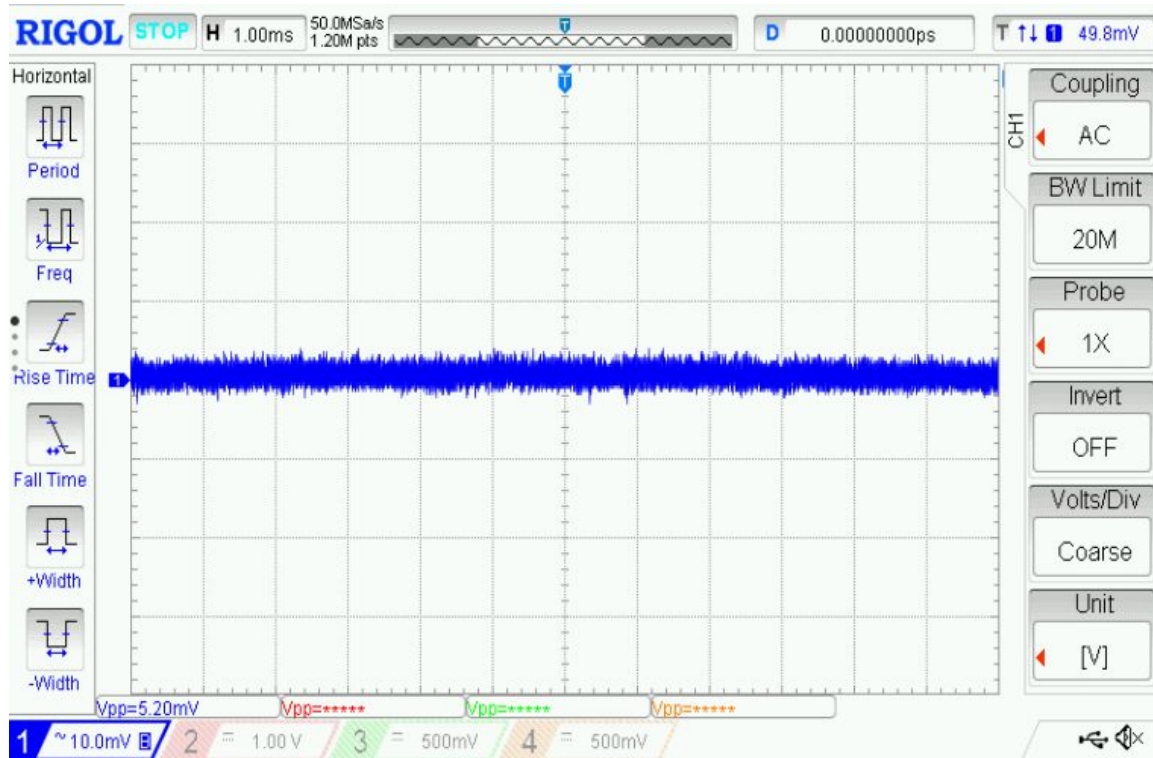
- C200 (Synchronous Buck)
- $F_{sw} = 0.571 \text{ MHz}$
- $L = 1 \text{ } \mu\text{H}$, P/N Wurth 74438366010
- $C = 4 \times 47 \text{ } \mu\text{F}$

Efficiency & Transient

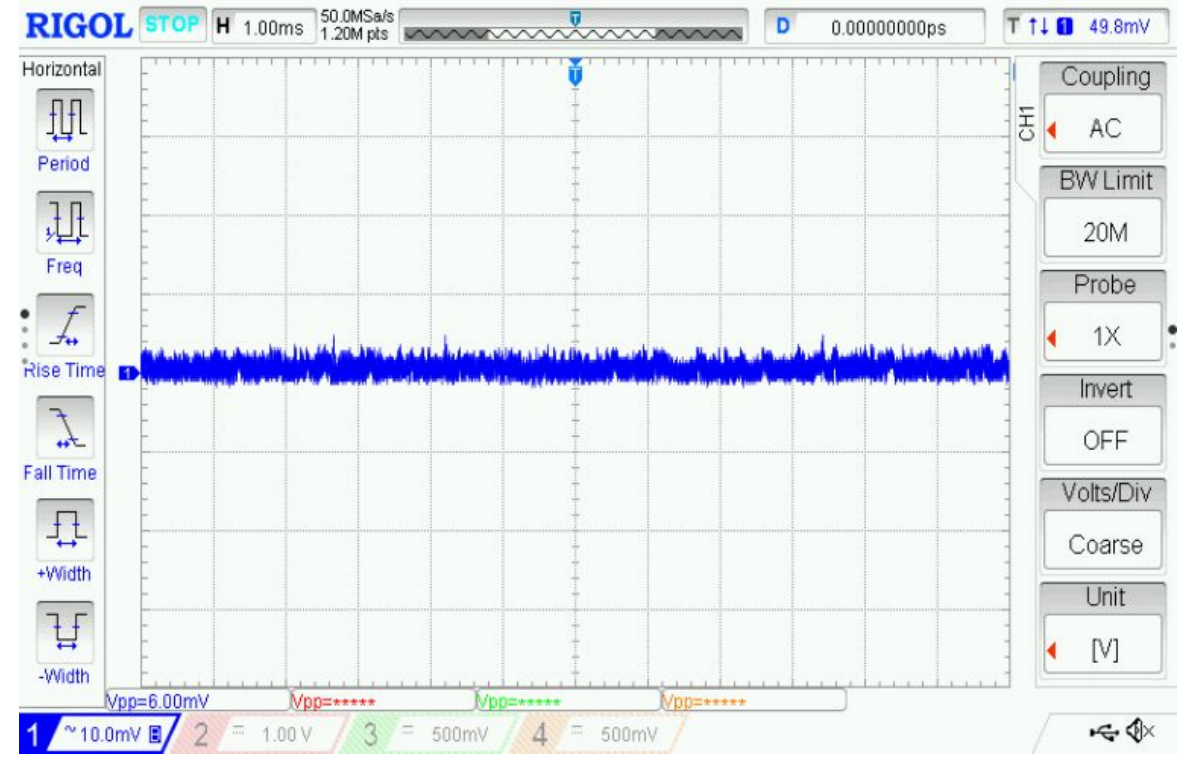


$V_{out} = 1.25V$
Transient 2.25 A – 3 A @ 60 A/ μ s
 $V_{PP} = 31.2$ mV
 $F_{sw} = 0.571$ MHz
 $L = 1$ μ H, $C = 4 \times 47$ μ F

Ripple



No Load
 $V_{PP} = 5.20 \text{ mV}$



3 A Load
 $V_{PP} = 6.00 \text{ mV}$

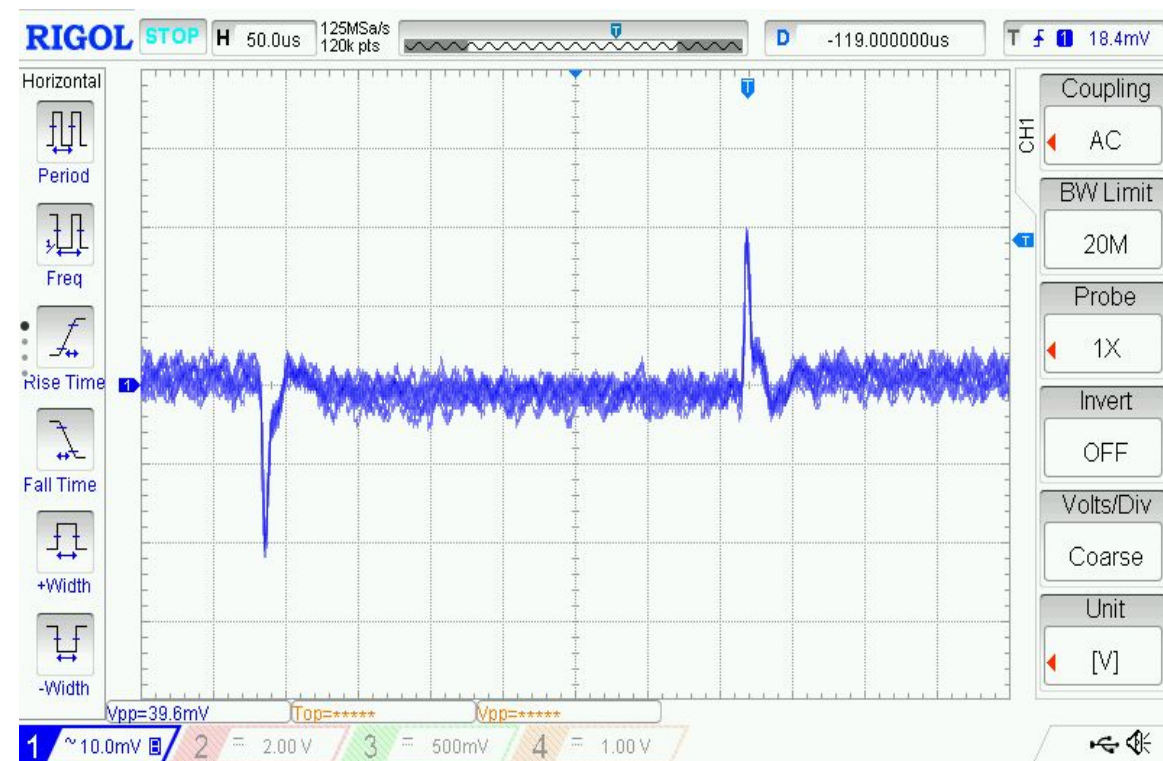
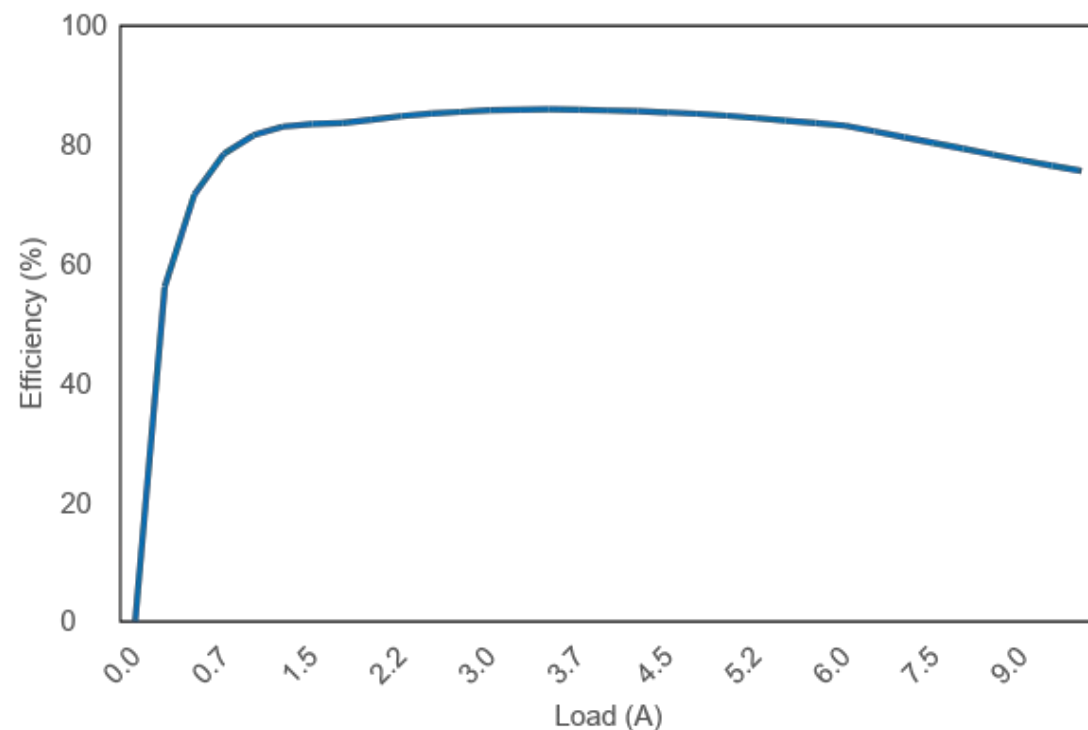
$V_{out} = 1.25 \text{ V}$

VCC_DDR

1.35 \bar{V} / 10 A

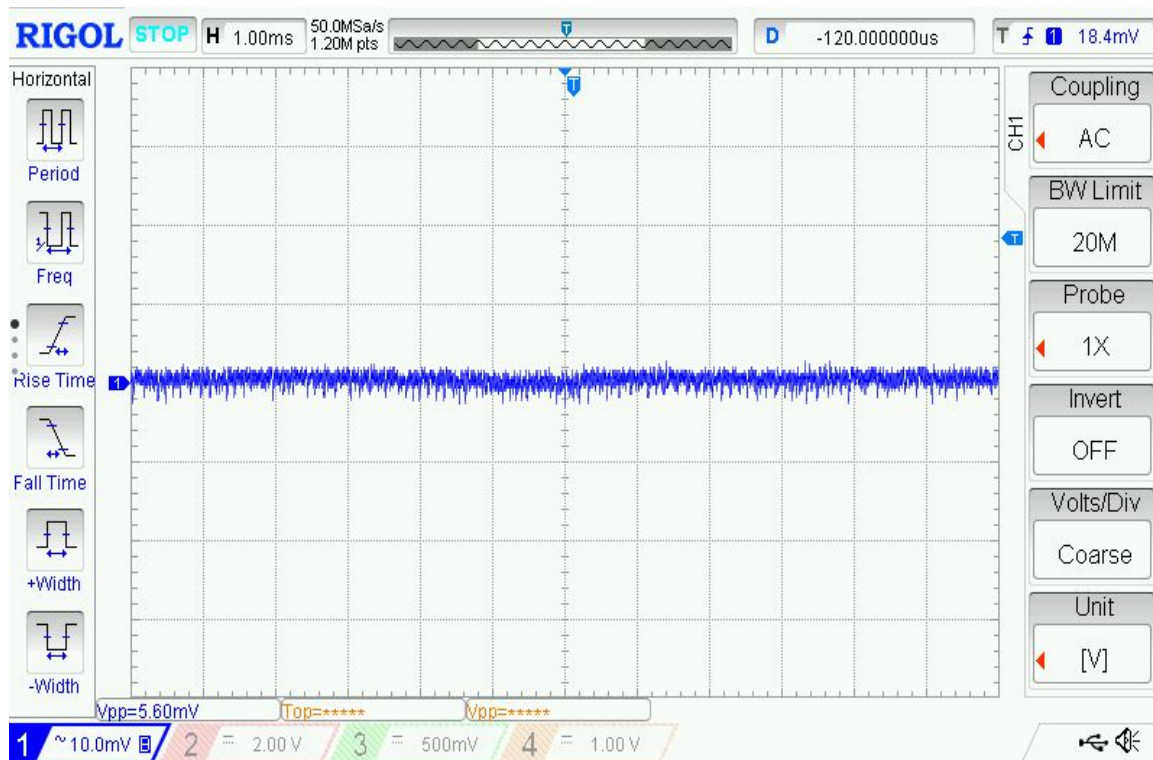
- C220 (High Current Synchronous Buck)
- $F_{sw} = 0.571 \text{ MHz}$
- $L = 0.33 \mu\text{H}$, P/N Wurth 744308033
- $C = 7 \times 47 \mu\text{F}$

Efficiency & Transient

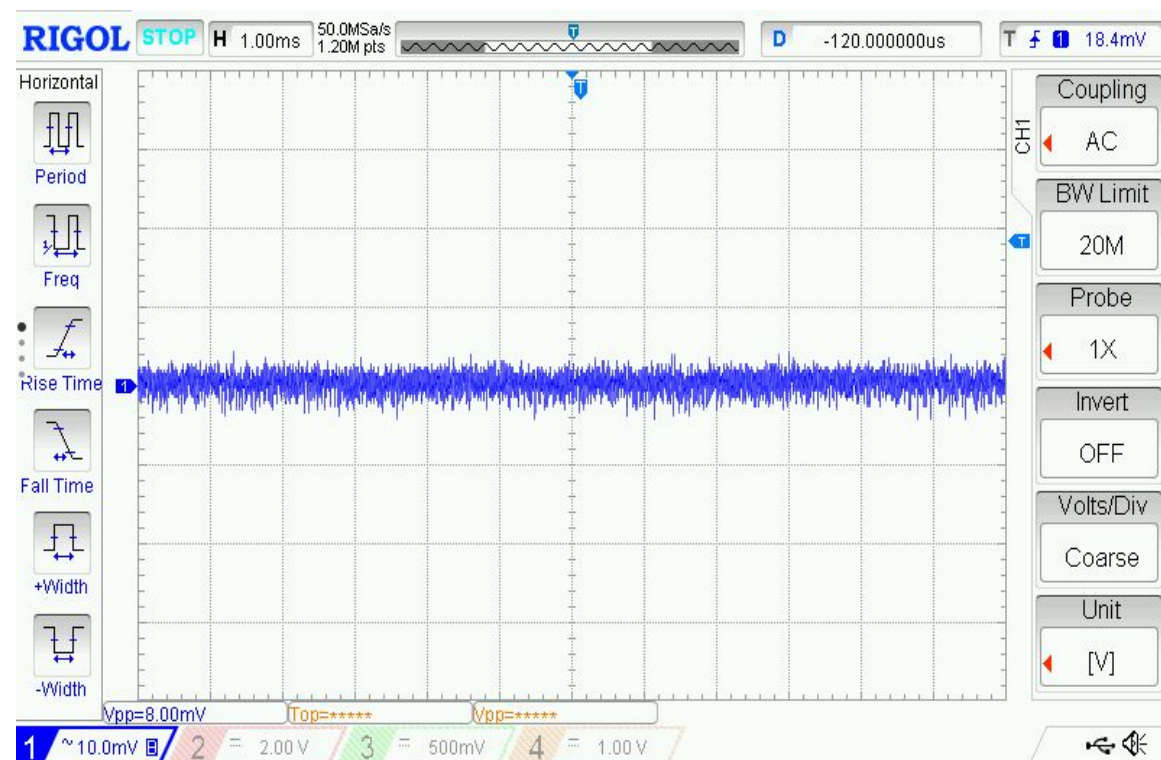


$V_{out} = 1.35V$
Transient 7.5 A – 10 A @ 10 A/ μs
 $V_{pp} = 39.6\text{ mV}$
 $F_{sw} = 0.571\text{ MHz}$
 $L = 0.33\text{ }\mu H$, $C = 7x47\text{ }\mu F$

Ripple



No Load
 $V_{PP} = 5.60 \text{ mV}$



10 A Load
 $V_{PP} = 8 \text{ mV}$

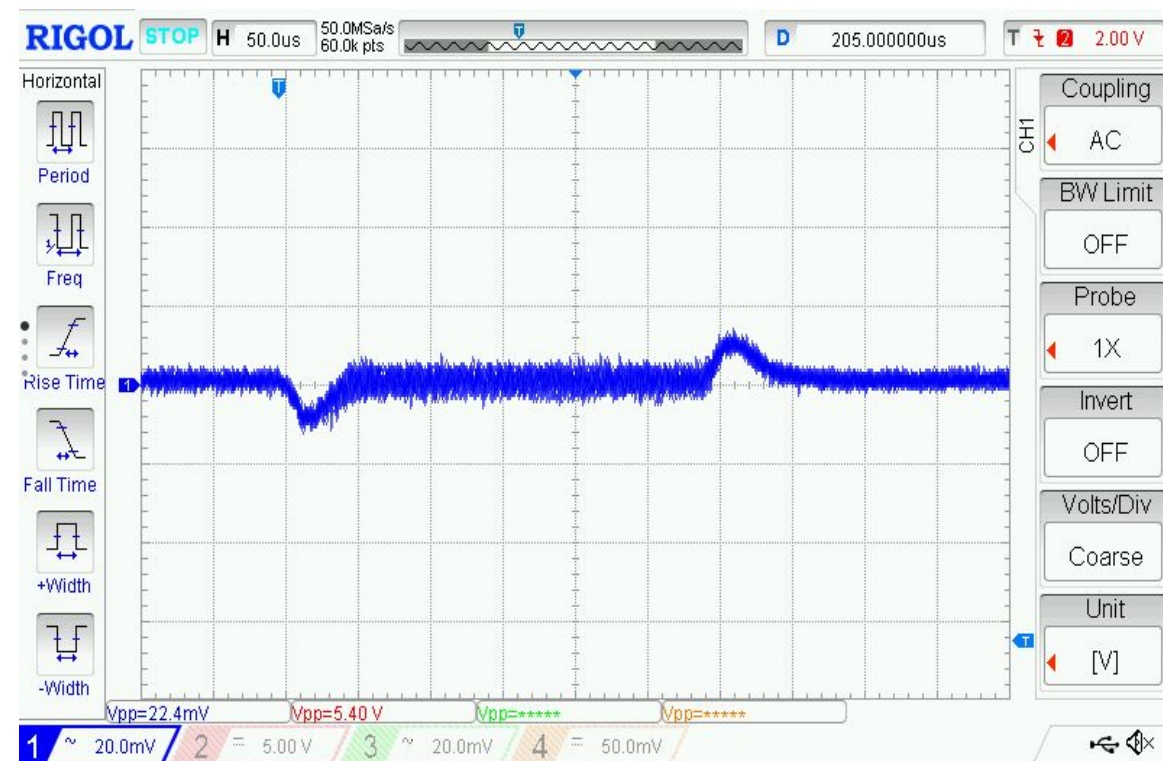
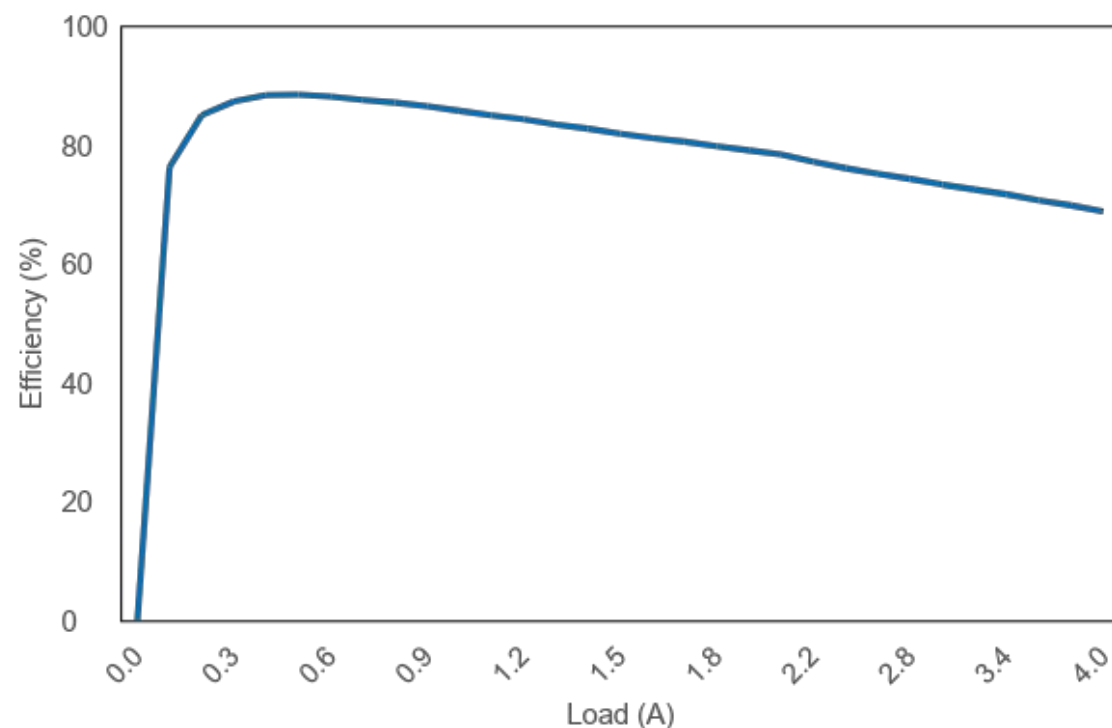
$V_{out} = 1.35 \text{ V}$

DDR_VTT

0.675 V/4 A

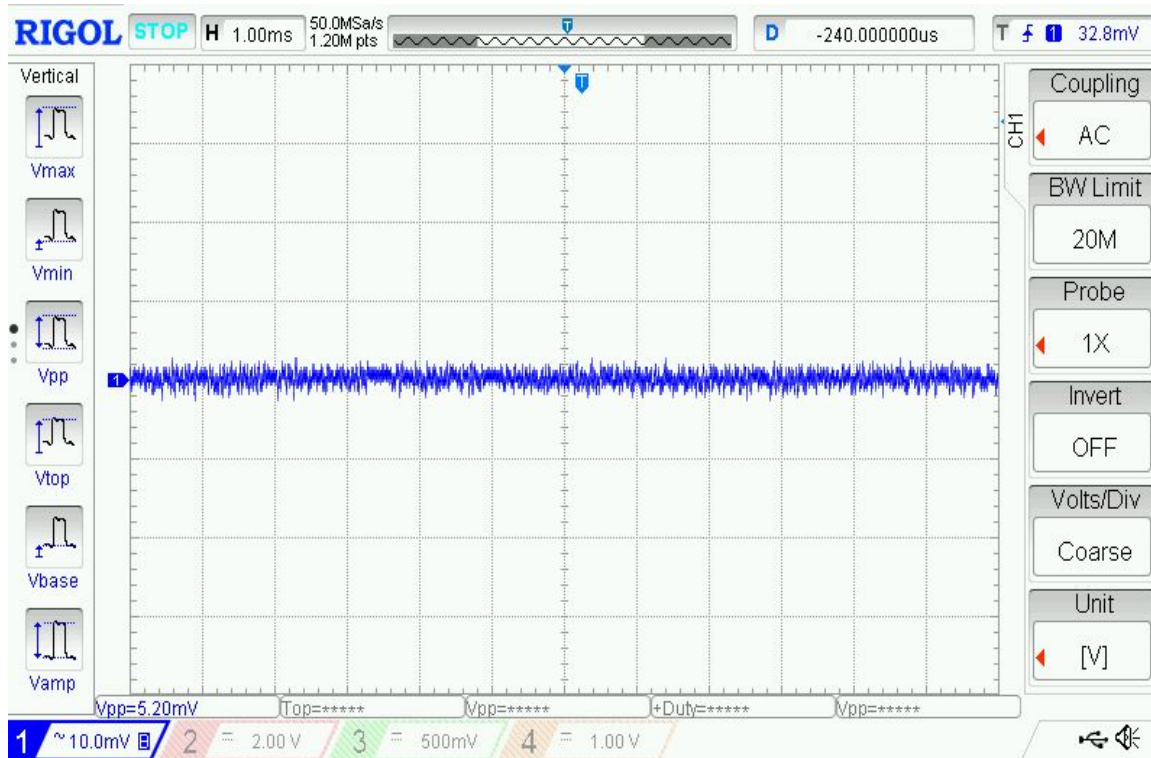
- C210 (VTT terminator)
- $F_{sw} = 1 \text{ MHz}$
- $L = 0.33 \text{ } \mu\text{H}$, P/N Wurth 744393440033
- $C = 8 \times 47 \text{ } \mu\text{F}$

Efficiency & Transient

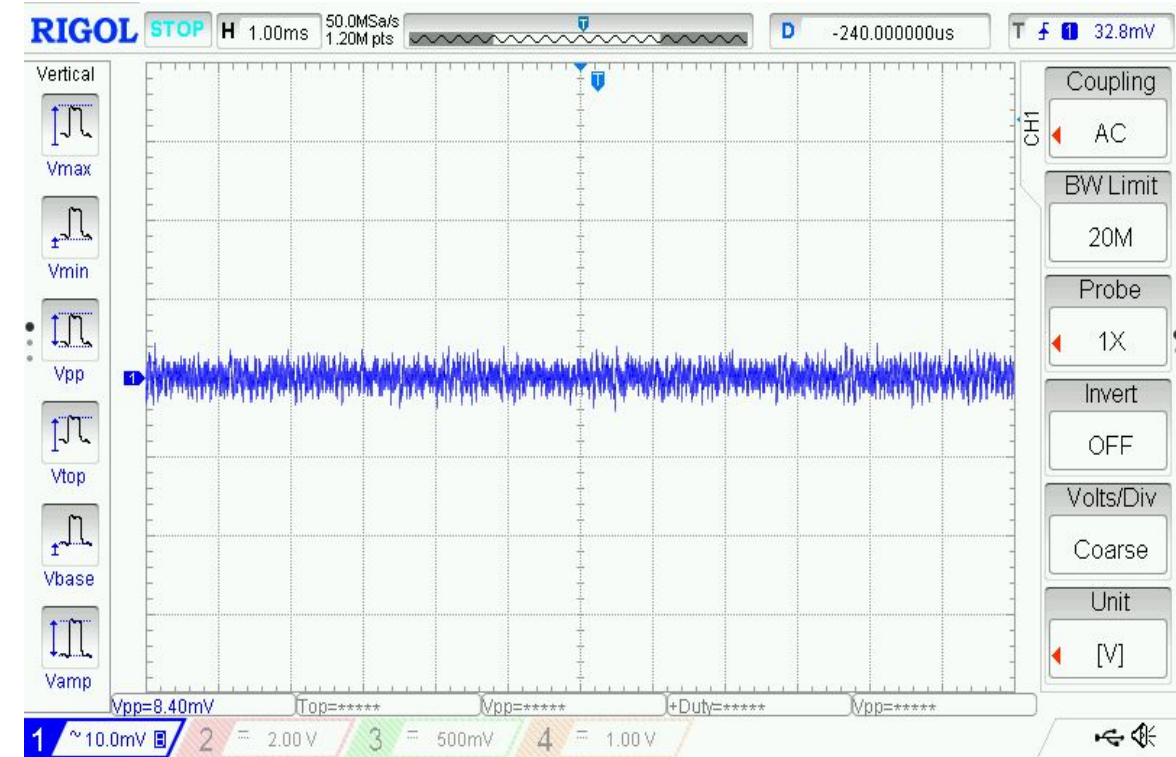


$V_{out} = 0.675\text{ V}$
Transient 3 A – 4 A @ 10 A/ μ s
 $V_{pp} = 22.4\text{ mV}$
 $F_{sw} = 1\text{ MHz}$
 $L = 0.33\text{ }\mu\text{H}$, $C = 8 \times 47\text{ }\mu\text{F}$

Ripple



No Load
 $V_{PP} = 5.20 \text{ mV}$



4 A Load
 $V_{PP} = 8.40 \text{ mV}$

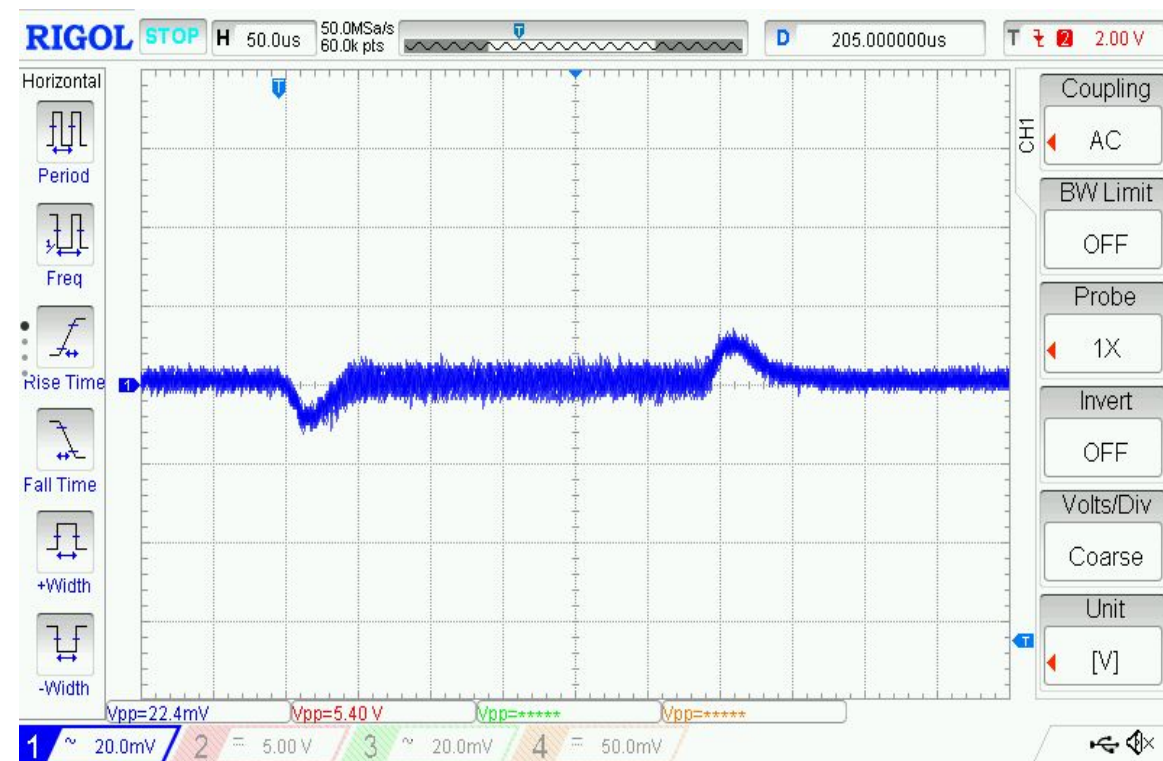
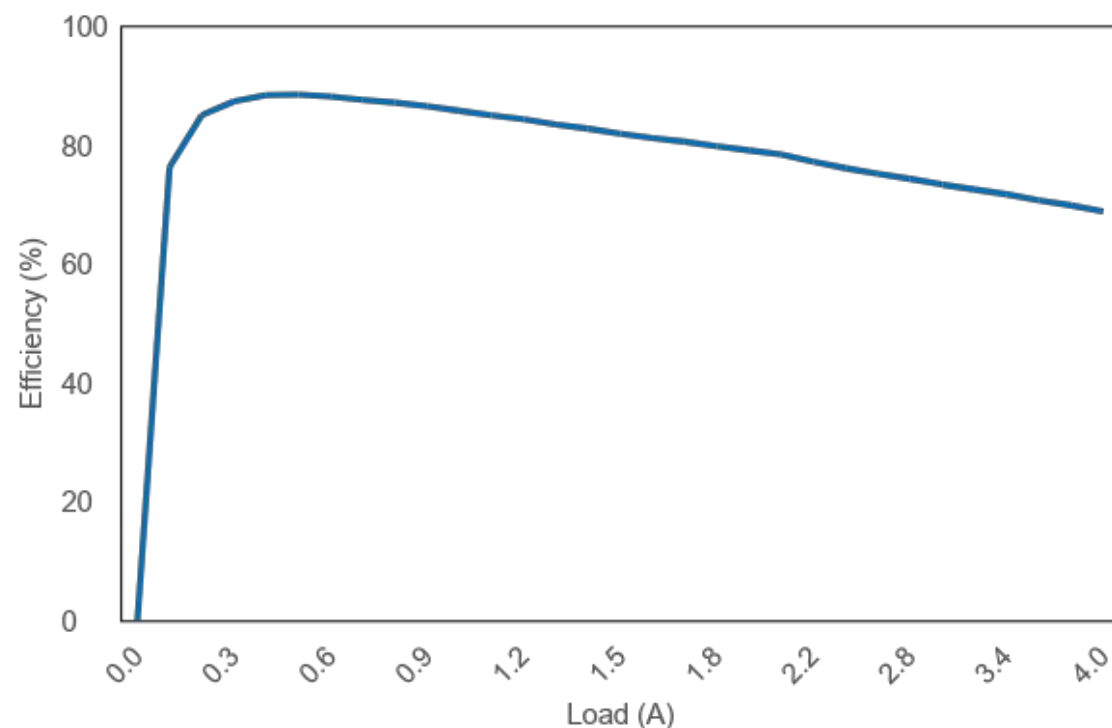
$V_{out} = 0.675 \text{ V}$

DDR_VREF

0.675 V/4 A

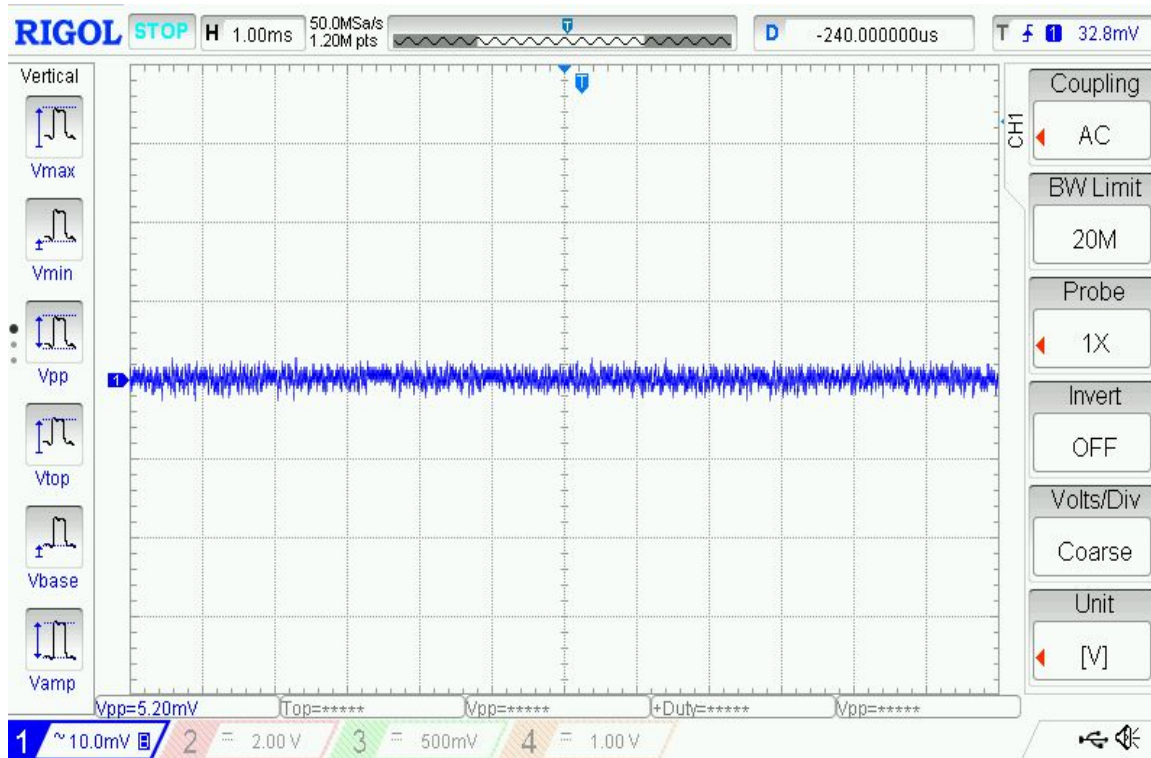
- C210 (VTT terminator)
- F_{sw} = 1 MHz
- L = 0.33 μ H, P/N Wurth 744393440033
- C = 8x47 μ F

Efficiency & Transient

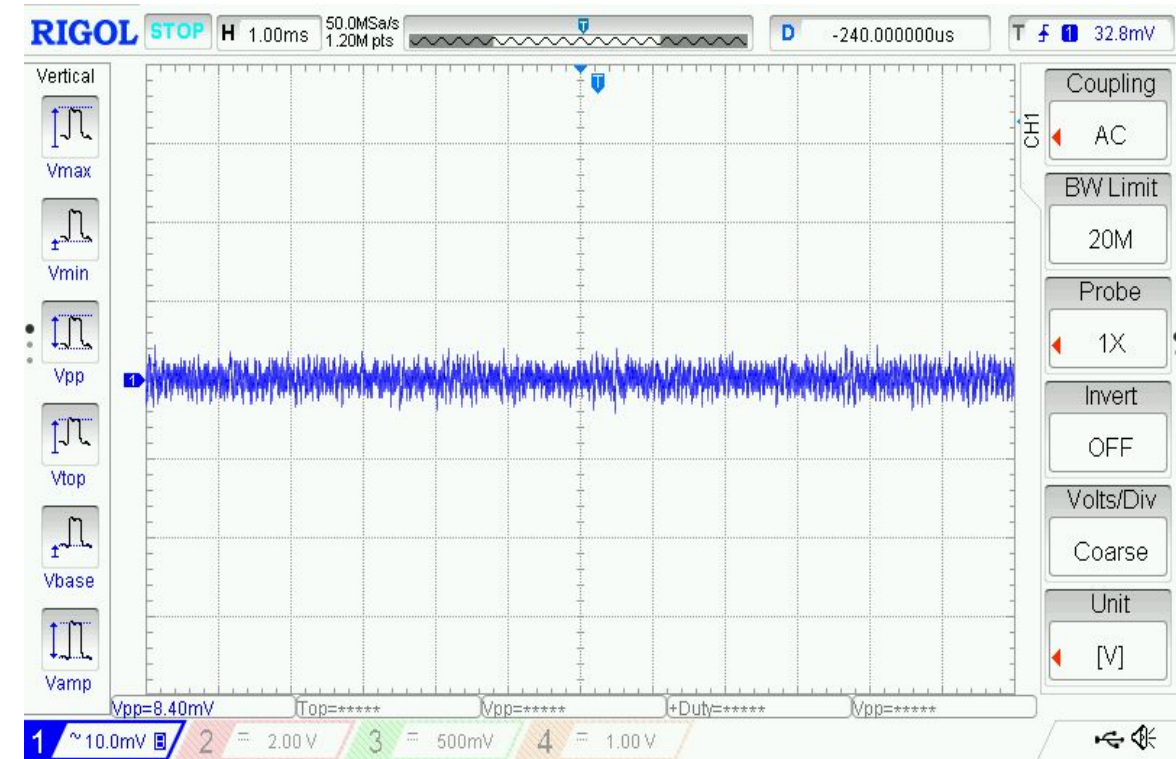


$V_{out} = 0.675\text{ V}$
Transient 3 A – 4 A @ 10 A/ μ s
 $V_{pp} = 22.4\text{ mV}$
 $F_{sw} = 1\text{ MHz}$
 $L = 0.33\text{ }\mu\text{H}$, $C = 8 \times 47\text{ }\mu\text{F}$

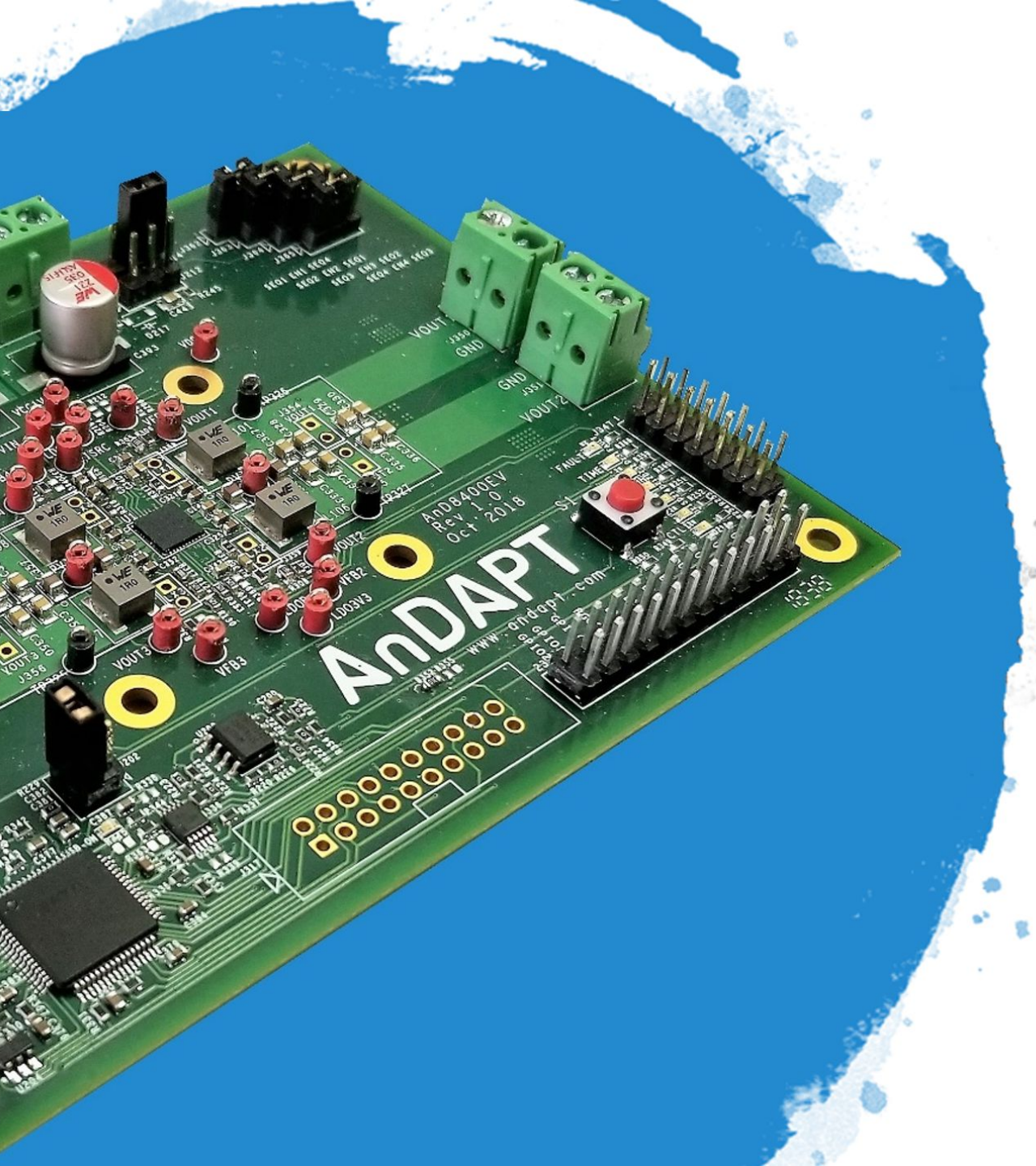
Ripple



No Load
 $V_{PP} = 5.20 \text{ mV}$



4 A Load
 $V_{PP} = 8.40 \text{ mV}$



Thank You