DrMOS Controller Dual Buck PMIC

Adaptable PMIC AnD7200

Product Description

The AnD7200 Adaptable PMIC uses AnDAPT AmP™ advanced technology consisting of fully flexible digital fabric embedded with high performance analog blocks. The AnD7200 consists of one configurable DrMOS controller, two 10A high current synchronous Buck regulators, along with an integrated sequencer and four additional auxiliary LDOs. The AnD7200 is fully tested and ready for use in designs. The AnD7200 Buck regulators use voltage-mode control. The user can modify output voltages and rail sequencing using external resistors or WebAdapter™ online tool. The sequencer can be programmed based on either timed delays or Power Good (PGOOD) signals. Adaptable PMICs provide fastest prototyping and time-to-market, while providing best-in-class performance and flexibility. The Adaptable PMIC is optimized to power high-end processors by integrating multiple power rails into single-chip designs.

Features

- One 40 A (thermally limited) DrMOS Controller V_{OUT}: 0.7 V to 5 V
- One 10 A Buck, PV_{IN} 4.75 V to 14 V, V_{OUT}: 0.7 V to 5.0 V
- Protections. Input output UVLO, OCP, OVP, OTP
- Four 200 mA aux. LDOs. V_{OUT}: 1.2 V, 1.8 V, 2.5 V, 3.3 V
- Adjustable output voltage with 2.4 mV resolution
- 1% load regulation
- Buck regulator efficiency up to 95%
- PGOOD flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- Easy WebAmP upgrade path to On-Demand PMIC

Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- Powering FPGA, processor, SSD, subsystem power control & sequencing

Product Detail

The AnD7200 adaptable PMIC consists of one customizable DrMOS Controller, two 10A and status pins including enable input and an optional PGOOD output. Evaluation Board support includes the AnD72XXEB. DrMOS device support includes: SiC645A Vishay Siliconix and ISL99227 Intersil Renesas. The AnD7200 is available in a 5mm x 5mm thermally enhanced QFN package.

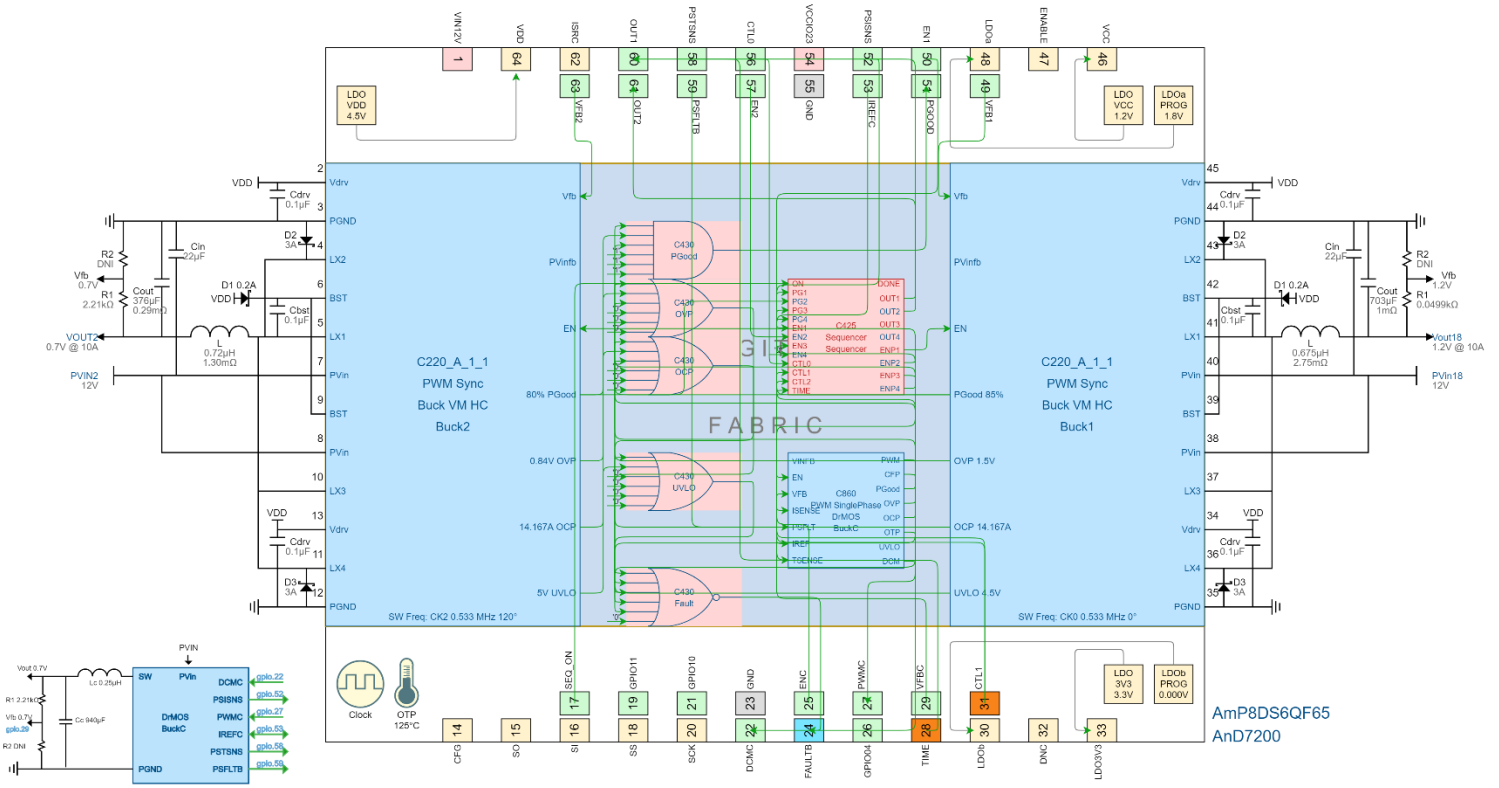
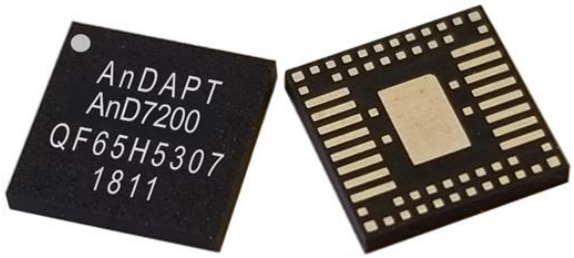


Figure 1. AnD7200 WebAmP Design View

Order Information

Part Number	Package	Description	Availability
AnD7200QF65	QF65	DrMOS Cntrl, Dual Buck PMIC	Now

Package Marking Example – QF65



Package Pinout

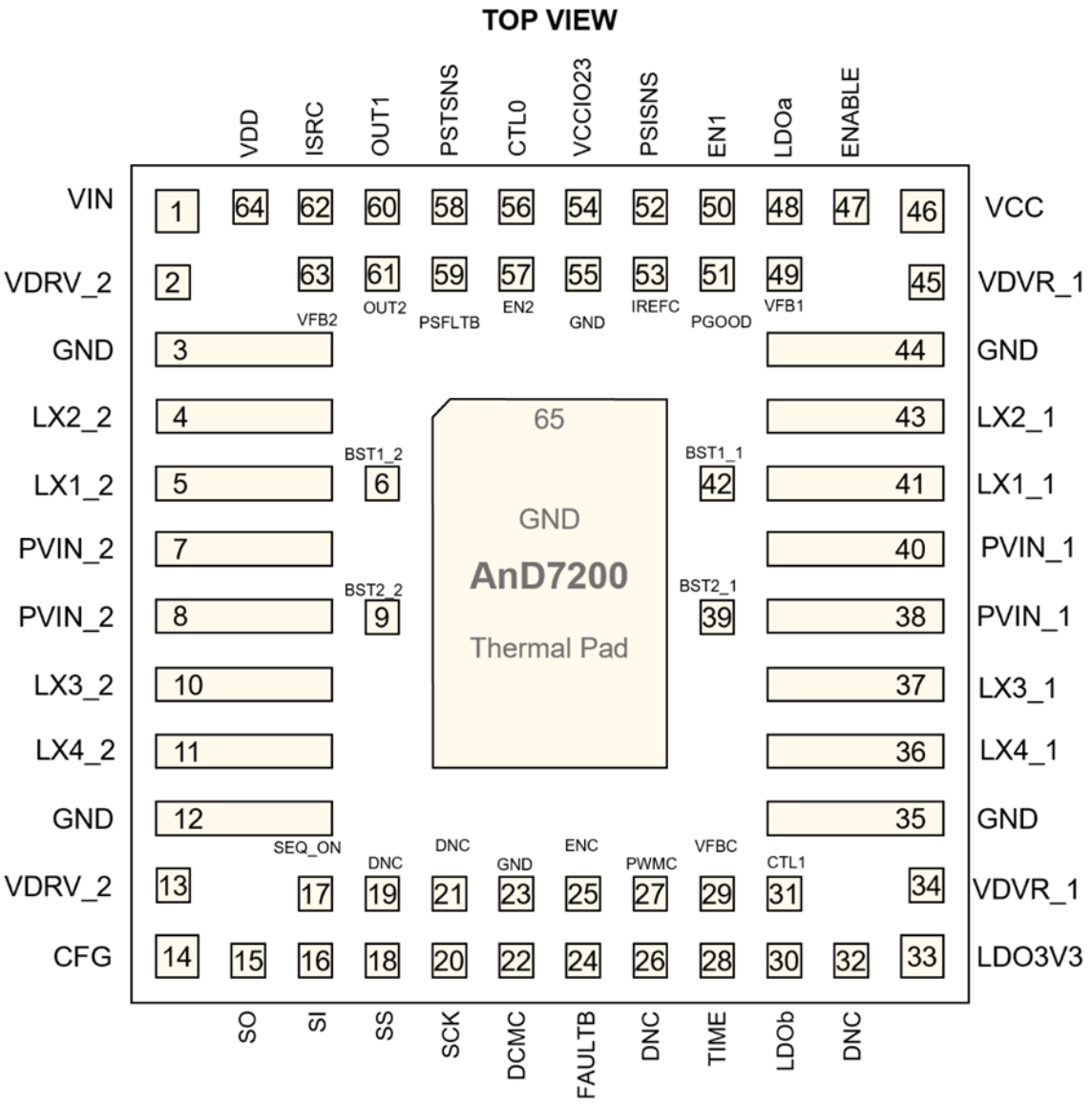


Figure 2. AnD7200 package pinout

Pin Function and Description

Pin Name	Pin #	Description
VIN	1	VIN bias supply for: VDD, VCC, LDO3V3, LDO1V8, LDO2V5
VDRV_2	2	Low side MOSFET gate drive supply for High Current Sync Buck 2
GND	3	Low side MOSFET source for Buck 2, must be connected to GND
LX2_2	4	Switch node (LX) Low side MOSFET drain for High Current Sync Buck 2
LX1_2	5	Switch node (LX) High side MOSFET source for High Current Sync Buck 2
BST1_2	6	Bootstrap pin High side MOSFET gate drive for High Current Sync Buck 2
PVIN_2	7	Power Input for High Current Sync Buck 2
PVIN_2	8	Power Input for High Current Sync Buck 2
BST2_2	9	Bootstrap pin High side MOSFET gate drive for High Current Sync Buck 2
LX3_2	10	Switch node (LX) High side MOSFET source for High Current Sync Buck 2
LX4_2	11	Switch node (LX) Low side MOSFET drain for High Current Sync Buck 2
GND	12	Low side MOSFET source for Buck2, must be connected to GND
VDRV_2	13	Low side MOSFET gate drive supply for High Current Sync Buck2
CFG	14	CFG input active high configuration restart. Device is held in reset while signal is high. Reconfiguration is triggered on negative edge.
SO	15	SPI SO output transmits SPI commands during configuration
SI	16	SPI SI input receives SPI data during configuration
SEQ_ON	17	Enable Sequencer
SS	18	SPI SS output slave, select when master, input when slave during configuration
ENL2	19	Enable LDO1
SCK	20	SPI SCK output clock when master, input clock when slave during configuration
ENL1	21	Enable LDO1
DCMC	22	DrMOS lower gate control signal output for Discontinuous current mode
GND	23	Ground
FAULTB	24	Fault output open drain active low. Dual function pin, shared with DONE output, signals end of configuration when high-Z
ENC	25	Enable DrMOS
DNC	26	Do not connect, floating
PWMC	27	PWM output for DrMOS power stage
TIME	28	Sequencer mode control, high = TIME mode, low = PGood mode
VFBC	29	Feedback voltage for DrMOS
LDOb	30	LDO 2.5V output
DNC	31	Do not connect, floating
DNC	32	Do not connect, floating

Table 1. AnD7200 pinout

Pin Function and Description (continued)

Pin Name	Pin #	Description
LDO3V3	33	LDO output 3.3V
VDRV_1	34	Low side MOSFET gate drive supply for Buck 1
GND	35	Low side MOSFET source for High Current Sync Buck2, must be connected to GND
LX4_1	36	Switch node (LX4) Low side MOSFET drain for High Current Sync Buck 1
LX3_1	37	Switch node (LX3) High side MOSFET source for High Current Sync Buck 1
PVIN_1	38	Power Input for Buck 1
BST2_1	39	Bootstrap pin High side MOSFET gate drive for High Current Sync Buck 1
PVIN_1	40	Power Input for Buck 1
LX1_1	41	Switch node (LX1) High side MOSFET source for High Current Sync Buck 1
BST1_1	42	Bootstrap pin High side MOSFET gate drive for High Current Sync Buck 1
LX2_1	43	Switch node (LX2) Low side MOSFET drain for High Current Sync Buck 1
GND	44	Low side MOSFET source for High Current Sync Buck 1, connect to GND
VDRV_1	45	Low side MOSFET gate drive supply for Buck 1
VCC	46	VCC, LDO 1.2V output and input for digital circuitry
ENABLE	47	Chip enable, AnD7200 powered on when floating (default), powered down when pulled low.
LDOa	48	LDO 1.8V adjustable output
VFB1	49	Feedback voltage for Buck 1
EN1	50	Enable Buck1
PGOOD	51	Global Power Good, includes Buck1, High Current Sync Buck 2 and DrMOS
PSISNS	52	Current monitor input from DrMOS Power Stage to controller
IREFC	53	DrMOS power stage REFIN signal
VCCIO23	54	Supply input to GPIO bank, 3.3V
GND	55	Digital ground
CTL0	56	Sequencer Control 0
EN2	57	Enable High Current Sync Buck 2
PSTSNS	58	Temperature monitor input from DrMOS Power Stage to controller
PSFLTB	59	Open drain fault input pin from DrMOS Power Stage to controller.
OUT1	60	Sequencer OUT1 Connect to Buck 1 EN pin to be the first in sequence.
OUT2	61	Sequencer OUT2 Connect to High Current Sync Buck 2 EN pin to be the second in sequence.
ISRC	62	NC (No connect)
VFB2	63	Feedback for High Current Sync Buck 2
VDD	64	VDD LDO 4.5V output, input bias for analog circuitry
GND	65	Thermal pad, connect to GND

Absolute Maximum Ratings

over operating free-air temperature range

		Min	Max	Unit
Drain to Source Voltage		-1	22	V
V_{IN} Bias Supply		-1	22	V
Boost Voltage, referenced to Source		-1	6.6	V
All other pins		-1	6.6	V
Continuous Drain Current	Package power dissipation may limit current		8	A
Temperature range	Operating Junction temperature range, TJ	–40	125	°C
	Storage temperature range, Tstg	–65	150	

ESD Ratings

		Value	Unit
Electrostatic Discharge	Human body model	±2000	V
	Charged device model	±500	V

Thermal Information

Symbol	Thermal Metric	QF65	Unit
$\theta_{JA(effective)}$	Effective Junction-to-ambient thermal resistance (System Level)*	20	°C/W
Package Manufacturer ratings (JEDEC reference)			
θ_{JC}	Junction-to-case (top) thermal resistance	11	°C/W
θ_{JB}	Junction-to-board thermal resistance	9	°C/W

*$\theta_{JA\{effective\}}$ measured on AnDAPT AnD8240EB Evaluation Board and AmP8DB1REV5.0 Demonstration Board

Package Dissipation Ratings

Package	$\Theta_{JA(effective)}$	T_A = 55°C Power Rating (W) Still air flow	T_A = 55°C Power Rating (W) 200 LFM air flow	T_A = 55°C Power Rating (W) 400 LFM air flow
QF65	20	3.5	3.8	4.1

Recommended Operating Conditions

over operating free-air temperature range

	Min	Max	Unit
PVIN_1, PVIN_2	4.75	14	V
LX1_1, LX2_1, LX1_2, LX2_2, LX3_2, LX4_2	-0.8	14	V
BST1_1 and BST2_1 to LX1_1, LX2_1, LX3_1 & LX4_1 pins; BST1_2 and BST2_2 to LX1_2, LX2_2, LX3_2 & LX4_2 pins	-0.1	5.5	V
VDRV_1, VDRV_2	3.0	5.5	V
VCCIO23	3.14	3.46	V
All other pins	-0.3	3.66	V
T_A	–40	85	°C
T_J	–40	125	°C

Digital GPIO Electrical Characteristics

V_{IN}=12V and T_A=25°C

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.24	0.4	V_{CCIO} – 0.5	2	-2

DrMOS Features

- PWM, voltage-mode DrMOS controller
- Output voltage resolution 2.4 mV
- 1% voltage accuracy
- Efficiency up to 94%
- Switching frequency 533 kHz
- Protections:
  Input Undervoltage Lockout (ViUVLO), Output Undervoltage Lockout (VoUVLO), Overcurrent Protection (OCP), Overvoltage Protection (OVP), Over temperature Protection (OTP), Short-circuit Protection (SCP)
- Power-good flag output and Enable input
- Controller junction temperature range –40°C to +125°C
- Component included in the WebAmP™ development tool

Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing

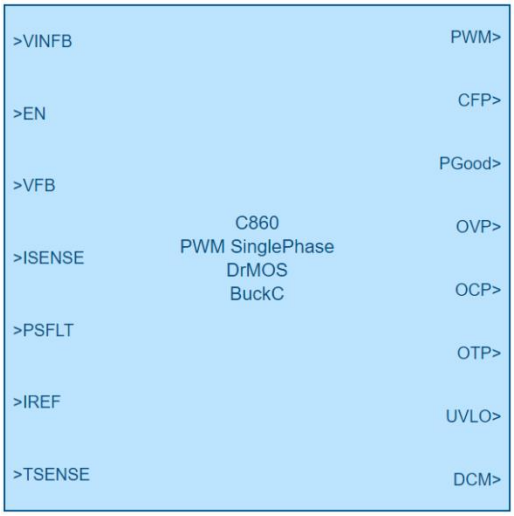


Figure 3. C860 Power Component

DrMOS Product Detail

The C860 Synchronous Buck controller power component symbol is shown in Figure 3. The controller drives a DrMOS integrated power stage with connections as shown in Figure 4 and described in the Pin Function and Description Table 2. A typical application diagram is shown in Figure 5.

Output voltage feedback is compared against an internal reference using a high-performance voltage-error digitizer that provides tight voltage regulation accuracy. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is either generated internally via an oscillator with selectable frequencies or provided via an external pin.

The customizable output voltage is specified during customization using AnDAPT's cloud-based WebAmp development software. The C860 component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), undervoltage lockout (UVLO), catastrophic DrMOS failure (CFP) or over temperature (OTP) condition. The threshold values are specified using the WebAmp tool. See C860 datasheet for more DrMOS details.

Customizable soft-start and soft-stop slew rates are set using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 Sequencer, by interconnecting signals EN and PGood to provide customizable dependencies and customizable delays between each sequence step. See C420 datasheet for more sequencer details.

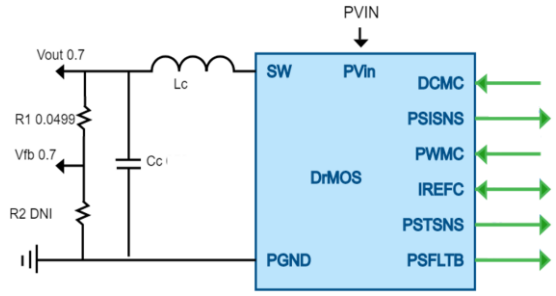


Figure 4. AnD7200 interface with DrMOS

DrMOS Compatible Devices

Compatible devices include:

SiC645A Vishay Siliconix

ISL99227 Intersil Renesas

Pin Function and Description Table

Port Name	GPIO Name	SiC645 pin Name	I/O	Description
OVP			O	Over Voltage Protection fault flag for internal connection to AmP fault manager
OCP			O	Over Current Protection fault flag for internal connection to AmP fault manager
OTP			O	Over Temperature Protection fault flag for internal connection to AmP fault manager
UVLO			O	Input Under Voltage Lock Out fault flag for internal connection to AmP fault manager
PGOOD			O	Controller Power Good signal
CFP			O	Catastrophic Fault Protection fault flag for internal connection to AmP fault manager.
VINFB			I	Internal - Input voltage measurement for ViUVLO protection
TSENSE	PSTSNS	TMON	I	Temperature monitor input from DrMOS Power Stage to C860 controller
PSFLT	PSFLTB	FAULT#	I	Open drain fault input pin from DrMOS Power Stage to C860 controller.
ISENSE	PSISNS	IMON	I	Current monitor input from DrMOS Power Stage to C860 controller.
IREF	IREFC	REFIN	I	Reference voltage connected to DrMOS power stage REFIN signal and to C860 controller. Recommend using AmP auxiliary 1.2V LDO to drive the signal.
DCM	DCMC	LGCTRL	O	DrMOS power stage lower gate control signal output from DrMOS controller. Used for Discontinuous current mode operation for light load efficiency when available on the DrMOS.
EN			I	Enable DrMOS controller
PWM	PWMC	PWM	O	DrMOS power stage gate driver control signal output from DrMOS controller
VFB	Vfb		I	VOUT feedback for DrMOS controller

Table 2. DrMOS pin interface with AnD7200

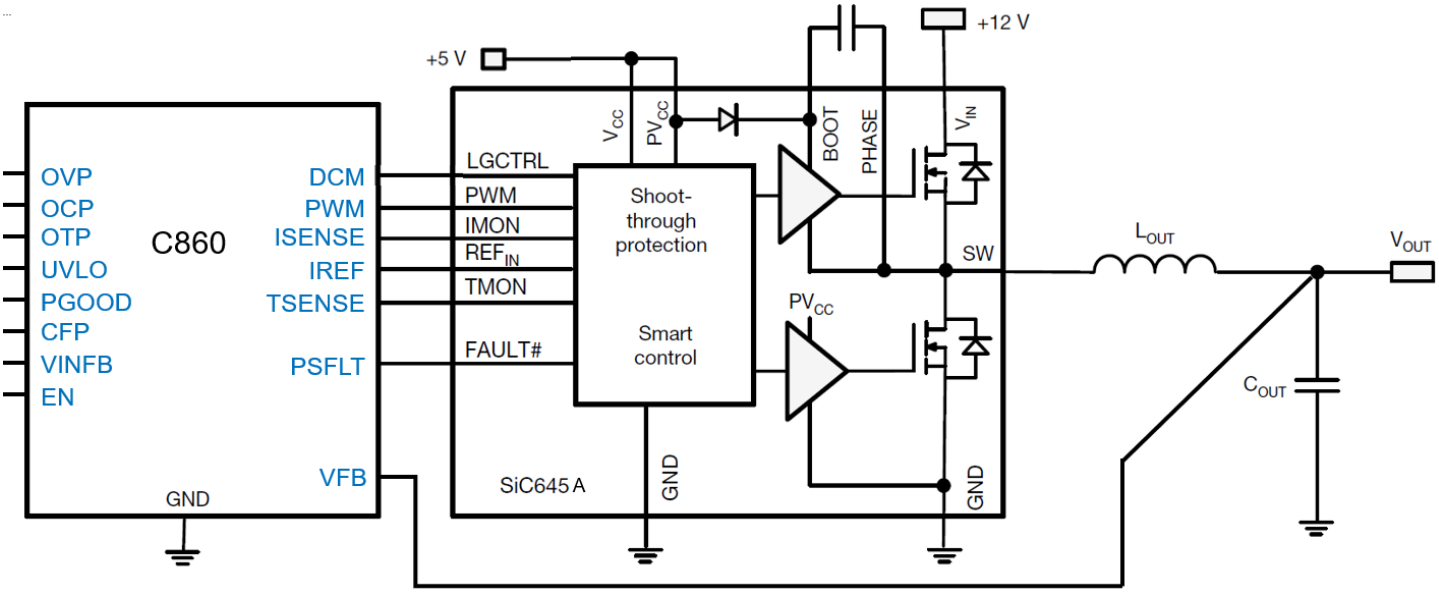


Figure 5. Typical Application Diagram

Electrical Characteristics DrMOS Controller

PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

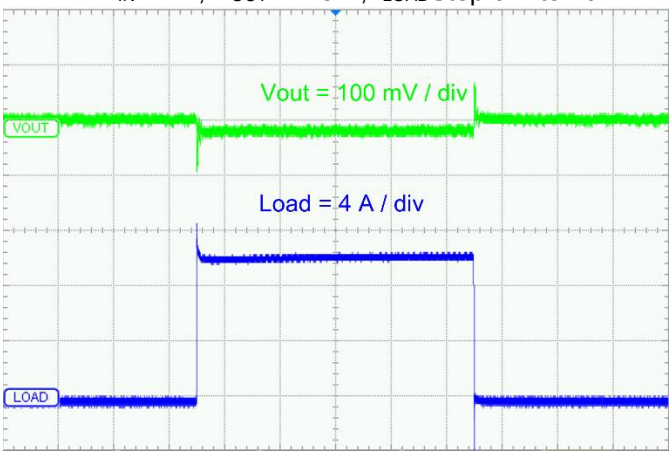
Parameters	Test Conditions		Min	Typ	Max	Units
Output Voltage (V_{OUT})			0.7		5.0	V
Output Voltage Accuracy	V_{IN} range (Including load line and temperature variation)	6V to 14V	-2		+1	%
		4.5V to 6V	-1		+1	%
Switching frequency (F_{SW})				533		kHz
Switching frequency accuracy			-5		+5	%
Efficiency	V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=10A			94		%
PROTECTION						
ViUVLO, input Undervoltage Lockout range			4		10	V
OCP, Over Current Protection (% I_{OUT})			150			%
OTP, Over Temperature Protection for AmP device	Shutdown (Power Good goes low) Hysteresis		125	150	175	°C
OVP, Overvoltage Protection trip point range (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration		+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration		-100		-432	mV
Power Good threshold (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration		-100		-432	mV

Typical Characteristics DrMOS Controller

Unless otherwise specified: TA = 25°C

Transient Response

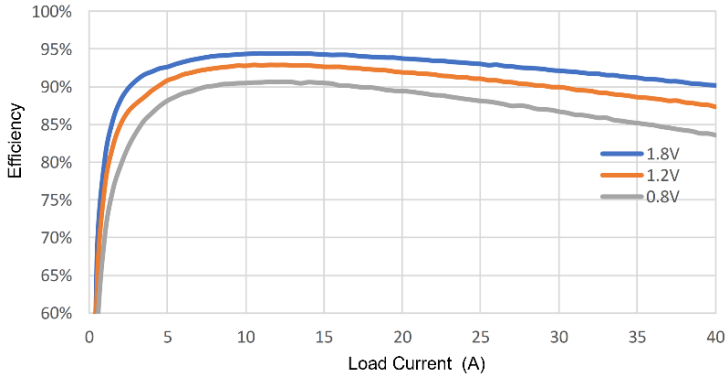
PV_{IN}=12V, V_{OUT} = 1.5 V, I_{LOAD}Step 0 A to 10 A



Time = 200 µs / div F_{SW}=571 kHz

Efficiency

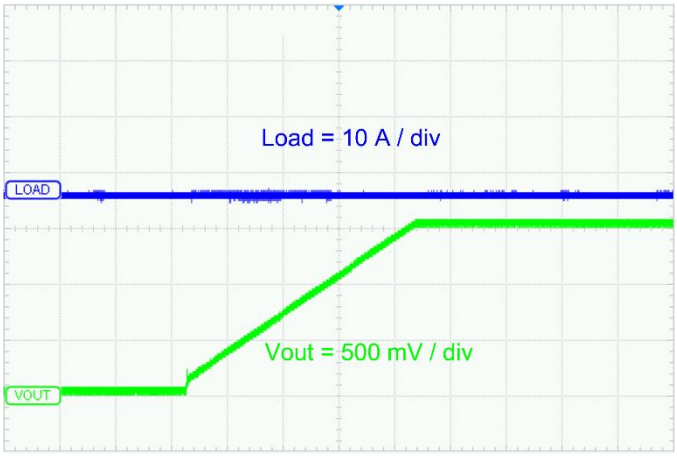
PVin=12 V, L_{OUT}=250 nH, C_{OUT}=564 uF



F_{SW}=571 kHz

Soft Start No Load

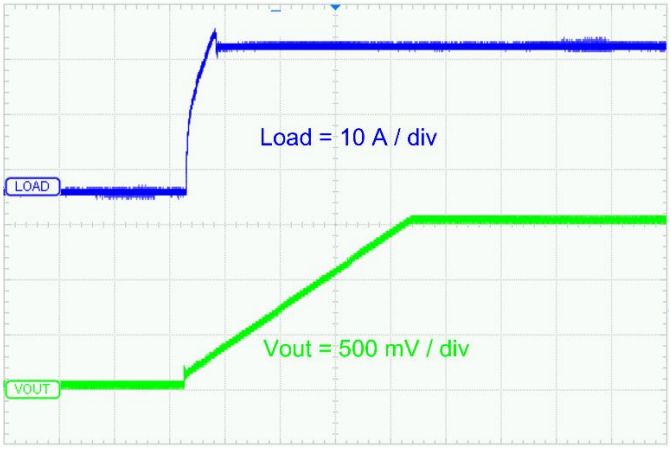
PV_{IN}=12 V, V_{OUT} = 1.5 V



Time = 2 ms / div FSW=571 kHz

Soft Start with Load

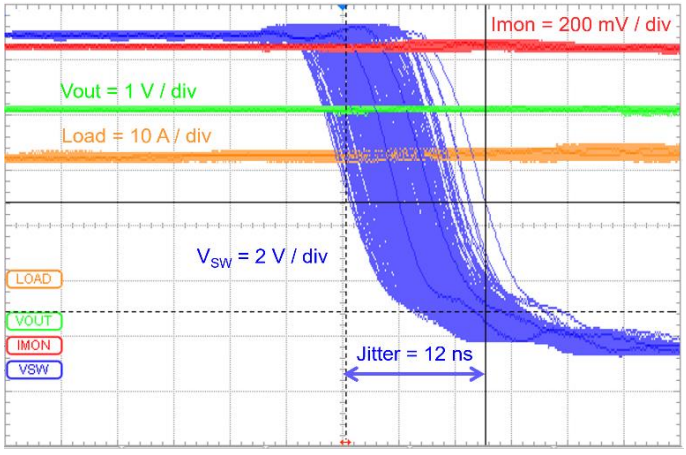
PV_{IN}=12 V, V_{OUT} = 1.5 V, I_{LOAD} = 28 A



Time = 2 ms / div FSW=571 kHz

Jitter

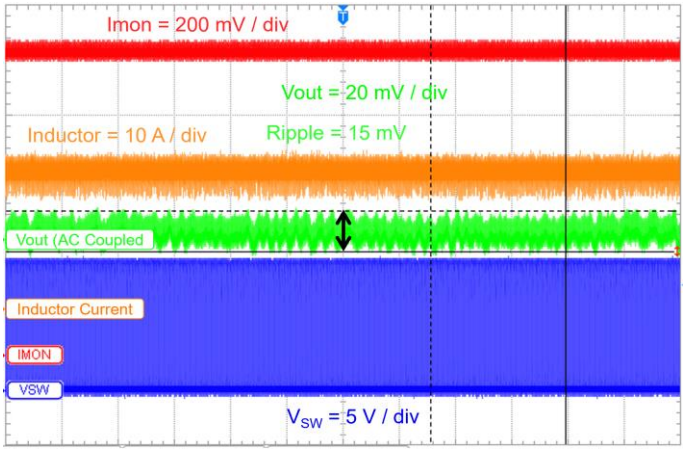
PV_{IN} = 12 V, V_{OUT} = 3.8 V, I_{LOAD} = 25 A



Time = 2 ms / div FSW=571 kHz

Ripple

PV_{IN} = 12 V, V_{OUT} = 0.8 V, I_{LOAD} = 30 A



Time = 200 µs / div FSW=571 kHz

Synchronous Buck Features

- PWM, voltage mode, point-of-load (POL) regulator
- Maximum output current: 10A
- PV_{IN}: 4.75V to 14V, V_{OUT}: 0.7V to 5.0V
- Switching Frequency: 533kHz
- Adjustable output voltage with 2.4 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 15mΩ (10A)
- 1% load regulation
- Efficiency up to 95%
- Internal single pole compensator minimizes external part count
- Protection: Input Undervoltage Lockout, (ViUVLO), Output Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature

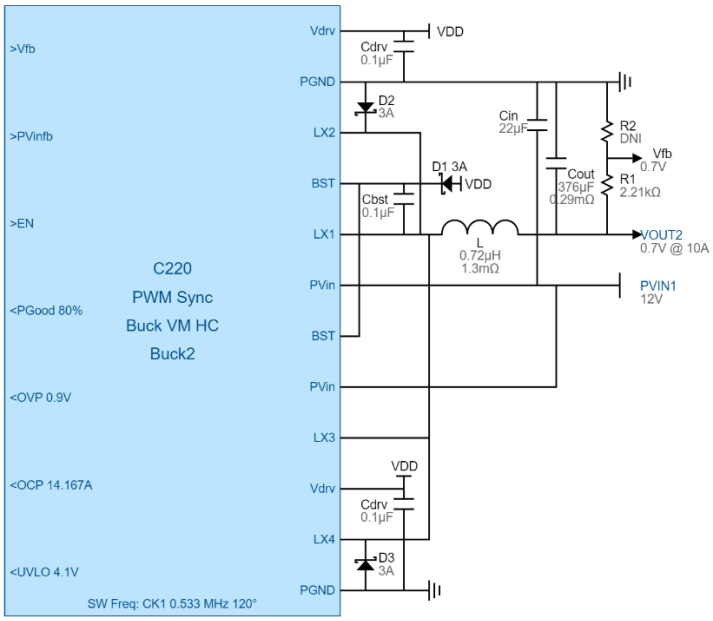


Figure 6. Buck, 10A Typical WebAmP Schematic

Synchronous Buck Detail

The AnD7200 Synchronous Buck Regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFETs (SIM) provide up to 10A output current.

Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is generated internally via an oscillator and is fixed at 533kHz.

The customizable output voltage is specified by the WebAdapter tool or an external resistor divider. The regulator has customizable control and status pins including enable input, power-good output, and output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition.

The soft-start and soft-stop slew rates are also specified at 4 ms. Additional sequencing options are available by using the WebAdapter tools or jumpers.

The AnD7200 uses predefined power components from the AmP power library. This allows an easy migration to On-Demand PMIC. The buck converters are based on the C220 power component.

Recommended Operating Conditions Synchronous Buck

Over operating free-air temperature range
This section applies to all two Power Regulators

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	4.75		14	V
I_{Lmax}	Load Current Maximum			10	A
V_{IN}	Bias Supply	4.75		14	V

Electrical Characteristics Synchronous Buck

PV_{IN} = V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

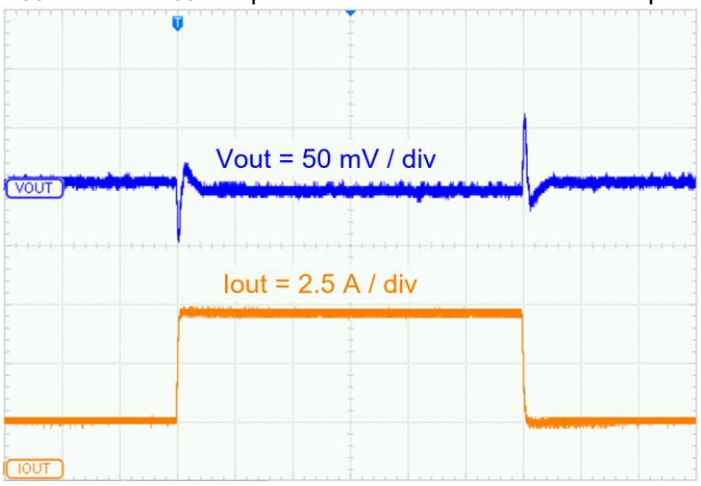
Parameters	Test Conditions		Min	Typ	Max	Units
Output Voltage (V_{OUT}) Range			0.7		5	V
Output Voltage Regulation	V_{IN} range (Including load line and temp. variation)	6V to 14V	-2		+1	%
		4.5V to 6V	-1		+1	%
Switching frequency (F_{SW})				533		kHz
Switching frequency accuracy			-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$)	Buck2			15		mΩ
Efficiency	V_{IN}=12V, V_{OUT}=1.2V, F_{SW}=533kHz, I_{OUT}=3A			83		%
Input Shutdown current (V_{IN})	EN = 0V			13		mA
Input quiescent current (PV_{IN})				7		mA
PROTECTION						
ViUVLO, input Undervoltage Lockout			4		10	V
OCP, Over Current Protection (% I_{OUT})				142		%
OTP, Over Temperature Protection	Shutdown (Power Good goes low) Hysteresis		125			°C
OVP, Overvoltage Protection trip point range (relative to Parameter Setting)			+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Parameter Setting)			-100		-432	mV
Power Good threshold (relative to Parameter Setting)			-100		-432	mV

Typical Characteristics Synchronous Buck: Buck2

Unless otherwise specified: T_A = 25°C, F_{SW} = 533 kHz, L_{OUT} = 1.2 µH, C_{OUT} = 376 µF

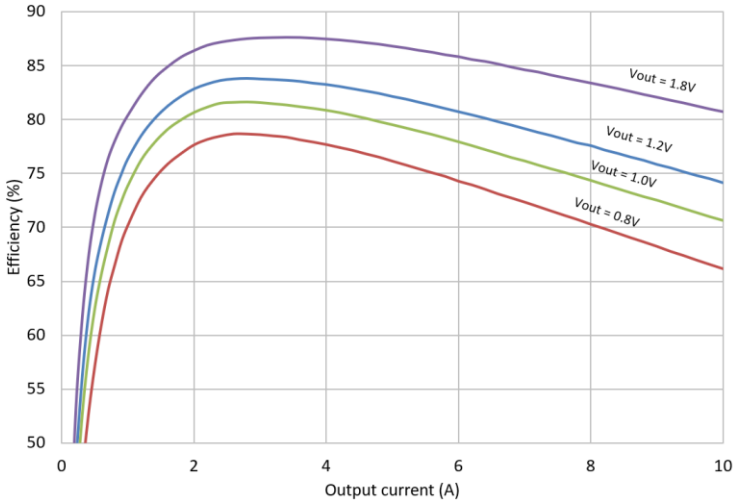
Transient Response

V_{OUT} = 1.2 V I_{OUT} step 2.5 A to 7.5 A Slew Rate: 2.5A/µs



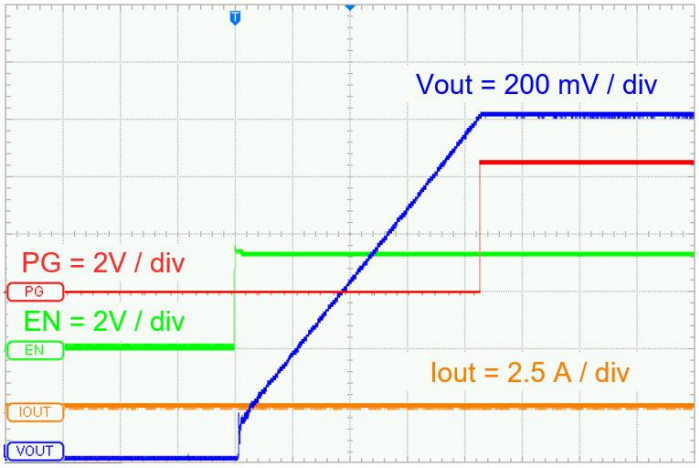
Time = 200 µs / div

Efficiency



Soft Start, No Load

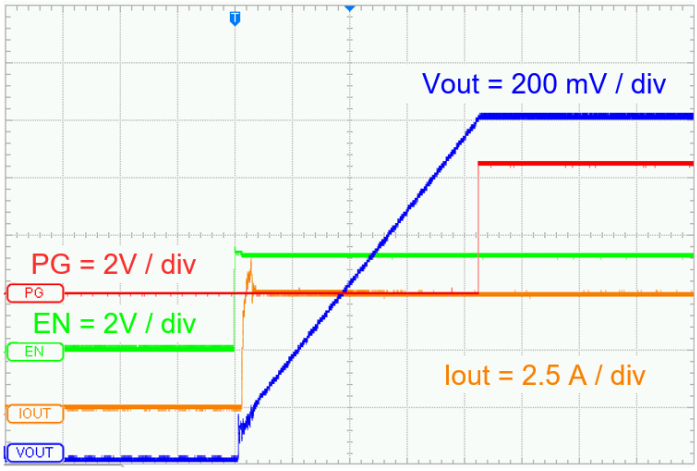
PV_{IN} = 12V, V_{OUT} = 1.2V



Time = 2 ms / div

Soft Start, Load = 5A

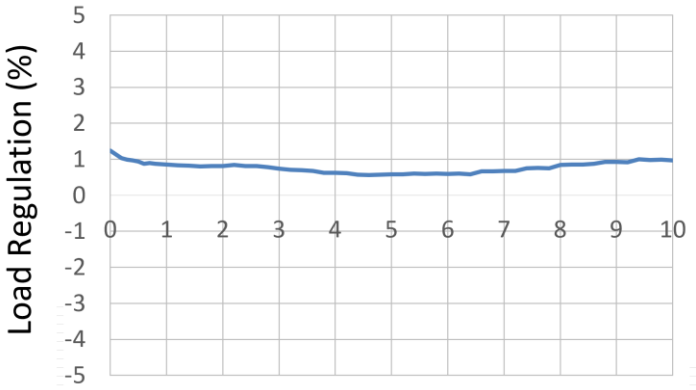
PV_{IN} = 12V, V_{OUT} = 1.2V



Time = 2 ms / div

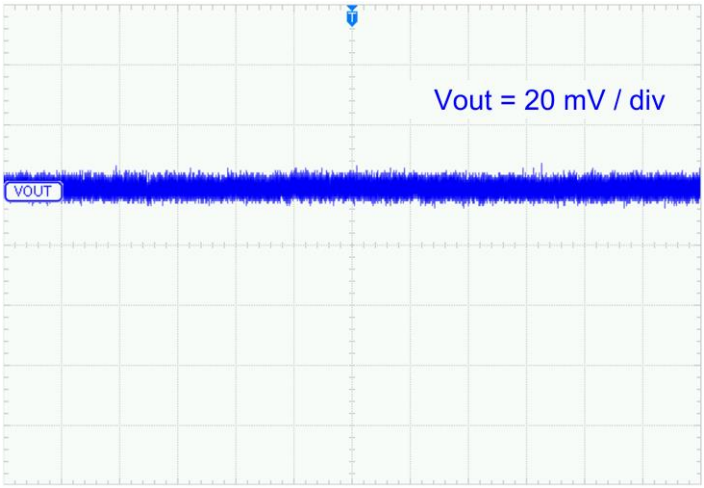
Load Regulation Percentage Error

PV_{IN} = 12V, V_{OUT} = 1.2V



Vout Ripple

PV_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 10A



Time = 100 ms / div

Inductor Selection

Based on output voltage target, the Table 3 shows recommended inductor and compensation capacitor value providing optimal performance.

Ct capacitance is required for higher output voltage range, in parallel with R1 resistor, to improve stability of the compensation without changing the PID coefficients.

As an example, for an output voltage ranging between 1.2 V to 2.5 V, use a 1.5uH inductor and capacitance Ct of 2.2nF.

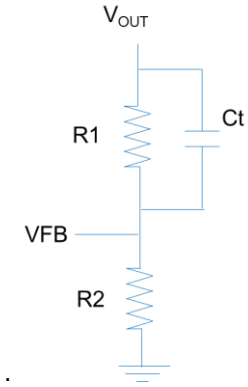


Figure 7. V_{OUT} feedback network

VIN = 12V	fsw = 530kHz-571kHz			
VOUT	L=0.68uH Ct=N/A	L=1uH Ct=N/A	L=1.5uH Ct=2.2nF	L=2.2uH Ct=4.7nF
0.7V				
1.0V				
1.2V				
1.5V				
1.8V				
2.5V				
3.3V				
5V				

L value is in the ideal range

L value just outside the ideal range, system works correctly

Table 3. Inductor selection

V_{OUT} Resistor Settings

V_{OUT} voltages for Buck1 and Buck2 POLs are set by the resistors R1 and R2. The AnD7200 internal feedback reference, VFB, is 0.7 V for Buck1 and Buck2 with feedback resistor recommended values of

R1 = 2.21 kΩ
R2 = DNI (Do Not Install).

For V_{OUT} values greater the 0.7 V, use the following resistor divider equations:

R1 = 2.21 kΩ

$$R2 = VFB \times \frac{R1}{(Vout - VFB)} \ k\Omega$$

1% resistors are recommended for best accuracy. A resistor calculator for closest E96 1% value is provided by the WebAdapter Software Tool.

These resistor values determine the actual V_{OUT} voltage calculated as shown above. A DNI value indicates “Do Not Install”. R1 and R2 values may now be applied to the Reference Designators for the user’s board design.

Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port. When EN goes high the output voltage, V_{OUT}, will ramp up according to the Soft Start ramp time. When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start preset ramp time.

PGOOD

The power-good, PGOOD, of all Synchronous Buck Converters are combined to generate the global Power Good signal, indicating the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time (Figure 8) and when all Faults are cleared . PGOOD will pull low either when V_{OUT} falls below the preset condition (80% of the V_{OUT}) or when faults occur. These faults include OCP fault , OVP fault , UVLO (both input and output) faults and OTP thermal shutdown fault. PGOOD will also go low if EN goes low.

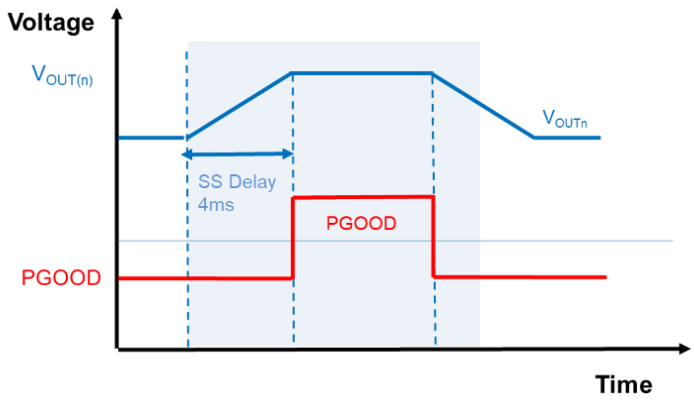


Figure 8 Soft-start and shutdown

Sequencer

The AnD7200 contains a sequencer that can operate either based on time delay or based on power good signal. The selection of power good or time delay is based on the setting of the TIME control pin 28. When the TIME control pin is high, the sequencer is based on time delay. When the TIME control pin is low, the sequencer is based on the PGood signal.

The sequencing delay is programmable from 3 ms to 16 ms using WebAdapter advanced mode. By default, it is set to 6 ms. The soft start is set to 2/3 of the programmed sequencing delay value allowing enough time for the previous sequencer to be fully ON before the next sequence starts.

The sequencer is activated by setting the SEQ_EN to high. TIME, CTL and OUT pins have an internal pull-up resistor, so they can be left floating (or not connected) to be in high state. Low signal can be set with a connection to ground (GND).

TIME Mode

TIME Mode is specified when the TIME pin is in a high state as defaulted in the AnD7200 . In this mode, each Buck[n] regulator tuns ON with a Soft Start when Enable[n], goes high. On completion of Soft Start period, Sequencer Delay remains before Enable[n+1] goes high, beginning the sequence for Buck[n+1]. In the example below, the sequencing delay is set to 6 ms .

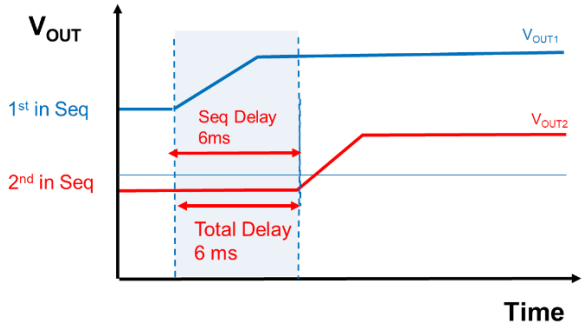


Figure 9. Soft-start TIME mode

Sequencer Pin Connections

POL power-on and power-off sequences for Buck1 and Buck2 are set by the sequence Pin Connections specified in the wire connection in Table 4. Apply these connections to the AnD7200 board design.

In time mode, the outputs (OUT1, OUT2) of the sequencer need to be connected to the appropriate Enable pins for each Buck.

Sequence Output		Enable Input	
Signal Name	AnD7200 Pin Number	Signal Name	AnD7200 Pin Number
OUT1	60	EN1	50
OUT2	61	EN2	57

Table 4. Sequencer pin connections in TIME mode

TIME/CTL Pin Connections

The control pins CTL0 must be held high as indicated in the wire connection Table 5.

Apply these conditions to the AnD7200 board design.

Controls		Signal Level	Function
Signal Name	Pin Number		
TIME	28	High	TIME Mode
CTL0	56	High	Sequence Select

Table 5. TIME and CTL pin behaviour in TIME mode

PGOOD Mode

The user has also the option to set the sequencing using Power good signal.

PGOOD Mode is selected when the TIME pin is in a low state as indicated by the “GND” Signal Level specified in the wire connection table below. Control pin CTL0 specifies the selected sequence.

Controls		Signal Level	Function
Signal Name	Pin Number		
TIME	28	Low	PGOOD Mode
CTL0	56	High	Sequence Select

Table 6. TIME/CTL pin connections

In this mode, each Buck[n] regulator begins a 4 ms Soft Start when Enable[n], goes high. On completion of Soft Start, PGOOD[n] goes high and starts the programmed Sequencer Delay followed by Enable[n+1] going high, beginning the sequence for Buck[n+1]. If the user sets the sequencer delay to 6ms, The total cycle delay is 4ms + 6ms = 10ms per Buck as shown in the timing diagram below.

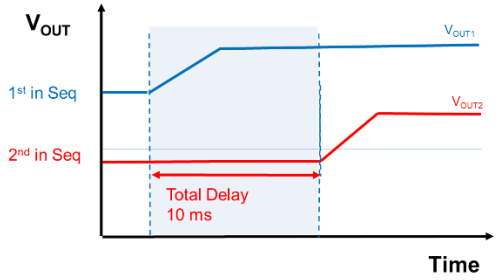


Figure 10. PGOOD mode

PGOOD and Sequencer Pin Connections

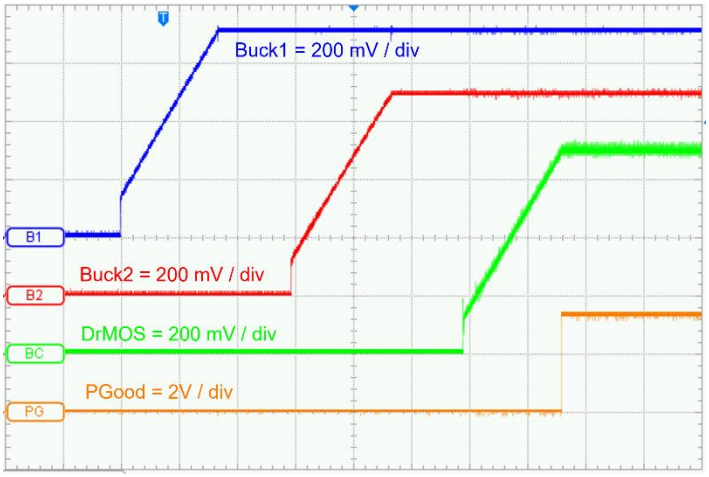
The Control pin, CTL0, specifies the selected sequence.

CTL0	Seq1	Seq2
High	Buck 1	Buck 2
Low	Buck2	Buck 1

Table 7. PGOOD sequence

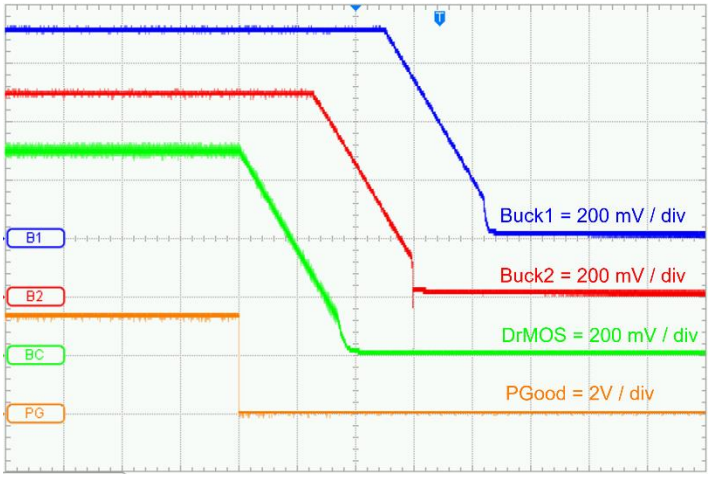
Sequencer Example Waveforms

PGOOD Mode, CTL0 = high



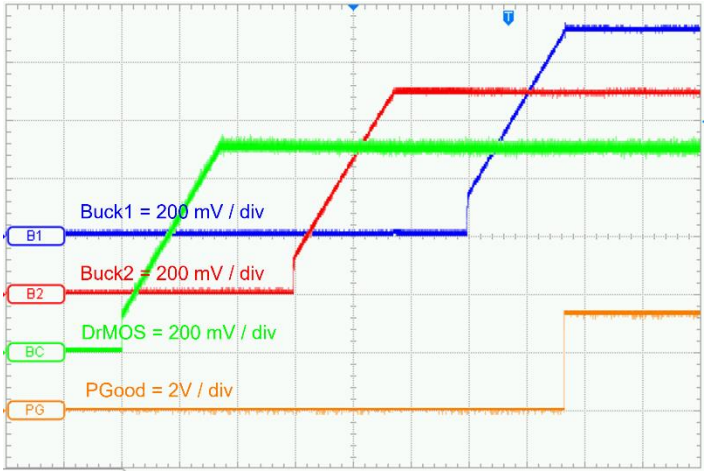
Time = 5 ms / div

PGood Mode, CTL0 = high



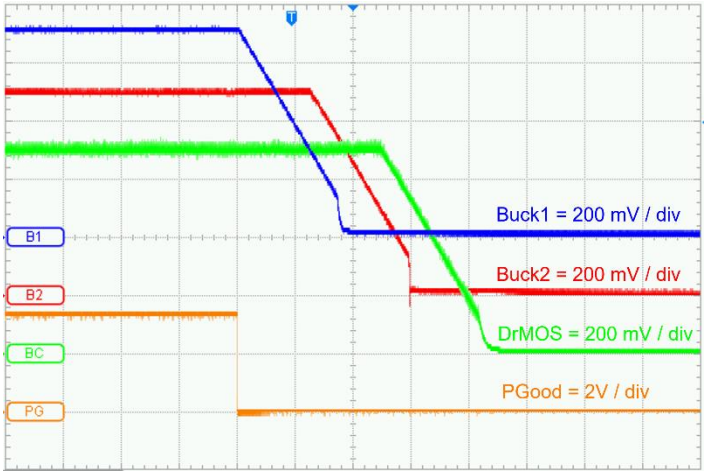
Time = 5 ms / div

PGood Mode, CTL0 = low



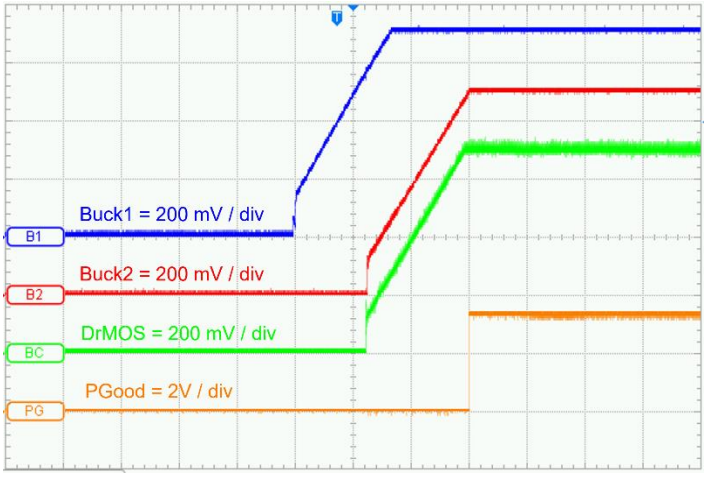
Time = 5 ms / div

PGood Mode, CTL0 = low



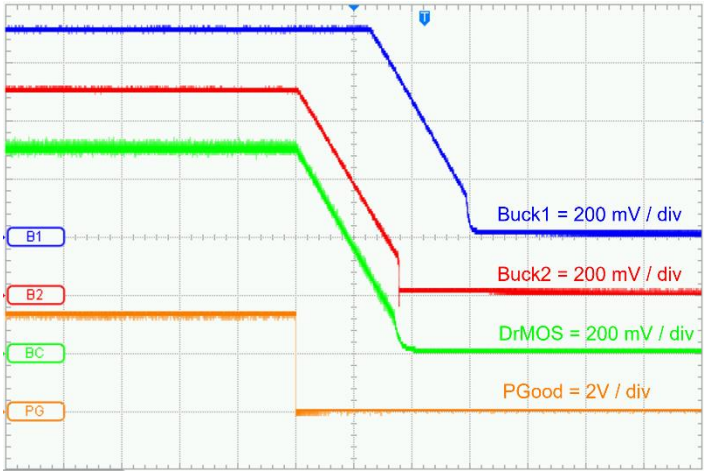
Time = 5 ms / div

TIME Mode, EN1 = OUT1, EN2 = ENC = OUT2



Time = 5 ms / div

TIME Mode, EN1 = OUT1, EN2 = ENC = OUT2



Time = 5 ms / div

Integrated Auxiliary LDOs

The AnD7200 has 4 integrated auxiliary LDOs which have default output voltages of 3.3 V, 2.5 V, 1.8 V, and 1.2 V. The input voltage of the four LDOs is from the internal 4.5 V bias voltage or externally supplied 5 V on the VDD pin. A decoupling capacitance of 10 µF minimum must be connected to the output of the LDO. The pin locations of these integrated LDOs, are fixed and cannot be modified by WebAmP Tools.

Electrical characteristics for Integrated Auxiliary LDOs are shown below in Table 8.

Two of these LDOs (LDOa and LDOb) output voltages are programmable by using the WebAdapter tool.

Electrical Characteristics Integrated Auxiliary LDOs

V_{IN}=12V, T_A=25°C, Cvdd = Cvcc = Cldoa = Cldob= C3v3 = 10µF unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LDO1V2	LDO 1.2V output voltage	I_{CC}=0mA, V_{IN}=4.5V	1.164	1.2	1.236	V
R_{OCC}	LDO 1.2V equivalent resistance			350		mΩ
I_{CC}	LDO 1.2V output current				200	mA
LDOa	LDO 1.8V output voltage	I1V8=0mA, V_{IN}=4.5V	1.746	1.8	1.854	V
R_{O1V8}	LDO 1.8V equivalent resistance			350		mΩ
I1V8	LDO 1.8V output current				200	mA
LDOb	LDO 2.5V output voltage	I2V5=0mA, V_{IN}=4.5V	2.425	2.5	2.575	V
R_{O2V5}	LDO 2.5V equivalent resistance			350		mΩ
I_{CC}	LDO 2.5V output current				200	mA
LDO3V3	LDO 3.3V output voltage	I3V3=0mA, V_{IN}=4.5V	3.201	3.3	3.399	V
R_{O3V3}	LDO 3.3V equivalent resistance			350		mΩ
I3V3	LDO 3.3V output current				200	mA

Table 8. Integrated auxiliary LDO characteristics

Additional Resources

- AnDAPT AmP Platform datasheet
- Power Component datasheets

ESD CONSIDERATIONS

Establish and use (Electrostatic Damage) ESD-safe handling precautions when unpacking and handling ESD-sensitive devices. Store ESD sensitive devices in ESD safe containers until ready for use. The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly. AnDAPT products are qualified to meet at least 500 V ESD-MM (Machine Model) 2000 V ESD-HM (Human Body Model). Restrict all device handling to ESD protected work areas that measure less than 400 V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

Assembly Recommendation

For part placement, please use standard pick and place machine with ± 0.05 mm accuracy. Mount the device with slower speed and higher force. Place the package 1 ~ 2 mils into the paste. The device package has excellent self-alignment during solder reflow if a minimum of 75% of the lead diameter intersect with the pad.

Solder Paste

The screen-printing quantity of solder paste is a key factor in producing high yield assemblies. Recommended solder paste alloy is Sn/Ag/Cu family for lead-free application. Low residue and no clean flux are recommended. Particle size type IV (25 ~ 38 μm) is preferred to improve printing performance. Particle size type III (25 ~ 45 μm) also is acceptable.

Solder Stencils

The contrast between large thermal pads and small terminal pads of the QFN package can present a challenge in production and even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow- solder processing. The solder joint thickness for QFN package terminal pads should be 50 – 75 μm. Stencil recommended type is laser cutting stainless steel with thickness of 100 ~ 150 μm (125 μm as a guide). The actual thickness of a stencil is depending on other SMD components on the PCB. Metal blade or polymer with 90-degree hardness squeegee is recommended. Aperture size for terminal pad should have aspect ratio (width / thickness) of greater than 1.5 and area ratio (Area of aperture opening / aperture wall area) of greater than 0.66. The stencil aperture is typically designed to match the pad size on the PCB 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. An oval-shaped opening should be used to get the optimum paste release and rounded corners to minimize clogging. Positive taper walls (5-degree tapering) with bottom opening larger than the top is recommended. Small multiple openings should be used instead of one big opening. 60% ~ 85% solder paste coverage is recommended to reduce the chance of having short connection.

Reflow Specification

AnDAPT products are qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling to avoid subsequent thermal and mechanical damage during the solder-reflow attachment phase of PCB assembly. Check solder paste data sheet for any additional or difference instruction. Using a forced convection reflow oven with nitrogen is recommended. Also, the reflow oven should have equal or less than ± 5°C temperature uniformity. The recommended reflow profile for lead-free solder paste shown in Figure 11.

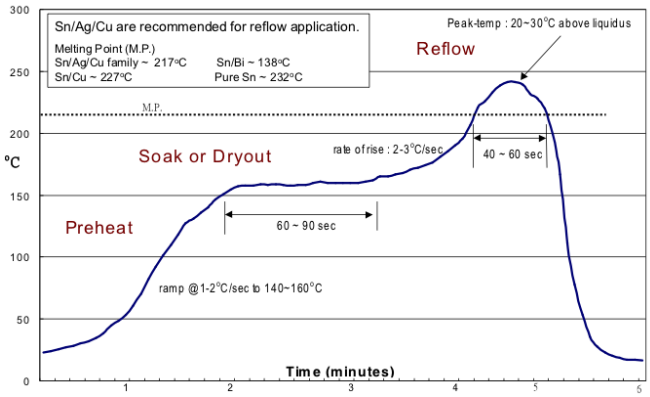


Figure 11. Solder paste

Compliance

Environmental Compliance

AnDAPT products are RoHS and Green compliant. AnDAPT products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC Compliance

AnDAPT products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

Compliance Declaration Disclaimer

AnDAPT believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. AnDAPT subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by AnDAPT.

Internal AnD7200 PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AND7200 PMIC. Listed below is a description of blocks and resources that are used to create Buck regulators.

Noise-immune references - Nrefs

- 10-bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, In Amp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 poles

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

$$P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c$$

1 pole: a1 = 1, a2 = 0 2 poles: a1 = 0.5, a2 = 0.5

$$E[n] = Vref - V_{OUT}[n]$$

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

Scalable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, drain voltage or current and Analog Fabric including programmable references (Nrefs).

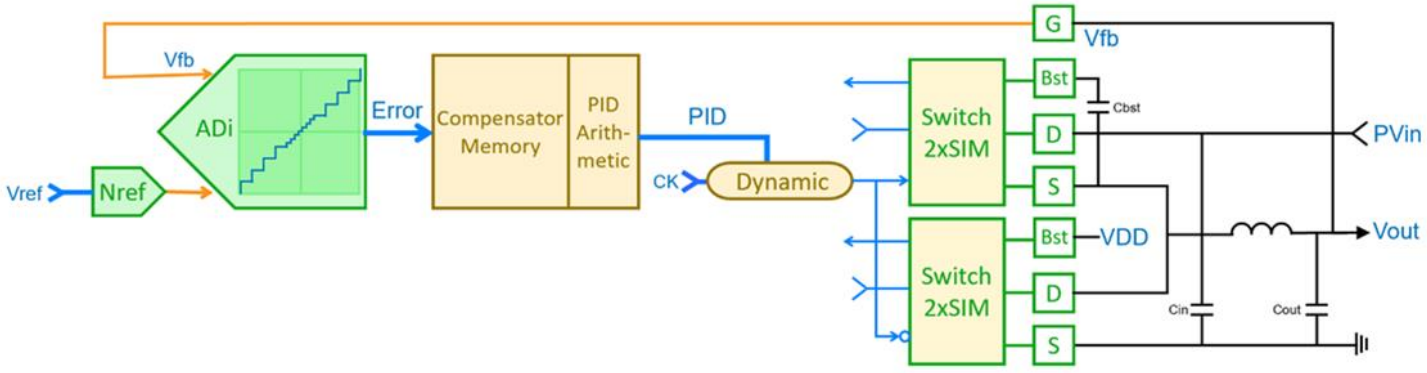
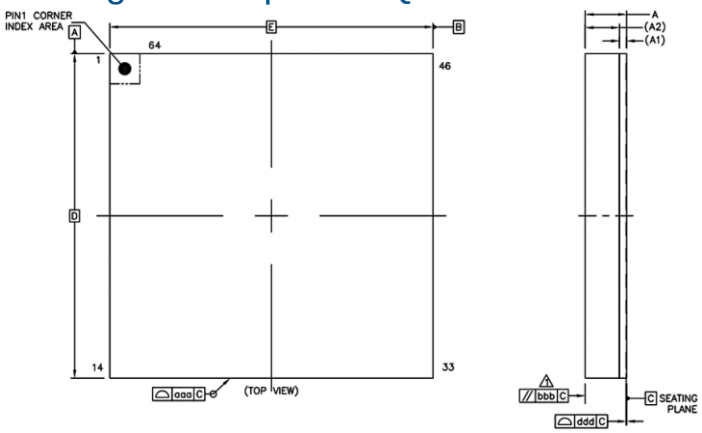
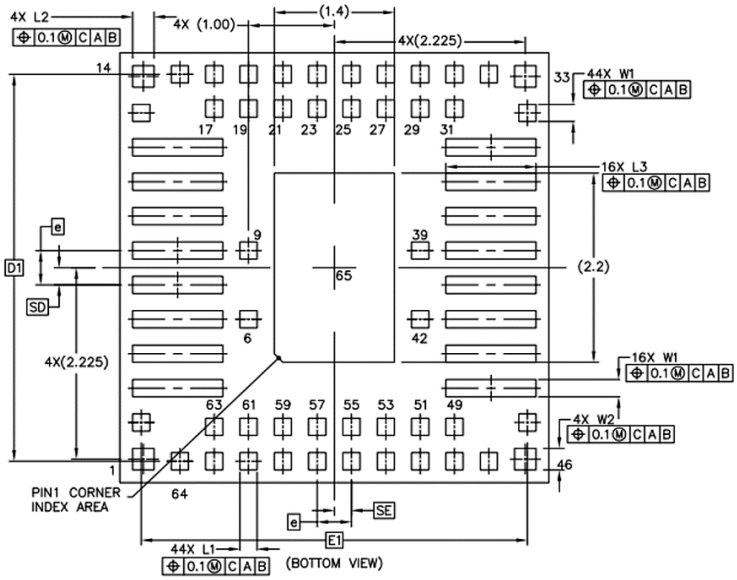


Figure 12: PMIC Blocks and Resources Example - Buck Regulator

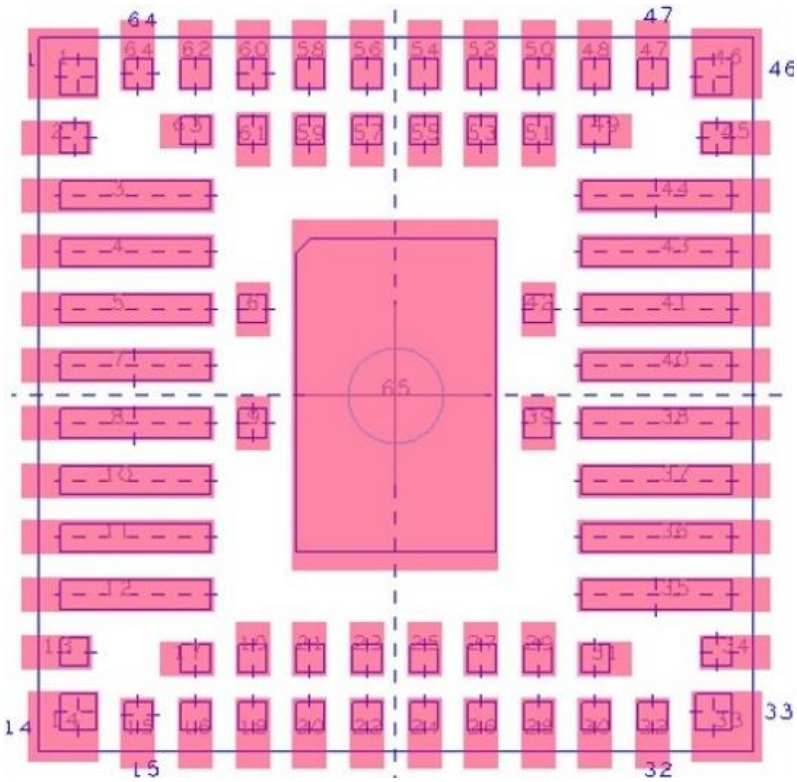
Package Description – QF65 5x5 mm





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.7
SUBSTRATE THICKNESS	A1		0.11	REF
MOLD THICKNESS	A2		0.53	REF
BODY SIZE	D	4.9	5	5.1
	E	4.9	5	5.1
LEAD WIDTH	W1	0.15	0.2	0.25
LEAD WIDTH	W2	0.2	0.25	0.3
LEAD LENGTH	L1	0.15	0.2	0.25
LEAD LENGTH	L2	0.2	0.25	0.3
LEAD LENGTH	L3	1	1.05	1.1
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		65	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

Solder Stencil – QF65 5x5 mm



Download files: AmP8DQF65footprint.zip

Errata

Date	description
12/28/2018	SIM Pin (MOSFET DRV-Drain) ESD 750V HBM

Revision History

Date	Revision
11/04/2019	Initial release

AnDAPT

On-Demand Power Management

www.AnDAPT.com

Trademarks