Dual Synchronous Buck PMIC

Adaptable PMIC AnD8240

Product Description

The AnD8240 Adaptable PMIC uses AnDAPT AmP™ advanced technology consisting of fully flexible digital fabric combined with high performance analog blocks. The AnD8240 consists of two configurable 6A Synchronous Buck Regulators and four high current LDOs. The AnD8240 is fully tested and ready to use in designs. The AnD8240 Buck regulators use Voltage Mode control. The AnD8240 also has an integrated sequencer and 4 additional auxiliary LDOs. The user can modify output voltage and rail sequencing using resistor or WebAdapter™ online tools. The sequencer has the capability to be based on timed delays or Power Good signals. Adaptable PMICs provide fastest prototyping and time to market, while providing best in class performance and flexibility. The AnD8240 design is available in the WebAmP™ software tool library for full customization capability. The Adaptable PMIC is optimized to power high end Processors by integrating multiple power rails into single chip designs.

Features

- Two 6A Synchronous Buck Regulators
- PVIN: 4.75V to 14V, V_{OUT}: 0.7V to 5.0V
- 571kHz Switching Frequency
- Integrated 30 mΩ MOSFET
- Protection: UVLO, OCP, OVP, OTP
- Four 1A LDO (V_{OUT}: 0.6V to 3.3V)
- Four auxiliary LDOs: 1.2V, 1.8V, 2.5V, 3.3V internal input voltage 4.75V, or external 5V up to 200mA output current
- Adjustable output voltage with 2.4 mV resolution
- 1% load regulation
- Buck efficiency up to 95%
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- Easy WebAmP upgrade path to On-Demand PMIC

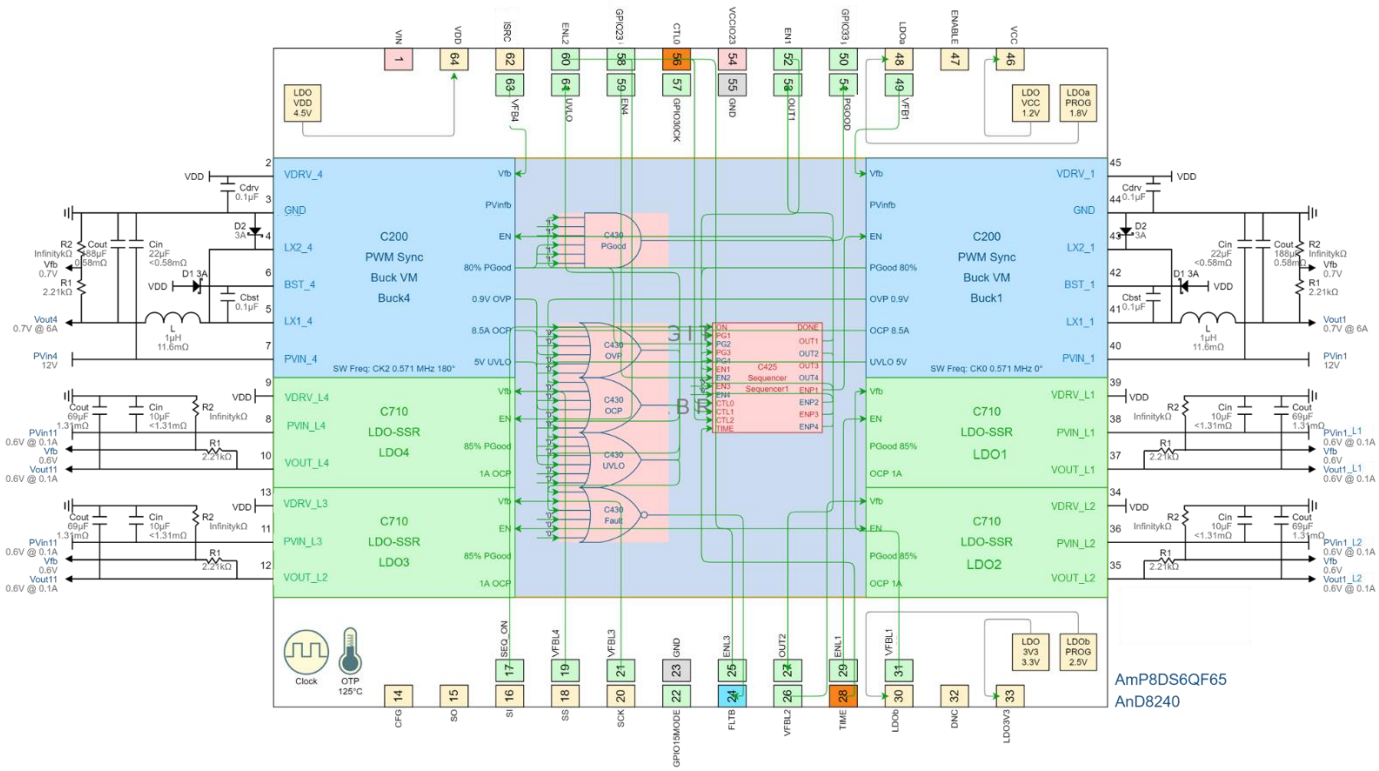
Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- Powering FPGA, processor, SSD, subsystem power control & sequencing

Product Detail

The AnD8240 Adaptable PMIC consists of two customizable, Synchronous Buck Regulators, customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition. It also includes four high current LDOs.

Dual Buck WebAmP Design View

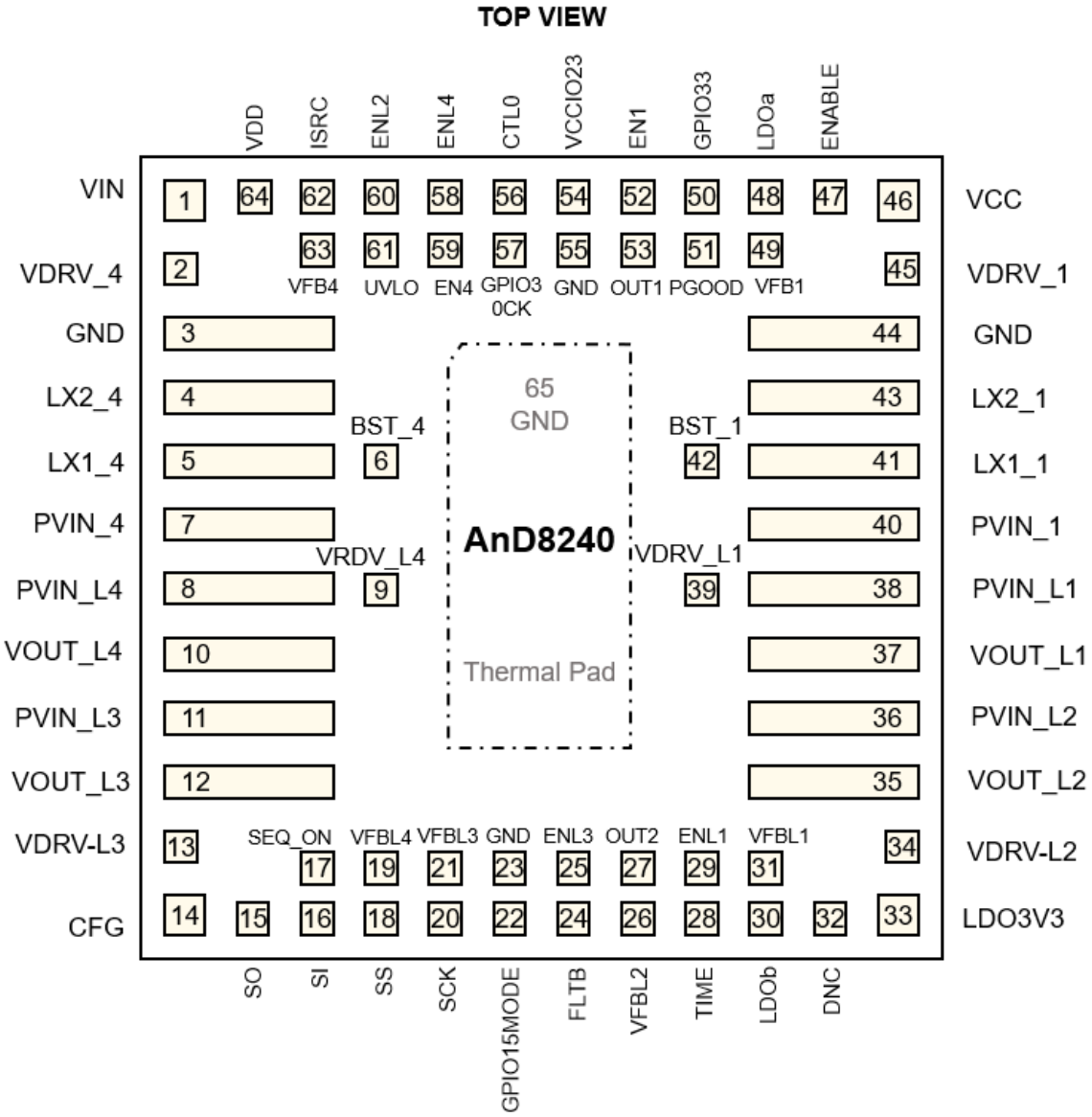


Order Information

Part Number	Package	Description	Availability
AnD8240QF65	QF65	Multi-Rail Dual Buck PMIC	Now

Package Marking Example – QF65

Package Pinout



Pin Function and Description

Table 1 Pins table

Pin Name	Pin #	Description
VIN	1	VIN bias supply for: VDD, VCC, LDO3V3, LDOa, LDOb
VDRV_4	2	Low side MOSFET gate drive supply for Buck 4
GND	3	Low side MOSFET source for Buck 4, must be connected to GND
LX2_4	4	Switch node (LX2) Low side MOSFET drain for Buck 4. Connect to LX1_4
LX1_4	5	Switch node (LX1) High side MOSFET source for Buck 4. Connect to LX2_4
BST_4	6	Bootstrap pin High side MOSFET gate drive for Buck 4
PVIN_4	7	Power Input for Buck 4
PVIN_L4	8	LDO 4 power input
VDRV_L4	9	LDO 4 bias driver
VOUT_L4	10	LDO 4 output
PVIN_L3	11	LDO 3 power input
VOUT_L3	12	LDO 3 output
VDRV_3	13	LDO 3 bias driver
CFG	14	CFG input active high configuration restart. Device is held in reset while signal is high. Reconfiguration is triggered on negative edge.
SO	15	SPI SO output transmits SPI commands during configuration
SI	16	SPI SI input receives SPI data during configuration
SEQ_ON	17	Enable Sequencer
SS	18	SPI SS output slave, select when master, input when slave during configuration
VFBL4	19	Feedback voltage for LDO4
SCK	20	SPI SCK output clock when master, input clock when slave during configuration
VFBL3	21	Feedback voltage for LDO3
GPIO15MODE	22	NC (No connect)
GND	23	Ground
FLTB	24	Fault output open drain active low. Dual function pin, shared with DONE output, signals end of configuration when high-Z
ENL3	25	Enable LDO3
VFBL2	26	Feedback voltage for LDO2
OUT2	27	Output 2 from Sequencer. Connect to relevant Buck EN pin to be the second in sequence.
TIME	28	Sequencer mode control, high = TIME mode, low = PGood mode
ENL1	29	Enable LDO1
LDOb	30	LDO 2.5V output
VFBL1	31	Feedback voltage for LDO1
DNC	32	Do not connect, floating

Pin Function and Description (continued)

Pin Name	Pin #	Description
LDO3V3	33	LDO output 3.3V
VDRV_L2	34	LDO 2 bias driver
VOUT_L2	35	LDO 2 output
PVIN_L2	36	LDO 2 power input
VOUT_L1	37	LDO 1 output
PVIN_L1	38	LDO 1 power input
VDRV_L1	39	LDO 1 bias driver
PVIN_1	40	Power Input for Buck 1
LX1_1	41	Switch node (LX1) High side MOSFET source for Buck 1. Connect to LX2_1
BST_1	42	Bootstrap pin High side MOSFET gate drive for Buck 1
LX2_1	43	Switch node (LX2) Low side MOSFET drain for Buck 1. Connect to LX1_1
GND	44	Low side MOSFET source for Buck 1, connect to GND
VDRV_1	45	Low side MOSFET gate drive supply for Buck 1
VCC	46	VCC, LDO 1.2V output and input for digital circuitry
ENABLE	47	Chip enable, AnD8240 powered on when floating (default), powered down when pulled low with 47kΩ pull-up to VDD through a diode (anode to VDD).
LDOa	48	LDO 1.8V adjustable output
VFB1	49	Feedback voltage for Buck 1
GPIO33	50	NC (No connect)
PGOOD	51	Global Power Good, includes both bucks
EN1	52	Enable Buck1
OUT1	53	Output 1 from Sequencer. Connect to relevant Buck EN pin to be the first in sequence.
VCCIO23	54	Supply input to GPIO bank, 3.3V
GND	55	Digital ground
CTL0	56	Sequencer Control 0
GPIO30CK	57	NC (No connect)
ENL4	58	Enable LD04
EN4	59	Enable Buck4
ENL2	60	Enable LDO2
UVLO	61	Global Under Voltage Lockout
ISRC	62	NC (No connect)
VFB4	63	Feedback for Buck 4
VDD	64	VDD LDO 4.5V output, input for analog circuitry
GND	65	Thermal pad, connect to GND

Absolute Maximum Ratings

over operating free-air temperature range

		Min	Max	Unit
Drain to Source Voltage		-1	22	V
V_{IN} Bias Supply		-1	22	V
Boost Voltage, referenced to Source		-1	6.6	V
Continuous Drain Current	Package power dissipation may limit current		8	A
Temperature range	Operating Junction temperature range, TJ	–40	125	°C
	Storage temperature range, Tstg	–65	150	

ESD Ratings

		Value	Unit
Electrostatic Discharge	Human body model	±2000	V
	Charged device model	±500	V

Thermal Information

Symbol	Thermal Metric	QF65	Unit
$\theta_{JA(effective)}$	Effective Junction-to-ambient thermal resistance (System Level)*	20	°C/W
Package Manufacturer ratings (JEDEC reference)			
θ_{JC}	Junction-to-case (top) thermal resistance	11	°C/W
θ_{JB}	Junction-to-board thermal resistance	9	°C/W

*$\theta_{JA\{effective\}}$ measured on AnDAPT AnD8240EB Evaluation Board and AmP8DB1REV5.0 Demonstration Board

Package Dissipation Ratings

Package	$\Theta_{JA(effective)}$	T_A = 55°C Power Rating (W) Still air flow	T_A = 55°C Power Rating (W) 200 LFM air flow	T_A = 55°C Power Rating (W) 400 LFM air flow
QF65	20	3.5	3.8	4.1

Recommended Operating Conditions

over operating free-air temperature range

	Min	Max	Unit
PVIN_1, PVIN_4	4.75	14	V
LX1_1, LX2_1,LX1_4, LX2_4	-0.8	14	V
BST_1 to LX1_1 & LX1_1 pins, BST_4 to LX1_4 & LX2_4 pins,	-0.1	5.5	V
VDRV_1, VDRV_4	3.0	5.5	V
CFG, SO, SI, SEQ_ON, SS, SCK, VFB1, VFB4, VFBL1, VFBL2, VFBL3, VFBL4, OUT1, OUT2, ENL1, ENL2, ENL3, ENL4, EN1, EN4, FLTB, TIME, PGOOD, UVLO	-0.3	3.66	V
VCCIO23	3.14	3.46	V
T_A	–40	85	°C
T_J	–40	125	°C

Digital GPIO Electrical Characteristics

V_{IN}=12V and T_A=25°C

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	2	-2

Synchronous Buck Features

- PWM, voltage mode, point-of-load (POL) regulator
- Maximum output current: 6A
- PV_{IN}: 4.75V to 14V, V_{OUT}: 0.7V to 5.0V
- 571kHz Switching Frequency
- Adjustable output voltage with 2.4 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 30mΩ
- 1% load regulation
- Efficiency up to 95%
- Internal single pole compensator minimizes external part count
- Protection: Input Undervoltage Lockout, (ViUVLO), Output Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature

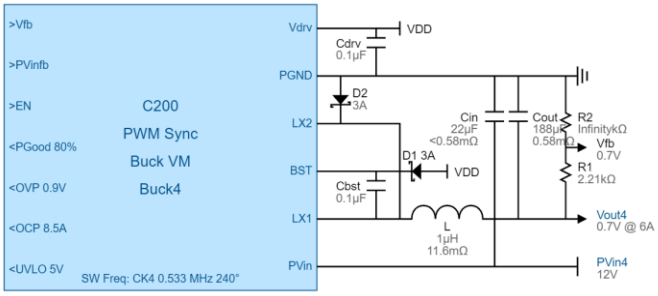


Figure 1: Buck Typical WebAmP Schematic

Synchronous Buck Detail

The AnD8240 Synchronous Buck Regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFETs (SIM) provide up to 6A output current.

Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is generated internally via an oscillator and it is fixed at 571kHz.

The customizable output voltage is specified by the WebAdapter tool or an external resistor divider. The regulator has customizable control and status pins including enable input, power-good output, and output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition.

The soft-start and soft-stop slew rates are also specified at 4ms. Additional sequencing options are available by using the WebAdapter tools or jumpers.

The AnD8240 uses predefined power components from the AmP power library. This allows an easy migration to On-Demand PMIC. The buck converter is based on the C200 power component.

Recommended Operating Conditions Buck Converters

Over operating free-air temperature range
This section applies to all two Power Regulators

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	4.75		14(1)	V
I_{Lmax}	Load Current Maximum	6			A
V_{IN}	Bias Supply	4.75		14(1)	V

Electrical Characteristics Buck Converters

PV_{IN} = V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
UVLO Input (ViUVLO)		3.9	4.1	4.2	V
Input Shutdown current (V_{IN})	EN = 0V		13		mA
Input quiescent current (OV_{IN})	Only 1 Buck enabled		7		mA
Output Voltage (V_{OUT})		0.7		5.5	V
Voltage Regulation			1		%
Switching frequency (F_{SW})			571		kHz
Switching frequency accuracy		-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$)			30		mΩ
Peak efficiency	V_{IN}=5V, V_{OUT}=3.3V, F_{SW}=571kHz I_{OUT}=3A		95		%
Efficiency	V_{IN}=12V, V_{OUT}=1.5V, F_{SW}=571kHz, I_{OUT}=3A		85		%
Power Good threshold (percentage of V_{OUT})			85		%
PROTECTION					
Current limit protection – OCP (I_{OUT})		8.5			A
Temperature limit protection (OTP) on the system	Shutdown (Power Good goes low) Hysteresis	125			°C
Overvoltage protection, OVP, trip point range (percentage of V_{OUT})			120		%
Undervoltage lockout, VoUVLO, threshold range (percentage of V_{OUT})			60		%
Soft start time (default)	V_{OUT} ramp time (EN High) - 2/3 of Seq_Delay		4		ms
Seq_Delay	Sequencer delay	3	6	16	ms

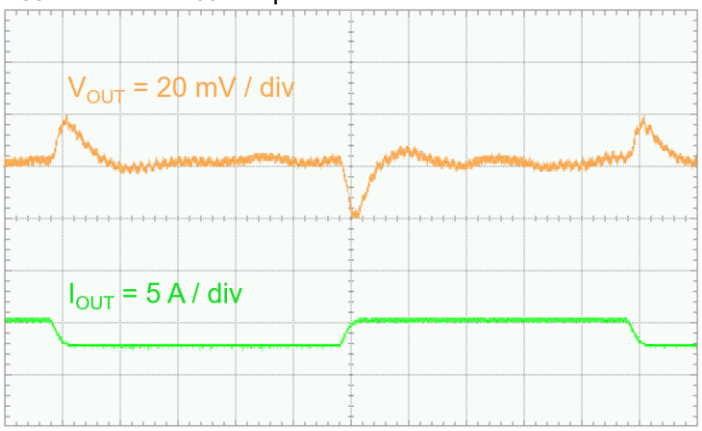
Notes (1) : Adaptable devices have an Integrated fixed compensation, optimized for the selected default inductor and for VIN range of 4.75V to 14V. For input voltage above 14V (14V to 17V), use On-Demand or contact AnDAPT “

Typical Characteristics Buck converters

Unless otherwise specified: TA = 25°C

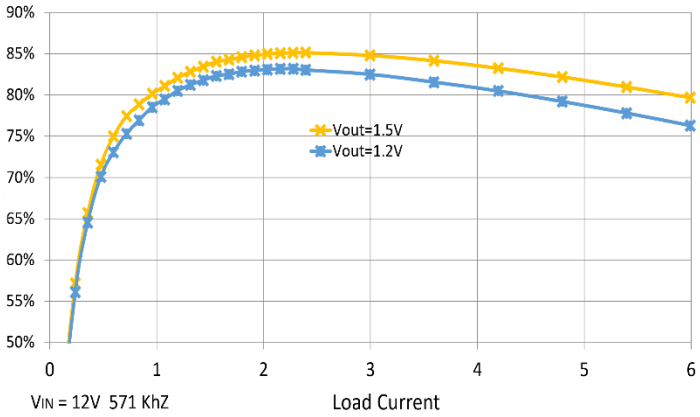
Transient Response

V_{OUT} = 1.8V I_{OUT} step 2.5 A to 5A



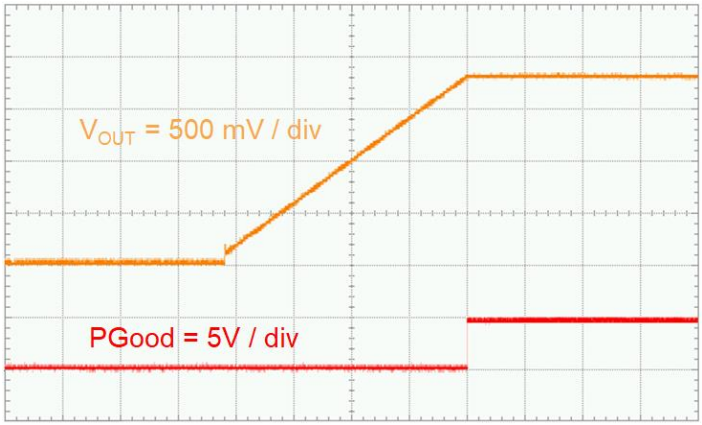
Time = 50µs / div

Efficiency



Soft Start

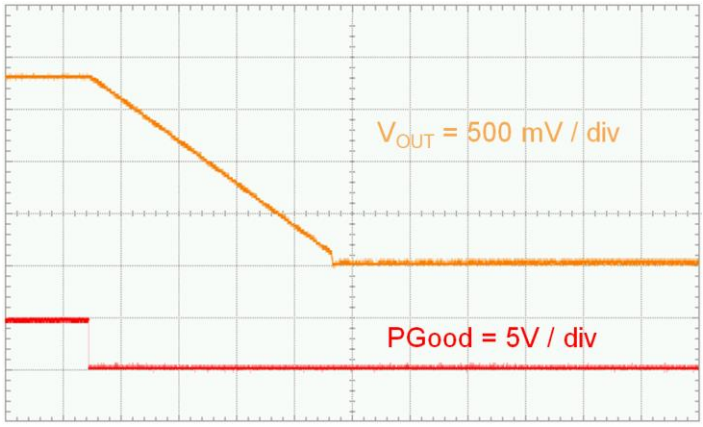
V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 2 ms / div

Soft Stop

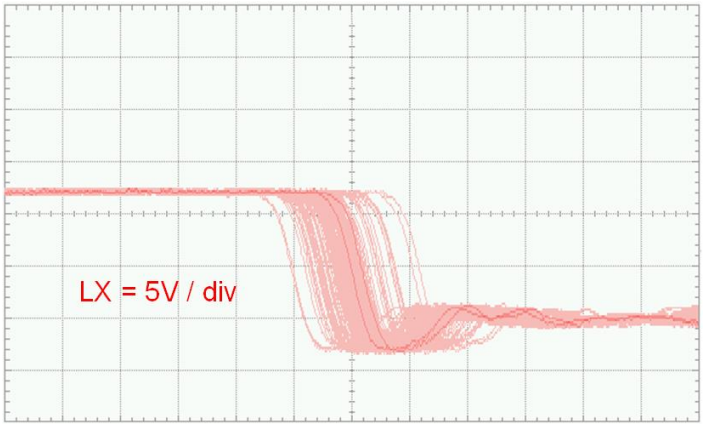
V_{IN} = 12V, V_{OUT} = 1.8V



Time = 2 ms / div

Jitter

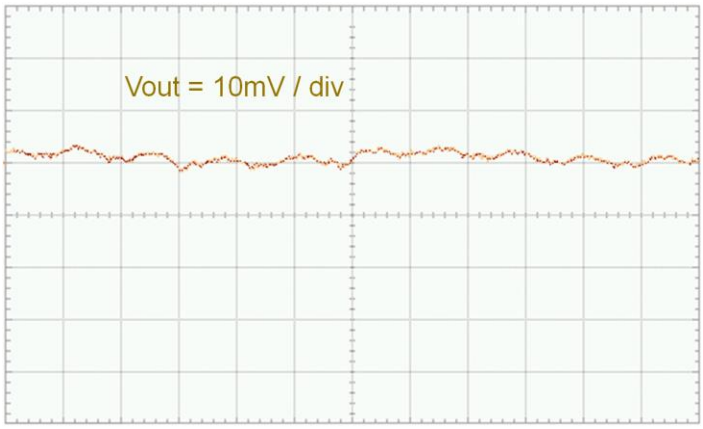
V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 5 ns / div

Ripple

V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 1 µs / div

Theory of Operation Buck Converters

The Synchronous Buck Regulator with integrated MOSFETs operates in voltage mode by comparing the V_{OUT} feedback voltage VFB, with a programmable reference Vref, to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the Hi-side and Lo-side MOSFET switches as shown in Figure 4.

In CCM (Continuous Conduction Mode), the PWM driver goes high turning the Hi-side switch “ON” to provide PVIN to the LX side of an inductor, L, where $V_L = PV_{IN} - V_{OUT}$. When the PWM driver goes low, the Hi-side switch turns “OFF”, and the Lo-side switch turns “ON” providing a path for the inductor current to decrease with $V_L = - V_{OUT}$, until the next PWM turns back “ON”. As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM duty cycle to optimize regulation and transient response over changing load conditions.

Inductor Selection

Based on output voltage target, the Figure 3 shows recommended inductor and compensation capacitor value providing optimal performance.

Ct capacitance is required for higher output voltage range, in parallel to R1 resistor, to improve stability of the compensation without changing the PID coefficients.

As an example, for an output voltage range from 1.2V to 2.5V, use a 1.5uH inductor and capacitance Ct of 2.2nF.

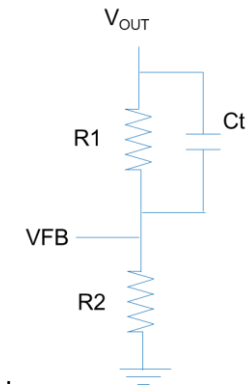


Figure 2

VIN = 12V	fsw = 530kHz-571kHz			
VOUT	L=0.68uH Ct=N/A	L=1uH Ct=N/A	L=1.5uH Ct=2.2nF	L=2.2uH Ct=4.7nF
0.7V				
1.0V				
1.2V				
1.5V				
1.8V				
2.5V				
3.3V				
5V				

L value is in the ideal range

L value just outside the ideal range, system works correctly

Figure 3 Inductor selection

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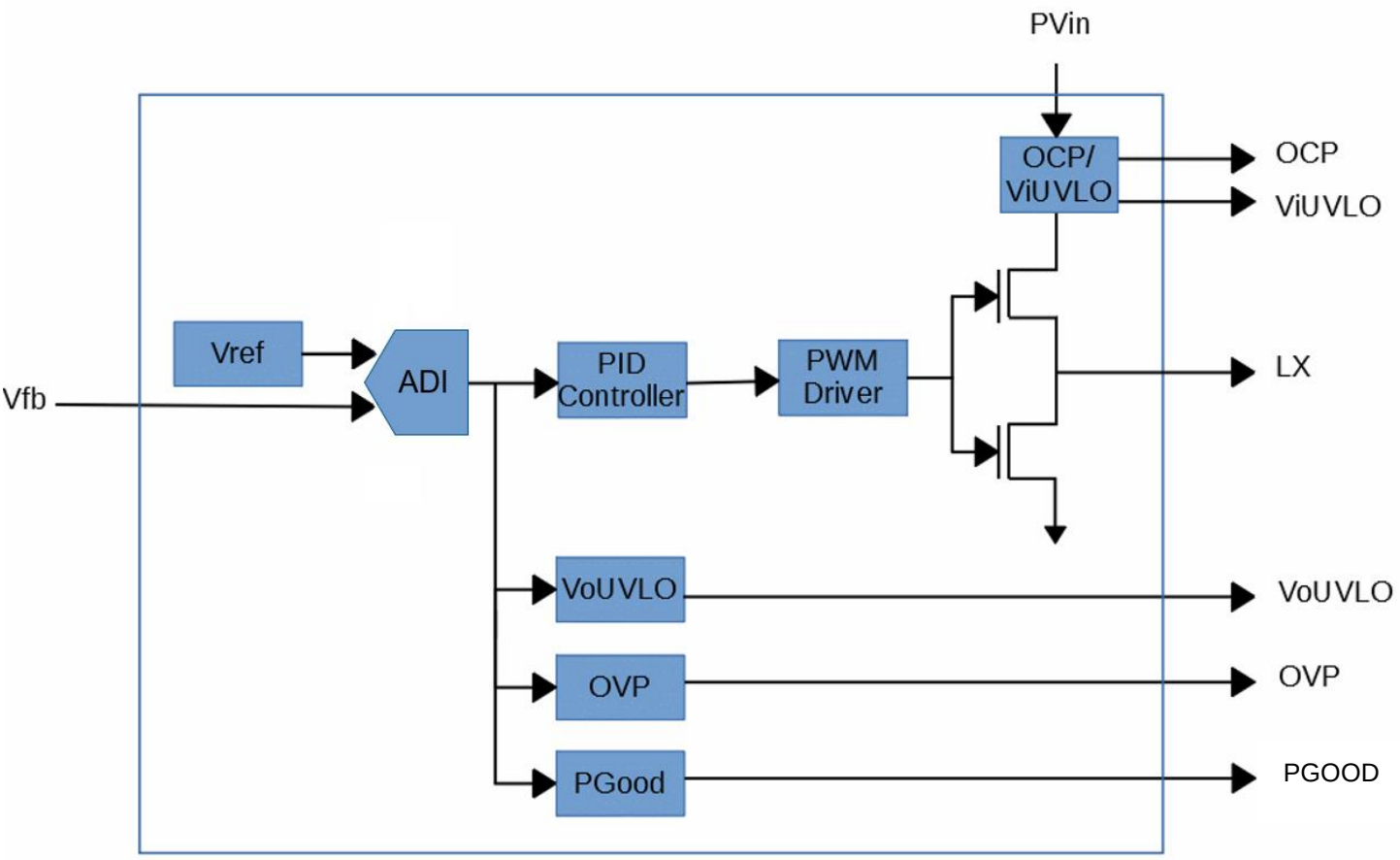


Figure 4: Buck converter Functional Block Diagram

Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port. When EN goes high the output voltage, V_{OUT}, will ramp up according to the Soft Start ramp time. When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start preset ramp time.

PGOOD

The power-good, PGOOD, of all Synchronous Buck Converters are combined to generate the global Power Good signal, indicating the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time (Figure 5) and when all Faults are cleared . PGOOD will go low when V_{OUT} goes below the preset condition (80% of the V_{OUT}) or when faults occur such as OCP current limit, OVP over voltage, UVLO or OTP thermal shutdown. PGOOD will also go low if EN goes low.

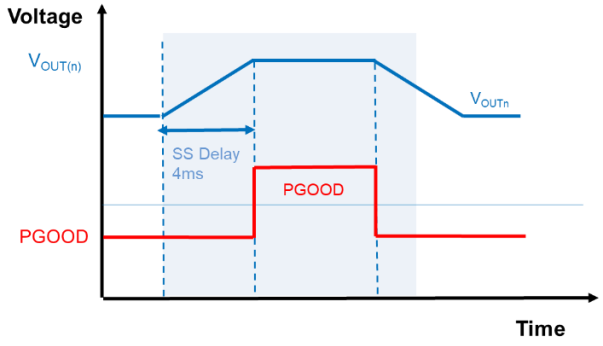


Figure 5.

Protection Features

As shown in Figure 4 each Synchronous Buck provides many protection features including UVLO, UVP, OVP, OCP and OTP.

Input Under Voltage (ViUVLO)

The input Under Voltage Lockout, ViUVLO, of all bucks, are combined to indicate the input voltage status of the entire device. The Global indication is UVLO. UVLO goes high when PV_{IN} voltage is lower than the preset condition (4.75V). UVLO goes low when PV_{IN} voltage is greater than the programmable preset condition in Parameter Settings, (default 4.75V). On detection of ViUVLO, the device will power down and PGOOD will go low. On ViUVLO returning high, the device will restart with a new Soft Start cycle.

Output Under Voltage VoUVLO

The output Under Voltage Protection, VoUVLO, of all regulators are combined to indicate the global output voltage status. VoUVLO goes high when any of the regulator outputs is lower than 60% of the specified V_{OUT}. VoUVLO goes low when all the output voltages are above 60% of the specified V_{OUT}. On detection of VoUVLO, the regulator will power down and PGOOD will go low. On VoUVLO returning low, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

Over Voltage Protection

The Over Voltage Protection, OVP, of all regulators are connected to a Fault Controller to indicate the output voltage status. FLTB is asserted low when any of the regulator outputs is 25% above specified V_{OUT}. FLTB is unasserted when all the outputs are less than 25% above the specified V_{OUT}. On detection of OVP, a regulator will skip Hi-side switch pulses until the fault condition is not present.

Over Current Protection

The Over Current Protection, OCP, of all regulators are combined to indicate the global output over current status. When the Output Current, $I_{OUT,}$ of any regulator is greater than 8.5A, the regulator will limit the Hi-side switch pulse width and OCP will go high. If I_{OUT} is greater than 10A, the regulator will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

V_{OUT} Resistor Settings

V_{OUT} voltages for Buck1 and Buck4 POLs are set by the resistors R1 and R2 (see Figure 2)

The AnD8240 internal feedback reference, VFB, is 0.7V for Buck1 and Buck4 with feedback resistor recommended values of

R1 = 2.21 kΩ
R2 = DNI (Do Not Install).

For V_{OUT} values greater the 0.7 V, use the following resistor divider equations:

R1 = 2.21 kΩ
R2 = VFB * R1 / (V_{OUT}-VFB) kΩ

Use 1% resistor values for best accuracy. A resistor calculator for closest E96 1% value is provided by the WebAdapter Software Tool.

These values determine the Actual V_{OUT} voltage calculated as shown. A DNI value indicates “Do Not Install”. R1 and R2 values may now be applied to the Reference Designators for the user’s board design.

Sequencer

The AnD8240 contains a sequencer that can operate either based on time delay or power good signal. The selection of power good or time delay is based on the setting of the TIME control pin 28. When the TIME control pin is high, the sequencer is based on time delay. When the TIME control pin is low, the sequencer is based on the PGood signal.
The user enters the desired sequencing delay. By default, the sequencing delay is 6ms.
The soft start will be set to 2/3 of the sequencing delay programmed allowing enough time for the previous sequencer to be fully ON before the next sequence start.
The sequencing delay is adjustable in WebAdapter advanced mode from 3ms to 16ms.
The sequencer is activated by setting the SEQ_EN to high.
TIME, CTL and OUT pins have an internal pull-up resistor, so they can be left floating (or not connected) to be in high state. Low signal can be set with a connection to ground (GND).

TIME Mode

TIME Mode is specified when the TIME pin is in a high state as defaulted in the AnD8240. In this mode, each Buck[n] regulator begins a Soft Start when Enable[n], goes high. On completion of Soft Start, Sequencer Delay remains before Enable[n+1] goes high, beginning the sequence for Buck[n+1]. In the example below, the sequencing delay is set to 6 ms .

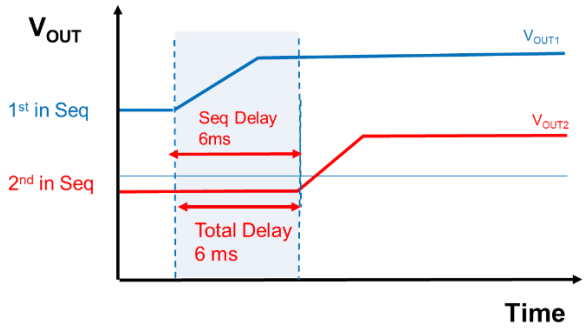


Figure 6 Soft start TIME mode

Sequencer Pin Connections

POL power-on and power-off sequences for Buck1 and Buck4 are set by the sequence Pin Connections specified in the wire connection table below. Apply these connections to the AnD8240 board design.

In time mode, the outputs (OUT1, OUT2) of the sequencer need to be connected to the appropriate Enable pins for each Buck.

Table 2

Sequence Output		Enable Input	
Signal Name	AnD8240 Pin Number	Signal Name	AnD8240 Pin Number
OUT1	53	EN1	52
OUT2	27	EN4	59

TIME/CTL Pin Connections

The control pins CTL0 must be held high as indicated in the wire connection in Table 3

Apply these conditions to the AnD8240 board design.

Table 3

Controls		Signal Level	Function
Signal Name	Pin Number		
TIME	28	High	TIME Mode
CTL0	56	High	Sequence Select

PGOOD Mode

The user has also the option to set the sequencing using Power good signal.

PGood Mode is selected when the TIME pin is in a low state as indicated by the “GND” Signal Level specified in the wire connection table below. Control pin CTL0 specifies the selected sequence.

Table 4

Controls		Signal Level	Function
Signal Name	Pin Number		
TIME	28	Low	PGood Mode
CTL0	56	High	Sequence Select

In this mode, each Buck[n] regulator begins a 4ms Soft Start when Enable[n], goes high. On completion of Soft Start, PGood[n] goes high and starts the programmed Sequencer Delay followed by Enable[n+1] going high, beginning the sequence for Buck[n+1]. If the user sets the sequencer delay to 6ms, The total cycle delay is 4ms + 6ms = 10ms per Buck as shown in the timing diagram below.

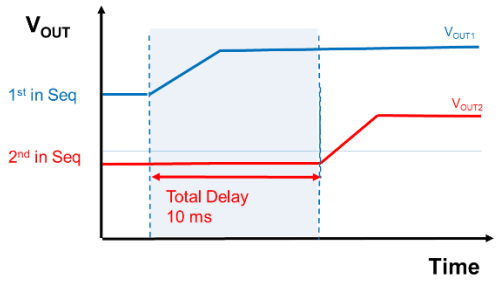


Figure 7 Power Good mode

PGOOD and Sequencer Pin Connections

The Control pin, CTL0, specifies the selected sequence.

Table 5 Power Good Sequence

CTL0	Seq1	Seq2
High	Buck 1	Buck 4
Low	Buck4	Buck 1

Integrated Auxiliary LDO

The AnD8240 has 4 integrated auxiliary LDOs which have default output voltages of 3.3V, 2.5V, 1.8V, and 1.2V. The input voltage of the four LDO's is from the internal 4.5V bias voltage. A decoupling capacitance of 10 µF minimum must be connected to the output of the LDO.

The pin locations of these integrated LDOs, are fixed and cannot be modified by WebAmP Tools.

Please see Table 6**Error! Reference source not found.** below for electrical characteristics of the LDOs.

Two of these LDos (LDOa and LDOb) can have an adjustable output voltage V_{OUT} when used with WebAdapter tool.

Electrical Characteristics Integrated LDO

Table 6

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LDO1V2	LDO 1.2V output voltage	I_{CC}=0mA, V_{IN}=4.5V	1.164	1.2	1.236	V
R_{OCC}	LDO 1.2V equivalent resistance			350		mΩ
I_{CC}	LDO 1.2V output current				200	mA
LDOa	LDO 1.8V output voltage	I1V8=0mA, V_{IN}=4.5V	1.746	1.8	1.854	V
R_{O1V8}	LDO 1.8V equivalent resistance			350		mΩ
I1V8	LDO 1.8V output current				200	mA
LDOb	LDO 2.5V output voltage	I2V5=0mA, V_{IN}=4.5V	2.425	2.5	2.575	V
R_{O2V5}	LDO 2.5V equivalent resistance			350		mΩ
I_{CC}	LDO 2.5V output current				200	mA
LDO3V3	LDO 3.3V output voltage	I3V3=0mA, V_{IN}=4.5V	3.201	3.3	3.399	V
R_{O3V3}	LDO 3.3V equivalent resistance			350		mΩ
I3V3	LDO 3.3V output current				200	mA

Product Detail – High current LDO

The AnD8240 has 4 high current LDOs which are parts of the AmP platform power components (C71x: C710 or C715)

The LDO is a 1A general purpose low-dropout (LDO) regulator. The integrated current sense provides over-current protection (OCP) and short circuit protection.

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAdapter development software or using resistor divider as described in Table 2

The LDO also incorporates a soft start feature to protect against inrush current. Sequencing options are available by interconnecting signals EN to provide dependencies and delays between each sequence step.

System Characteristics

Table 7 lists the system characteristics for the High current LDOs Power Component when implemented in an AnDAPT AmP device.

Table 7 LDOs System Characteristics

Parameters	Min	Typ	Max	Units
Input Drain Voltage (PV_{IN}) *	V_{OUT}+ V_{DO}		17	V
Output Voltage (V_{OUT})	0.6		3.3	V
Output Current (I_{OUT})			1	A
Dropout Voltage (V_{LDO}) @ V_{OUT} =1.8V I_{DS}=0.1A I_{DS}=1A		 20 100		 mV mV
Dropout Voltage (V_{LDO}) @ V_{OUT} =3.3V I_{DS}=0.1A I_{DS}=1A		 20 200		 mV mV
Voltage regulation		0.5		%
Current Limit – OCP	1			A
C_{OUT}	69			µF

*Note: The maximum power dissipation for the LDO, $(V_{IN}-V_{OUT})*I_{OUT}$, is limited to 1.5W

Theory of Operation LDO

The High current LDO is a linear voltage regulator. It consists of a reference voltage, a feedback path for the output voltage (which may use a resistor divider) to compare it to the reference, a feedback amplifier, and a series pass transistor (NMOS in the case of the C710/C715), whose voltage drop is controlled by the amplifier to maintain the output at the required value. A block diagram is shown in Figure 8

When setting the voltage above 1.8V, a resistor (Rpu) and a Zener diode (DZ) need to be added for additional protection.

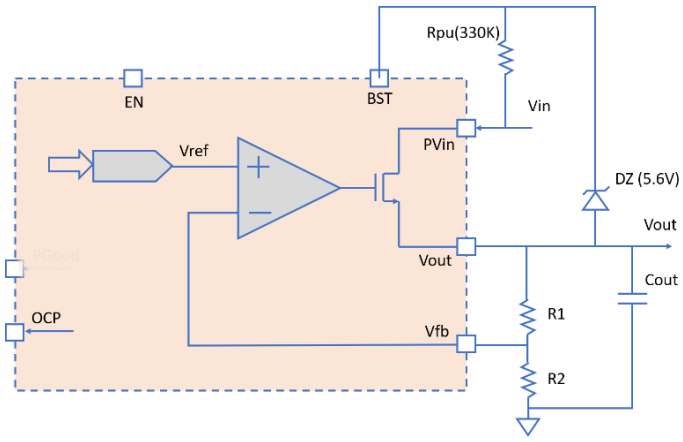


Figure 8: LDO bloc diagram

If the load current increases causing the output to drop the error voltage will increase and the amplifier output will fall. This in turn causes the voltage across the pass transistor to decrease and the output will return to its original value.

Note that a linear regulator efficiency depends on the voltage difference between input and output and is nominally given by:

$100 \times (V_{OUT} \times I_{OUT})/(V_{IN} \times I_{IN})$

$= 100 \times V_{OUT} / V_{IN}$ assuming $I_{OUT} = I_{IN}$

with the power loss being $(V_{IN} - V_{OUT}) \times I_{OUT}$.

The maximum power dissipation for the LDO is limited to 1.5W.

Protection Features

The LDO provides protection features including OCP which is fixed at 1A. It can be enabled or disabled using the WebAdapter interface.

Over Current Protection (OCP)

On detection of OCP, the LDO will shut down. If OCP is triggered, the C71x will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the LDO with a new Soft Start cycle.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the LDO will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the LDO with a new Soft Start cycle.

Additional Resources

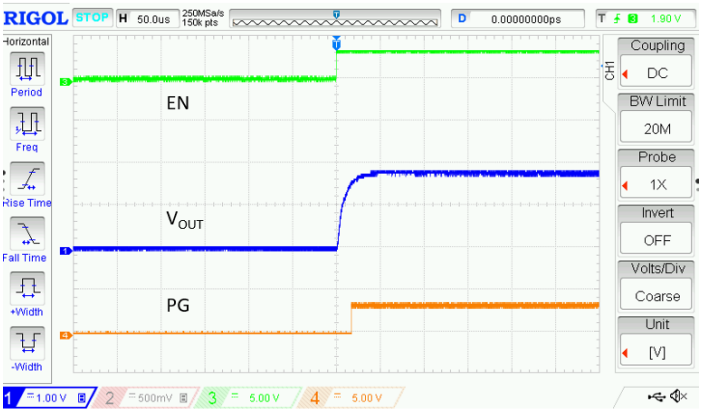
- AnDAPT AmP Platform datasheet

Typical Characteristics High Current LDO

Unless otherwise specified: TA = 25°C, C_{OUT} = 69 µF

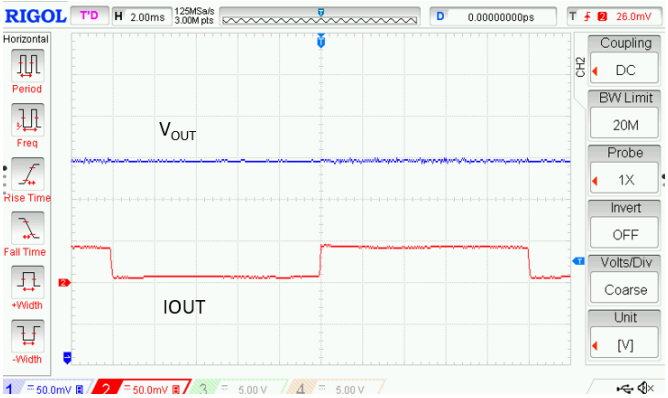
Soft Start

V_{IN} = 12V, V_{OUT} = 1.8V No load



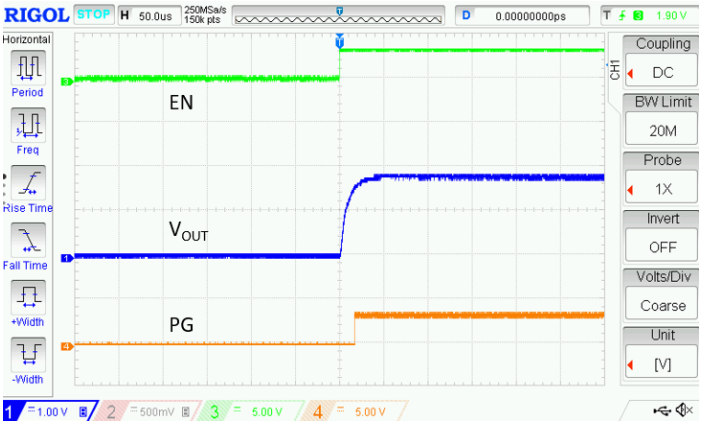
Transient Response

V_{IN} = 1.8V, V_{OUT} = 1.5V I_{OUT} = 0 to 100 mA Load step



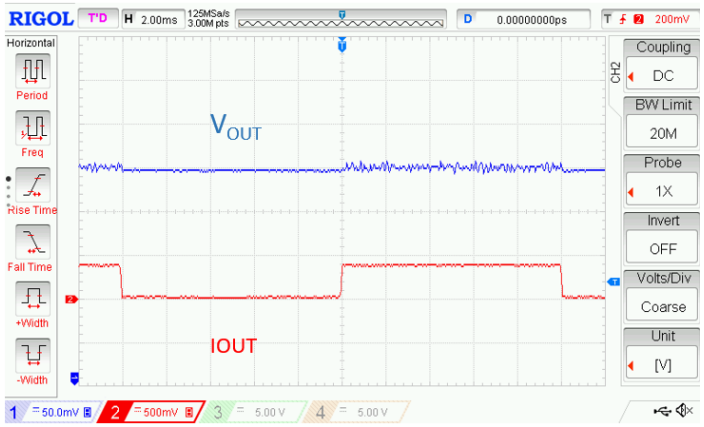
Soft Start

V_{IN} = 2V, V_{OUT} = 1.8V, 2 Ohm



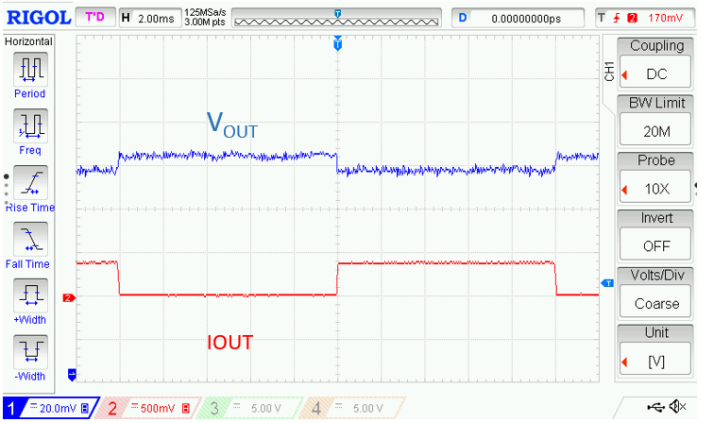
Transient Response

V_{IN} = 1.8V, V_{OUT} = 1.5V I_{OUT} = 0 to 0.5A Load step



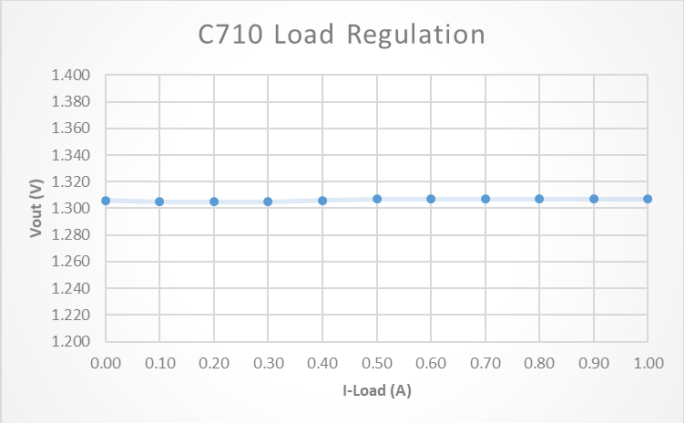
Transient Response C715

V_{IN} = 12V, V_{OUT} = 3.3V I_{OUT} = 0 to 1A Load step



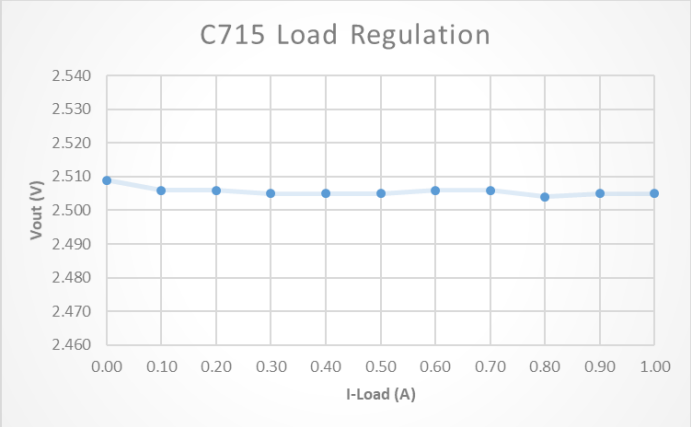
Load Regulation

PV_{IN} = 1.5V, V_{OUT} = 1.3V



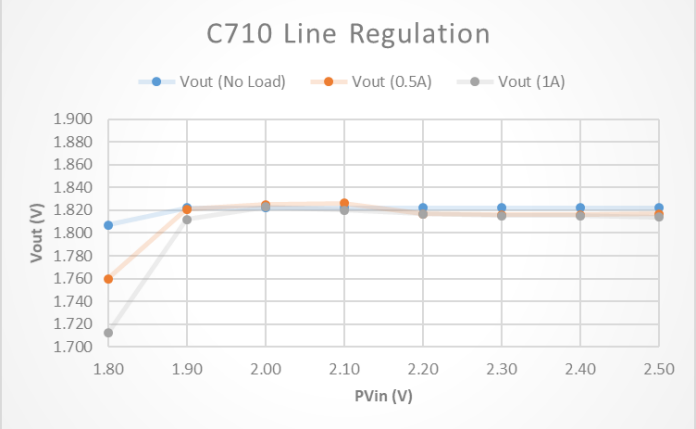
Load Regulation

PV_{IN} = 2.8V, V_{OUT} = 2.5V



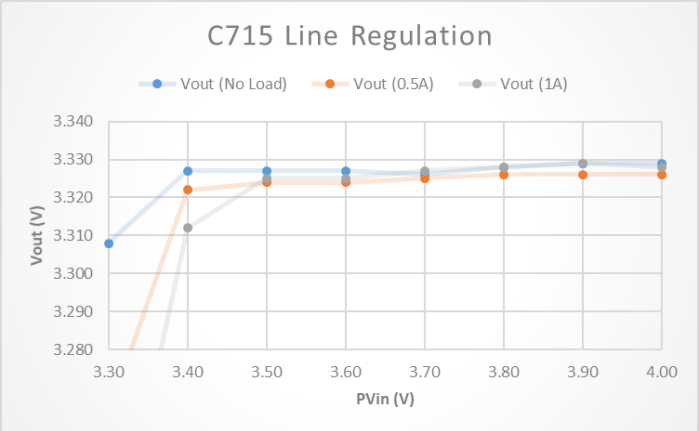
Line Regulation

V_{OUT} = 1.8V



Line Regulation

V_{OUT} = 3.3V



ESD CONSIDERATIONS

Establish and use (Electrostatic Damage) ESD-safe handling precautions when unpacking and handling ESD-sensitive devices. Store ESD sensitive devices in ESD safe containers until ready for use. The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly. AnDAPT products are qualified to meet at least 500V ESD-MM (Machine Model) 2000V ESD-HM (Human Body Model). Restrict all device handling to ESD protected work areas that measure less than 400V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

Assembly Recommendation

For part placement, please use standard pick and place machine with ± 0.05 mm accuracy. Mount the device with slower speed and higher force. Place the package 1 ~ 2 mils into the paste. The device package has excellent self-alignment during solder reflow if a minimum of 75% of the lead diameter intersect with the pad.

Solder Paste

The screen-printing quantity of solder paste is a key factor in producing high yield assemblies. Recommended solder paste alloy is Sn/Ag/Cu family for lead-free application. Low residue and no clean flux are recommended. Particle size type IV (25 ~ 38 μm) is preferred to improve printing performance. Particle size type III (25 ~ 45 μm) also is acceptable.

Solder Stencils

The contrast between large thermal pads and small terminal pads of the QFN package can present a challenge in production and even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow- solder processing. The solder joint thickness for QFN package terminal pads should be 50 – 75 μm. Stencil recommended type is laser cutting stainless steel with thickness of 100 ~ 150 μm (125 μm as a guide). The actual thickness of a stencil is depending on other SMD components on the PCB. Metal blade or polymer with 90-degree hardness squeegee is recommended. Aperture size for terminal pad should have aspect ratio (width / thickness) of greater than 1.5 and area ratio (Area of aperture opening / aperture wall area) of greater than 0.66. The stencil aperture is typically designed to match the pad size on the PCB 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. An oval-shaped opening should be used to get the optimum paste release and rounded corners to minimize clogging. Positive taper walls (5-degree tapering) with bottom opening larger than the top is recommended. Small multiple openings should be used instead of one big opening. 60% ~ 85% solder paste coverage is recommended to reduce the chance of having short connection.

Reflow Specification

AnDAPT products are qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling to avoid subsequent thermal and mechanical damage during the solder-reflow attachment phase of PCB assembly. Check solder paste data sheet for any additional or difference instruction. Using a forced convection reflow oven with nitrogen is recommended. Also, the reflow oven should have equal or less than ± 5°C temperature uniformity. The recommended reflow profile for lead-free solder paste shown in Figure 9.

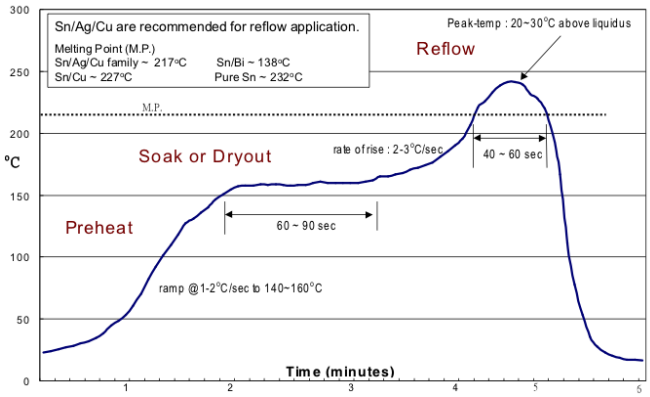


Figure 9 Solder paste

Compliance

Environmental Compliance

AnDAPT products are RoHS and Green compliant. AnDAPT products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC Compliance

AnDAPT products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

Compliance Declaration Disclaimer

AnDAPT believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. AnDAPT subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by AnDAPT.

Internal AnD8240 PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AND8240 PMIC. Listed below is a description of blocks and resources that are used to create Buck regulators.

Noise-immune references - Nrefs

- 10-bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, In Amp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 poles

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

$$P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c$$

1 pole: a1 = 1, a2 = 0 2 poles: a1 = 0.5, a2 = 0.5

$$E[n] = Vref - V_{OUT}[n]$$

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

Scalable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, drain voltage or current and Analog Fabric including programmable references (Nrefs).

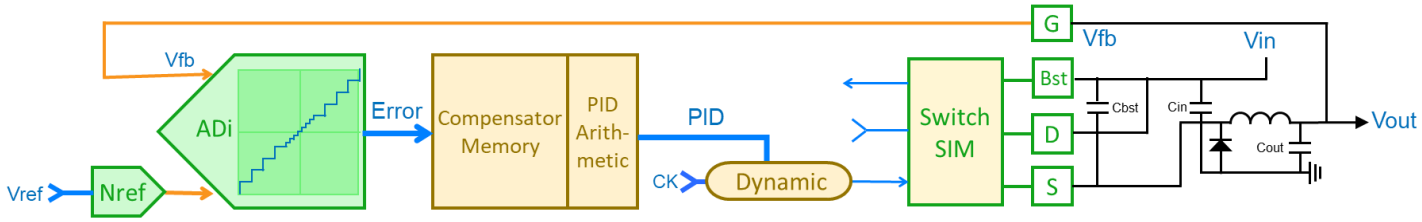
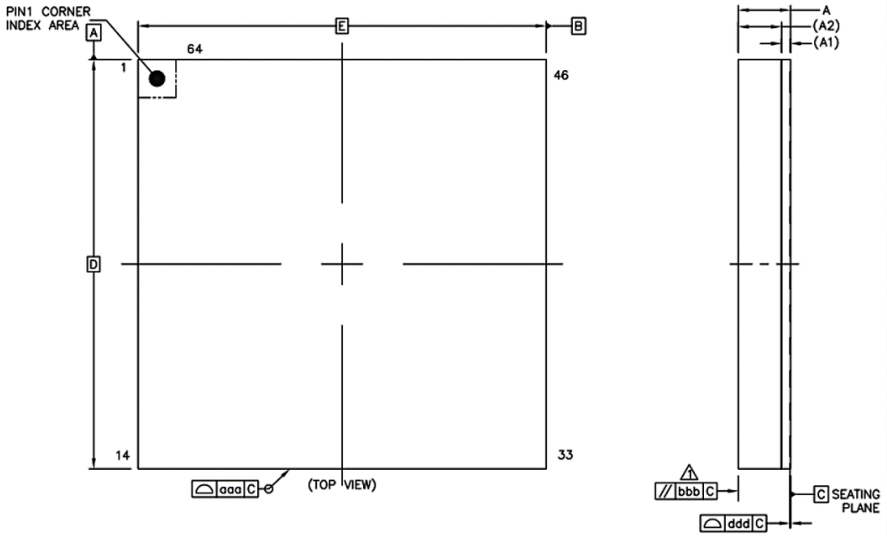
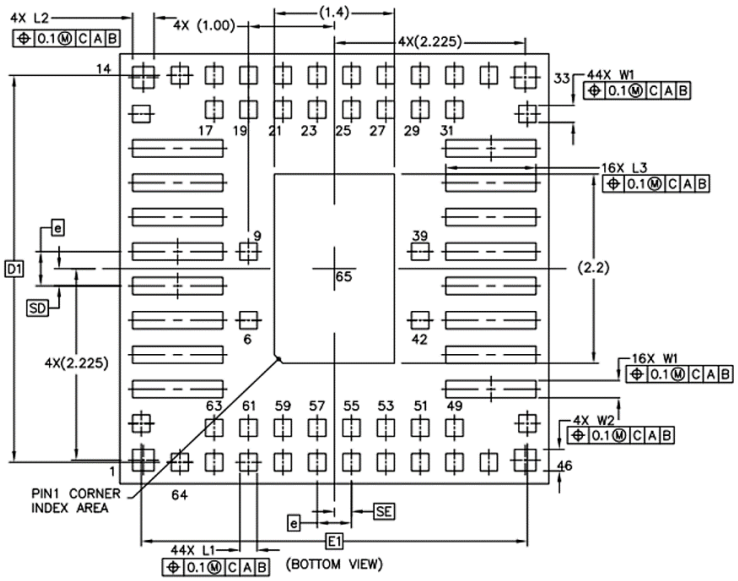


Figure 10: PMIC Blocks and Resources Example - Buck Regulator

Package Description – QF65 5x5 mm



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.7
SUBSTRATE THICKNESS	A1		0.11	REF
MOLD THICKNESS	A2		0.53	REF
BODY SIZE	D	4.9	5	5.1
	E	4.9	5	5.1
LEAD WIDTH	W1	0.15	0.2	0.25
LEAD WIDTH	W2	0.2	0.25	0.3
LEAD LENGTH	L1	0.15	0.2	0.25
LEAD LENGTH	L2	0.2	0.25	0.3
LEAD LENGTH	L3	1	1.05	1.1
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		65	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	



Errata

Date	description
12/28/2018	SIM Pin (MOSFET DRV-Drain) ESD 750V HBM

Revision History

Date	Revision
02/25/2019	Initial release

AnDAPT

On-Demand Power Management

www.AnDAPT.com

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