Quad Synchronous Buck PMIC

Adaptable PMIC AnD8400

Product Description

The AnD8400 Adaptable PMIC uses AnDAPT AmP™ advanced technology consisting of fully flexible digital fabric combined with high performance analog blocks. The AnD8400 consists of four configurable 6A Synchronous Buck Regulators. The AnD8400 is fully tested and ready to use in designs. The AnD8400 Buck regulators use Voltage Mode control. The AnD8400 also has an integrated sequencer and 4 additional integrated auxiliary LDOs. The user can modify output voltage and rail sequencing using resistors or WebAdapter™ online tools. The sequencer has the capability to be based on timed delays or Power Good signals. Adaptable PMICs provide fastest prototyping and time to market, while providing best in class performance and flexibility. The AnD8400 design is available in the WebAmP™ software tool library for full customization capability. The Adaptable PMIC is optimized to power high end Processors by integrating multiple power rails into single chip designs.

Features

- Four 6A Synchronous Buck Regulators
- PVIN: 6 V to 14V, V_{OUT}: 0.7V to 5.0V
- 571 kHz Switching Frequency
- Integrated 30mΩ MOSFET
- Protection: UVLO, OCP, OVP, OTP
- Four auxiliary LDOs: 1.2V, 1.8V, 2.5V, 3.3V internal input voltage 4.5V, or external 5V up to 200mA output current
- Adjustable output voltage with 2.4 mV resolution
- 1% load regulation
- Efficiency up to 93%
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- Easy WebAdapter™ upgrade path to On-Demand PMIC

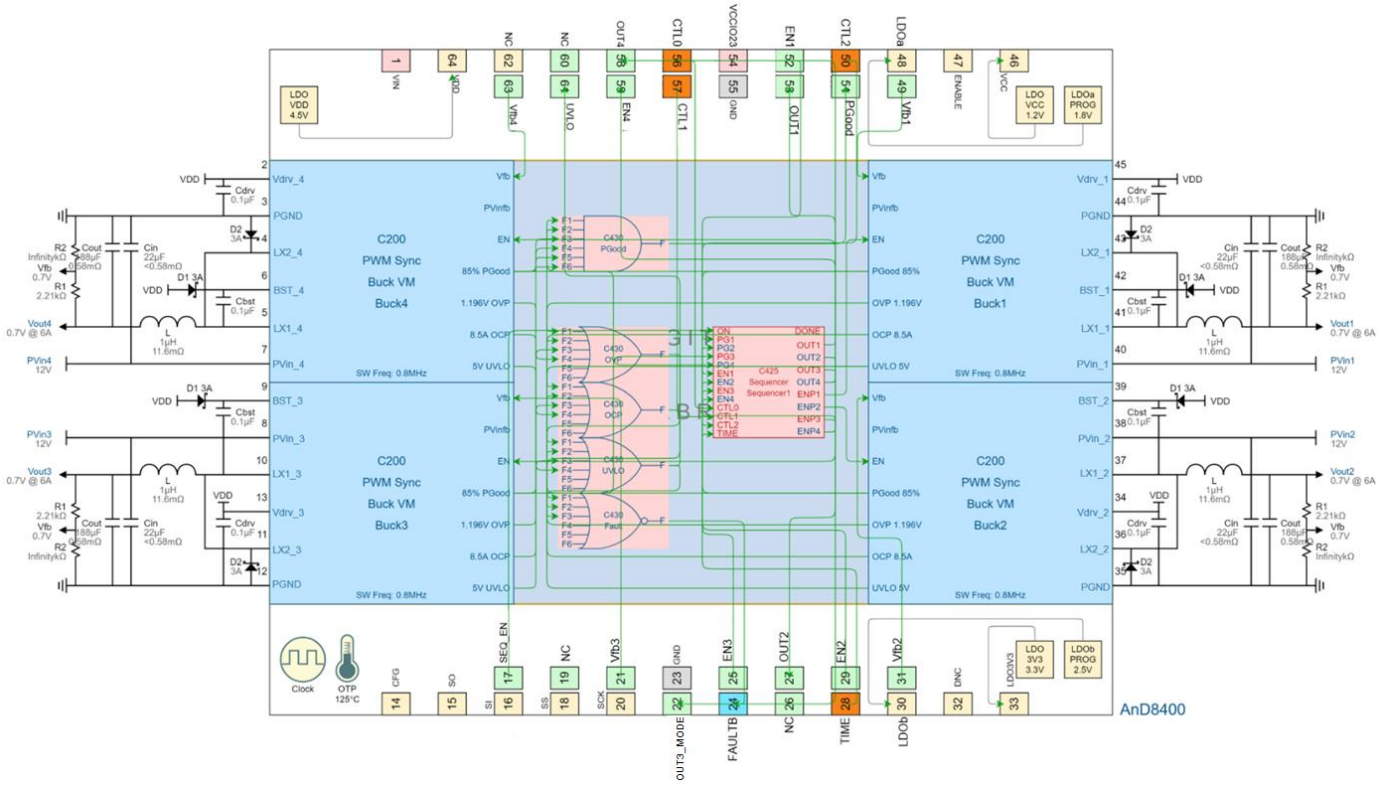
Applications

- On-demand power management, multi-rail power integration
- Server, processor, memory, storage, network switcher and router platforms
- Powering FPGA, processor, SSD, subsystem power control & sequencing

Product Detail

The AnD8400 Adaptable PMIC consists of four customizable, Synchronous Buck Regulators, customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition.

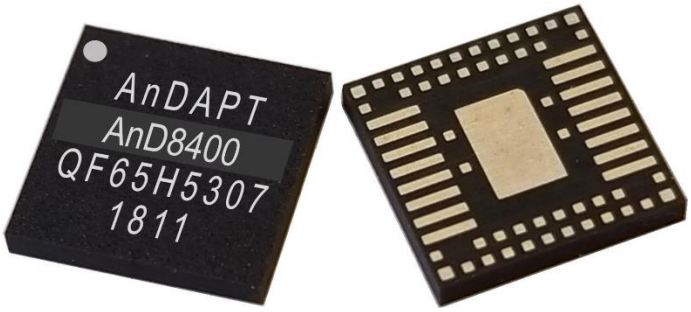
Quad Buck Design View



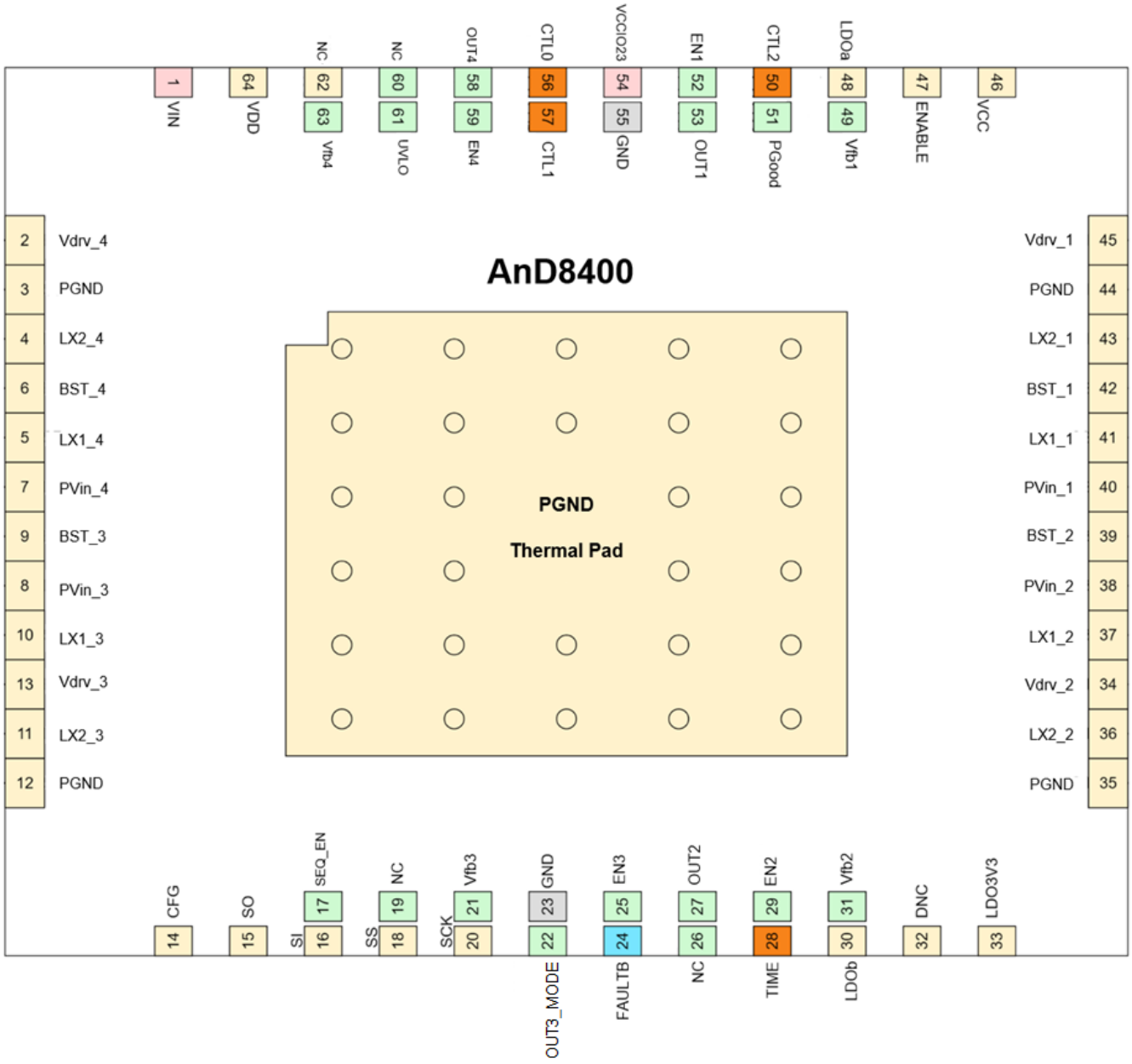
Order Information

Part Number	Package	Description	Availability
AnD8400QF65	QF65	Multi-Rail Quad Buck PMIC	Now

Package Marking Example – QF65



Package Pinout



Pin Function and Description

Pin Name	Pin #	Description
VIN	1	VIN bias supply for: VDD, VCC, LDO3V3, LDOa, LDOb
VDRV_4	2	Low side MOSFET gate drive supply for Buck 4
PGND	3	Low side MOSFET source for Buck 4, must be connected to GND
LX2_4	4	Switch node (LX2) Low side MOSFET drain for Buck 4,
LX1_4	5	Switch node (LX1) High side MOSFET source for Buck 4
BST_4	6	Bootstrap pin High side MOSFET gate drive for Buck 4
PVIN_4	7	Power Input for Buck 4
PVIN_3	8	Power Input for Buck 3
BST_3	9	Bootstrap pin High side MOSFET gate drive for Buck 3
LX1_3	10	Switch node (LX1) High side MOSFET source for Buck 3
LX2_3	11	Switch node (LX2) Low side MOSFET drain for Buck 3
PGND	12	Low side MOSFET source for Buck 3, must be connected to GND
VDRV_3	13	Low side MOSFET gate drive supply Buck 3
CFG	14	CFG input active high configuration restart. AmP is held in reset while signal is high. Reconfiguration is triggered on negative edge.
SO	15	SPI SO output transmits SPI commands during configuration
SI	16	SPI SI input receives SPI data during configuration
SEQ_EN	17	Sequence On control
SS	18	SPI SS output slave select when master, input when slave during configuration
NC	19	No Connect
SCK	20	SPI SCK output clock when master, input clock when slave during configuration
VFB3	21	Feedback for buck 3
OUT3_MODE	22	Dual function: Before config, pin in Mode function; after config, pin in Sequencer function. Mode function: Host ROM mode: Always connect high through 47kΩ resistor. Sequencer function: Output from Sequence 3. Connect to relevant Buck EN pin to be the third in sequence. Do not leave floating.
GND	23	Digital ground
FAULTB	24	Fault output open drain active low Dual function pin, shared with DONE output, signals end of configuration when high-Z
EN3	25	Enable Buck3
NC	26	No Connect
OUT2	27	Output from Sequencer 2. Connect to relevant Buck EN pin to be the second in sequence.
TIME	28	Sequencer mode control, high = TIME mode, low = PGood mode
EN2	29	Enable Buck2
LDOb	30	LDO 2.5V output, adjustable
VFB2	31	Feedback for buck 2
DNC	32	Do not connect, floating

Pin Function and Description (continued)

Pin Name	Pin #	Description
LDO3V3	33	LDO output 3.3V
VDRV_2	34	Low side MOSFET gate drive supply for Buck 2
PGND	35	Low side MOSFET source for Buck 2
LX2_2	36	Switch node (LX2) Low side MOSFET drain for Buck 2
LX1_2	37	Switch node (LX1) High side MOSFET source for Buck 2
PVIN_2	38	Power Input High side MOSFET drain for Buck 2
BST_2	39	Bootstrap pin High side MOSFET gate drive for Buck 2
PVIN1	40	Power Input High side MOSFET drain for Buck 1
LX1_1	41	Switch node (LX1) High side MOSFET source for Buck 1
BST_1	42	Bootstrap pin High side MOSFET gate drive for Buck 1
LX2_1	43	Switch node (LX2) Low side MOSFET drain for Buck 1
PGND	44	Low side MOSFET source for Buck 1
VDRV_1	45	Low side MOSFET gate drive supply for Buck 1
VCC1V2	46	VCC, LDO 1.2V output and input for digital circuitry
ENABLE	47	Chip enable, AnD8400 powered on when floating (default), powered down when pulled low with 47kΩ pull-up to VDD through a diode (anode to VDD)
LDOa	48	LDO 1.8V output, adjustable
VFB1	49	Feedback for buck 1
CTL2	50	Sequence Control 2
PGOOD	51	Global Power Good, includes all four Bucks
EN1	52	Enable Buck1
OUT1	53	Output 1 from Sequencer. Connect to relevant Buck EN pin to be the first in sequence
VCCIO23	54	Supply input to GPIO bank, 3.3V
GND	55	Digital ground
CTL0	56	Sequencer Control 0
CTL1	57	Sequencer Control 1
OUT4	58	Output 4 from Sequencer. Connect to relevant Buck EN pin to be the fourth in sequence
EN4	59	Enable Buck4
NC	60	No connect
UVLO	61	Global Under Voltage Lockout
NC	62	No Connect
VFB4	63	Feedback for buck 4
VDD4V5	64	VDD LDO 4.5V output
GND	65	Thermal pad, connect to GND

Absolute Maximum Ratings

over operating free-air temperature range

		Min	Max	Unit
Drain to Source Voltage		-1	22	V
V_{IN} Bias Supply		-1	22	V
Boost Voltage, referenced to Source		-1	6.6	V
Continuous Drain Current	Package power dissipation may limit current		6	A
Temperature range	Operating Junction temperature range, TJ	–40	125	°C
	Storage temperature range, Tstg	–65	150	

ESD Ratings

		Value	Unit
Electrostatic Discharge	Human body model	±2000	V
	Charged device model	±500	V

Thermal Information

Symbol	Thermal Metric	QF65	Unit
$\theta_{JA(effective)}$	Effective Junction-to-ambient thermal resistance (System Level)*	20	°C/W
Package Manufacturer ratings (JEDEC reference)			
θ_{JC}	Junction-to-case (top) thermal resistance	11	°C/W
θ_{JB}	Junction-to-board thermal resistance	9	°C/W

*$\theta_{JA\{effective\}}$ measured on AnDAPT AnD8400EB Evaluation Board and AmP8DB1REV5.0 Demonstration Board

Package Dissipation Ratings

Package	$\Theta_{JA(effective)}$	T_A = 55°C Power Rating (W) Still air flow	T_A = 55°C Power Rating (W) 200 LFM air flow	T_A = 55°C Power Rating (W) 400 LFM air flow
QF65	20	3.5	3.8	4.1

Recommended Operating Conditions

over operating free-air temperature range

	Min	Max	Unit
PVin_1, PVin_2, PVin_3, PVin_4	6	14	V
LX1_1, LX2_1, LX1_2, LX2_2, LX1_3, LX2_3, LX1_4, LX2_4	-0.8	14	V
BST_1, referenced to LX1_1 & LX1_1 pins, BST_2, referenced to LX2_2 & LX2_2 pins, BST_3, referenced to LX1_3 & LX2_3 pins, BST_4, referenced to LX1_4 & LX2_4 pins	-0.1	5.5	V
Vdrv_1, Vdrv_2, Vdrv_3, Vdrv_4	3.0	5.5	V
CFG, SO,SI, SEQ_EN, SS, SCK, Vfb1, Vfb2, Vfb3, Vfb4, OUT1, OUT2, OUT3, OUT4, EN1, EN2, EN3, EN4, FAULTB, TIME, PGood, UVLO	-0.3	3.66	V
VCCIO23	3.14	3.46	V
T_A	–40	85	°C
T_J	–40	125	°C

Digital GPIO Electrical Characteristics

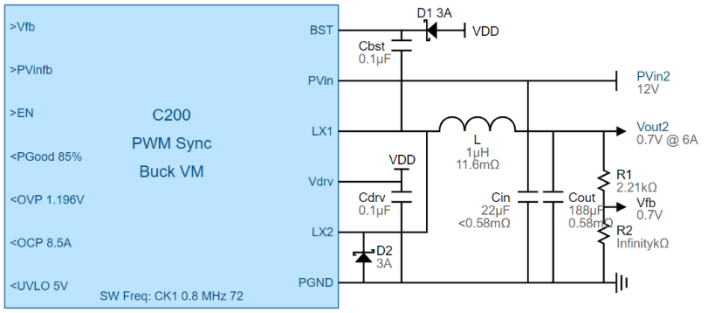
V_{IN}=12V and T_A=25°C

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	2	-2

Synchronous Buck Features

- PWM, voltage mode, point-of-load (POL) regulator
- Maximum output current: 6A
- PV_{IN}: 6 V to 14V, V_{OUT}: 0.7V to 5.0V
- Adjustable output voltage with down to 2.4 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 30mΩ
- 1% typical accuracy
- Efficiency up to 93%
- Internal single pole compensator minimizes external part count
- Protection: Input Undervoltage Lockout, (ViUVLO), Output Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature

Figure 1: Buck application schematic



Synchronous Buck Detail

The AnD8400 Synchronous Buck Regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFETs (SIM) provide up to 6A output current.

Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is generated internally via an oscillator and it is fixed at 571 kHz.

The customizable output voltage is specified by the WebAdapter tool or an external resistor divider. The regulator has customizable control and status pins including enable input, power-good output, and output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition.

The soft-start and soft-stop slew rates are also specified at 4ms. Additional sequencing options and soft start times are available by using the WebAdapter tools or jumpers.

Recommended Operating Conditions Synchronous Buck

over operating free-air temperature range
This section applies to all four Power Regulators

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	6		14(1)	V
I_{Lmax}	Load Current Maximum	6			A
V_{IN}	Bias Supply	6		14(1)	V

Electrical Characteristics Synchronous Buck

PV_{IN} = V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT})		0.7		5.5	V
Voltage Regulation	V_{IN} range (Including load line and temp. variation)	-1		+1	%
Switching frequency (F_{SW})			571		kHz
Switching frequency accuracy		-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$)			30		mΩ
Efficiency	V_{IN}=12V, V_{OUT}=1.2V, F_{SW}=571kHz, I_{OUT}=3A		83		%
Input Shutdown current (V_{IN})	EN = 0V		13		mA
Input quiescent current (PV_{IN})			7		mA
PROTECTION					
ViUVLO, input Undervoltage Lockout		4		10	V
OCP, Over Current Protection (% I_{OUT})			142		%
OTP, Over Temperature Protection	Shutdown (Power Good goes low) Hysteresis	125			°C
OVP, Overvoltage Protection trip point range (relative to Parameter Setting)		+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Parameter Setting)		-100		-432	mV
Power Good threshold (relative to Parameter Setting)		-100		-432	mV

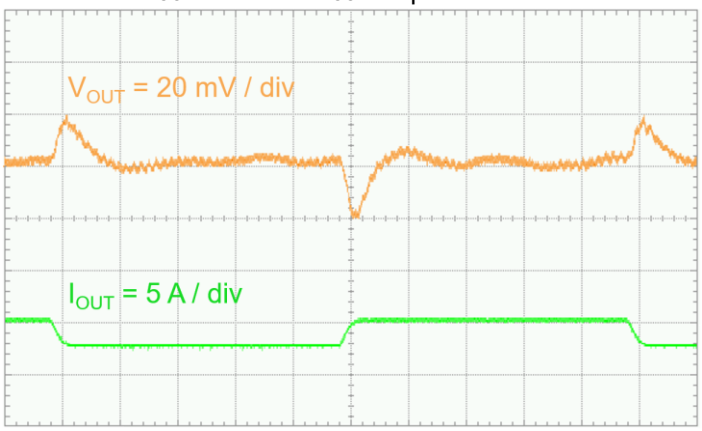
Notes (1) : Adaptable devices have an Integrated fixed compensation, optimized for the selected default inductor and for VIN range of 6 V to 14V. For input voltage above 14V (14V to 17V), use On-Demand or contact AnDAPT

Typical Characteristics

Unless otherwise specified: TA = 25°C

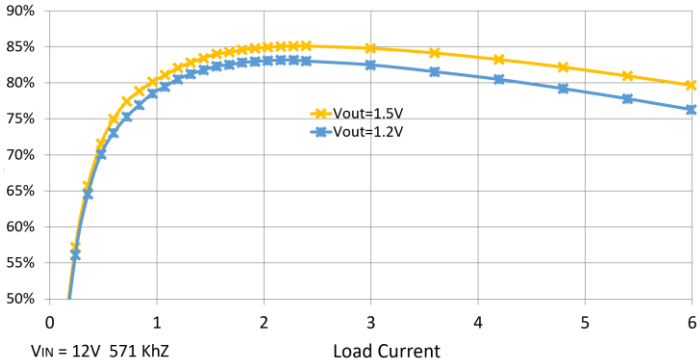
Transient Response

V_{OUT} = 1.8V I_{OUT} step 2.5 A to 5A



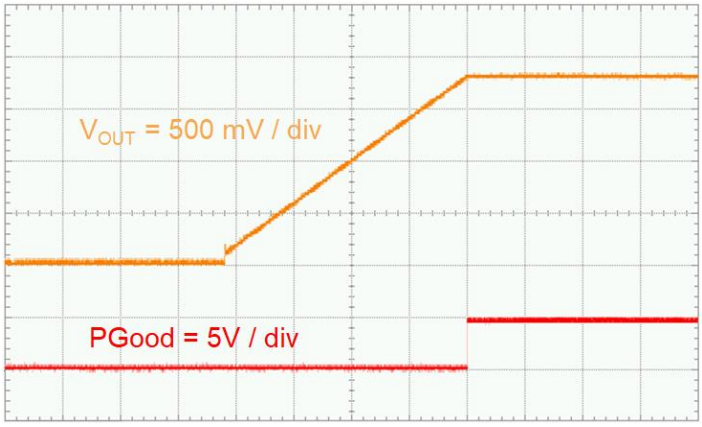
Time = 50µs / div

Efficiency



Soft Start

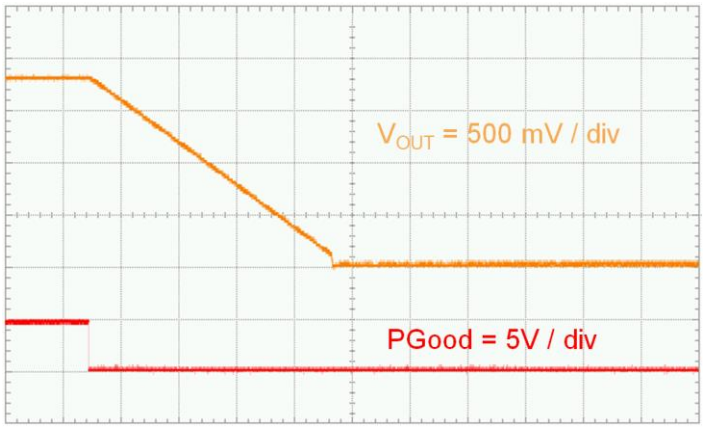
V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 2 ms / div

Soft Stop

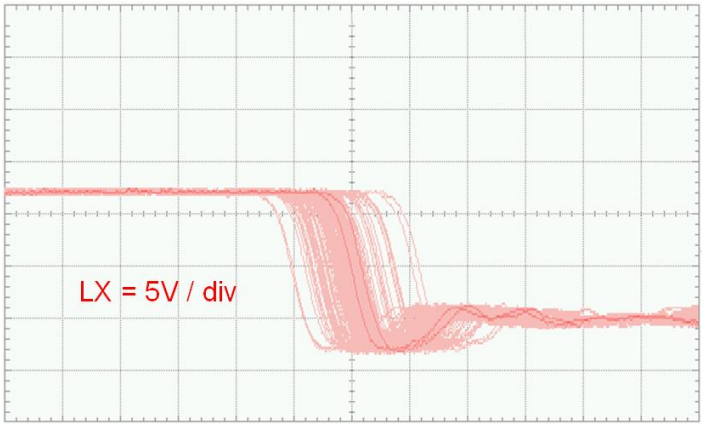
V_{IN} = 12V, V_{OUT} = 1.8V



Time = 2 ms / div

Jitter

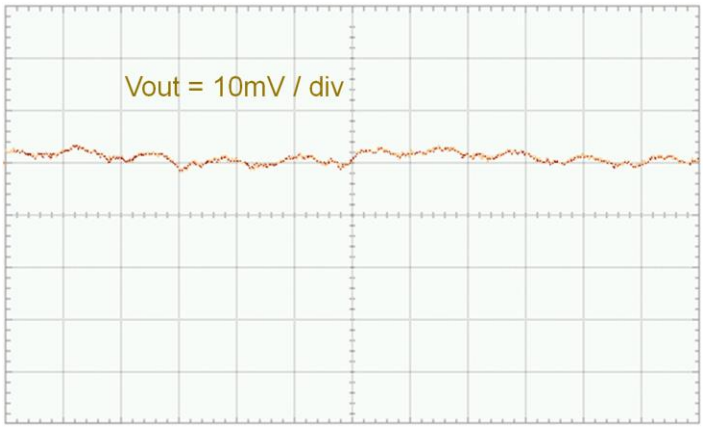
V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 5 ns / div

Ripple

V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2.5A



Time = 1 µs / div

Theory of Operation Buck Converters

The Synchronous Buck Regulator with integrated MOSFETs operates in voltage mode by comparing the V_{OUT} feedback voltage VFB, with a programmable reference Vref, to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the Hi-side and Lo-side MOSFET switches as shown in Figure 4.

In CCM (Continuous Conduction Mode), the PWM driver goes high turning the Hi-side switch "ON" to provide PVIN to the LX side of an inductor, L, where $V_L = PV_{IN} - V_{OUT}$. When the PWM driver goes low, the Hi-side switch turns "OFF", and the Lo-side switch turns "ON" providing a path for the inductor current to decrease with $V_L = -V_{OUT}$, until the next PWM turns back "ON". As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM duty cycle to optimize regulation and transient response over changing load conditions.

Output Capacitor Selection

Output Capacitor, Cout, is fixed at 188 µF (recommended 4x 47 µF Ceramic Capacitors) as tuned in the PID Bode plot design. This value is absolutely required for the stability of the AnD8400 Adaptable PMIC. If any system variation is required, the On-Demand AmP Platform which is tunable for optimum system performance parameters including stability, bandwidth, transient response, steady-state error, settling time, and damping using WebAmP tools is recommended.

Inductor Selection

Based on output voltage target, the Figure 3 shows recommended inductor and compensation capacitor value providing optimal performance.

Ct capacitance is required for higher output voltage range, in parallel to R1 resistor, to improve stability of the compensation without changing the PID coefficients.

As an example, for an output voltage range from 1.2V to 2.5V, use a 1.5uH inductor and capacitance Ct of 2.2nF.

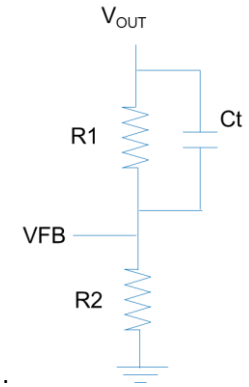


Figure 2

VIN = 12V	fsw = 530kHz-571kHz			
VOUT	L=0.68uH Ct=N/A	L=1uH Ct=N/A	L=1.5uH Ct=2.2nF	L=2.2uH Ct=4.7nF
0.7V				
1.0V				
1.2V				
1.5V				
1.8V				
2.5V				
3.3V				
5V				

L value is in the ideal range

L value just outside the ideal range, system works correctly

Figure 3 Inductor selection

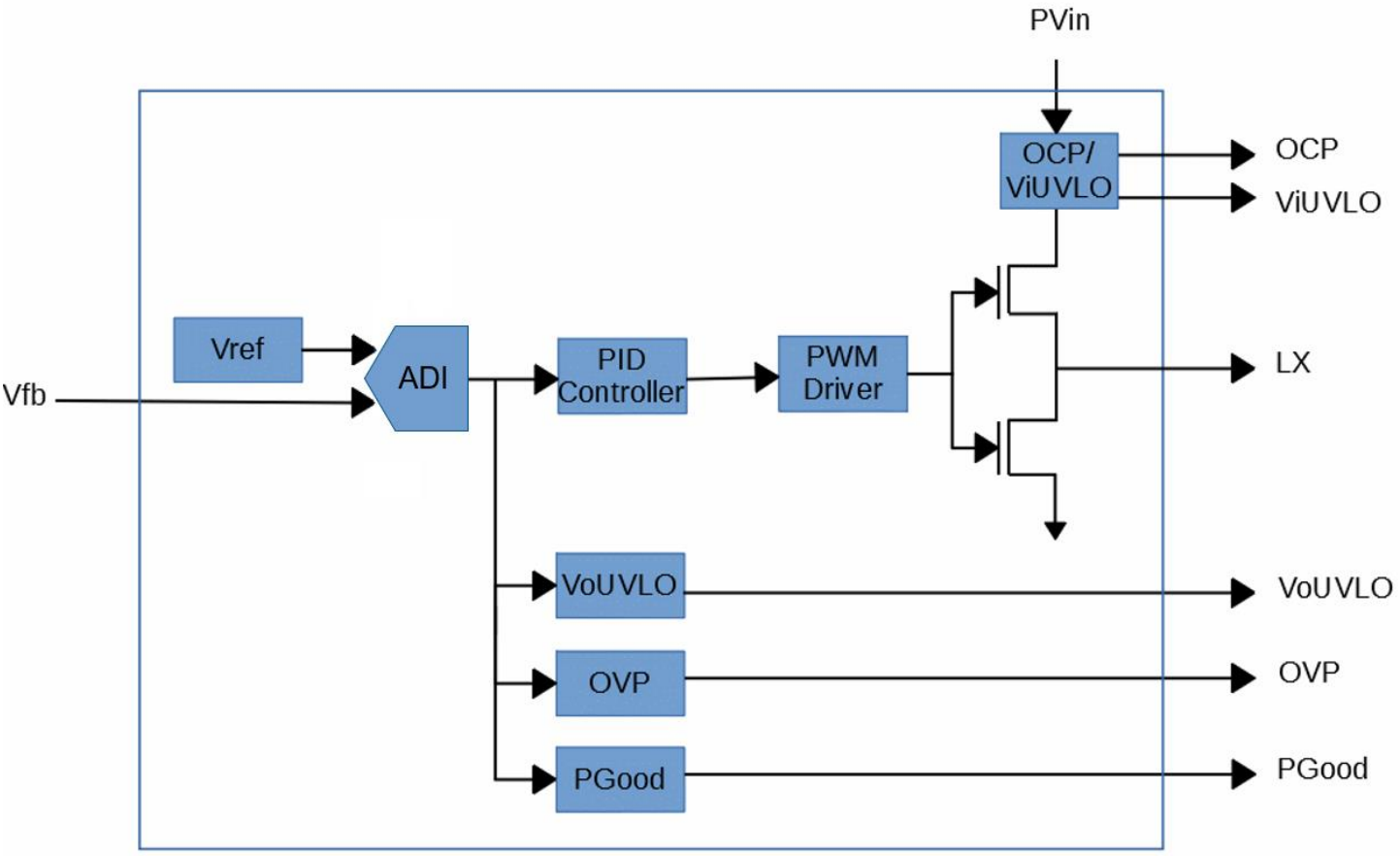


Figure 4: Functional Block Diagram

Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port. When EN goes high the output voltage, V_{OUT}, will ramp up according to the Soft Start ramp time. When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start preset ramp time.

PGOOD

The power-good, PGOOD, of all Synchronous Buck Converters are combined to generate the global Power Good signal, indicating the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time (Figure 5) and when all Faults are cleared . PGOOD will go low when V_{OUT} goes below the preset condition (80% of the V_{OUT}) or when faults occur such as OCP current limit, OVP over voltage, UVLO or OTP thermal shutdown. PGOOD will also go low if EN goes low.

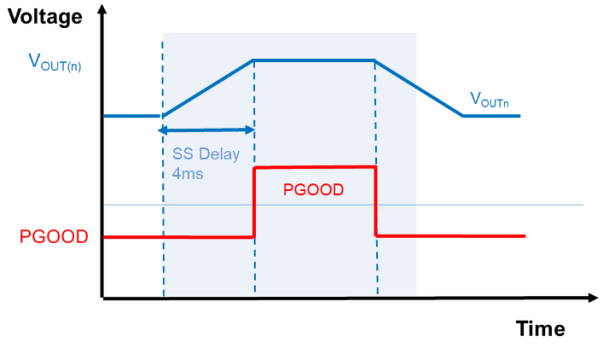


Figure 5.

Protection Features

As shown in Figure 4 each Synchronous Buck provides many protection features including UVLO, OVP, OCP and OTP.

Input Under Voltage (ViUVLO)

The input Under Voltage Lockout, ViUVLO, of all bucks, are combined to indicate the input voltage status of the entire device. The Global indication is UVLO. UVLO goes high when PV_{IN} voltage is lower than the preset condition (6 V). UVLO goes low when PV_{IN} voltage is greater than the preset condition in Parameter Settings, (6 V). On detection of ViUVLO, the device will power down and PGOOD will go low. On ViUVLO returning high, the device will restart with a new Soft Start cycle.

Output Under Voltage VoUVLO

The output Under Voltage Protection, VoUVLO, of all regulators are combined to indicate the global output voltage status. VoUVLO goes high when any of the regulator outputs is lower than 60% of the specified V_{OUT}. VoUVLO goes low when all the output voltages are above 60% of the specified V_{OUT}. On detection of VoUVLO, the regulator will power down and PGOOD will go low. EN cycling low-to-high, will restart the device with a new Soft Start cycle.

Over Voltage Protection

The Over Voltage Protection, OVP, of all regulators are combined to indicate the global output voltage status. FLTB is asserted low when any of the regulator outputs is 20% above specified V_{OUT}. FLTB is unasserted when all the outputs are less than 20% above the specified V_{OUT}. On detection of OVP, a regulator will skip Hi-side switch pulses until the fault condition is not present.

Over Current Protection

The Over Current Protection, OCP, of all regulators are combined to indicate the global output over current status. When the Output Current, $I_{OUT,}$ of any regulator is greater than 8.5A, the regulator will limit the Hi-side switch pulse width and OCP will go high. If I_{OUT} is greater than 10A, the regulator will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

V_{OUT} Resistor Settings

V_{OUT} voltages for Buck1, Buck3 and Buck4 POLs are set by the resistors R1 and R2.

The AnD8400 internal feedback reference, VFB, is 0.7V for Buck1, Buck3, and Buck4 with feedback resistor recommended values of

R1 = 2.21 kΩ
R2 = DNI (Do Not Install).

For V_{OUT} values greater the 0.7 V, use the following resistor divider equations:

R1 = 2.21 kΩ
R2 = VFB * R1 / (V_{OUT}-VFB) kΩ

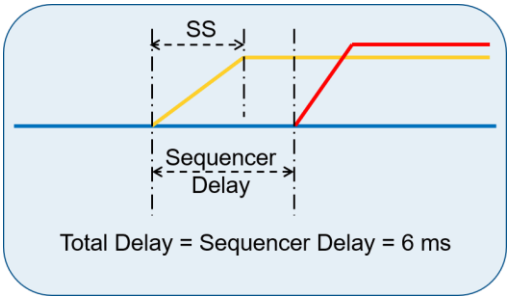
Use 1% resistor values for best accuracy. A resistor calculator for closest E96 1% value is provided by the WebAdapter Software Tool.

Sequencer Settings

The AnD8400 contains a sequencer that can operate either based on time delay or power good signal from prior rail in addition to time delay. The selection of power good or time delay is based on the setting of the TIME control pin 28. When the TIME control pin is high, the sequencer is based on time delay. When the TIME control pin is low, the sequencer is based on the PGood signal.

TIME Mode

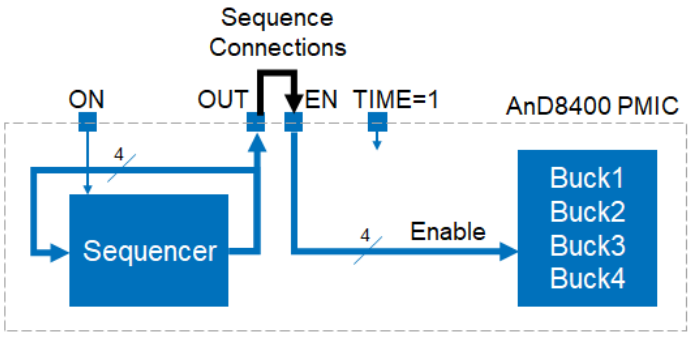
TIME Mode is specified when the TIME pin is in a high state as defaulted in the AnD8400. In this mode, each Buck[n] regulator begins a 4ms Soft Start when Enable[n], goes high. On completion of Soft Start, 2ms of Sequencer Delay remains before Enable[n+1] goes high, beginning the sequence for Buck[n+1]. The total cycle delay is 4ms + 2ms = 6ms per Buck as shown in the timing diagram below.



TIME Mode Sequencer Pin Connections

POL power-on and power-off sequences are set by the sequence Pin Connections. For example, Buck1, Buck2, Buck3 and Buck4 are sequenced in order as specified in the wire connection table below.

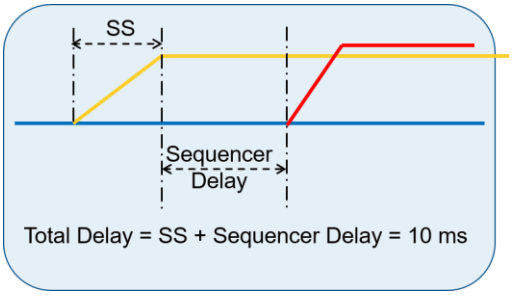
	OUT1 pin 53	OUT2 pin 27	OUT3 pin 22	OUT4 pin 58
Buck1 EN1 pin 52	√			
Buck2 EN2 pin 29		√		
Buck3 EN3 pin 25			√	
Buck4 EN4 pin 59				√



Grouping is accomplished with pin connections from one of the OUT pins, OUT1 to OUT4, to multiple EN pins EN1 to EN4. Time delay and Soft Start delay may be changed using WebAdapter software tool Advanced Mode.

PGood Mode

PGood Mode is specified when the TIME pin is in a low state (TIME =0). In this mode, each Buck[n] regulator begins a 4ms Soft Start when Enable[n], goes high. When Soft Start reaches 80% of Vout, PGood[n] goes high and starts a 6ms Sequencer Delay followed by Enable[n+1] going high, beginning the sequence for Buck[n+1]. The total cycle delay is 4ms + 6ms = 10ms per Buck as shown in the timing diagram below.

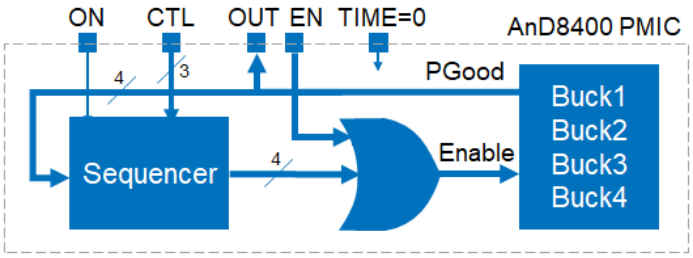


PGood Mode Sequencer Pin Connections

PGood mode sequencing change is accomplished with the three control pins, CTL0, CTL1, CTL2 as defined in the truth table below. Apply these signal level connections to the AnD8400 board design. CTL0, CTL1 and CTL2 are defaulted high to a 1 state with a weak current source pull-up of about 50 µA. To assert a low 0 state, connect to GND.

CTL2 pin 50	CTL1 pin 57	CTL0 pin 65	Buck Sequence n= 1,2,3,4			
0	0	0	4	3	2	1
0	0	1	4	3	1	2
0	1	0	3	4	2	1
0	1	1	3	4	1	2
1	0	0	2	1	4	3
1	0	1	1	2	4	3
1	1	0	2	1	3	4
1	1	1	1	2	3	4

Additional control flexibility is provided with independent enables EN[1 to 4] as shown in the block diagram below.



Grouping, Time delay and Soft Start delay may be changed using WebAdapter software tool Advanced Mode.

Integrated Auxiliary LDO

The AnD8400 has 4 integrated LDOs that are fixed output voltages (3.3V, 2.5V, 1.8V, and 1.2V). The input voltage to the four LDO's is from the internal 4.5V bias voltage. The pin locations of these integrated LDOs, are fixed and cannot be modified by WebAdapter Tools. The 3.3V output pin is 33. The 1.2V LDO output is pin 46. The 1.8V LDO output is pin 30. The 2.5V LDO output is pin 48. Please see table below for electrical characteristics of these LDOs.

Electrical Characteristics Integrated LDO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LDO1V2	LDO 1.2V output voltage	I_{CC}=0mA, V_{IN}=4.5V	1.164	1.2	1.236	V
I_{CC}	LDO 1.2V output current				200	mA
LDO1V8	LDO 1.8V output voltage	I1V8=0mA, V_{IN}=4.5V	1.746	1.8	1.854	V
I1V8	LDO 1.8V output current				200	mA
LDO2V5	LDO 2.5V output voltage	I2V5=0mA, V_{IN}=4.5V	2.425	2.5	2.575	V
I_{CC}	LDO 2.5V output current				200	mA
LDO3V3	LDO 3.3V output voltage	I3V3=0mA, V_{IN}=4.5V	3.201	3.3	3.399	V
I3V3	LDO 3.3V output current				200	mA

Over Temperature Protection (OTP)

The AnD8400 has an integrated temperature sensor for over temperature monitoring and protection. For system safety, the AnD8400 will shut down if the device junction temperature goes over 125°C. This will shut down all the power rails. After cooling down, sequencer SEQ_ON pin needs to be triggered by a rising edge. There will be no chattering of operation mode when the temperature hovers around the 125°C limit.

ESD CONSIDERATIONS

Establish and use (Electrostatic Damage) ESD-safe handling precautions when unpacking and handling ESD-sensitive devices. Store ESD sensitive devices in ESD safe containers until ready for use. The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly. AnDAPT products are qualified to meet at least 500V ESD-MM (Machine Model) 2000V ESD-HM (Human Body Model). Restrict all device handling to ESD protected work areas that measure less than 400V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

Assembly Recommendation

For part placement, please use standard pick and place machine with ± 0.05 mm accuracy. Mount the device with slower speed and higher force. Place the package 1 ~ 2 mils into the paste. The device package has excellent self-alignment during solder reflow if a minimum of 75% of the lead diameter intersect with the pad.

Solder Paste

The screen printing quantity of solder paste is a key factor in producing high yield assemblies. Recommended solder paste alloy is Sn/Ag/Cu family for lead-free application. Low residue and no clean flux is recommended. Particle size type IV (25 ~ 38 μm) is preferred to improve printing performance. Particle size type III (25 ~ 45 μm) also is acceptable.

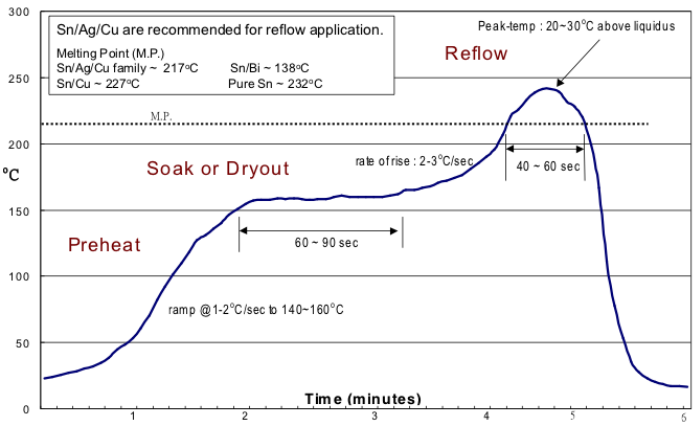
Solder Stencils

The contrast between large thermal pads and small terminal pads of the QFN package can present a challenge in production and even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow- solder processing. The solder joint thickness for QFN package terminal pads should be 50 – 75 μm. Stencil recommended type is laser cutting stainless steel with thickness of 100 ~ 150 μm (125 μm as a guide). The actual thickness of a stencil is depending on other SMD components on the PCB. Metal blade or polymer with 90-degree hardness squeegee is recommended. Aperture size for terminal pad should have aspect ratio (width / thickness) of greater than 1.5 and area ratio (Area of aperture opening / aperture wall area) of greater than 0.66. The stencil aperture is typically designed to match the pad size on the PCB 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. An oval-shaped opening should be used to get the optimum paste release and rounded corners to minimize clogging. Positive taper

walls (5-degree tapering) with bottom opening larger than the top is recommended. Small multiple openings should be used instead of one big opening. 60% ~ 85% solder paste coverage is recommended to reduce the chance of having short connection.

REFLOW SPECIFICATION

AnDAPT products are qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling to avoid subsequent thermal and mechanical damage during the solder-reflow attachment phase of PCB assembly. Check solder paste data sheet for any additional or difference instruction. Using a forced convection reflow oven with nitrogen is recommended. Also, the reflow oven should have equal or less than ± 5°C temperature uniformity. The recommended reflow profile for lead-free solder past shown below.



COMPLIANCE

ENVIRONMENTAL COMPLIANCE

AnDAPT products are RoHS and Green compliant. AnDAPT products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC COMPLIANCE

AnDAPT products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

COMPLIANCE DECLARATION DISCLAIMER

AnDAPT believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. AnDAPT subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by AnDAPT.

GENERAL

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Internal AnD8400 PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AND8400 PMIC. Listed below is a description of blocks and resources that are used to create Buck regulators.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, In Amp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref- V_{OUT}[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.
-

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

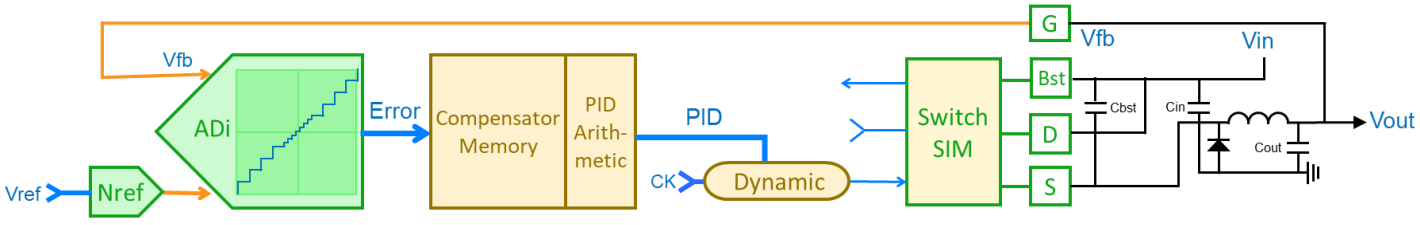
Scalable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

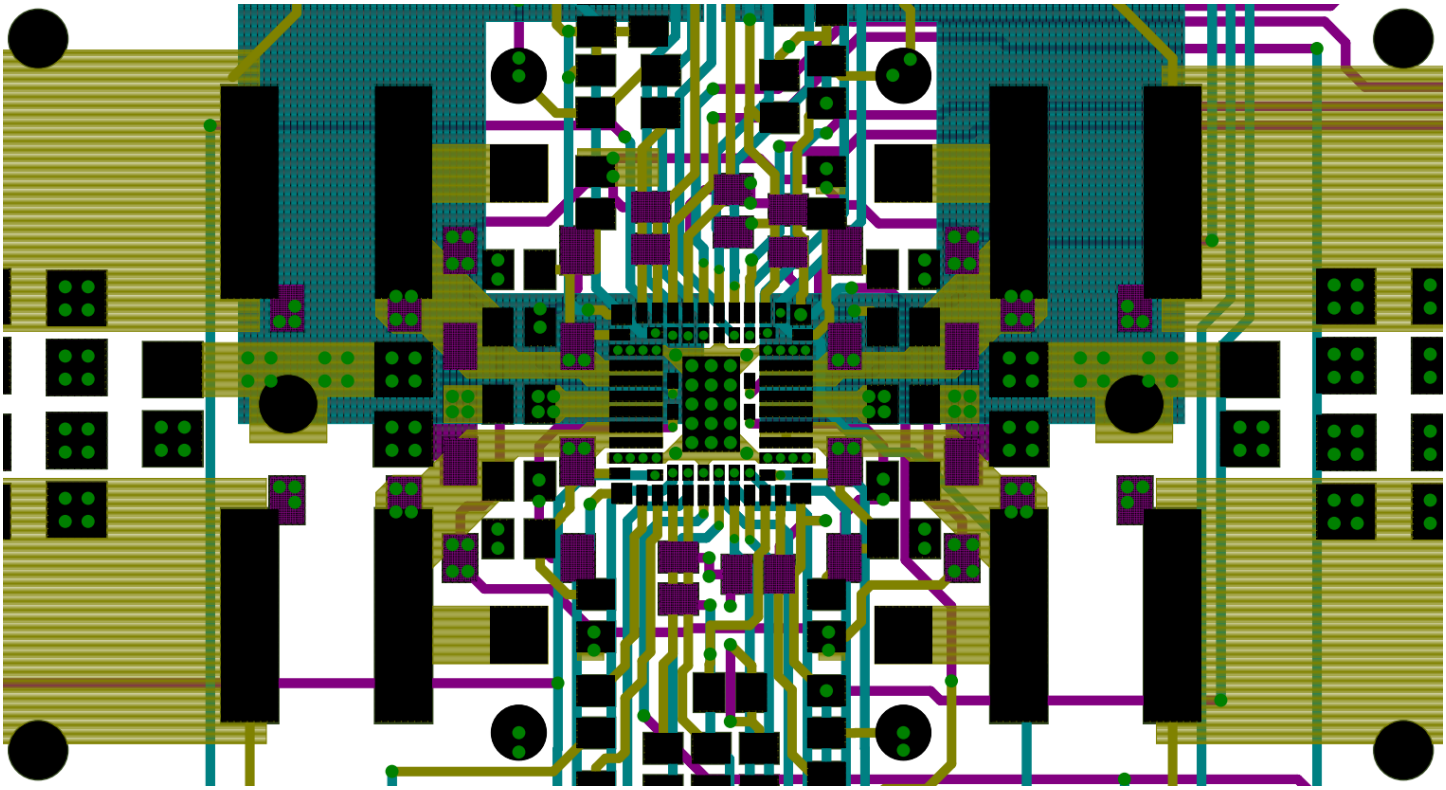
SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, Drain voltage or current and Analog Fabric including programmable references (Nrefs).

Figure 6: PMIC Blocks and Resources Example - Buck Regulator



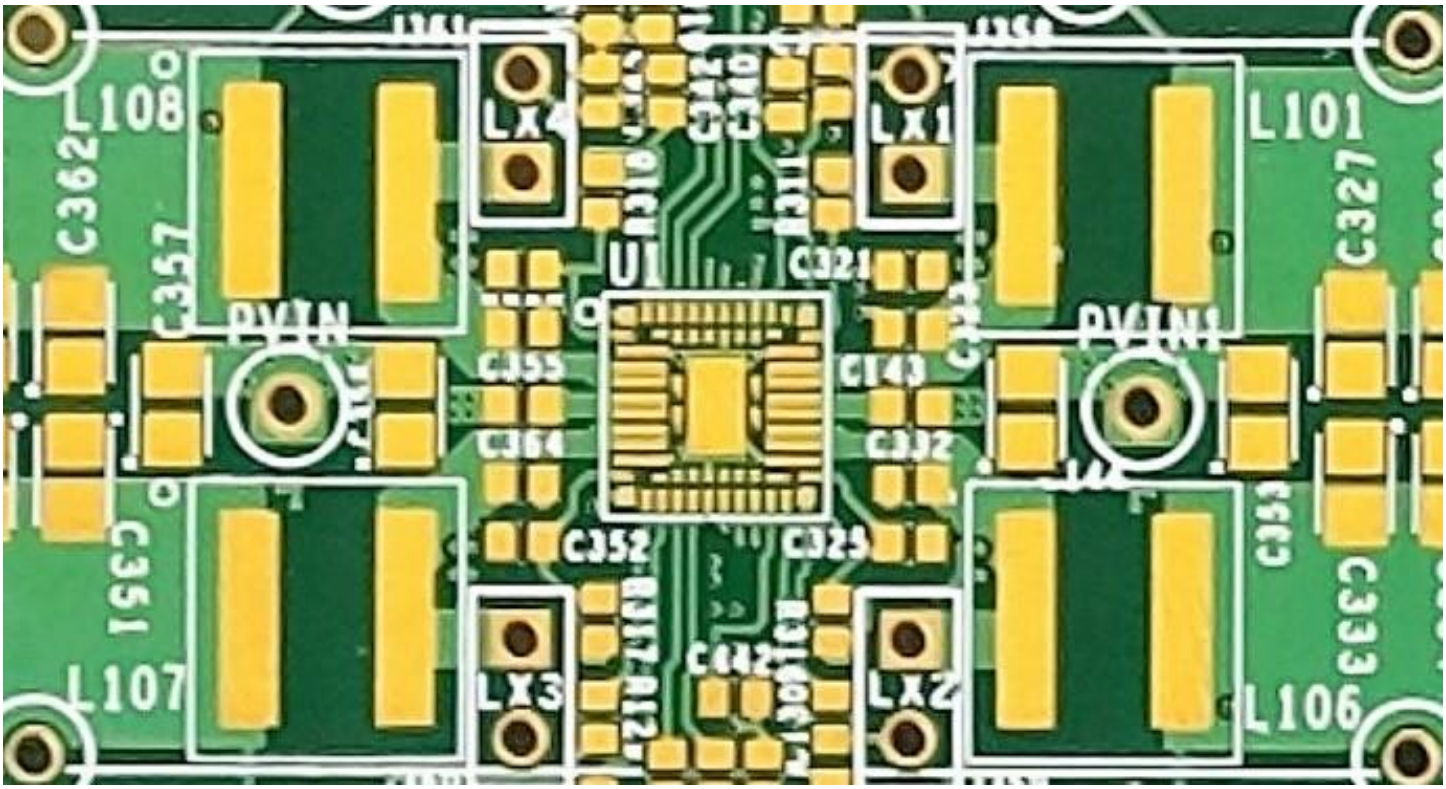
Example Cadence Allegro CAD Layout

Pitch minimum: 0.4mm, 0.25mm trace, 0.15mm space; 4 layers: top 2oz GND 1oz, power/signal 1oz, bottom 2 oz

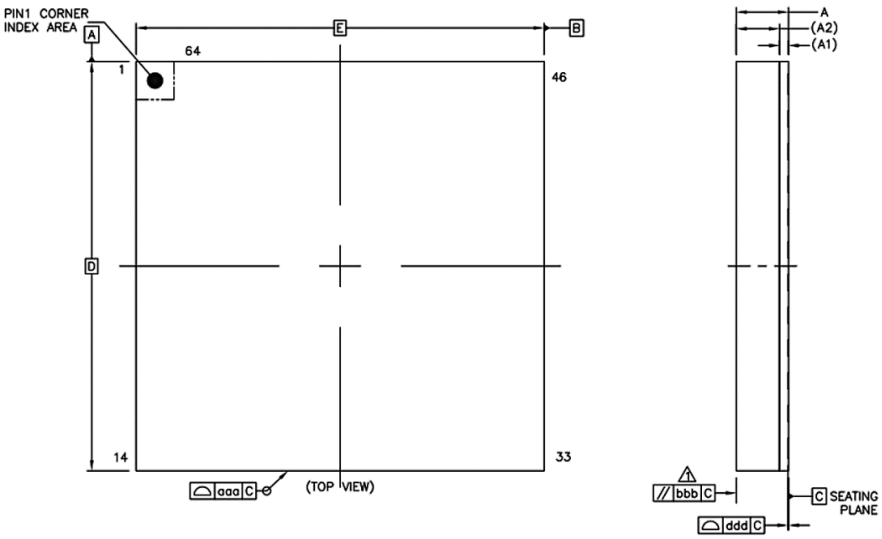


Example PCB Layout

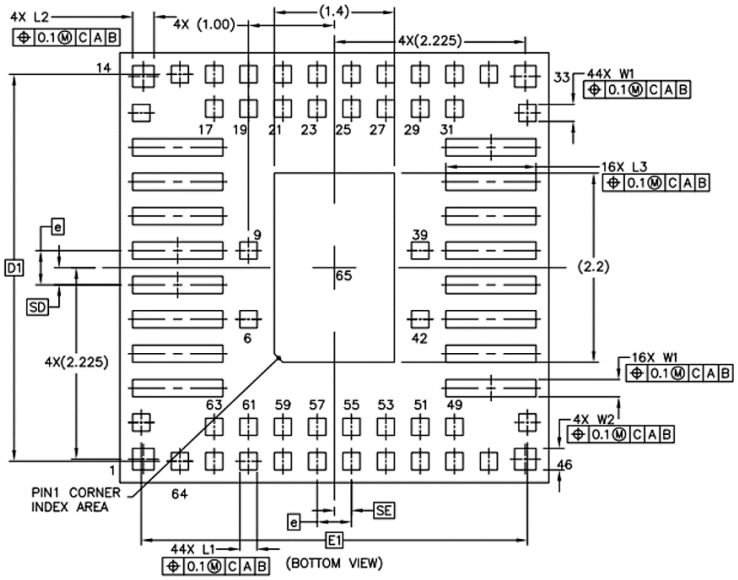
Symmetric layout: One Buck in each quadrant, AnD8400 Adaptable PMIC in center



Package Description – QF65 5x5 mm



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.7
SUBSTRATE THICKNESS	A1		0.11	REF
MOLD THICKNESS	A2		0.53	REF
BODY SIZE	D		5	BSC
	E		5	BSC
LEAD WIDTH	W1	0.15	0.2	0.25
LEAD WIDTH	W2	0.2	0.25	0.3
LEAD LENGTH	L1	0.15	0.2	0.25
LEAD LENGTH	L2	0.2	0.25	0.3
LEAD LENGTH	L3	1	1.05	1.1
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		65	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

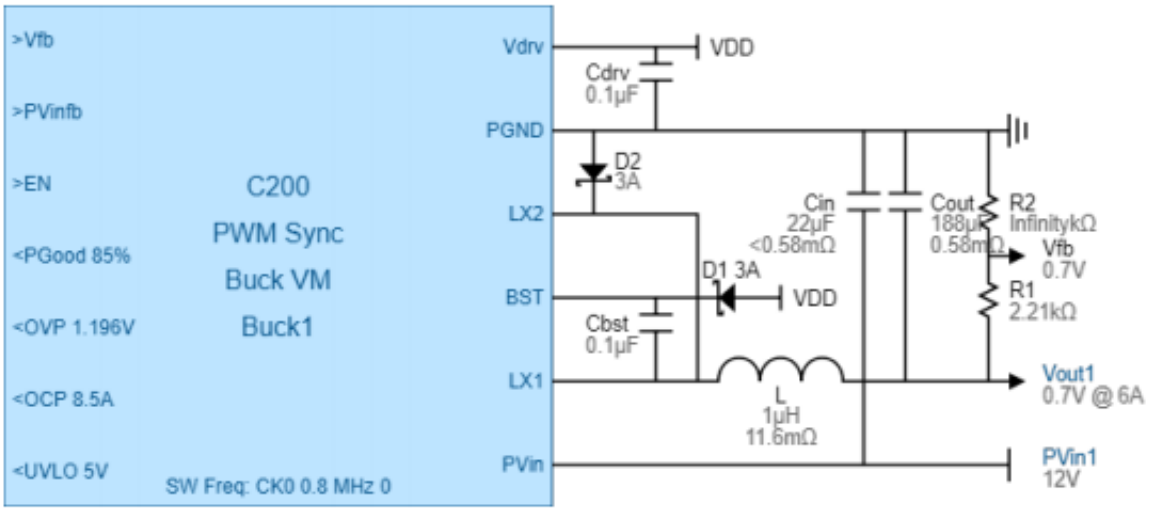


AnD8400 Design File Generated by WebAmP Software Tools

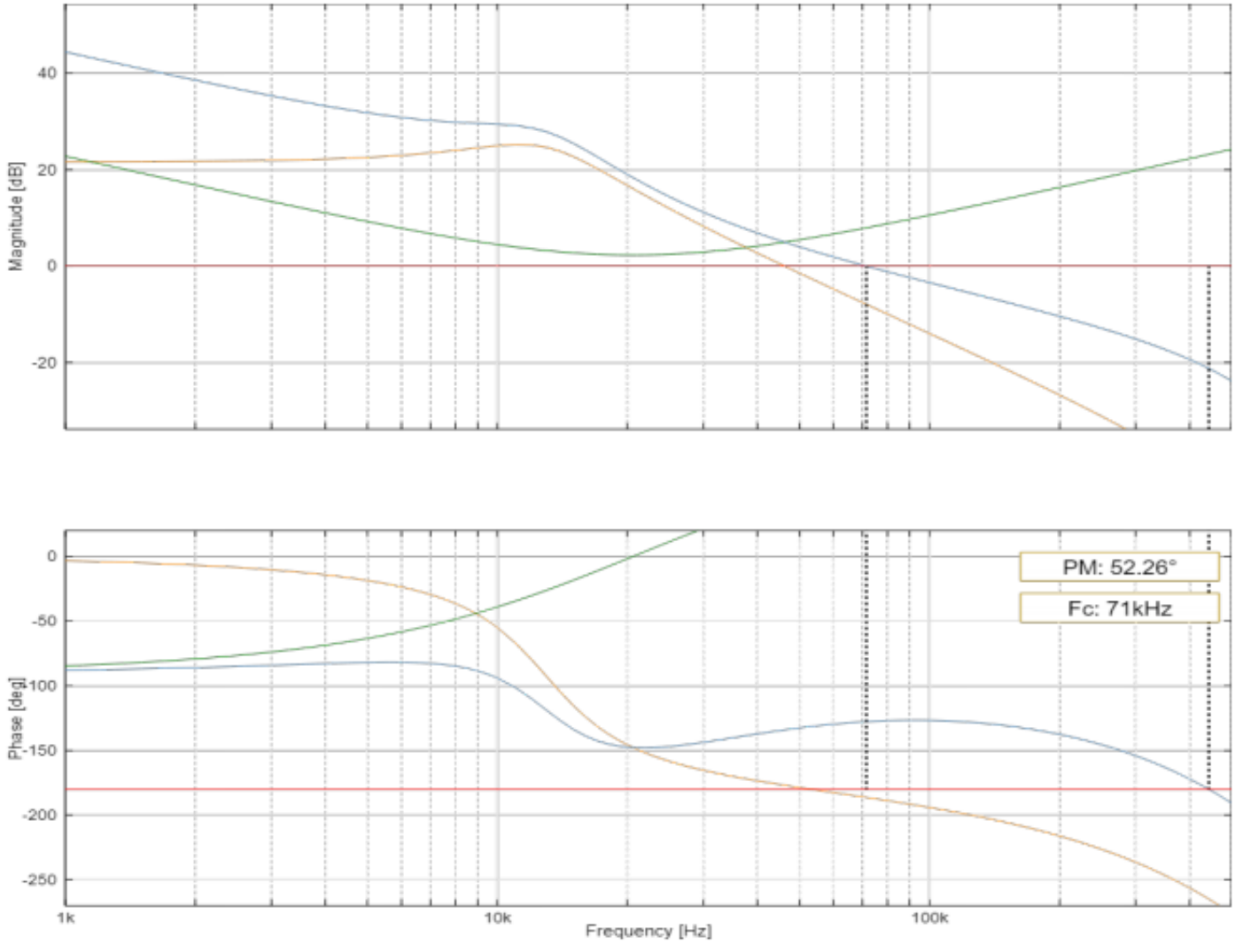
C200S PWM Sync Buck VM

AmP Power Buck1

Schematic



Bode Plot



C200S PWM Sync Buck VM

AmP Power Buck1

BoM

Part	Description	Recommended Attributes	Attributes	Quantity	Part Number	Spec	Manufacturer
C200S	PWM Sync Buck VM		Vout1,0.7V @ 6A	1	V180501		
L	Inductor	0.458µH, 10mΩ, >6A	1µH, 11.6mΩ, 7.4A	1	74438357010		Wurth Elektronik
Cout	Capacitor	214µF, 4mΩ, >0.7V	47µF, 2.31mΩ, 6.3V	4	885012107006		Wurth Elektronik
Cin	Capacitor	22µF, <4mΩ, >12V	22µF, 2.99mΩ, 16V	1	885012108018		Wurth Elektronik
Cbst	Capacitor	0.1µF, >6V	0.1µF, >6V	1			
Cdrv	Capacitor	0.1µF, >6V	0.1µF, >6V	1			
D1	Schottky Diode	3A, 0.54V	3A, 0.54V	1	DB2W40300L		Panasonic Electronic Components
D2	Schottky Diode	3A, 0.54V	3A, 0.54V	1	DB2W40300L		Panasonic Electronic Components
R1	Resistor	0.0499kΩ, 1%, 0.063W	2.21kΩ, 1%, 0.063W	1			
R2	Resistor	DNS	DNS	0			

C200S PWM Sync Buck VM

AmP Power Buck1

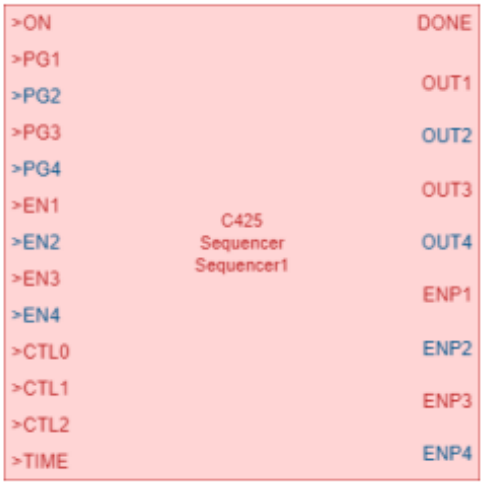
Parameters

Category	Parameter	Description	Value	Units
Basic Configuration	Fsw	Switching Frequency	0	
	Vin	Nominal Input Voltage	12	V
	Vin_Name	Used in The Schematics View	PVin1	
	Vout	Nominal Output Voltage	0.7	V
	Vout_Name	Used in The Schematics View	Vout1	
	V_Ripple	Max Ripple. Used for LC Recommendations	0.1	%
	V_Overshoot	Max Overshoot for a transient of Iout Delta	0.03	V
	Iout	Maximum Converter Current	6	A
	I_Ripple	Desired Ripple. Used for LC Recommendations	13.73	%
	I_Delta	Used to Calculate Overshoot and Transient Response	3	A
LC Components	Inductor	Nominal Inductor Value	1	µH
	Inductor_DCR	Nominal Inductor DC Resistance	11.6	mΩ
	Capacitor	Nominal Capacitor value	188	µF
	Cap_ESR	Nominal Capacitor Equivalent Series Resistance	0.58	mΩ
	fLC	LC Resonant Frequency	11.6	kHz
Vfb Resistor Components	R1		2.21	kΩ
	R2		Infinity	kΩ
	Vfb	Vfb = Vout * R2 / (R1 + R2)	0.7	V
	R3		1370	kΩ
	R4		107	kΩ
	PVinfb		0.869	V
	Ext_Div_Ratio		1	
	Ext_Div_Ratio2		13.804	
Controller	Gain	Proportional Gain	650	
	Fz1	First Compensation Zero	10.6	kHz
	Fz2	Second Compensation Zero	40	kHz
	Ki	Integral Gain	4.329115e+7	
	Kd	Derivative gain	2.586268e-3	
	Controller_Type		0	
Fault Protection	UVLO	Input Under Voltage Lockout	5	V
	UVLOSense	Internal: Sensed through High Side Drain pin. External: Sensed through a GPIO	Internal	
	VoUVLO	Output Under Voltage Lockout Threshold	0.5	V
	OCP	Cycle by Cycle Current Protection Level	8.5	A
	OVP	Output Over Voltage Protection Level	1.196	V
Constraints	UseCM	Use CM	enable	
	Rise_Time	Soft Start Length	4	ms
	PGood	Power Good percentage of Nominal Vout	85	%

C425 Sequencer

AmP Power Sequencer1

Schematic



C425 Sequencer

AmP Power Sequencer1

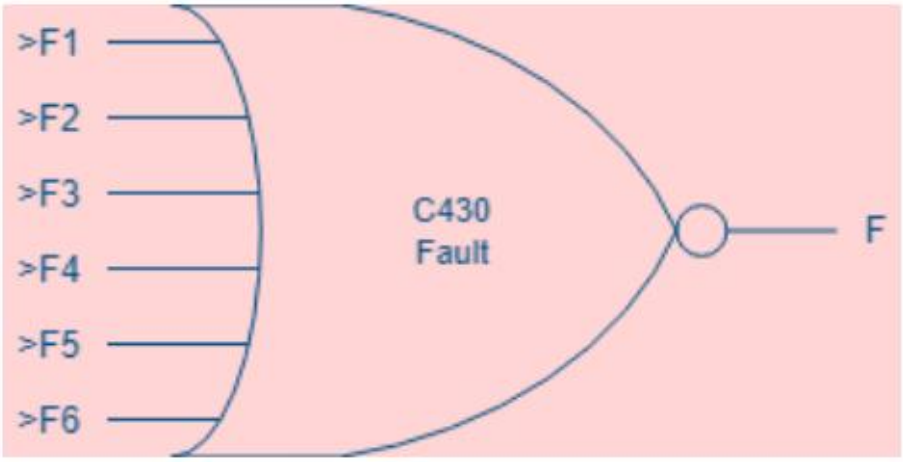
Parameters

Category	Parameter	Description	Value	Units
Sequencer	Number_of_POLs	Number of POLs	4	
	Number_of_Seq_Groups	Number of Sequencer Groups	4	
	Time_Step	Time Step	1	ms
	Number_of_Steps	Number of Steps	16	
	Maximum_Delay	Maximum Delay	16	ms
	Groups		11110000	
	Target_Delays		66660000	
	Actual_Delays		66660000	

C430 Fault Manager

AmP Power Fault

Schematic



Global BoM

Component	Part	Description	Attributes	Quantity	Part Number	Manufacturer
Platform	AnP8D86QF65	AnP Power IC	8 MOSFETS, 6A	1		AnDAPT, Inc
Platform	Cvin1	Capacitor	0.1µF, >25V	1		
Platform	Cvin2	Capacitor	1µF, >25V	1		
Platform	Cvin3	Capacitor	10µF, >25V	1		
Platform	Cvdd1	Capacitor	0.1µF, >6V	1		
Platform	Cvdd2	Capacitor	10µF, >6V	1		
Platform	Cvcc1	Capacitor	0.1µF, >6V	1		
Platform	Cvcc2	Capacitor	1µF, >6V	1		
Platform	C3v31	Capacitor	0.1µF, >6V	1		
Platform	C3v32	Capacitor	1µF, >6V	1		
Platform	Cldoa1	Capacitor	0.1µF, >6V	1		
Platform	Cldoa2	Capacitor	1µF, >6V	1		
Platform	Cldob1	Capacitor	0.1µF, >6V	1		
Platform	Cldob2	Capacitor	1µF, >6V	1		
Platform	Cvcco0	Capacitor	0.1µF, >6V	1		
Platform	Cvcco1	Capacitor	0.1µF, >6V	1		
Platform	Cvcco2	Capacitor	0.1µF, >6V	1		
Platform	Cvcco3	Capacitor	0.1µF, >6V	1		
Buck1	C200S	PWM Sync Buck VM	Vout1.0.7V @ 6A	1	V180501	
Buck1	L	Inductor	1µH, 11.6mΩ, 7.4A	1	74438357010	Wurth Elektronik
Buck1	Cout	Capacitor	47µF, 2.31mΩ, 6.3V	4	885012107006	Wurth Elektronik
Buck1	Cin	Capacitor	22µF, 2.99mΩ, 16V	1	885012108018	Wurth Elektronik
Buck1	Cbst	Capacitor	0.1µF, >6V	1		
Buck1	Cdrv	Capacitor	0.1µF, >6V	1		
Buck1	D1	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck1	D2	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck1	R1	Resistor	2.21kΩ, 1%, 0.063W	1		
Buck1	R2	Resistor	DNS	0		
Buck2	C200S	PWM Sync Buck VM	Vout2.0.7V @ 6A	1	V180501	
Buck2	L	Inductor	1µH, 11.6mΩ, 7.4A	1	74438357010	Wurth Elektronik
Buck2	Cout	Capacitor	47µF, 2.31mΩ, 6.3V	4	885012107006	Wurth Elektronik
Buck2	Cin	Capacitor	22µF, 2.99mΩ, 16V	1	885012108018	Wurth Elektronik
Buck2	Cbst	Capacitor	0.1µF, >6V	1		
Buck2	Cdrv	Capacitor	0.1µF, >6V	1		
Buck2	D1	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck2	D2	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck2	R1	Resistor	2.21kΩ, 1%, 0.063W	1		
Buck2	R2	Resistor	DNS	0		
Buck3	C200S	PWM Sync Buck VM	Vout3.0.7V @ 6A	1	V180501	
Buck3	L	Inductor	1µH, 11.6mΩ, 7.4A	1	74438357010	Wurth Elektronik
Buck3	Cout	Capacitor	47µF, 2.31mΩ, 6.3V	4	885012107006	Wurth Elektronik
Buck3	Cin	Capacitor	22µF, 2.99mΩ, 16V	1	885012108018	Wurth Elektronik
Buck3	Cbst	Capacitor	0.1µF, >6V	1		
Buck3	Cdrv	Capacitor	0.1µF, >6V	1		
Buck3	D1	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck3	D2	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck3	R1	Resistor	2.21kΩ, 1%, 0.063W	1		
Buck3	R2	Resistor	DNS	0		
Buck4	C200S	PWM Sync Buck VM	Vout4.0.7V @ 6A	1	V180501	
Buck4	L	Inductor	1µH, 11.6mΩ, 7.4A	1	78438357010	Wurth Elektronik
Buck4	Cout	Capacitor	47µF, 2.31mΩ, 6.3V	4	885012107006	Wurth Elektronik
Buck4	Cin	Capacitor	22µF, 2.99mΩ, 16V	1	885012108018	Wurth Elektronik
Buck4	Cbst	Capacitor	0.1µF, >6V	1		
Buck4	Cdrv	Capacitor	0.1µF, >6V	1		
Buck4	D1	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck4	D2	Schottky Diode	3A, 0.54V	1	DB2W40300L	Panasonic Electronic Components
Buck4	R1	Resistor	2.21kΩ, 1%, 0.063W	1		
Buck4	R2	Resistor	DNS	0		
Sequencer1	C425	Sequencer		1		
Fault	C430	Fault Manager		1		
UVLO	C430	Fault Manager		1		
OCP	C430	Fault Manager		1		
OVP	C430	Fault Manager		1		
PGood	C430	Fault Manager		1		

Errata

Date	Description
07/15/2019	LDOb output is disabled
12/19/2018	SIM Pin (MOSFET DRV-Drain) ESD 750V HBM

Revision History

Date	Revision
03/03/2020	Added Output Capacitor Specification, update pin 22 description.
01/14/2020	Updated PVIN range to min 6 V and max 14 V
07/15/2019	Updated Inductor Selection Based on output voltage target, Figure 3
03/22/2019	Updated PVIN range to min 4.75V and max 14V
12/05/2018	Update Typical Characteristic Efficiency, PGood Mode 80% VOUT
11/01/2018	Update to V181031
09/27/2018	Advanced Release V180910

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Trademarks