PWM Async Buck, Current Mode

Power Component: C150_B

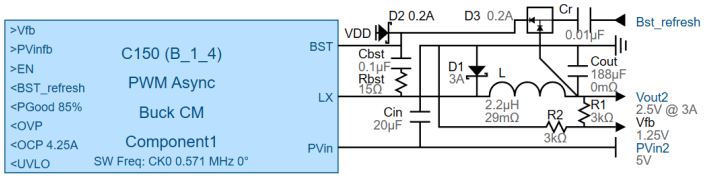
Product Description

The C150_B Power Component is a customizable, PWM Asynchronous Buck, Current Mode Switching Regulator. Combine the C150_B component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management integrated circuit (PMIC).

Features

- PWM, Current Mode, point-of-load (POL) regulator
- Maximum output current: 6A
- PV_{IN}: 3 to 14V, V_{OUT}: 0.7V to 5.5V
- Adjustable output voltage with down to 2.5 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 30mΩ
- 1% load regulation
- Efficiency up to 95%
- Internal compensator minimizes external part count
- Adjustable switching frequency from 500 kHz to 1 MHz
- Adaptable compensation, bandwidth, gain & phase margin
- Adjustable protection: Input Undervoltage Lockout, (ViUVLO), Output Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- One SIM element; integrate up to eight C150_B Power Components in one AmP Platform

Figure 1: C150_B application schematic



Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing

Product Detail

The C150_B Asynchronous Buck Regulator includes an integrated MOSFET, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFET-(SIM) provides up to 6A output current. Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. MOSFET current is sensed through an internal current mirror and compared with a current reference using digital compensation. The switching frequency is either generated internally via an oscillator with selectable frequencies or provided via an external pin.

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmp development software. The C150_B component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or input undervoltage lockout (ViUVLO) condition. The threshold values are specified by the power engineer using the WebAmp tool.

The customizable soft-start and soft-stop slew rates are also specified by the power engineer using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 customizable Sequencer, by interconnecting signals EN and PGood to provide customizable dependencies and customizable delays between each sequence step.

Recommended Operating Conditions

over operating free-air temperature range

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	3		14	V
I_{OUT}	I_{OUT} Output Current Maximum†			6	A

Electrical Characteristics

PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT})		0.7		5.5	V
Voltage Regulation	Including load line and temperature variation V_{IN} range: 6V to 14V	-1		+1	%
Switching frequency (F_{SW})		500		1000	kHz
Switching frequency accuracy		-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$)			30		mΩ
Peak efficiency	V_{IN}=9V, V_{OUT}=5V, F_{SW}=800kHz I_{OUT}=2.2A		94		%
Full Load Efficiency	V_{IN}=12V, V_{OUT}=5V, F_{SW}=800kHz, I_{OUT}=6.0A		91		%
Input Shutdown current (V_{IN})	EN = Low		3.1		mA
Input Shutdown current (PV_{IN})			0.1		mA
Input Quiescent current (V_{IN})	EN = High, I_{OUT} = 0A, Fsw = 571 kHz V_{OUT} = 5V		3.8		mA
Input Quiescent current (PV_{IN})			3.3		mA
PROTECTION					
ViUVLO, input Undervoltage Lockout		2.5		10	V
OCP, Over Current Protection (% I_{OUT})			140		%
OTP, Over Temperature Protection	Shutdown (Power Good goes low) Hysteresis	125			°C
OVP, Overvoltage Protection trip point range (relative to Vfb Setting)**		+100		+320	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Vfb Setting)**		-100		-320	mV
Power Good threshold (relative to Vfb Setting)**		-100		-320	mV

† max current also depends on Vin, Vout and Fsw as outlined in Figure 4 Maximum Output Current, IOUT

* Parameters shaded in green are user customizable as set in WebAmP development software

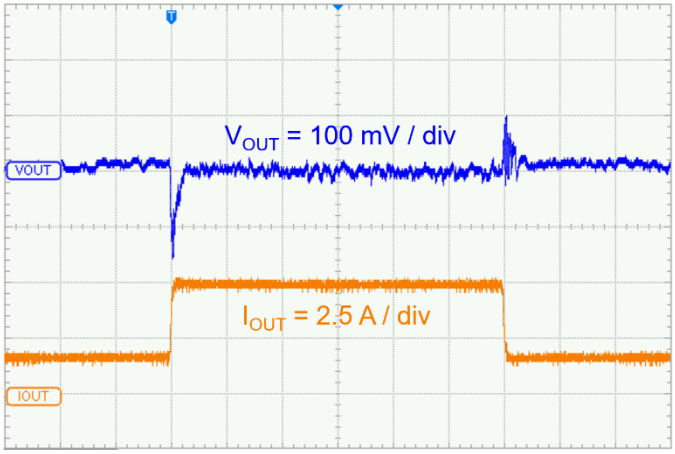
** Vfb is equal to Vout multiplied by the feedback resistor divider ratio, R2/(R1+R2) (See page 7, Vfb Resistor Components)

Typical Characteristics

Unless otherwise specified: TA = 25°C, PV_{IN} =12V, F_{SW} = 800kHz, L_{OUT} = 2.2 µH, C_{OUT} = 188µF

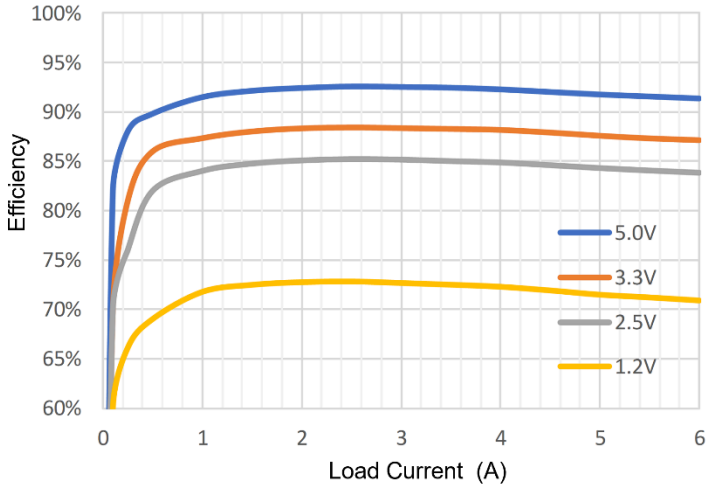
Transient Response

V_{OUT} = 5 V, I_{OUT} step 1.5 A to 4.5 A, Slew Rate: 2.5A/µs



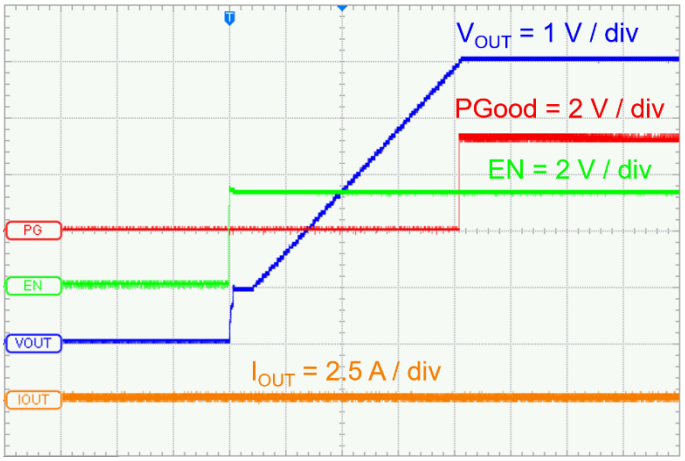
Time = 200 µs / div

Efficiency



Soft Start, No Load

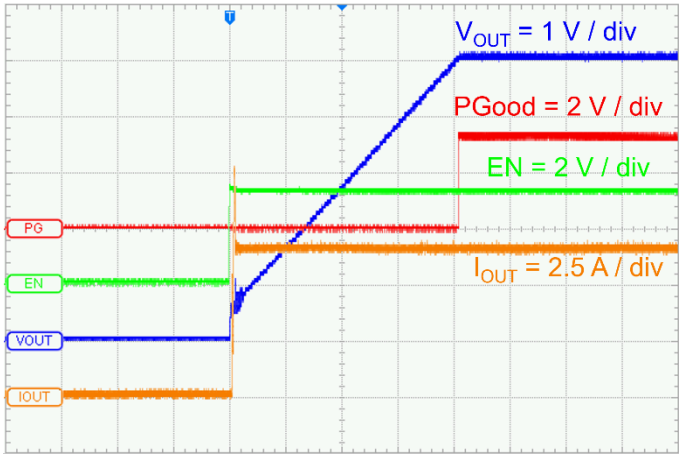
PVin = 12V, Vout = 5V



Time = 2 ms / div

Soft Start, Load = 6A

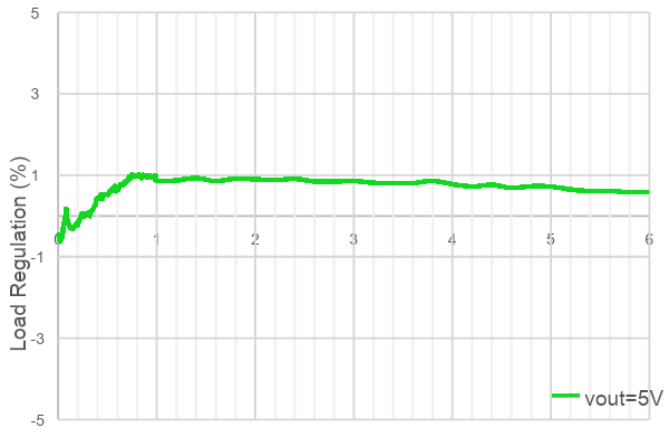
PVin = 12V, Vout = 5V



Time = 2 ms / div

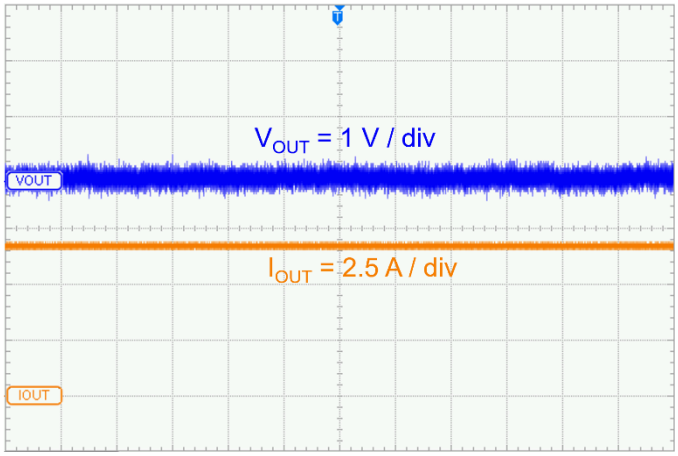
Load Regulation Percentage Error

PVin = 12V, Vout = 5V



Vout Ripple

PVin = 12V, Vout = 5V, Iout = 6A



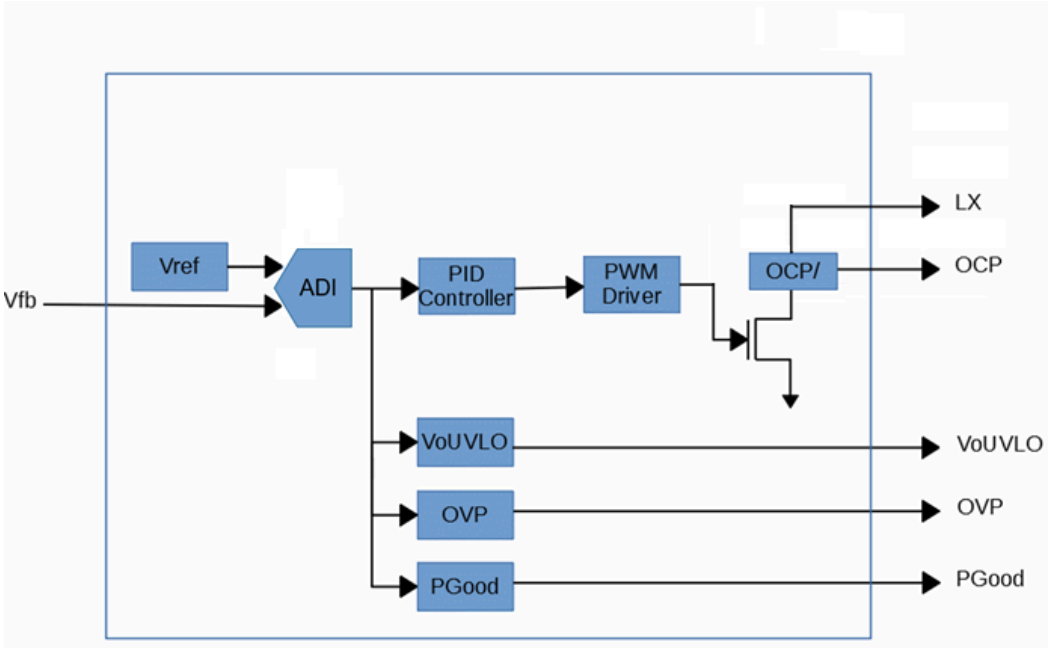
Time = 100 ms / div

Theory of Operation

The C150_B Asynchronous Buck Regulator with integrated MOSFET operates in Peak Current Mode by comparing the V_{OUT} feedback voltage, Vfb, with a programmable reference, Vref to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the LX MOSFET switch as shown in Figure 2.

The PWM driver goes high turning the LX switch "ON" to provide PVin to the LX side of an inductor, L, where $V_L = V_{LX} - V_{OUT}$. When the PWM driver goes low, the LX switch turns "OFF", and the external Schottky diode turns on "ON" providing a path for the inductor current to decrease with $V_L = - V_{OUT}$, until the next PWM turns back "ON" or the inductor currents reaches 0A. As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM cycle to optimize regulation and transient response over changing load conditions.

Figure 2. Functional Block Diagram



Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port which may be connected to a GPIO pin or a control component such as the C420 Sequencer. When EN goes high, the output voltage, V_{OUT}, will ramp up according to the Soft Start programmable preset ramp time in Parameter Settings, (default 8 ms). When EN goes low, the reference voltage will ramp down according to the Soft Start programmable preset ramp time in Parameter Settings (default 8 ms).

PGood

The power-good, PGood, digital port may be connected to a GPIO pin or a control component such as the C420 Sequencer to indicate the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time and when all Faults are cleared. PGOOD will go low for faults such as ViUVLO, VoUVLO, OVP over voltage, OCP current limit, or OTP thermal shutdown. PGOOD will also go low if EN goes low.

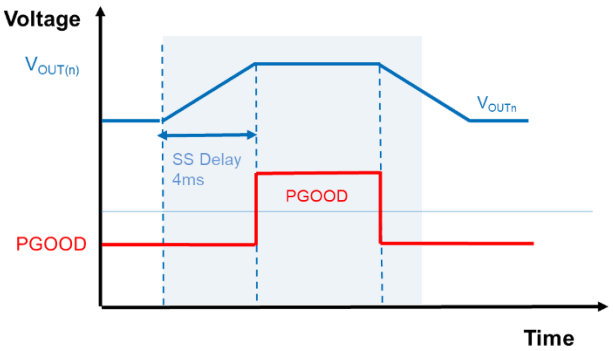


Figure 3: PGOOD Timing

Protection Features

As shown in Figure 2 the C150_B provides many protection features including ViUVLO, VoUVLO, OVP, OCP and OTP.

Input Under Voltage (ViUVLO)

The input Under Voltage Lockout, ViUVLO, indicates the input voltage status of the C150_B. ViUVLO goes high when PV_{IN} voltage is lower than the programmable preset condition and goes low when PV_{IN} voltage is greater than the programmable preset condition. PVin may be sensed on the PVin pin when the Parameter Setting is set to Internal or may be sensed on a GPIO pin connected to the PVinfb analog port when the Parameter Setting is set to External. On detection of ViUVLO, the C150_B will power down and PGOOD will go low. On ViUVLO returning high, the C150_B will restart with a new Soft Start cycle.

Global Input Under Voltage (ViUVLO)

When there are multiple power components in the design, the ViUVLO set closest to 4.1 V is used as global ViUVLO

In any design on global ViUVLO going high, all the power components will power down, until global ViUVLO goes low, then the power components will power up.

Output Under Voltage (VoUVLO)

The output Under Voltage Protection, VoUVLO, indicates the output voltage status. VoUVLO goes high when the regulator output is lower than the specified Parameter Setting. VoUVLO goes low when the output voltage is above the specified Parameter Setting. On detection of VoUVLO, the regulator will power down and PGOOD will go low. On VoUVLO returning low, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

Over Voltage Protection

The Over Voltage Protection, OVP, of the regulator indicates the output voltage status. OVP is high when the regulator output is above specified Parameter Setting. OVP is low when the output is less than the specified Parameter Setting. On detection of OVP, a regulator will skip Hi-side switch pulses until the fault condition is not present.

Over Current Protection

The Over Current Protection, OCP, of the regulator indicates the over current status. When the Output Current, $I_{OUT,}$ of the regulator is greater than 142% of the Output Current setting, the regulator will limit the Hi-side switch pulse width and OCP will go high. As Vout will then decrease, VoUVLO may go high with resulting in the regulator powering down and PGood will going low. In that case, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

OTP

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C150_B will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C150_B with a new Soft Start cycle.

Port Name Table

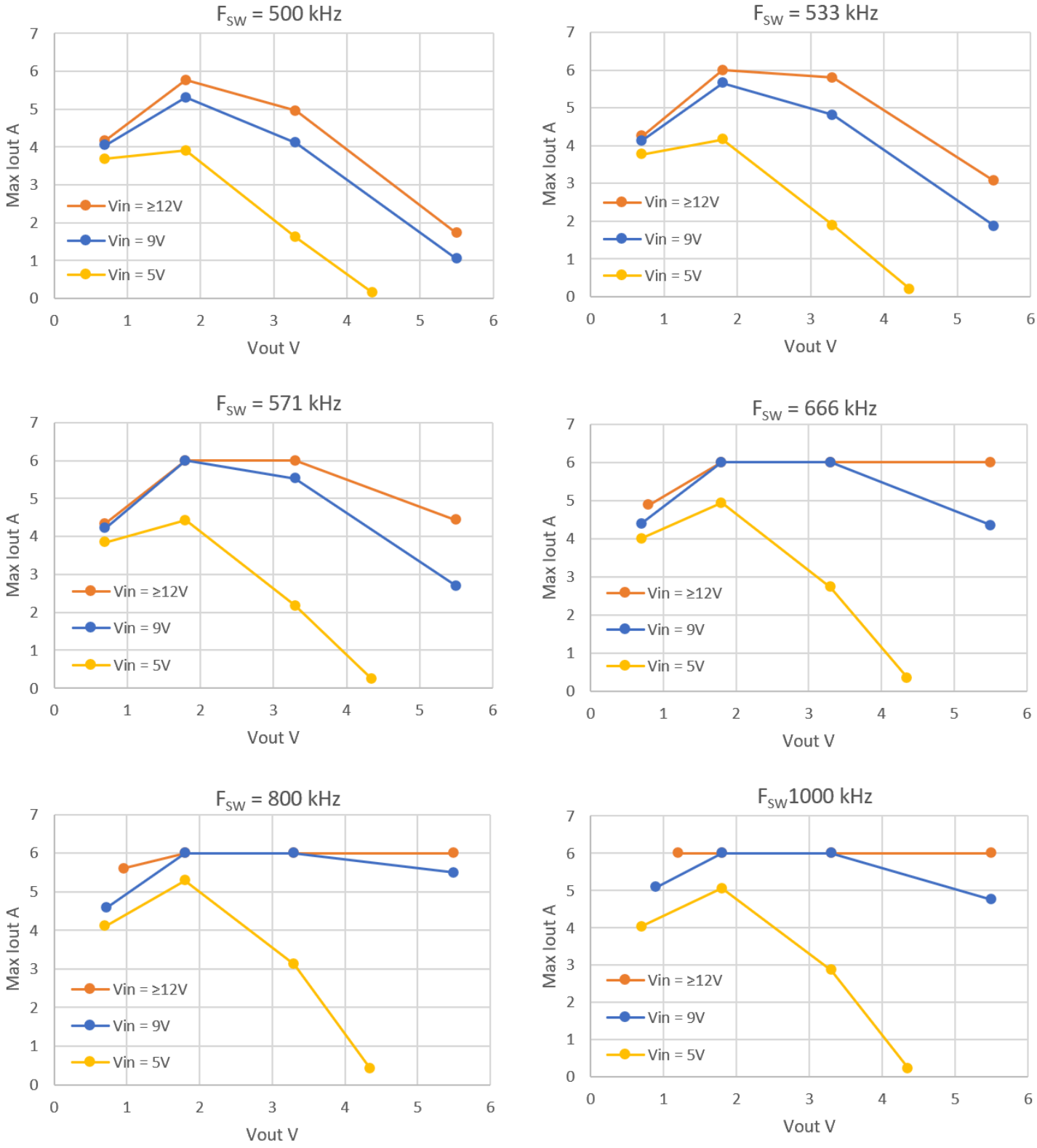
Port Name	I/O	Description
Vfb	input	Vout feedback
PVinfb	input	PVin feedback
EN	input	Enable
PGOOD	output	Power Good
OVP	output	Over Voltage Protection
OCP	output	Over Current Protection
UVLO	output	Input Under Voltage Lockout
BST_refresh	output	Boost refresh
BST	input	Boost
PVin	input	Power Voltage in
LX	output	Switch

Maximum Output Current, I_{OUT}

The maximum output current, I_{OUT}, is 6 A or less, depending on switching frequency, F_{SW}, input voltage, V_{IN}, and output voltage, V_{OUT}, as depicted in the charts below.

When selecting V_{OUT} and V_{IN}, using WebAmP tools, these maximum values are automatically selected.

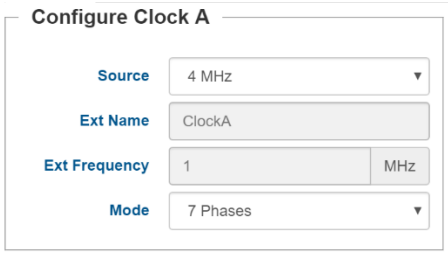
Figure 4 Maximum Output Current, I_{OUT}



Parameter Settings

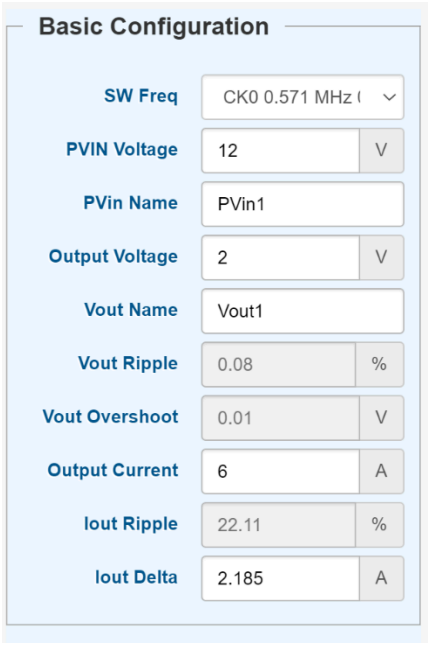
Project Settings

In Settings menu, configure clock settings to the desired switch frequency, F_{SW}. For example, to generate 571 kHz choose 4 MHz and divide by 7 phases.



Basic Configuration

Default parameters may be changed per user requirement.



Vout Ripple is computed as follows:

$V_{OUTripple}$ = Iripple/(8*Cout*Fsw)

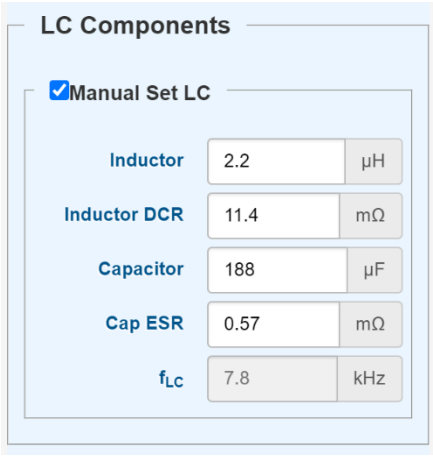
LC Component Selection

Default values for Inductance, L, and output capacitance, Cout, are computed as follows:

$L = (V_{IN}-V_{OUT})*V_{OUT} / (V_{IN}*Fsw*Iripple)$

$Cout = Ioutdelta^2*L / (2*V_{OUT}*Vos)$

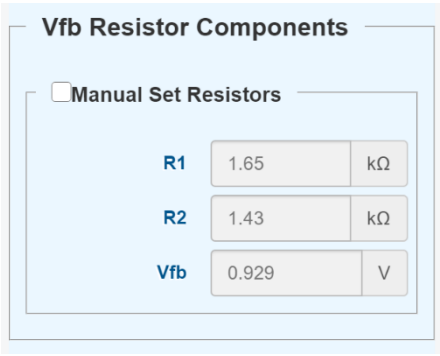
Inductor and Capacitor values may be changed by checking Manual Set LC or selecting the BoM tab where manufacturers part numbers may be selected. For example, choose L = 2.2 µH, C_{OUT} = 188 µF.



Vfb Resistor Components

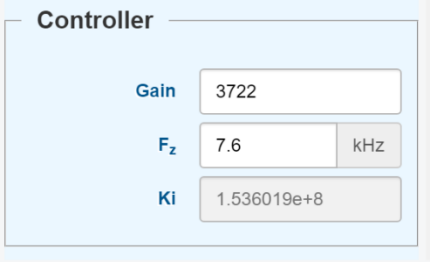
Feedback divider resistors R1 and R2 default to 0.392 kΩ and 1.43 kΩ. The resistor divider ratio is computed to select 1% resistor values for both R1 and R2.

$$Vfb = Vout * R2/(R2 + R1)$$

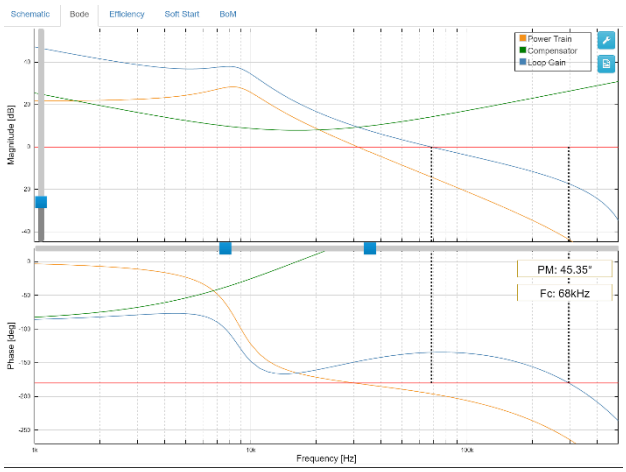


Controller

The controller compensation memory block provides PI compensation of error signals using the integrated compensation logic without external passives or an arithmetic unit. The user can adjust a bandwidth, a gain, and a phase margin of the compensation logic. For example, a user can interactively adjust the gain and the gains Fz as shown below to effectively adjust the derivative and integral gains Kd and Ki as well as the bandwidth and the phase margin.



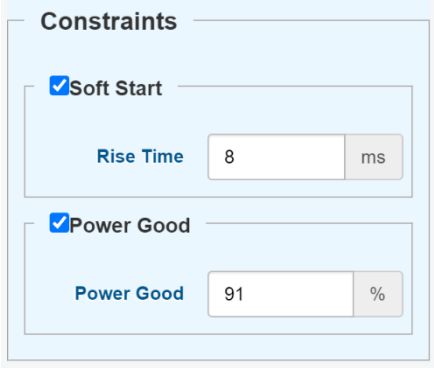
Gain and Fz are chosen to provide best Phase Margin and Crossover Frequency, Fc, as adjusted in the Bode Plot shown below:



Gain, Fz is chosen to provide best Phase Margin and Crossover Frequency, Fc.

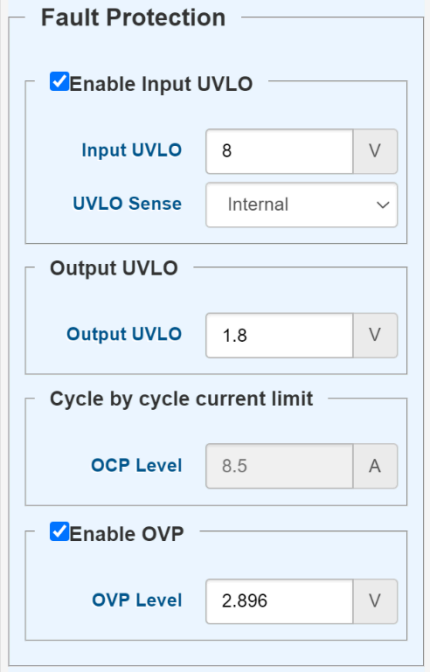
Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good ranges 59% to 100% and default is 85%.



Fault Protection

Input voltage Under Voltage Lockout, ViUVLO, indicates the input voltage status greater or less than a programmable preset condition. Output voltage Under Voltage Lockout, VoUVLO, indicates the output voltage status greater or less than programmable preset condition. Over Voltage Protection, OVP, indicates output voltage status greater or less than the programmable preset condition. Over Current Protection, OCP, indicates the output over current greater or less than the programmable preset condition. Over Temperature Protection, OTP, indicates thermal shutdown has occurred. (set to 125°C).



Power Component Version Table

Power Component Name	Description
C150_B_1_0	First Version B
C150_A_2_0	Enhanced high current support for both load transient and DC operation up to 6A
C150	First Version

C150_B Resource Usage

Circuit Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	1
Number of AnD_SIM_Protect	1
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	6
Number of AnD_ATC_IO	2
Number of AnD_ATC_Comp	2
Number of AnD_PMT	3
Number of AnD_CM_PID	2
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phs_Cnt	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	11
Number of AnD_DFF	29
Number of LUT4	93

Resource Usage...

io	2 used	(Capacity 24)
clb	13 used	(Capacity 64)
cm	2 used	(Capacity 8)
pmt	3 used	(Capacity 16)
sim	1 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	4 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	93 used	(Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	26
AnD_DFFN	4

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	2
AnD_Nref_dyn	1
AnD_Nref_fix	3
AnD_PMT	3
AnD_SIM_Protect	1
AnD_SIM_SW	1
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C150_B power components.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, InAmp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

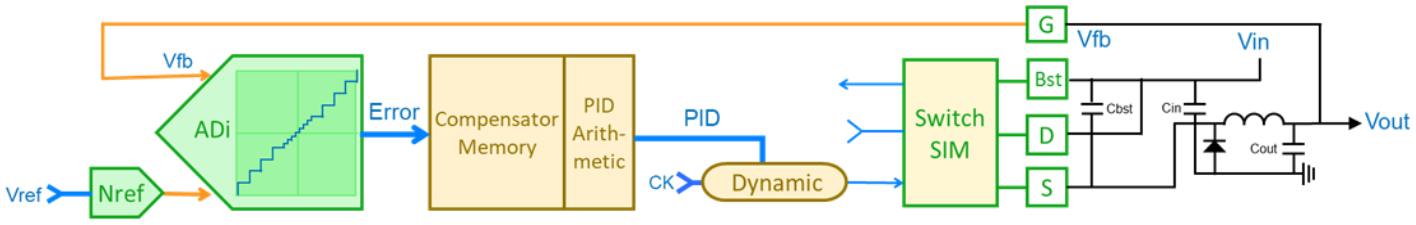
Scalable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ for a single SIM

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, Drain voltage or current and Analog Fabric including programmable references (Nrefs).

Figure 4: AmP Blocks and Resources Example - PWM Asynchronous Buck, Current Mode Switching Regulator



Additional Resources

- AnDAPT AmP Platform B datasheet

Revision History

Date	Revision
06/19/2024	Update application diagram to include BST resistor
1/24/2024	OVP, VoUVLO, Pgood max values updated to 320 mV in EC table
12/17/2022	Adjustable output voltage with down to 2.4 mV resolution changed to 2.5 mV resolution
06/09/2022	Updated Input Shutdown current (PV_{IN}) and Input Quiescent current (V_{IN})
06/09/2022	Updated max PVIN to 14V
07/13/2020	Platform B, Revision B
09/20/2019	Added C710_A_2_0, Increased performance up to 6A
04/12/2019	Preliminary release

AnDAPT

On-Demand Power Management

www.AnDAPT.com

Trademarks