PWM Synchronous Buck, Voltage Mode

Power Component: C200, I200

Product Description

The C200 Power Component is a customizable, high-output-current PWM Synchronous Buck, Voltage Mode Switching Regulator. Combine the C200 component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management device. The I200 Power Component includes the C200 Synchronous Buck and extends it with I2C communication for dynamic voltage scaling, and optional current telemetry.

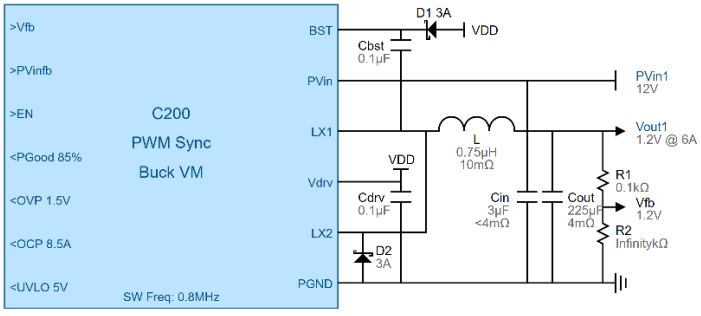
Features

- PWM, voltage mode, point-of-load (POL) regulator
- Maximum output current: Defined by selected device 1A=AmP8D1, 3A=AmP8D3, 6A=AmP8D6
- PV_{IN}: 3.0 to 13.2 V, V_{OUT}: 0.6V to 5.5V
- Adjustable output voltage with down to 2.4 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 30mΩ
- 1% typical load regulation
- Efficiency up to 93%
- Internal single pole compensator minimizes external part count
- Adjustable switching frequency
- Additional capabilities – see I200, P200
- Adaptable stability, bandwidth, gain & phase margin
- Frequency synchronization: adjustable up to 2000 kHz
- Adjustable protection: Input Undervoltage Lockout, (ViUVLO), Ouput Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- Two SIM elements; integrate up to four C200 Power Components in one AmP Platform
- Included free with WebAmP™ development tool

Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing

Figure 1: C200 application schematic



Product Detail

The C200 Synchronous Buck Regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFETs (SIM) provide up to 6A output current. The maximum current is defined by the AmP device selected.

Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is either generated internally via an oscillator with selectable frequencies or provided via an external pin.

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmp development software. The C200 component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or undervoltage lockout (UVLO) condition. The threshold values are specified by the power engineer using the WebAmp tool.

The customizable soft-start and soft-stop slew rates are also specified by the power engineer using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 customizable Sequencer, by interconnecting signals EN and PGood to provide customizable dependencies and customizable delays between each sequence step.

Customizable Options

Table 1 lists the various customizable options available for the C200 Power Component. These options are set graphically in the WebAmp development software.

Table 1: C200 Customizable Options

Option	Units
Switching frequency	MHz
Input voltage*	V
Output voltage	V
Ripple, % of output voltage*	%
Overshoot, output voltage*	V
Output Current	A
Ripple, % of maximum output current*	%
Output Current Delta*	A
Output UVLO voltage	V
LC Component Manual/Auto select	On/Off
Inductor	µH
Inductor DCR	mΩ
Capacitor	µF
Capacitor ESR	mΩ
PID regulation coefficients (K_P, K_I, K_D)	
Enable OCP output to signal when overcurrent protection is triggered	On/Off
Overcurrent protection level (Read only)	A
Enable OVP output to signal when overvoltage protection is triggered	On/Off
Overvoltage protection level	V
Enable input UVLO to signal when undervoltage lockout protection is triggered	On/Off
Undervoltage lockout sense level	V
UVLO sense	Ext/Int
Soft start rise time after enable	ms
Use optional PGood output to signal “power good”	On/Off
“Power good” threshold, percentage of output	%

* to generate passive component recommendations

Advanced Capabilities and Options

Table 2 lists derivatives of the C200 component with additional capabilities plus other similar components potentially suitable for this application.

Table 2: C200 Advanced Capabilities Options

Description	Part Number
Standard Pro Series version (this component)	C200
Add I^2C bus interface for telemetry and dynamic output voltage specification	I200
Add telemetry and dynamic voltage scaling via DVS interface	P200
Single-phase buck regulator, asynchronous, PWM, current mode regulation	C150

System Characteristics

Table 3 lists the system characteristics for the C200 Power Component when implemented in an AnDAPT AmP device. “Prog” column specifies parameters that are user selectable.

Table 3: C200 System Characteristics

Parameters		Min	Typ	Max	Units	Prog
Input Drain Voltage (PV_{IN})		3		13.2	V	
Output Voltage (V_{OUT})		0.6		5.5	V	√
Output Current (I_{OUT})	D6			6	A	√
	D3			3		
	D1			1		
Switching frequency (F_{SW})				2	MHz	√
Switching frequency accuracy		-5		+5	%	
Output MOSFET switch ($R_{DS(on)}$)			30		mΩ	
Voltage Regulation			1*		%/V	
Peak efficiency (V_{IN}=5V, V_{OUT}=3.3V, F_{SW}=500kHz)			95		%	
Current Limit – OCP		0.2		8.5	A	
Overvoltage protection trip point range (OVP)				8.5	V	
Undervoltage lockout threshold range (Vout UVLO)				5.3	V	√

*1% regulation tolerance requires no voltage divider feedback.

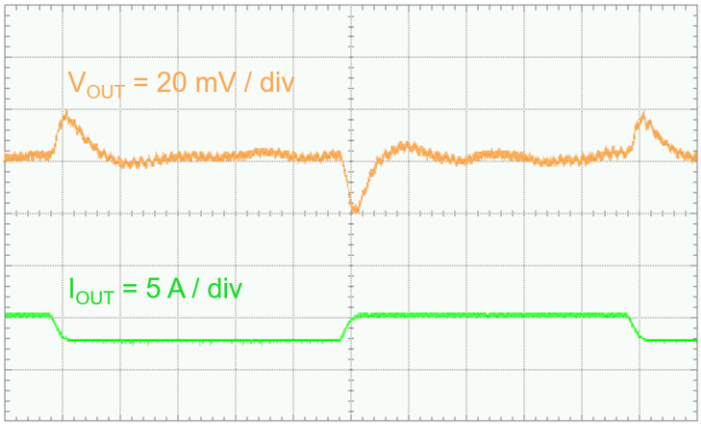
For other device specifications, see the AnDAPT AmP Platform datasheet.

Typical Characteristics

Unless otherwise specified: TA = 25°C

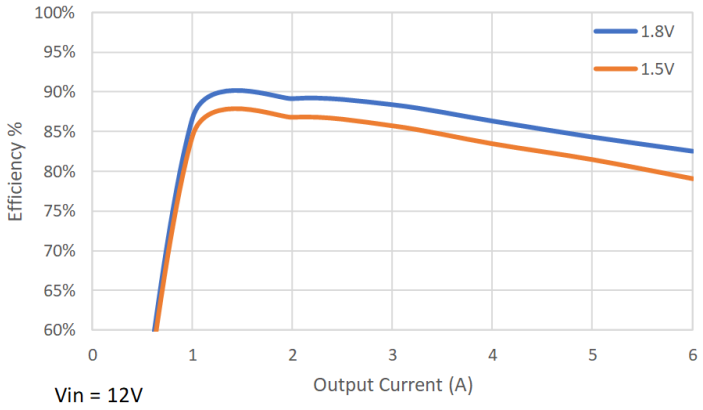
Transient Response

V_{OUT} = 1.8 V I_{OUT} step 2.5 A to 5 A



Time = 50 µs / div

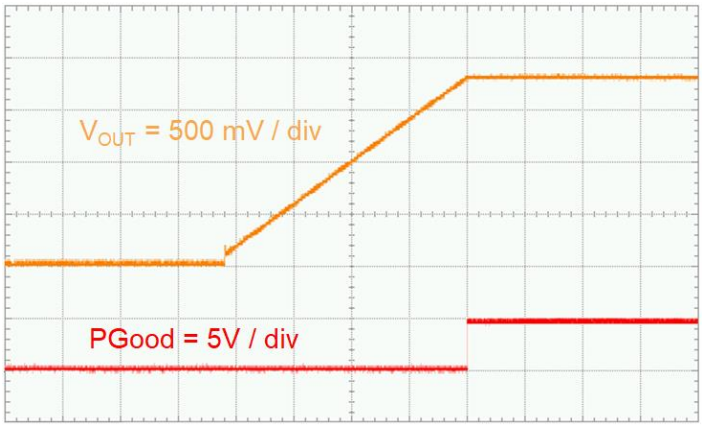
Efficiency



Vin = 12V

Soft Start

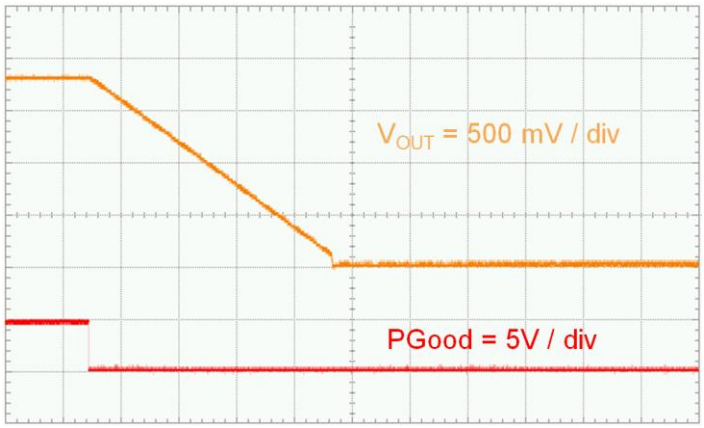
Vin = 12V, Vout = 1.8V, Iout = 2.5A



Time = 2 ms / div

Soft Stop

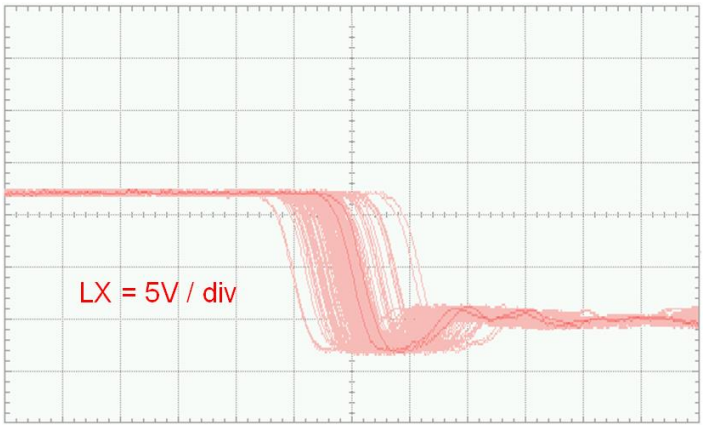
Vin = 12V, Vout = 1.8V



Time = 2 ms / div

Jitter

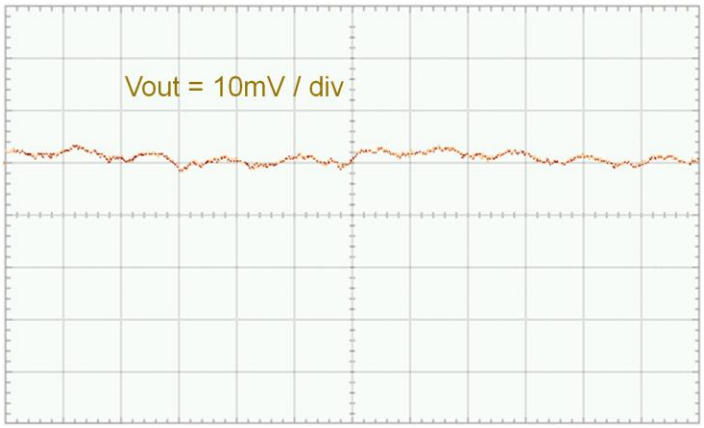
Vin = 12V, Vout = 1.8V, Iout = 2.5A



Time = 5 ns / div

Ripple

Vin = 12V, Vout = 1.8V, Iout = 2.5A



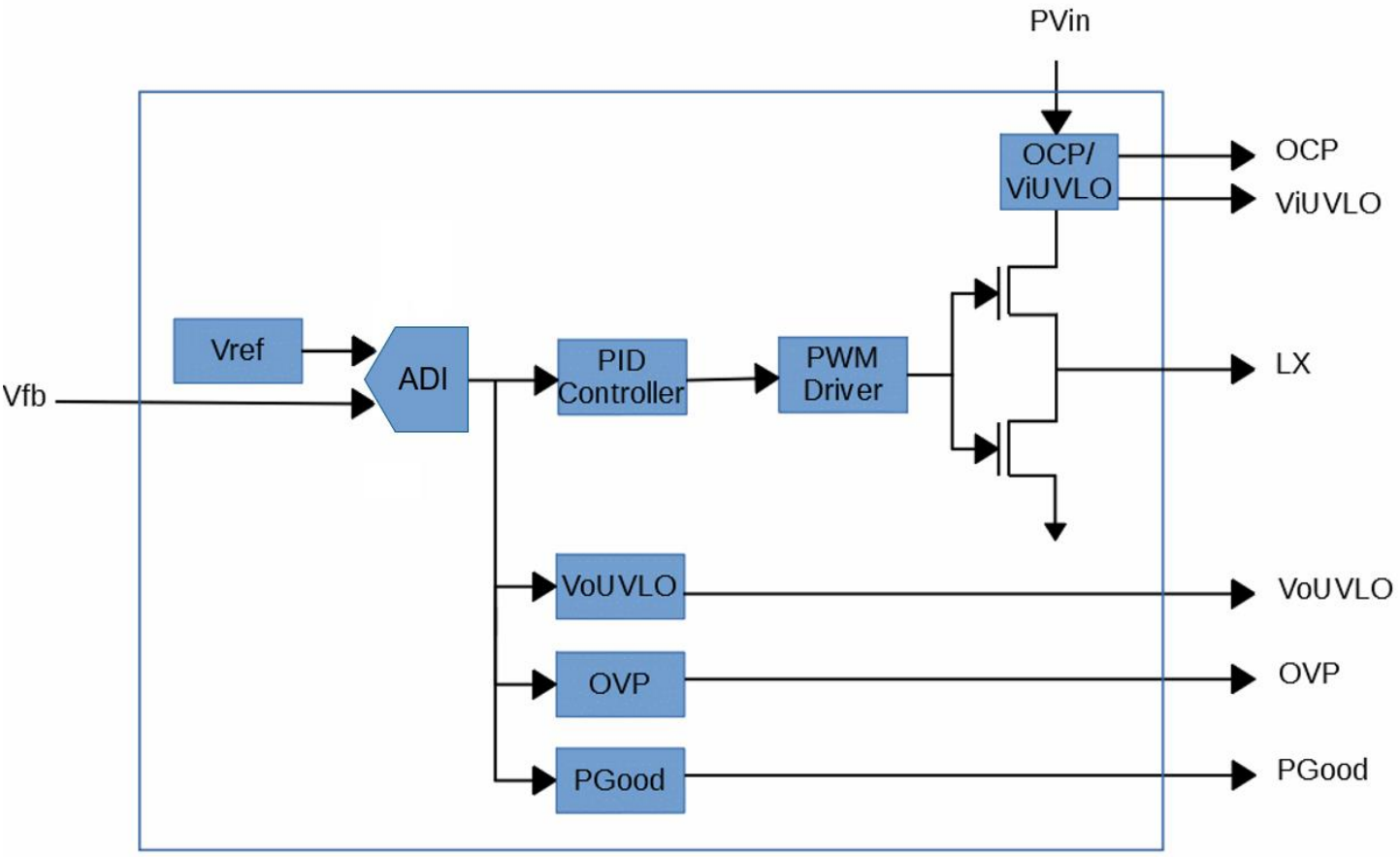
Time = 1 µs / div

Theory of Operation

The C200 Synchronous Buck Regulator with integrated MOSFETs operates in voltage mode by comparing the V_{OUT} feedback voltage, Vfb, with a programmable reference, Vref to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the Hi-side and Lo-side MOSFET switches as shown in Figure 2.

In CCM (Continuous Conduction Mode), the PWM driver goes high turning the Hi-side switch "ON" to provide PVin to the LX side of an inductor, L, where $V_L = V_{LX} - V_{OUT}$. When the PWM driver goes low, the Hi-side switch turns "OFF", and after a shoot through delay, the Lo-side switch turns "ON" providing a path for the inductor current to decrease with $V_L = - V_{OUT}$, until the next PWM turns back "ON". As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM cycle to optimize ripple, regulation, efficiency and transient response over changing load conditions.

Figure 2: Functional Block Diagram



Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port which may be connected to a GPIO pin or a control component such as the C420 Sequencer. When EN goes high or when an I2C EN command for the I200 is given, the output voltage, V_{OUT}, will ramp up according to the Soft Start programmable preset ramp time in Parameter Settings, (default 8 ms). When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start programmable preset ramp time in Parameter Settings, (default 8 ms)

PGood

The power-good, PGood, digital port may be connected to a GPIO pin or a control component such as the C420 Sequencer to indicate the output voltage regulation status. PGood goes high on power-up when the Soft Start completes and output voltage, V_{OUT}, reaches the programmable preset condition in Parameter Settings, (default 85%). PGood will go low when V_{OUT} goes below the programmable preset condition or the Enable pin (EN) is deasserted.

Protection Features

As shown in Figure 3, the C200 provides many protection features including ViUVLO, VoUVLO, OVP, OCP and OTP.

ViUVLO

The PVin voltage Under Voltage Lockout, ViUVLO, digital port may be connected to a GPIO pin or a control component such as the C430 Fault Controller to indicate the PVin voltage status. ViUVLO goes high when PVin voltage is higher than the programmable preset condition in Parameter Settings, (default 5V). ViUVLO goes low when PVin voltage is less than the programmable preset condition in Parameter Settings, (default 5V). PVin may be sensed on the PVin pin when the Parameter Setting is set to Internal or Internal or may be sensed on a GPIO pin connected to the PVinfb analog port when the Parameter Setting is set to External. On detection of ViUVLO, the C200 will power down and PGood will go low. On ViUVLO returning low, the C200 will restart with a new Soft Start cycle.

VoUVLO

The output voltage Under Voltage Lockout, VoUVLO, digital port may be connected to a GPIO pin or a control component such as the C430 Fault Controller to indicate the output voltage status. VoUVLO goes high when output voltage, V_{OUT}, is higher than the programmable preset condition in Parameter Settings, (default 75% of V_{OUT}). VoUVLO goes low when output voltage, V_{OUT}, is less than the programmable preset condition in Parameter Settings, (default 75% of V_{OUT}). On detection of VoUVLO, the C200 will power down and PGood will go low. On VoUVLO returning low, an EN cycling low-to-high, will restart the C200 with a new Soft Start cycle.

OVP

The Over Voltage Protection, OVP, digital port may be connected to a GPIO pin or a control component such as the C430 Fault Manager to indicate the output voltage over voltage status. OVP goes high when output voltage, V_{OUT}, is higher than the programmable preset condition in Parameter Settings, (default 25% above Vout). OVP goes low when output voltage, V_{OUT}, is less than the programmable preset condition in Parameter Settings, (default 25% above V_{OUT}). On detection of OVP, the C200 will skip Hi-side switch pulses until OVP returns low.

OCP

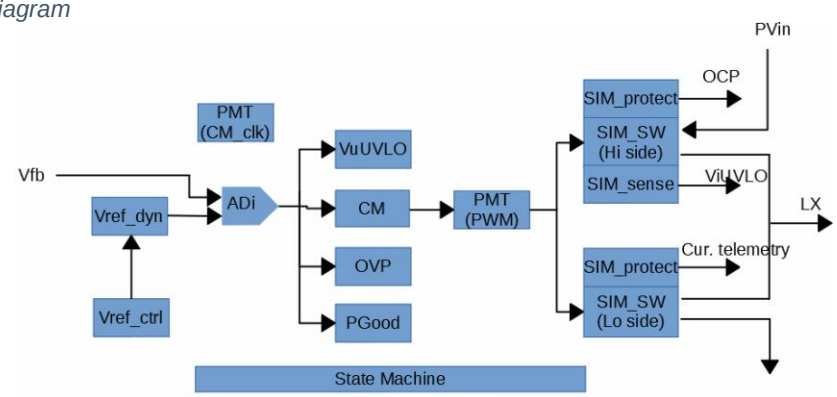
The Over Current Protection, OCP, digital port may be connected to a GPIO pin or a control component such as the C430 Fault Manager to indicate the output over current status. When I_{OUT}, is greater than 140% of the Output Current setting, the C200 will limit the Hi-side switch pulse width and OCP will go high. If I_{OUT} is greater than 165% of Output Current setting, the C200 will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the C200 with a new Soft Start cycle.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C200 will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C200 with a new Soft Start cycle.

Port Name Table

Port Name	I/O	Description
Vfb	input	Vout feedback
PVinfb	input	PVin feedback
EN	input	Enable
PGood	output	Power Good
OVP	output	Over Voltage Protection
OCP	output	Over Current Protection
UVLO	output	Under Voltage Lockout
BST	input	Boost
PVin	input	Power Voltage in
LX1	output	Switch
Vdvr	input	Driver Voltage
LX2	output	Switch
PGND	input	Power Ground

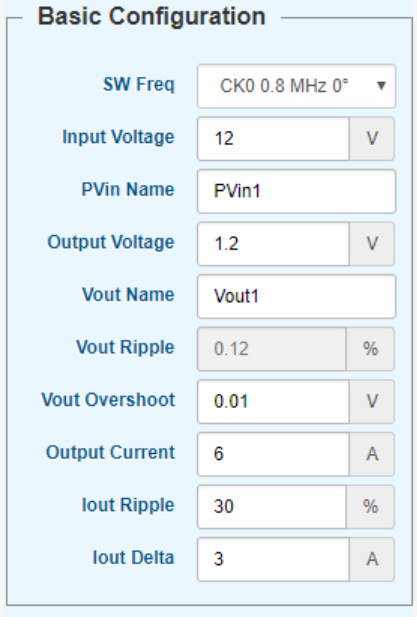
Figure 3: Structural Block Diagram



Parameter Settings

Basic Configuration

Default parameters may be changed per user requirement.



Vout Ripple is computed as follows:

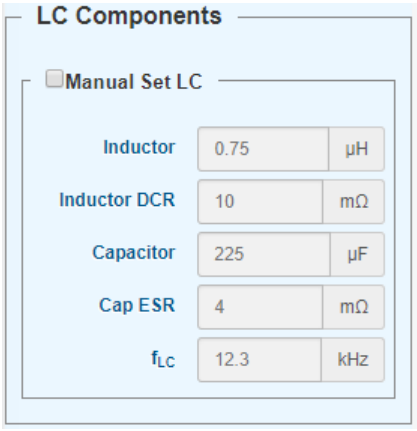
$V_{OUTripple}$ = Iripple/(8*Cout*Fsw)

LC Component Selection

Default values for Inductance, L, and output capacitance, Cout, are computed as follows:

L = (Vin-Vout)*Vout / (Vin*Fsw*Iripple)

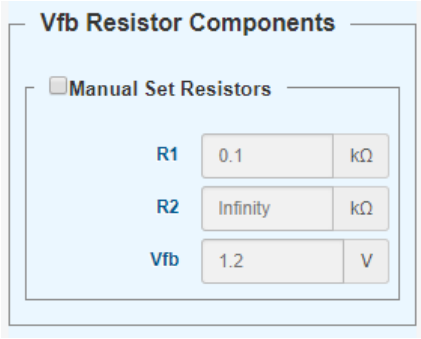
Cout = Ioutdelta^2*L / (2*Vout*Vos)



Inductor and Capacitor values may be changed by checking Manual Set LC or selecting the BoM tab where manufacturers part numbers may be selected.

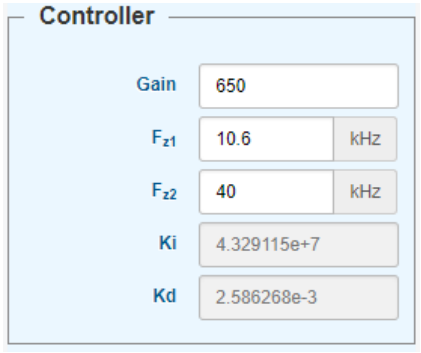
Vfb Resistor Components

Feedback divider resistors R1 and R2 default to 100 Ω and open (infinity). When Vout is larger than 2.3V, a resistor divider ratio is computed to select 1% resistor values for both R1 and R2.

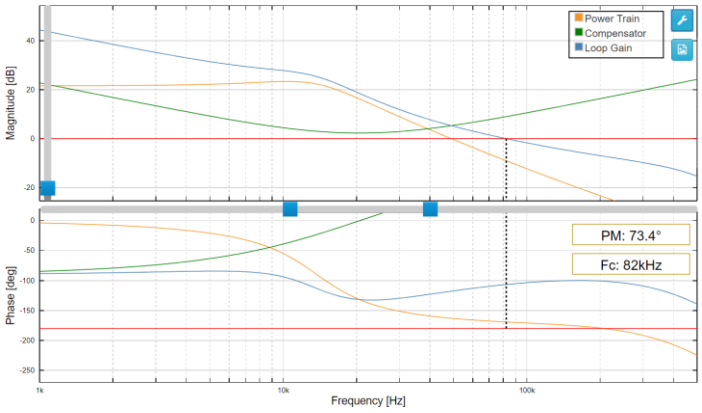


Controller

The controller compensation memory block provides PID compensation of error signals using the integrated compensation logic without external passives or an arithmetic unit. The user can adjust a bandwidth, a gain, and a phase margin of the compensation logic. For example, a user can interactively adjust the proportional gain Kp and the gains Fz1 and Fz2 shown below to effectively adjust the derivative and integral gains Kd and Ki as well as the bandwidth and the phase margin.

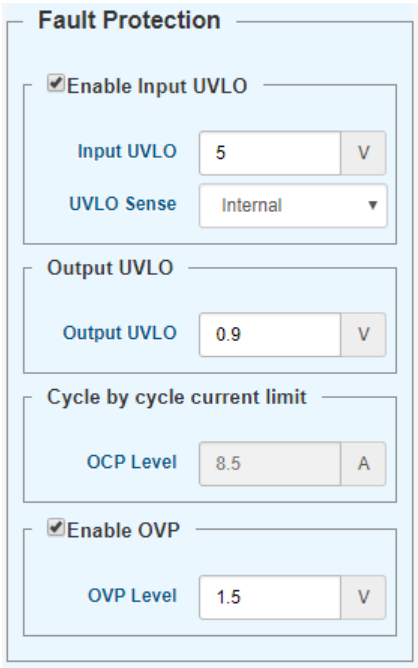


Gain, Fz1 and Fz2 are chosen to provide best Phase Margin and Crossover Frequency, Fc, as adjusted in the Bode Plot shown below:



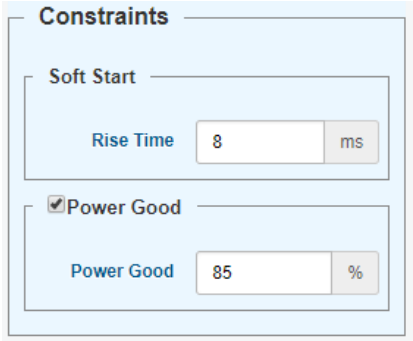
Fault Protection

Input voltage Under Voltage Lockout, ViUVLO, indicates the input voltage status greater or less than programmable preset condition (default 5V). Output voltage Under Voltage Lockout, VoUVLO, indicates the output voltage status greater or less than programmable preset condition (default 75% of V_{OUT}). Over Voltage Protection, OVP, indicates output voltage status greater or less than the programmable preset condition (default 25% above Vout). Over Current Protection, OCP, indicates the output over current greater or less than the programmable preset condition (default 8.5A). Over Temperature Protection, OTP, indicates thermal shutdown has occurred. (set to 125°C).

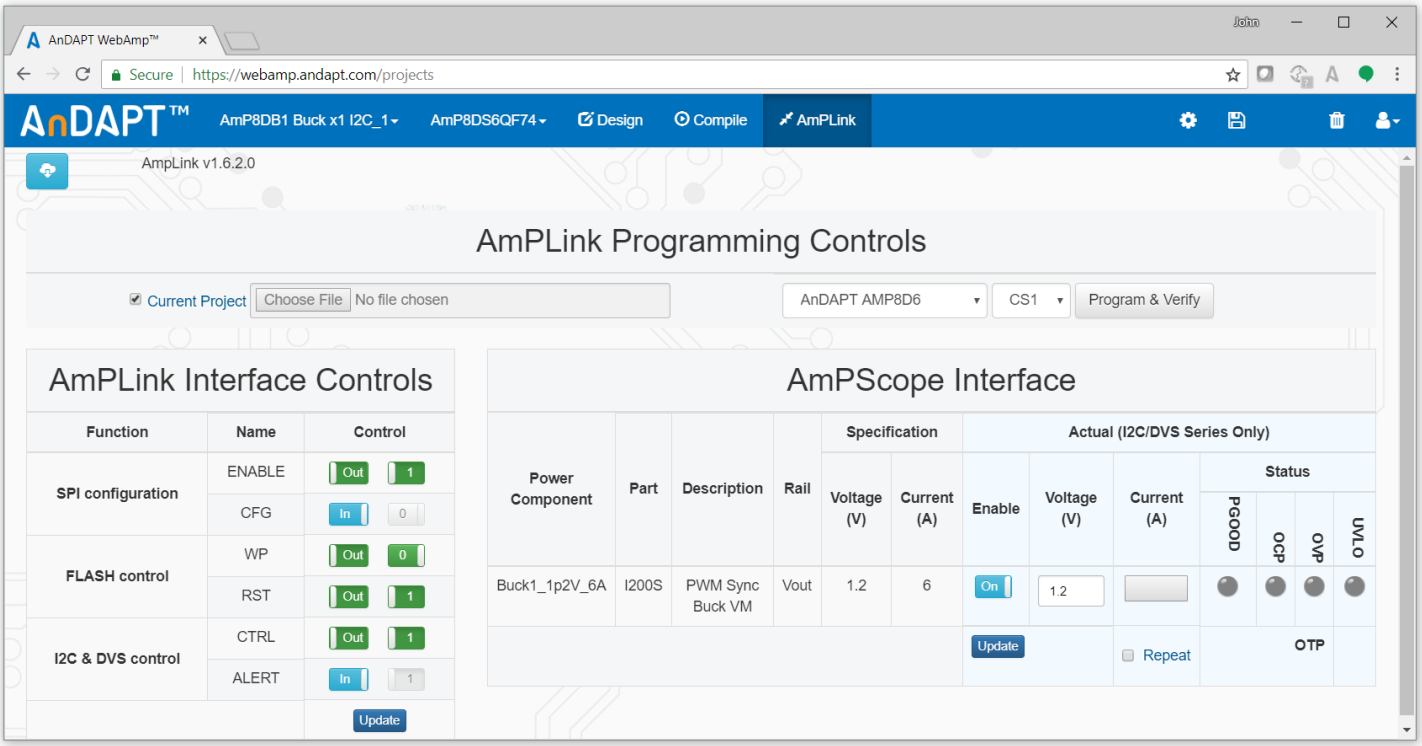


Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good ranges 59% to 100% and default is 85%.



I2C AmpScope Interface



The I200 Power Component is a version of the C200 with additional telemetry capabilities provided by the I2C interface including:

- Fault status for PGOOD, OCP, OVP and UVLO
- Current Measuring
- Voltage Margining Vout setting

The I2C commands are summarized in Table 4
Note that the first I2C series Power Component will automatically insert one I480 Telemetry Interface Power Component with additional SDA and SCL signal pins. Additional I2C series Power Components will not insert an I480 as one I480 supports multiple I2C series Power Components.

The I2C AmpScope Interface above provides a user interface to read and write the I2C commands for all the I2C series Power Components contained in the AmP device.

Table 4:I2C Register Map

Address*	Register Name	Comment	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x08	STATUS	Status & Iout hi bits	Iout[9]	Iout[8]	0	0	UVLO	OVP	OCP	Pgood
0x09	Iout	Iout low bits	Iout[7]	Iout[6]	Iout[5]	Iout[4]	Iout[3]	Iout[2]	Iout[1]	Iout[0]
0x0A	Vout	Vout low bits	Vout[7]	Vout[6]	Vout[5]	Vout[4]	Vout[3]	Vout[2]	Vout[1]	Vout[0]
0x0B	Vout	Vout Hi bits and control	0	0	0	0	amp_ctrl	reg-ctrl**	Vout[9]	Vout[8]

* Address increments by 8 for additional I2C POLs, for example next I2C POL addresses are: 0x10, 0x11, 0x12, 0x13.
** reg_ctrl: If '1' writes all 10-bits of Vout to the component
*** Slave Address can be set in I480 Module

I2C Command Summary

For EN and Vout Write Only Registers:

- [Start] [Slave_Add*** + Write] [Register_Add*] [VOUTCMD_1] [VOUTCMD_0] [Stop]

For STATUS and IOUT Read Only Registers:

- [Start] [Slave_Add + Write] [Register_Add]
- [Start_Repeat] [Slave_Add + Read] [STATUS-REGISTERS] [IOUT] [STOP]

For Device ID, Rev, and CS Read Only Registers:

- [Start] [Slave_Add + Write] [0x00]
- [Start_Repeat] [Slave_Add + Read] [Device_ID] [Device_REV] [Device_CSUM_1] [Device_CSUM_0]

C200 Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	2
Number of AnD_SIM_Protect	2
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	11
Number of AnD_ATC_IO	6
Number of AnD_ATC_Comp	2
Number of AnD_PMT	3
Number of AnD_CM_PID	1
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	15
Number of AnD_DFF	27
Number of AnD_ADCR	10
Number of LUT4	111

Resource Usage...

io	6 used	(Capacity 24)
clb	16 used	(Capacity 64)
cm	1 used	(Capacity 8)
pmt	3 used	(Capacity 16)
sim	2 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	2 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	121 used	(Capacity 512)

Components Stats...

$techmap\OTP_fuse_module

AnD_DFF	1

$techmap\buck_1_1_v_2_6_a

AnD_DFF	26
AnD_DFFN	15

OTP_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

buck_1_1_v_2_6_a

AnD_ADCR	10
AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	1
AnD_Nref_dyn	1
AnD_Nref_fix	3
AnD_PMT	3
AnD_SIM_Protect	2
AnD_SIM_SW	2
AnD_SIM_Sense	1

I200 Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_I2C_Phy	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	2
Number of AnD_SIM_Protect	2
Number of AnD_SIM_Sense	2
Number of AnD_Analog_IO	11
Number of AnD_ATC_IO	8
Number of AnD_ATC_Comp	2
Number of AnD_PMT	4
Number of AnD_CM_PID	1
Number of AnD_CM_RAM_256x18	1
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phase_Count	2
Number of AnD_PTG_GBUF	2
Number of AnD_PTG_OSC	2
Number of AnD_DFFN	33
Number of AnD_DFF	75
Number of AnD_ADCR	10
Number of LUT4	213

Resource Usage...

io	8 used	(Capacity 24)
clb	28 used	(Capacity 64)
cm	2 used	(Capacity 8)
pmt	4 used	(Capacity 16)
sim	2 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	2 used	(Capacity 4)
ptg	2 used	(Capacity 2)
uLogic	223 used	(Capacity 512)

Components Stats...

$techmap\OTP_fuse_module

AnD_DFF	1

$techmap\buck_1_1_v_2_6_a

AnD_DFF	64
AnD_DFFN	33

$techmap\i_2_c_1

AnD_DFF	10

OTP_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

buck_1_1_v_2_6_a

AnD_ADCR	10
AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	1
AnD_Nref_dyn	1
AnD_Nref_fix	3
AnD_PMT	4
AnD_SIM_Protect	2
AnD_SIM_SW	2
AnD_SIM_Sense	2

i_2_c_1

AnD_CM_RAM_256x

C200 Resource Utilization

Resource Utilization			
Primitive	**Used**	**Total**	**Usage**
Temp_Sensor	1	1	1.00
ADi_dual	1	4	0.25
SIM	2	8	0.25
I/Os	6	24	0.25
Comparator	2	8	0.25
PMT	3	16	0.19
CM	1	8	0.13
Nref	5	24	0.21
LUT4	107	512	0.21
uLogic	117	512	0.23
clb	15	64	0.23

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C200 / I200 power components.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, InAmp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

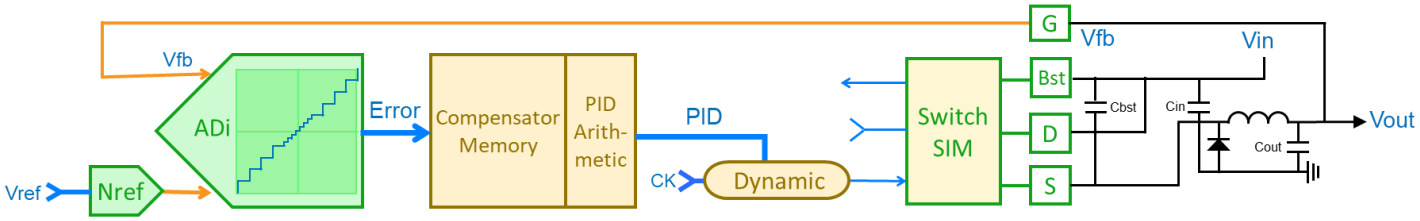
Scaleable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, Drain voltage or current and Analog Fabric including programmable references (Nrefs).

Figure 4: PMIC Blocks and Resources Example - Buck Regulator



Additional Resources

- AnDAPT AmP Platform datasheet

Revision History

Date	Revision
04/08/2019	PGood power-up go high/low conditions updated
09/10/2018	Updated to V180910
06/11/2018	Preliminary release

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On-Demand Power Management

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Trademarks