VTT Terminator

Power Component: C210_B

Product Description

The C210_B Power Component is a customizable voltage-mode PWM synchronous buck regulator to track another voltage rail and produce half its output voltage while both sourcing or sinking currents. These two rails are typically the DDR memory VDDQ and VTT respectively. The C210_B is powered from a voltage reference, the output of a C200_B, or a C220_B (High Current) synchronous buck regulator located in the same AmP device, to enable accurate DC and dynamic tracking.

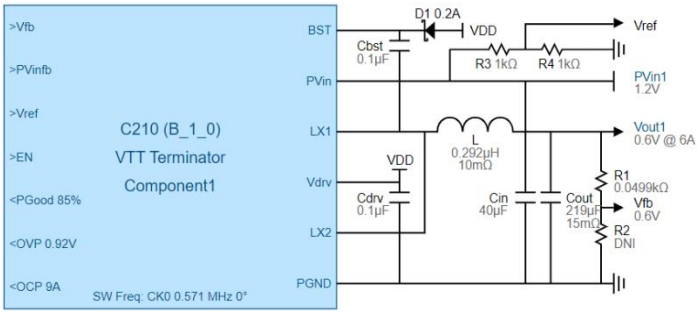
Features

- PWM, voltage-mode, point-of-load (POL) regulator
- Input voltage, PV_{IN}: 0.8 to 11V, V_{OUT}: 0.4V to 5.5V
- Integrated MOSFETs, $R_{DS(on)}$: 30mΩ
- 1% typical accuracy
- Efficiency up to 90%
- Internal Compensation
- Adjustable bandwidth, gain and phase margin
- Adjustable switching frequency
- Frequency synchronization with selectable phase shift: adjustable up to 1 MHz
- Adjustable protection: Ouput Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Pre-bias startup
- Uses two of the available power MOSFETs

Applications

DDR memory VTT power rail

Figure 1: C210_B application schematic



Product Details

The C210_B synchronous buck regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated low-Rdson MOSFETs provide up to 6A output current. A digital feedback loop subtracts the output voltage from a divide-by-two resistor voltage divider on the power rail (VDDQ) that it is tracking. The C210_B will track the VDDQ rail and produce half the voltage, as the latter starts up, shuts down, or is perturbed by a load transient. The VDDQ is typically provided by a C200 synchronous buck or a C220 high-current synchronous buck regulator power component.

Pulse-width modulated (PWM), voltage-mode control is implemented using digital PID compensation. The switching frequency is generated internally via an oscillator with selectable frequencies and phase angles relative to other power components on the device.

The output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmP development software. The C210_B component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), or overcurrent (OCP) condition. The threshold values are specified using the WebAmP tool.

Recommended Operating Conditions

Over operating free-air temperature range

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	0.8		11	V
I_{OUT}	I_{OUT} Output Current Maximum			6	A

Electrical Characteristics Buck Converters

PV_{IN}=1.8V, V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT})		0.4		5.5	V
Voltage Regulation	Including load line and temperature variation, V_{IN} range: 6V to 14V	-1		+1	%
Switching frequency (F_{SW})		300		1143	kHz
Switching frequency accuracy		-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$)			30		mΩ
Peak efficiency	V_{IN}=1.8V, V_{OUT}=0.9V, F_{SW}=571kHz I_{OUT}=0.9A		94		%
Efficiency	V_{IN}=1.8V, V_{OUT}=0.9V, F_{SW}=571kHz, I_{OUT}=3A		86		%
Input Shutdown current (V_{IN})	EN = Low		1.3		mA
Input Shutdown current (PV_{IN})			0.1		mA
Input Quiescent current (V_{IN})	EN = High, I_{OUT} = 0A, Fsw = 571 kHz, V_{OUT} = 0.9V		5.9		mA
Input Quiescent current (PV_{IN})			5		mA
PROTECTION					
OCP, Over Current Protection (% I_{OUT})			140		%
OVP, Overvoltage Protection trip point range (relative to Parameter Setting)		+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Parameter Setting)		-100		-432	mV
Power Good threshold (relative to Parameter Setting)		-100		-432	mV

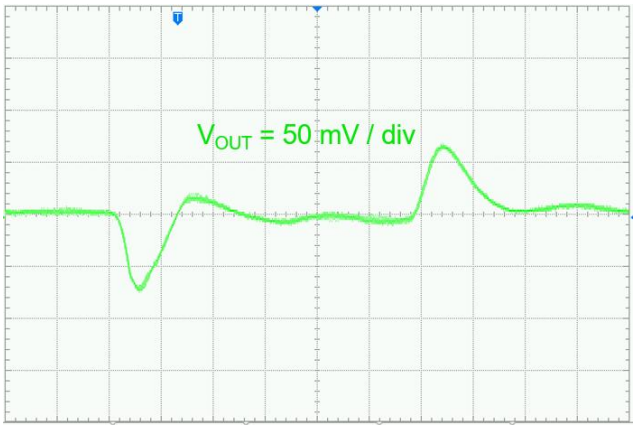
* Parameters shaded in green are user customizable as set in WebAmP development software

Typical Characteristics

Unless otherwise specified: TA = 25°C

Transient Response

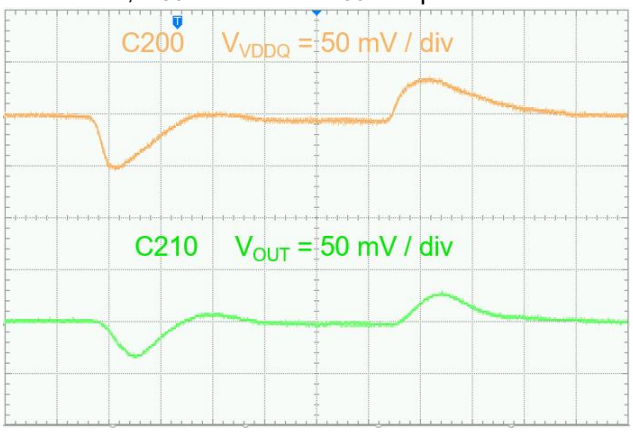
Vin = 1.8V, V_{OUT} = 0.9 V I_{OUT} step 3 A to 6A on C210



Time = 50 µs / div

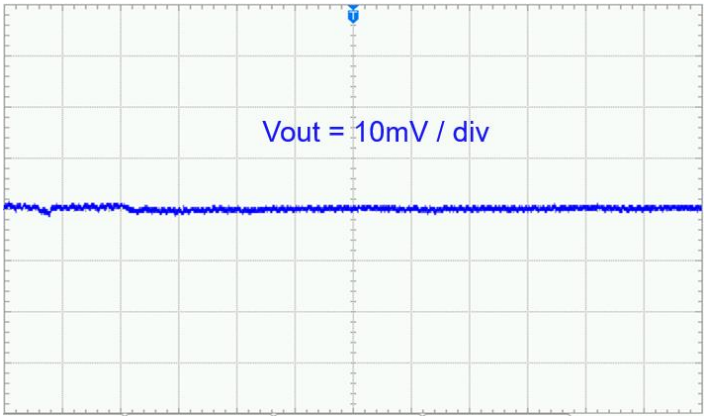
Transient Response

Vin = 1.8V, V_{OUT} = 0.9 V I_{OUT} step 3 A to 6A on VDDQ



Ripple no load

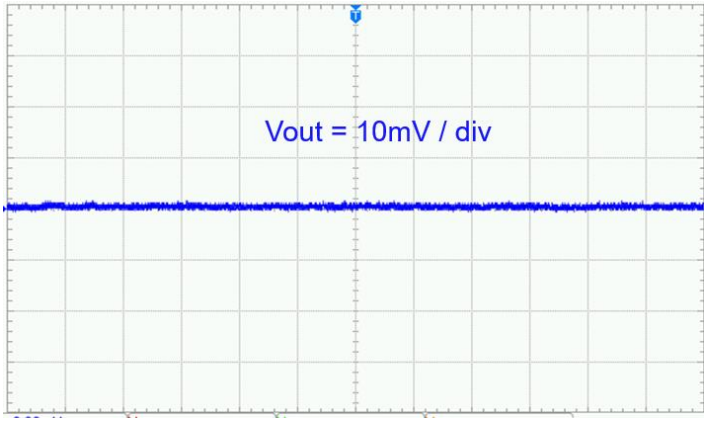
Vin = 1.2V, Vout = 0.6V, Iout = 0A



Time = 1 ms / div

Ripple full load

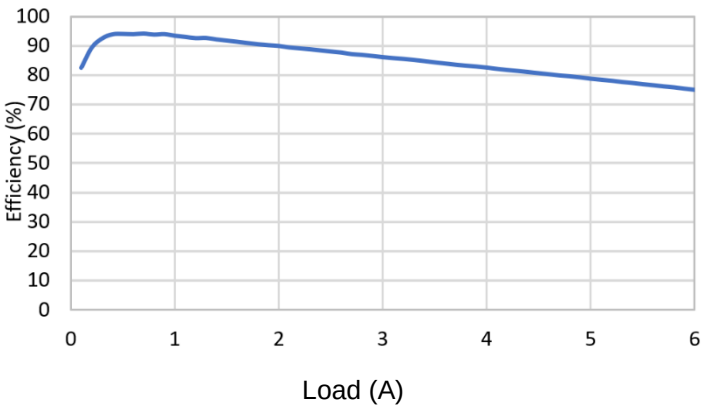
Vin = 1.2V, Vout = 0.6V, Iout = 1.5A



Time = 1 ms / div

Efficiency

Vout = 0.9V

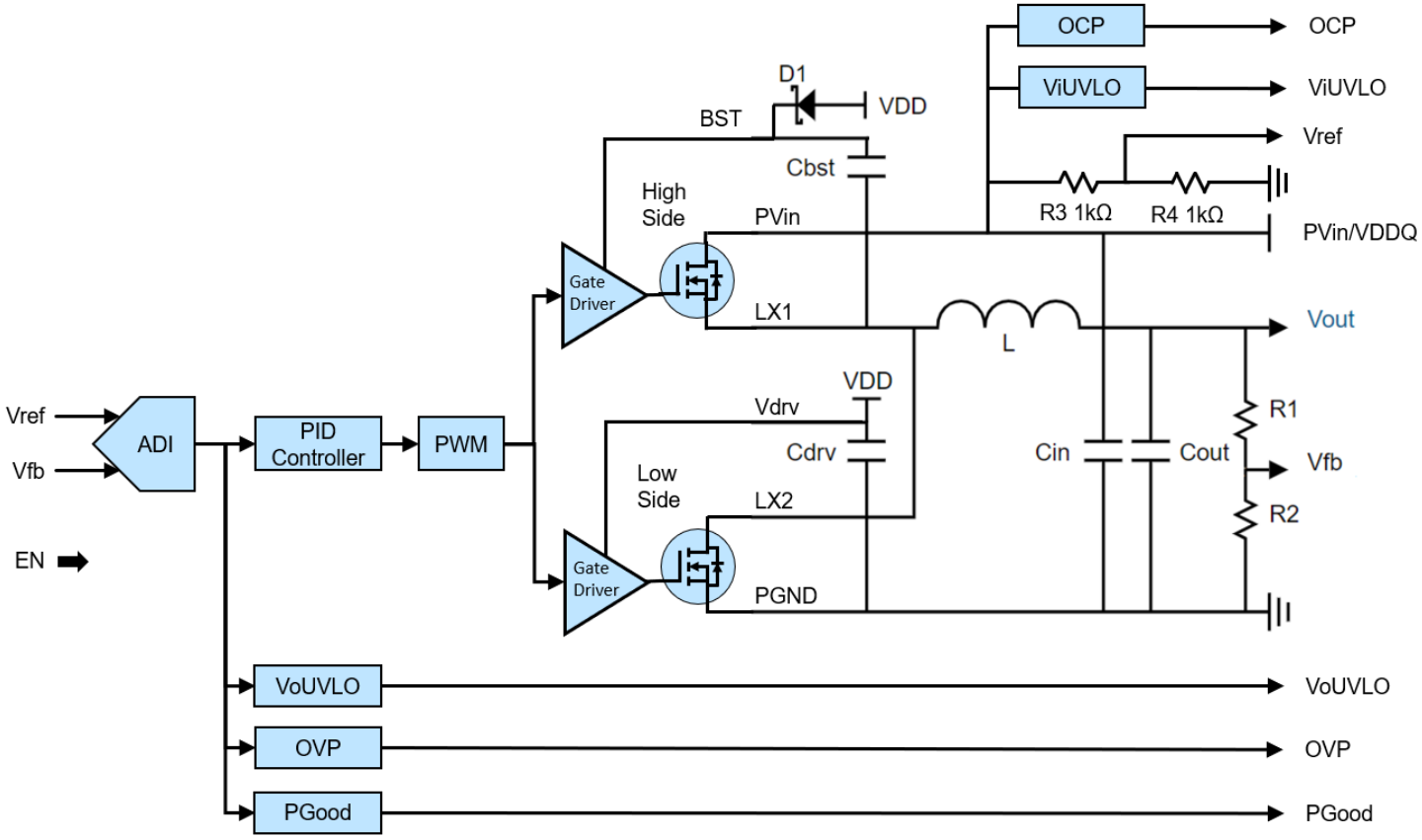


Theory of Operation

The C210_B synchronous buck regulator with integrated MOSFETs operates in PWM voltage mode. It subtracts the digitized Vref input which is connected to a voltage divider which halves the PVin/VDDQ voltage, from the digitized V_{OUT} voltage. The resulting digital error voltage feeds a PID controller whose output determines the MOSFETs' duty cycle. The C210_B output thus produces half the VDDQ/Vref voltage, tracking even rapid voltage perturbations on the VDDQ due to load transients on it. See Figure 2

The C210_B always runs in CCM (Continuous Conduction Mode). When the PWM driver goes high, it turns the Hi-side switch "ON" to provide VDDQ to the LX side of an inductor, L, where $V_L = V_{LX} – V_{OUT}$, causing its current to ramp up. When the PWM driver goes low, the Hi-side switch turns "OFF", and after a short shoot-through-prevention delay time, the Low-side switch turns "ON" providing a path for the inductor current to decrease with voltage $V_L = - V_{OUT}$, until the next PWM turns back "ON". At low load currents this inductor current can reverse polarity. As this cycle repeats, the PID algorithm regulates V_{OUT} by updating the PWM duty cycle at every cycle to maintain regulation, with fast transient response to changing load conditions.

Figure 2: Functional Block Diagram



Typical Application with a C200

Figure 3: WebamP schematic of C210 with a C200

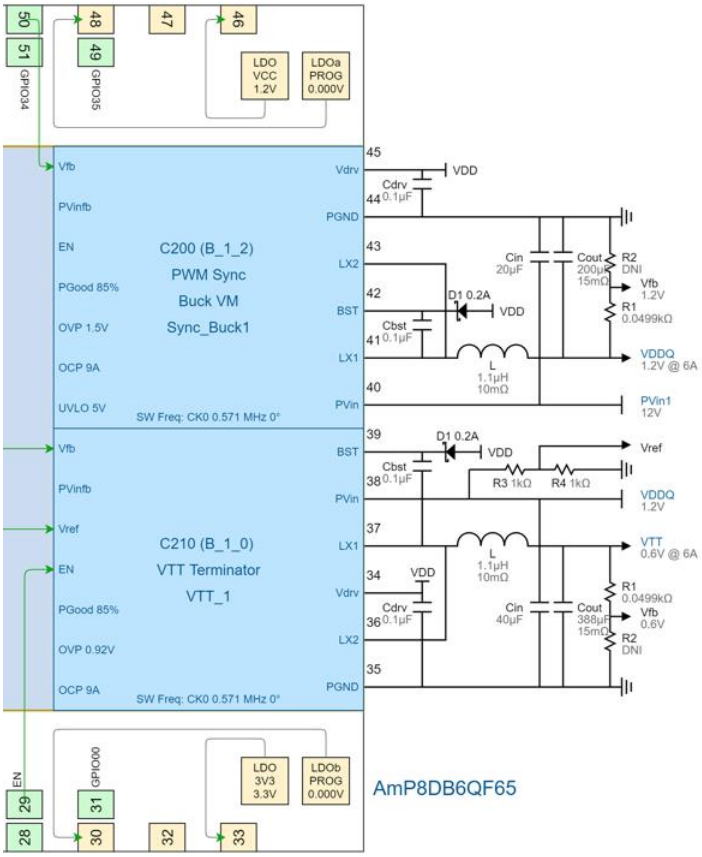


Figure 3 shows partial WebAmP schematics of the C210 with a C200 (synchronous buck converter) as the main VDDQ rail. Note the following:

- The PVin name of the C210 has been set to the same name as the output of the C200. In this example it is VDDQ.
- The EN input of the C210 is connected to the same signal as the EN input of the C200.
- The input voltage spec of the C210 has been set to the same value as VDDQ. In this example, 1.2 V.
- The C210 converter will draw current from the C200 and the current available for the C200's load will reduce accordingly.

The 1 kΩ + 1 kΩ Vref divider for the C210 can also be used as the Vfb output sense divider for the C200. In this case, in WebamP, connect the Vfb input of the C200 to the same GPIO pin as the Vref signal of the C210. In WebAmP, set the C200 divider to 1 kΩ and 1 kΩ. This is only recommended when the C200 output voltage is > 2.2 V, when a divider for the C200 is required because of the max allowable voltage on a GPIO pin (GPIO pin set as an analog input).

Switching Frequency

It is recommended that the C210 and the converter powering it run at the same switching frequency to prevent potential frequency beating effects that may resemble ringing during transients. Additionally, making Cin large, which is the Cout of the C200 in this schematic, will help with the C210's transient response. This is because a load attack on the C210 will tend to cause a dip on Cin; and because the C210 tracks the voltage on Cin, will cause a dip on its output that's larger than in a standard, non-tracking converter. For many applications, 1 MHz for both converters works well, for best transient performance.

Feedback loop design

The C210 is a tracking converter, and thus the output impedance (i.e. output capacitance and crossover frequency) of the converter powering it (e.g. a C200), affects the feedback loop dynamics of the C210. For this reason, the C210 runs better with a more limited crossover frequency, in the range of 20-50 kHz using WebAmp's Bode plotter. Phase margin can be as low as 30° and still have good results.

Start-up and Shutdown

Soft-start and soft-shutdown of the C210_B will track the VDDQ converter. The user-specified soft-start time in WebAmP for the C210 must be set to the same value as the C200. This specified time is used internally to enable output undervoltage protection.

PGood

The power-good, PGood, digital port may be connected to a GPIO pin or a control component such as the C420 sequencer to indicate output voltage regulation status. PGood goes high when the C210_B output is above the user-programmed value (default 85%) of the specified Vout voltage as configured in WebAmP. Because it is tracking the VDDQ converter at start-up, if the PGood setting of the latter is the same percentage, the PGood of both converters will assert at about the same time during soft-start. They will also de-assert at about the same time during soft-shutdown.

Protection Features

As shown in Figure 4, the C210_B provides many protection features including VoUVLO, OVP, OCP and OTP.

VoUVLO

VoUVLO goes high when output voltage, V_{OUT}, is lower than the programmable preset condition in Parameter Settings, (default 75% of V_{OUT}). VoUVLO goes low when output voltage, V_{OUT}, is greater than the programmable preset condition in Parameter Settings, (default 75% of V_{OUT}). On detection of VoUVLO, the C210_B will power down and PGood will go low. On VoUVLO returning low, an EN cycling low-to-high, will restart the C210_B with a new Soft Start cycle.

OVP

The Over Voltage Protection, OVP, digital port may be connected to a GPIO pin to indicate the output voltage over voltage status. OVP goes high when output voltage, V_{OUT}, is greater than the programmable preset condition in Parameter Settings, (default 25% above Vout). OVP goes low when output voltage, V_{OUT}, is less than the programmable preset condition in Parameter Settings, (default 25% above V_{OUT}). On detection of OVP, the C210_B will skip Hi-side switch pulses until OVP returns low.

OCP

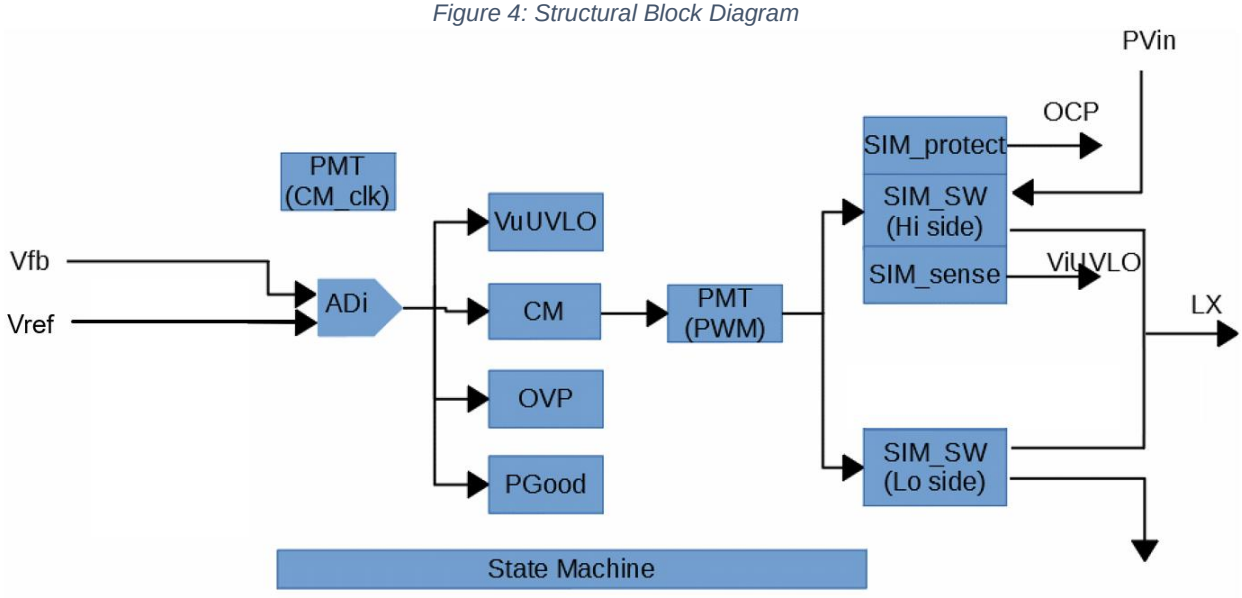
The Over Current Protection, OCP, digital port may be connected to indicate the output over current status. When I_{OUT}, is greater than 140% of the Output Current setting, the C210_B will limit the Hi-side switch pulse width and OCP will go high. If I_{OUT} is greater than 165% of Output Current setting, the C210_B will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the C210_B with a new Soft Start cycle.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C210_B will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C210_B with a new Soft Start cycle.

Port Name Table

Port Name	I/O	Description
Vfb	input	Vout feedback
Vref	input	PVin/VDDQ feedback
PVinfb	input	PVin feedback
EN	input	Enable
PGood	output	Power Good
OVP	output	Over Voltage Protection
OCP	output	Over Current Protection
UVLO	output	Under Voltage Lockout
BST	input	Boost
PVin	input	Power Voltage in
LX1	output	Switch
Vdvr	input	Driver Voltage
LX2	output	Switch
PGND	input	Power Ground

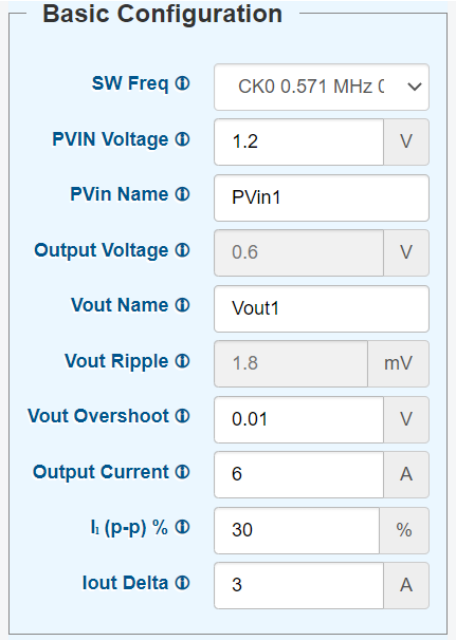
Figure 4: Structural Block Diagram



Parameter Settings

Basic Configuration

Default parameters may be changed per user requirement.



Vout Ripple is computed as follows:

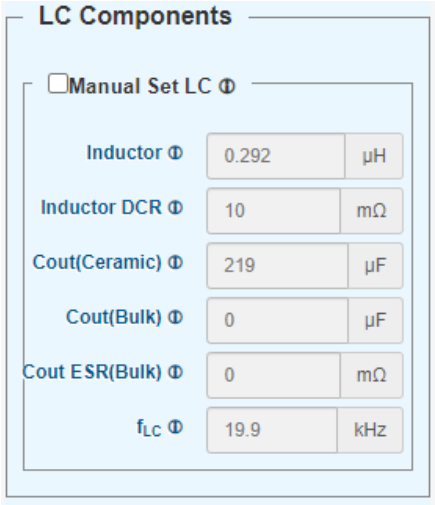
$V_{OUTripple}$ = Iripple/(8*Cout*Fsw)

LC Component Selection

Default values for Inductance, L, and output capacitance, Cout, are computed as follows:

L = (Vin-Vout)*Vout / (Vin*Fsw*Iripple)

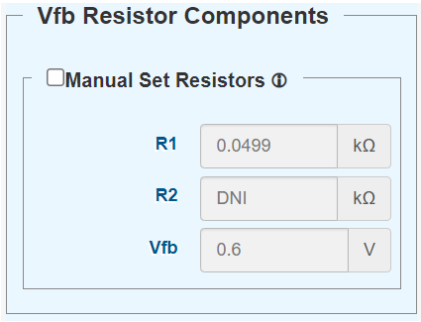
Cout = Ioutdelta^2*L / (2*Vout*Vos)



Inductor and Capacitor values may be changed by checking Manual Set LC or selecting the BoM tab where manufacturer's part numbers may be selected.

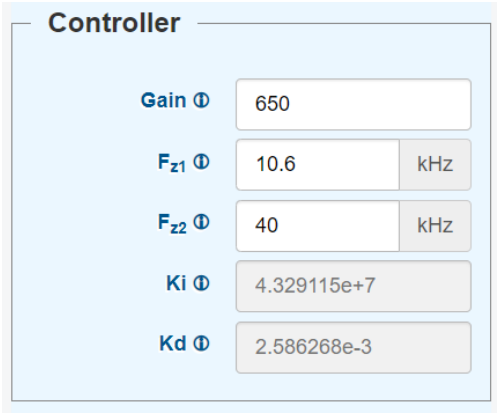
Vfb Resistor Components

Feedback divider resistors R1 and R2 default to 50 Ω and open (infinity). When Vout is greater than 2.2V, a resistor divider ratio is computed to select 1% resistor values for both R1 and R2.

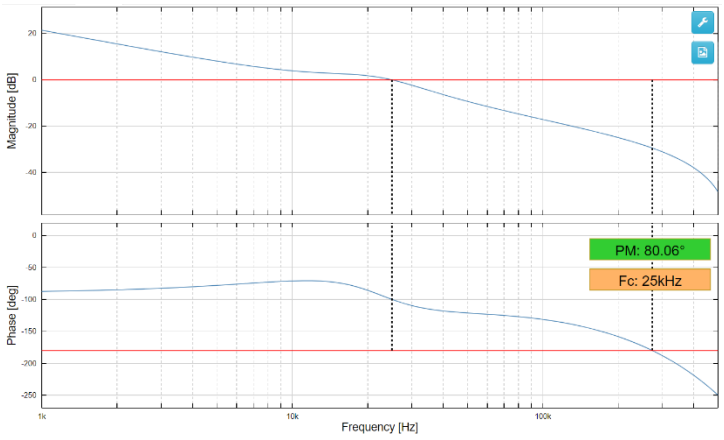


Controller

The controller compensation memory block provides PID compensation of error signals using the integrated compensation logic without external passives or an arithmetic unit. User can adjust bandwidth, gain, and phase margin of the compensation logic. For example, a user can interactively adjust the proportional gain Kp and the gains Fz1 and Fz2 shown below to effectively adjust the derivative and integral gains Kd and Ki as well as the bandwidth and the phase margin.

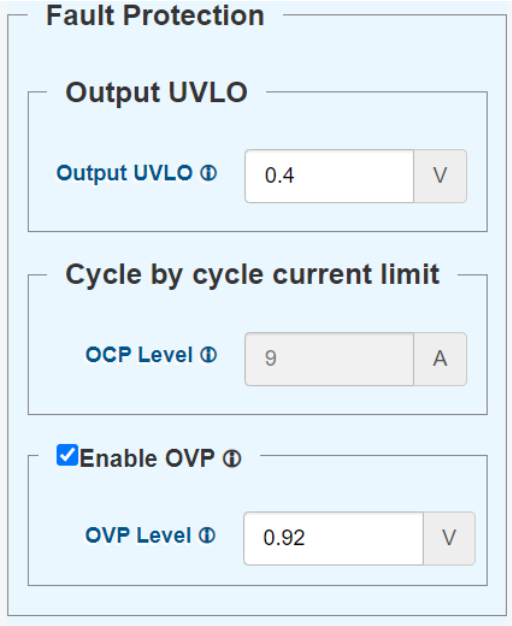


Gain, Fz1 and Fz2 are chosen to provide best Phase Margin and Crossover Frequency, Fc, as adjusted in the Bode Plot shown below:



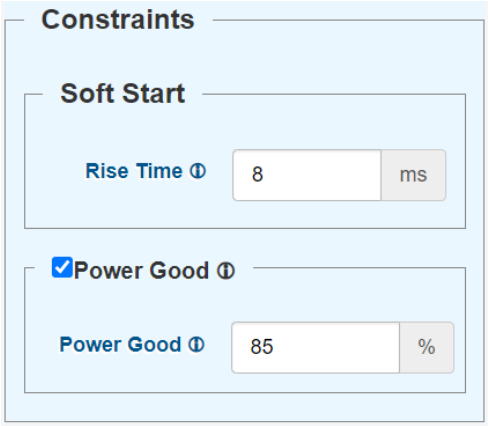
Fault Protection

Output voltage Under Voltage Lockout, VoUVLO, indicates the output voltage status greater or less than programmable preset condition (default 75% of V_{OUT}). Over Voltage Protection, OVP, indicates output voltage status greater or less than the programmable preset condition (default 25% above Vout). Over Current Protection, OCP, indicates the output over current greater or less than the programmable preset condition (default 9A). Over Temperature Protection, OTP, indicates thermal shutdown has occurred. (set to 125°C).



Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good ranges 59% to 100% and default is 85%.



Power Component Version Table

Power Component Name	Description
C210_B_1_0	First Version B

C210_B Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	2
Number of AnD_SIM_Protect	2
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	11
Number of AnD_ATC_IO	2
Number of AnD_ATC_Comp	2
Number of AnD_PMT	3
Number of AnD_CM_PID	2
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	13
Number of AnD_DFF	25
Number of LUT4	101

Resource Usage...

io	2 used	(Capacity 24)
clb	15 used	(Capacity 64)
cm	2 used	(Capacity 8)
pmt	3 used	(Capacity 16)
sim	2 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	4 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	101 used	(Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	22
AnD_DFFN	6

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	2
AnD_Nref_dyn	1
AnD_Nref_fix	3
AnD_PMT	3
AnD_SIM_Protect	2
AnD_SIM_SW	2
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C210_B power components.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature-compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, InAmp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

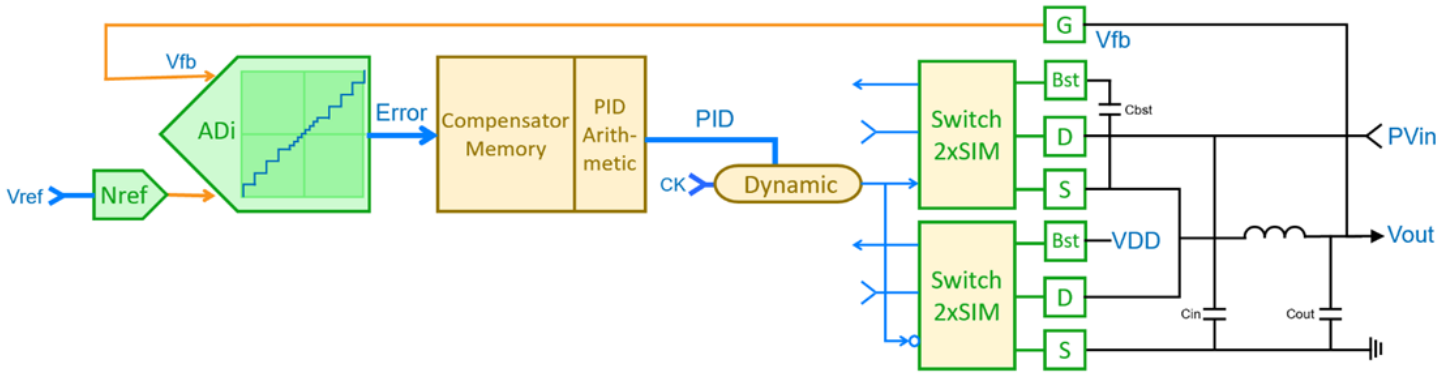
Scalable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, Drain voltage or current and Analog Fabric including programmable references (Nrefs).

Figure 5: PMIC Blocks and Resources Example - Buck Regulator



Additional Resources

- AnDAPT AmP Platform datasheet

Revision History

Date	Revision
10/11/2022	Added Switching Frequency and Feedback loop design reccomendations
06/09/2022	Preliminary release

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