PWM Synch Buck, Voltage Mode, 10A HC

Power Component: C220_B, I220_B

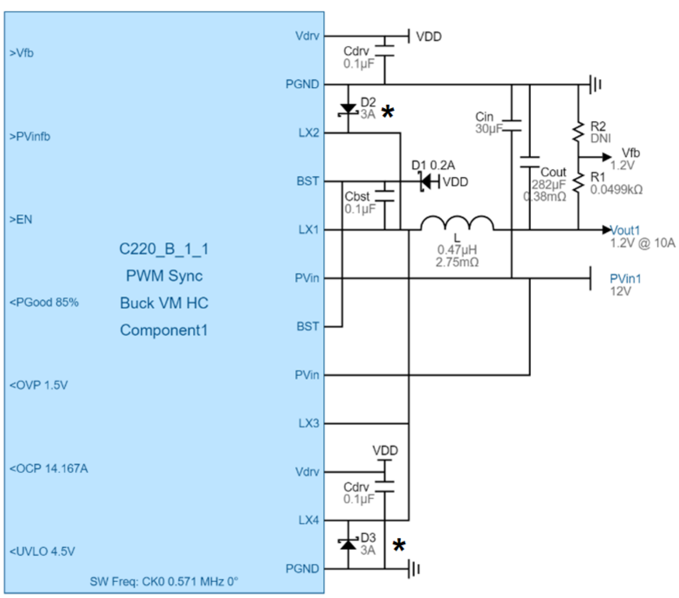
Product Description

The C220_B Power Component is a customizable, high-output-current (HC) PWM Synchronous Buck, Voltage Mode Switching Regulator. Combine the C220_B component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management integrated circuit (PMIC). The I220_B Power Component includes the C220_B Synchronous Buck and extends it with I2C communication for dynamic voltage scaling.

Features

- PWM, voltage mode, point-of-load (POL) regulator
- Maximum output current: 10A
- PV_{IN}: 3 to 14V, V_{OUT}: 0.6V to 5.5V
- Adjustable output voltage with down to 2.4 mV resolution
- Integrated MOSFETs, $R_{DS(on)}$: 15mΩ (2 in parallel)
- 1% load regulation
- Efficiency up to 95%
- Internal compensator minimizes external part count
- Adjustable switching frequency from 300 kHz to 1.1 MHz
- Adaptable compensation, bandwidth, gain & phase margin
- Adjustable protection: Input Undervoltage Lockout, (ViUVLO), Output Undervoltage Lockout, (VoUVLO), Overcurrent (OCP), Overvoltage (OVP)
- Over Temperature Protection (OTP) (part of platform)
- Short-circuit protection (SCP)
- Power-good flag output and Enable input
- Soft start/stop, sequencing, pre-bias startup
- –40°C to +125°C operating junction temperature
- Four SIM elements; integrate up to two C220_B Power Components in one AmP Platform

Figure 1: C220_B application schematic



Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing

Product Detail

The C220_B Synchronous Buck Regulator includes integrated MOSFETs, customizable PWM controller and various protection circuits.

The integrated, low-resistance switching Scalable Integrated MOSFETs (SIM) provide up to 10A output current. Output voltage feedback is compared against an internal reference using a high-performance, voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is either generated internally via an oscillator with selectable frequencies or provided via an external pin.

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmp development software. The C220_B component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), or input undervoltage lockout (ViUVLO) condition. The threshold values are specified by the power engineer using the WebAmp tool.

The customizable soft-start and soft-stop slew rates are also specified by the power engineer using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 customizable Sequencer, by interconnecting signals EN and PGood to provide customizable dependencies and customizable delays between each sequence step.

* LX to GND Schottky Diodes D2 & D3 are optional and guarantee the best system level efficiency on versions B_1_2 and higher

Recommended Operating Conditions

over operating free-air temperature range

Symbol	Parameter	Min	Typ	Max	Unit
PV_{IN}	Power Input Voltage	3		14	V
I_{OUT}	I_{OUT} Output Current Maximum	10			A

Electrical Characteristics Buck Converters

PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10μF, Cvcc=1μF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT})		0.6		5.5	V
Voltage Regulation	Including load line and temperature variation V_{IN} range: 4.5V to 14V	-1		+1	%
Switching frequency (F_{SW})		300		1143	kHz
Switching frequency accuracy		-5		+5	%
MOSFET switch on-resistance ($R_{DS(on)}$) (two SIMs in parallel)			15		mΩ
Peak efficiency	V_{IN}=5V, V_{OUT}=3.3V, F_{SW}=571kHz I_{OUT}=3A		95		%
Efficiency	V_{IN}=12V, V_{OUT}=1.8V, F_{SW}=571kHz, I_{OUT}=4A		88		%
Input Shutdown current (V_{IN})	EN = Low		3.0		mA
Input Shutdown current (PV_{IN})			0.1		mA
Input Quiescent current (V_{IN})	EN = High, I_{OUT} = 0A, Fsw = 571 kHz, V_{OUT} = 1.2V		11		mA
Input Quiescent current (PV_{IN})			9		mA
PROTECTION					
ViUVLO, input Undervoltage Lockout		4		10	V
OCP, Over Current Protection (% **I_{OUT}**)			140		%
OVP, Overvoltage Protection trip point range (relative to Parameter Setting)		+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Parameter Setting)		-100		-432	mV
Power Good threshold (relative to Parameter Setting)		-100		-432	mV

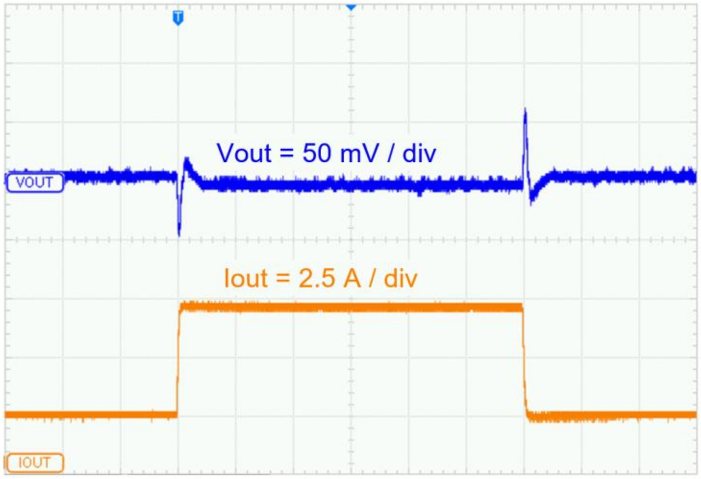
* Parameters shaded in green are user customizable as set in WebAmP development software

Typical Characteristics

Unless otherwise specified: TA = 25°C, F_{SW} = 571kHz, L_{OUT} = 1.2 µH, C_{OUT} = 376µF

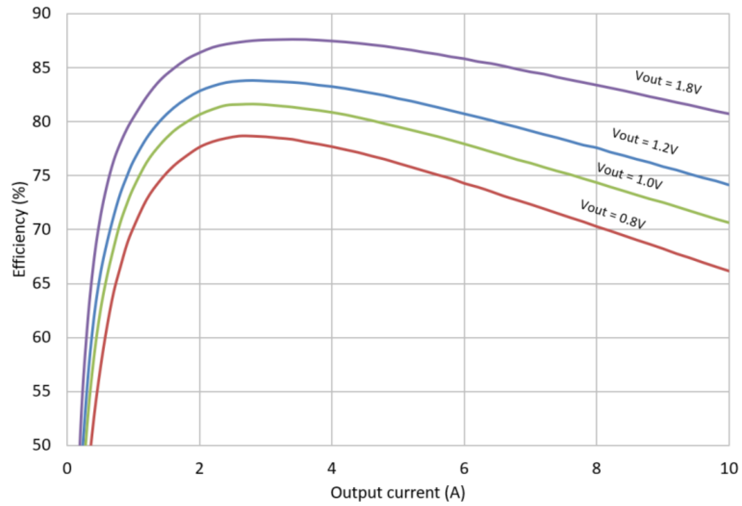
Transient Response

V_{OUT} = 1.2 V I_{OUT} step 2.5 A to 7.5 A Slew Rate: 2.5A/µs



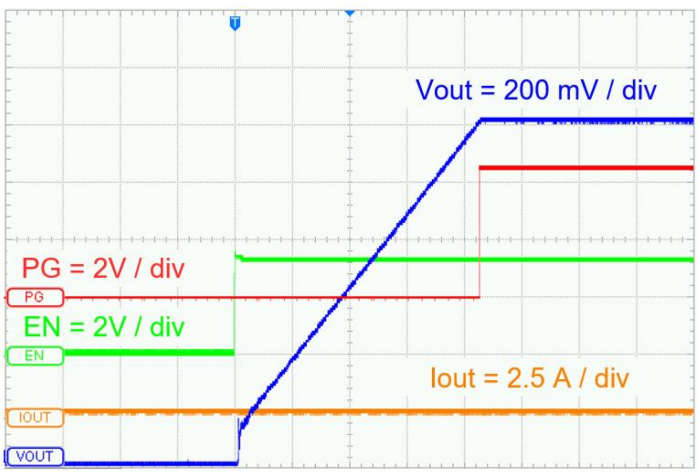
Time = 200 µs / div

Efficiency



Soft Start, No Load

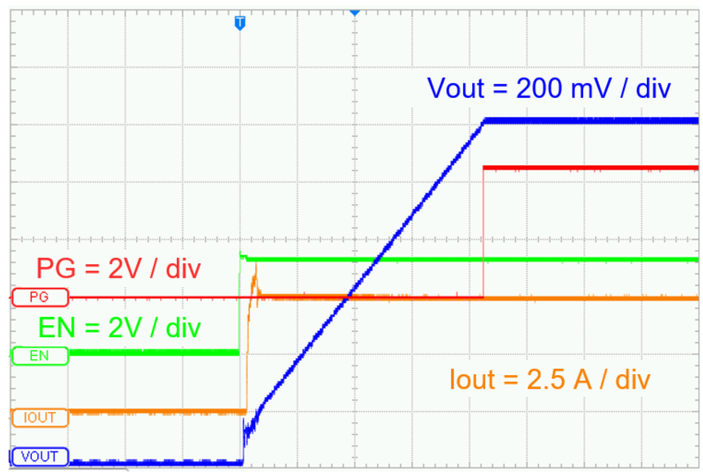
PVin = 12V, Vout = 1.2V



Time = 2 ms / div

Soft Start, Load = 5A

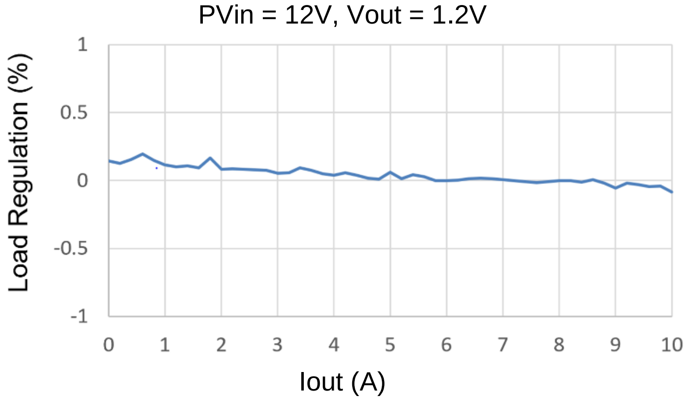
PVin = 12V, Vout = 1.2V



Time = 2 ms / div

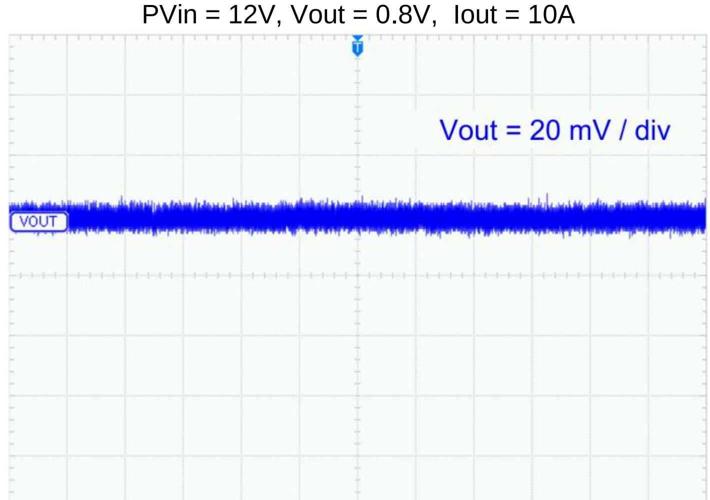
Load Regulation Percentage Error

PVin = 12V, Vout = 1.2V



Vout Ripple

PVin = 12V, Vout = 0.8V, Iout = 10A



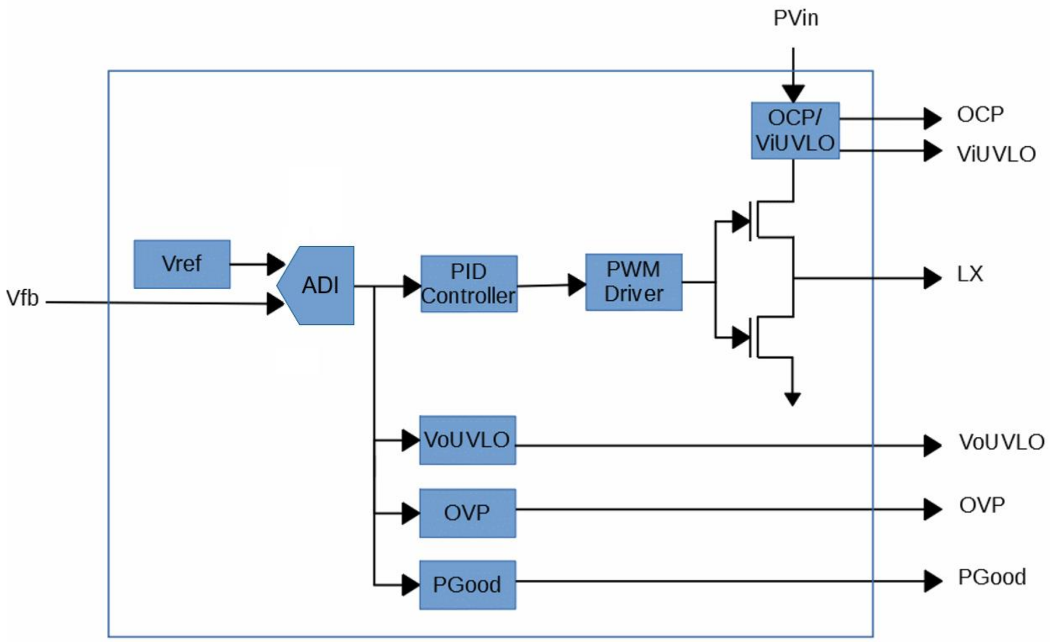
Time = 100 ms / div

Theory of Operation

The C220_B Synchronous Buck Regulator with integrated MOSFETs operates in voltage mode by comparing the V_{OUT} feedback voltage, Vfb, with a programmable reference, Vref to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the Hi-side and Lo-side MOSFET switches as shown in Figure 2

In CCM (Continuous Conduction Mode), the PWM driver goes high turning the Hi-side switch "ON" to provide PVin to the LX side of an inductor, L, where $V_L = V_{LX} - V_{OUT}$. When the PWM driver goes low, the Hi-side switch turns "OFF", and after a shoot through delay, the Lo-side switch turns "ON" providing a path for the inductor current to decrease with $V_L = - V_{OUT}$, until the next PWM turns back "ON". As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM cycle to optimize regulation and transient response over changing load conditions.

Figure 2 Functional Block Diagram



Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port which may be connected to a GPIO pin or a control component such as the C420 Sequencer. When EN goes high or when an I2C EN command for the I220_B is given, the output voltage, V_{OUT}, will ramp up according to the Soft Start programmable preset ramp time in Parameter Settings, (default 8 ms). When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start programmable preset ramp time in Parameter Settings (default 8 ms).

PGood

The power-good, PGood, digital port may be connected to a GPIO pin or a control component such as the C420 Sequencer to indicate the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time and when all Faults are cleared. PGOOD will go low for faults such as ViUVLO, VoUVLO, OVP over voltage, OCP current limit, or OTP thermal shutdown. PGOOD will also go low if EN goes low.

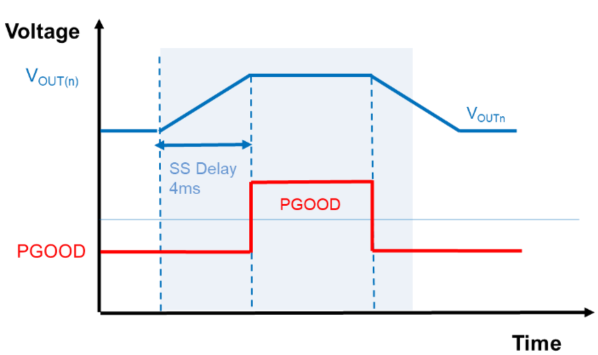


Figure 3: PGOOD Timing

Protection Features

As shown in Figure 4 the C220_B provides many protection features including ViUVLO, VoUVLO, OVP, OCP and OTP.

Input Under Voltage (ViUVLO)

The input Under Voltage Lockout, ViUVLO, indicates the input voltage status of the C220_B. ViUVLO goes high when PV_{IN} voltage is lower than the programmable preset condition and goes low when PV_{IN} voltage is greater than the programmable preset condition. PVin may be sensed on the PVin pin when the Parameter Setting is set to Internal or may be sensed on a GPIO pin connected to the PVinfb analog port when the Parameter Setting is set to External. On detection of ViUVLO, the C220_B will power down and PGOOD will go low. On ViUVLO returning high, the C220_B will restart with a new Soft Start cycle.

Output Under Voltage (VoUVLO)

The output Under Voltage Protection, VoUVLO, indicates the output voltage status. VoUVLO goes high when the regulator output is lower than the specified Parameter Setting. VoUVLO goes low when the output voltage is above the specified Parameter Setting. On detection of VoUVLO, the regulator will power down and PGOOD will go low. On VoUVLO returning low, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

Over Voltage Protection

The Over Voltage Protection, OVP, of the regulator indicates the output voltage status. OVP is high when the regulator output is above specified Parameter Setting. OVP is low when the output is less than the specified Parameter Setting. On detection of OVP, a regulator will skip Hi-side switch pulses until the fault condition is not present.

Over Current Protection

The Over Current Protection, OCP, of the regulator indicates the over current status. When the Output Current, I_{OUT}, of the regulator is greater than 142% of the Output Current setting, the regulator will limit the Hi-side switch pulse width and OCP will go high. If I_{OUT} is greater than 165% of the Output Current setting, the regulator will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the device with a new Soft Start cycle.

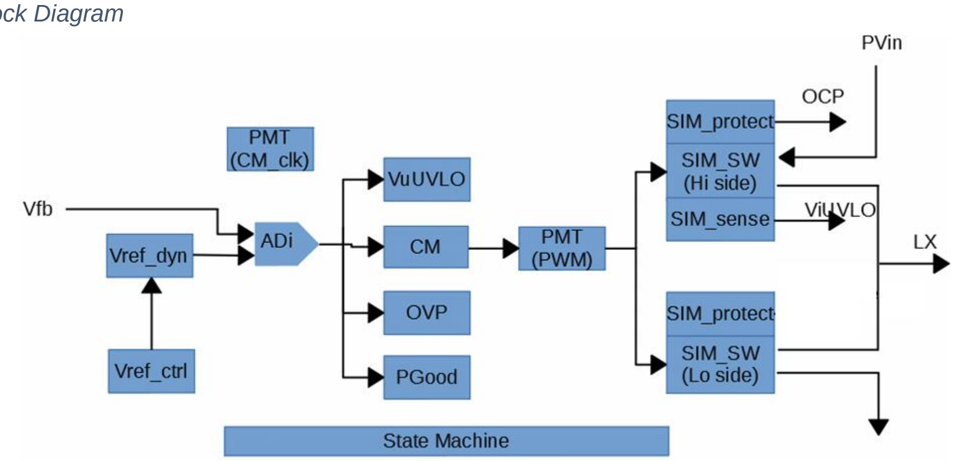
OTP

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C220_B will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C220_B with a new Soft Start cycle.

Port Name Table

Port Name	I/O	Description
Vfb	input	Vout feedback
PVinfb	input	PVin feedback
EN	input	Enable
PGOOD	output	Power Good
OVP	output	Over Voltage Protection
OCP	output	Over Current Protection
UVLO	output	Input Under Voltage Lockout
BST	input	Boost
PVin	input	Power Voltage in
LX1	output	Switch
Vdvr	input	Driver Voltage
LX2	output	Switch
PGND	input	Power Ground

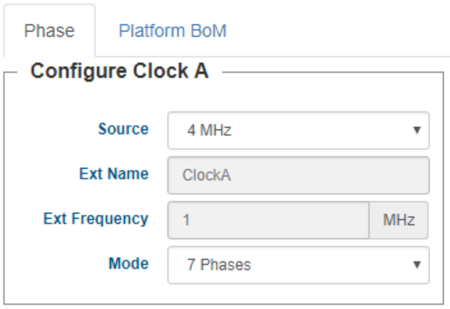
Figure 4 Structural Block Diagram



Parameter Settings

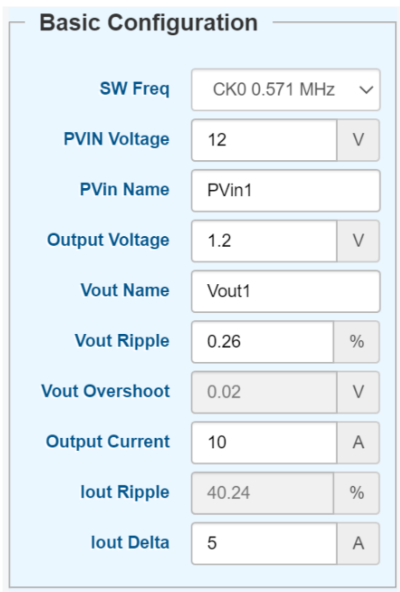
Project Settings

In Settings menu, configure clock settings to the desired switch frequency, F_{SW}. For example, to generate 571 kHz choose 4 MHz and divide by 7 phases.



Basic Configuration

Default parameters may be changed per user requirement.



Vout Ripple is computed as follows:

$V_{OUTripple}$ = Iripple/(8*Cout*Fsw)

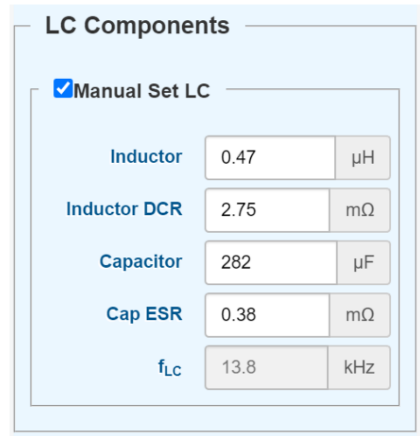
LC Component Selection

Default values for Inductance, L, and output capacitance, Cout, are computed as follows:

$$L = (V_{IN}-V_{OUT})*V_{OUT} / (V_{IN}*Fsw*Iripple)$$

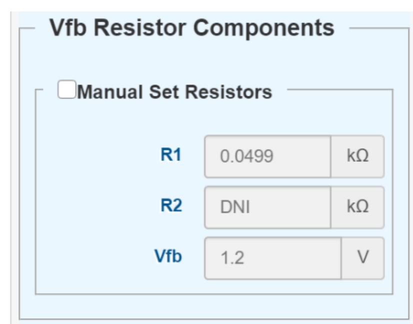
$$Cout = Ioutdelta^2*L / (2*V_{OUT}*Vos)$$

Inductor and Capacitor values may be changed by checking Manual Set LC or selecting the BoM tab where manufacturers part numbers may be selected. For example, choose L = 1.2 µH, C_{OUT} = 376µF.



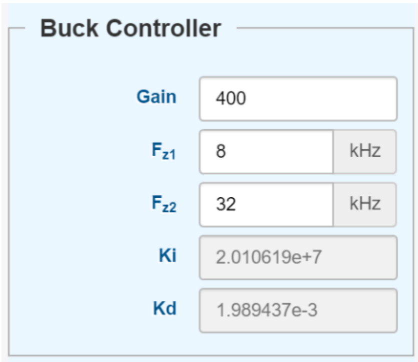
Vfb Resistor Components

Feedback divider resistors R1 and R2 default to 49.9 Ω and open (infinity). When Vout is larger than 2.3V, a resistor divider ratio is computed to select 1% resistor values for both R1 and R2.



Controller

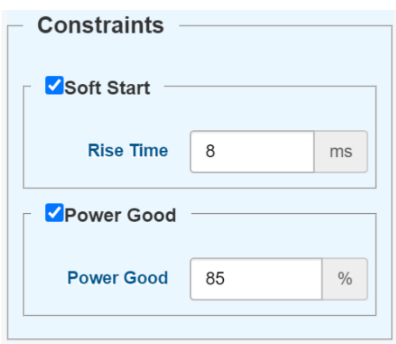
The controller compensation memory block provides PID compensation of error signals using the integrated compensation logic without external passives or an arithmetic unit. The user can adjust a bandwidth, a gain, and a phase margin of the compensation logic. For example, a user can interactively adjust the proportional gain Kp and the gains Fz1 and Fz2 shown below to effectively adjust the derivative and integral gains Kd and Ki as well as the bandwidth and the phase margin.



Gain, Fz1 and Fz2 are chosen to provide best Phase Margin and Crossover Frequency, Fc.

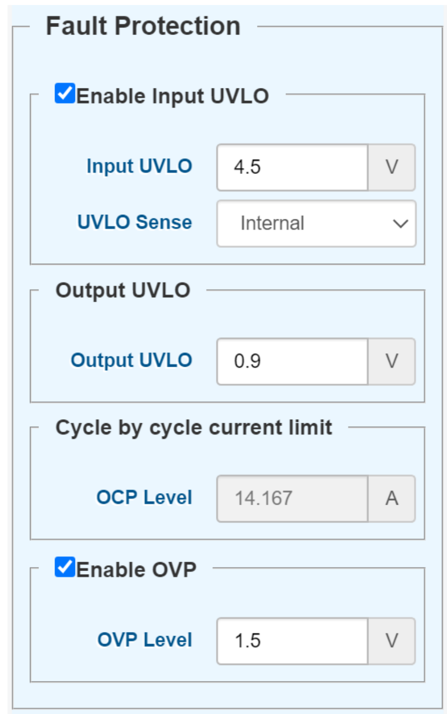
Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good ranges 59% to 100% and default is 85%.



Fault Protection

Input voltage Under Voltage Lockout, ViUVLO, indicates the input voltage status greater or less than programmable preset condition (default 4.5V). Output voltage Under Voltage Lockout, VoUVLO, indicates the output voltage status greater or less than programmable preset condition (default 75% of V_{OUT}). Over Voltage Protection, OVP, indicates output voltage status greater or less than the programmable preset condition (default 25% above Vout). Over Current Protection, OCP, indicates the output over current greater or less than the programmable preset condition (default 14.167A). Over Temperature Protection, OTP, indicates thermal shutdown has occurred. (set to 125°C).

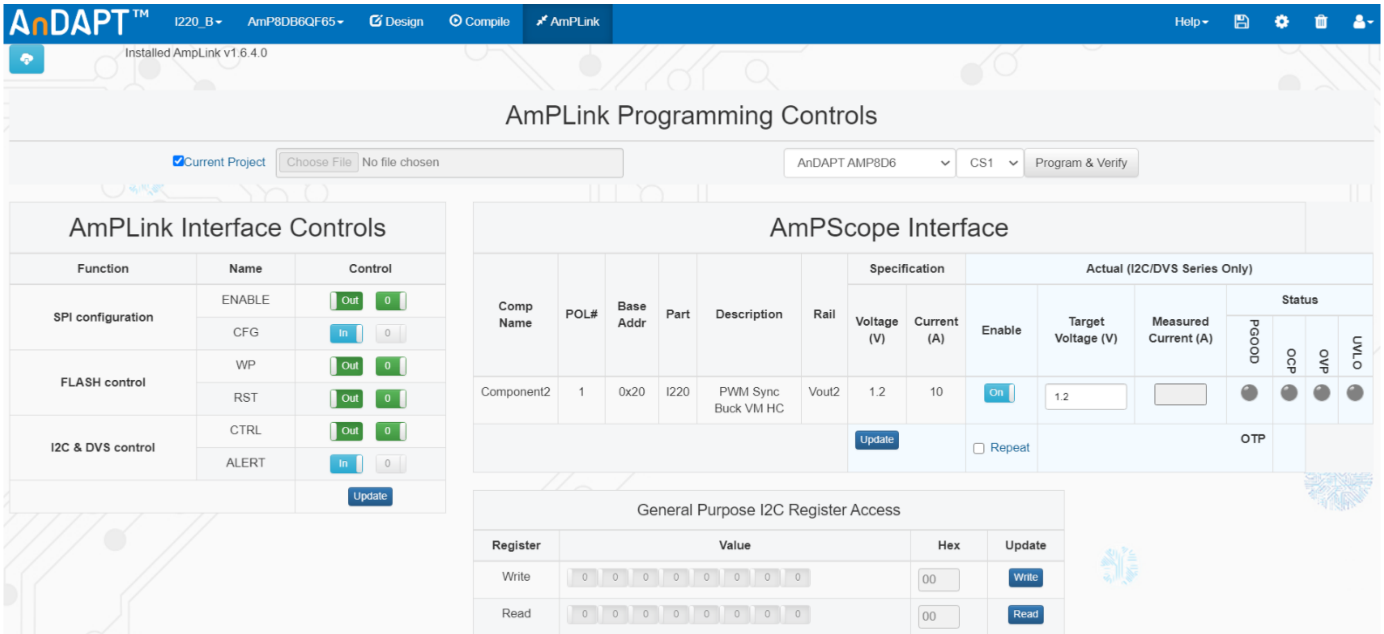


Power Component Version Table

Name	Description
I220_B_1_0	First Version
C220_B_1_1	First Version B
C220_A_1_1	Improved soft start monotonicity Enhanced support for pre bias startup
C220	First Version

Grayed out: Not recommended for new designs

I2C AmpScope Interface



The I220_B Power Component is a version of the C220_B with additional telemetry capabilities provided by the I2C interface including:

- Fault status for PGOOD, OCP, OVP and UVLO
- Voltage Margining Vout setting

The I2C commands are summarized Table 1.
Note that the first I2C series Power Component will automatically insert one I480 I2C Controller Power Component with additional SDA and SCL signal pins. Additional I2C series Power Components will not insert an I480 as one I480 supports multiple I2C series Power Components.

The I2C AmpScope Interface above provides a user interface to read and write the I2C commands for all the I2C series Power Components contained in the AmP device. When I2C enabled component is present in the design, users will be able to read several device and design parameters. Refer to "I2C Design and Usage Guide" for details on I2C register architecture and accessing I2C registers. The registers used for I220 component are shown in Table 1.

Table 1: I2C Register Map

Address*	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x28	STATUS					UVLO	OVP	OCP	PGood
0x30	ENABLE								ENB
0x32	Vout (lo)	Vout[7]	Vout[6]	Vout[5]	Vout[4]	Vout[3]	Vout[2]	Vout[1]	Vout[0]
0x33	Vout (hi)							Vout[9]	Vout[8]

* Address page+offset methodology as in Figure 9.
** Slave Address can be set in I480 Module

I2C Write/Read Protocol

An Amp device is addressed by its pre-defined 7-bit device physical address (default address is 0x55). Along with the 7-bit address, an 8^{th} bit is added to the LSB position to identify whether the following transaction is a read or write, making it an 8-bit address byte. If the least significant bit of the address byte is zero, it is a write transaction whereas a 1 is a read transaction. The Amp device parameters as well as the read/write parameters of the different POLs in the device are accessed through 256 8-bit registers. Every I2C transaction to the Amp device therefore needs another 8-bit register address. The general format of I2C-Amp device write/read protocol is shown in Figure 5. Note that the Amp device is always the slave. In Figure 5, the shaded portion is sent by the master and the unshaded portion by the slave.

Figure 5 I2C read/write protocol

I2C write to the device

S	Device Address	Wr	A	Register Address	A	Write byte 1	A	Write byte 2	A	P

I2C read from the device

S	Device Address	Wr	A	Register Address	A	Sr	Device Address	Rd	A	…

…	Read byte 1	A	Read byte 2	N	P

Details of the bit notation

S	Start	Sr	Repeated Start	P	Stop
Wr	Write Bit	Rd	Read Bit		
A	Ack	N	Nack		
(shaded)			Data from Master		
(unshaded)			Data from Slave		

Both write and read transactions can be either a one byte or a multi-byte transfer. Accordingly, the register address is either the address of the register that is being accessed or the starting address of a sequence of registers that is being accessed. For a write transaction, the device updates write data to successive registers until it receives an I2C stop signal. For read transactions, the master first writes the starting address into the device and starts accepting read from the device after a repeated start signal. The device sends successive register data until the master issues a NACK for the last byte read.

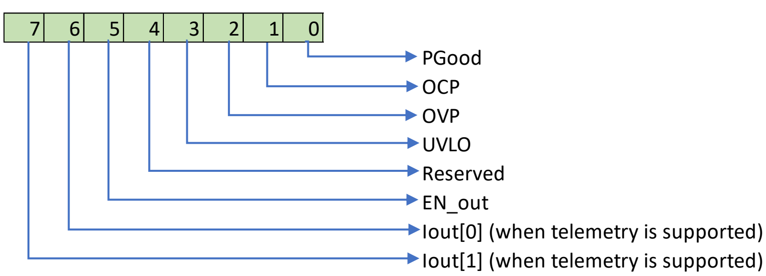
Status Read (0x28, 0x48, …)

Status read is a byte command and its format is shown in Figure 6. The address for status register is 0x28 for POL1 and 0x48,0x68,etc., for subsequent POLs.

Figure 6 Format of status read command

S	Device Address	0	A	0x28, 0x48, …	A	Sr	Device Address	1	A	…

…	{Iout Lo, Status}	N	P



The PGood status and OCP, OVP and ViUVLO fault bits are packed into the status byte as shown in Figure 6. The fault bits are “sticky” in the sense that a fault, even if it is momentary, sets the bit high and that bit remains high even if the fault went away until the POL is read. All fault bits are all cleared when the next I2C read transaction happens from that POL. The EN_out status bit has not yet been implemented.

Component Enable (0x30, 0x50, …)

Component Enable is a byte command and its format is shown in Figure 7. Bit 0 of the command byte controls component enable, with a zero being enable and a 1 disable. Bit 1 is used to define enable mode, but it is not currently implemented. The component is enabled when both the direct EN pin into the component is high and its I2C enable bit is zero. All the I2C write and read transactions are valid even when the component is disabled.

Figure 7 Format component enable command

S	Device Address	0	A	0x30, 0x50, …	A	Component Enable	A	P

Vout Set (0x32, 0x52, …)

The format of the Vout (output voltage) set command is shown in Figure 8. The address for Vout register is 0x32 for POL 1 and 0x52, 0x72, etc., for the subsequent POLs. Vout set value is a 10-bit coded quantity proportional to the output voltage to be set. The lower 8 bits of the Vout code is set to the first Vout register (0x32, 0x52,…) and the upper 2 bits are set to the lower 2 bits of the second Vout register (0x33, 0x53,…). Note that Vout must be set as a word by issuing a 2 byte write command. The Vout code to voltage relationship for platform B Amp devices is as given below.

Vout (in volts) = Vout_code * 2.5 / 1000

The Vout setting is for the output voltage factored by the voltage divider, if any. In other words,Vout set actually sets the feedback voltage.

Figure 8 Format of Vout set command

S	Device Address	0	A	0x32, 0x52, …	A	Vout[7:0]	A	{6'hxx,Vout[9:8]}	A	P

Register Address Format

The register address format for the Amp device is shown in Figure 9. The register address is an 8-bit number which can take on any value from 0x00 to 0xFF. The register space is divided in to eight pages, with page 0 dedicated to device-wide registers and pages 1 through 7 to support up to 7 POLs.

Figure 9 Amp I2C register address format

I2C Register Addressing Method

7	6	5	4	3	2	1	0
Page Number			Offset				

Page Table

3'b000	Device
3'b001	POL1
3'b010	POL2
3'b011	POL3
3'b100	POL4
3'b101	POL5
3'b110	POL6
3'b111	POL7

C220_B Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	4
Number of AnD_SIM_Protect	4
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	21
Number of AnD_ATC_IO	2
Number of AnD_ATC_Comp	2
Number of AnD_PMT	3
Number of AnD_CM_PID	2
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	6
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	12
Number of AnD_DFF	25
Number of LUT4	105

Resource Usage...

io	2 used (Capacity 24)
clb	14 used (Capacity 64)
cm	2 used (Capacity 8)
pmt	3 used (Capacity 16)
sim	4 used (Capacity 8)
atc	1 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	2 used (Capacity 2)
uLogic	105 used (Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	22
AnD_DFFN	5

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	2
AnD_Nref_dyn	1
AnD_Nref_fix	5
AnD_PMT	3
AnD_SIM_Protect	4
AnD_SIM_SW	4
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

I220_B plus I480 Resource Usage

Circuit Stats...

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_I2C_Phy	1
Number of AnD_ADi_dual	1
Number of AnD_SIM_SW	4
Number of AnD_SIM_Protect	4
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	21
Number of AnD_ATC_IO	4
Number of AnD_ATC_Comp	2
Number of AnD_PMT	3
Number of AnD_CM_PID	2
Number of AnD_CM_RAM_256x18	1
Number of AnD_Nref_dyn	1
Number of AnD_Nref_fix	6
Number of AnD_PTG_Phase_Count	2
Number of AnD_PTG_GBUF	2
Number of AnD_PTG_OSC	2
Number of AnD_DFFN	15
Number of AnD_DFF	56
Number of LUT4	182

Resource Usage...

io	4 used (Capacity 24)
clb	24 used (Capacity 64)
cm	3 used (Capacity 8)
pmt	3 used (Capacity 16)
sim	4 used (Capacity 8)
atc	1 used (Capacity 6)
corner	4 used (Capacity 4)
ptg	2 used (Capacity 2)
uLogic	182 used (Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	18

$techmap\component_2

AnD_DFF	35
AnD_DFFN	8

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_CM_RAM_256x18	1

component_2

AnD_ADi_dual	1
AnD_ATC_Comp	1
AnD_CM_PID	2
AnD_Nref_dyn	1
AnD_Nref_fix	5
AnD_PMT	3
AnD_SIM_Protect	4
AnD_SIM_SW	4
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C220_B, I220_B power components.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, InAmp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

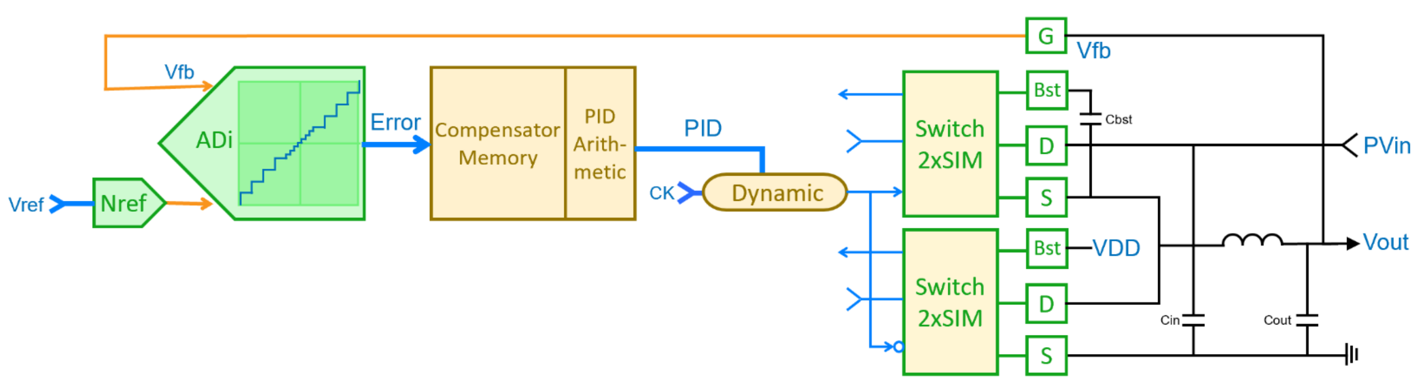
Scaleable Integrated MOSFET– SIM

- R_{DSON} of 30 mΩ for a single SIM
- R_{DSON} of 15 mΩ for two SIMs in parallel (C220_B)

The SIM in switch mode provides integrated MOSFETs to perform switching regulator and gate driver functions. The MOSFET gate may be driven directly from fabric, from the Gate Flip-flop or adjacent SIM Gate Flip-flops. The Gate Flip-flop is set from the fabric, then reset from fabric, current sense peak/valley/limit1/limit2 or zero detect. The MOSFET gate may be segmented in up to 15 individual gates to reduce gate capacitance. The GateOn signal detects the actual on-status of the MOSFET gate for precise timing control of Hi-side and Lo-side topologies.

SIM in linear mode provides integrated MOSFETs to perform LDO and Load Switch functions. The MOSFET gate is driven by a linear Operational Amplifier to implement linear, voltage or current, regulators. Op Amp inputs include Source, Drain voltage or current and Analog Fabric including programmable references (Nrefs).

Figure 10: AmP Blocks and Resources Example - high-output-current (HC) PWM Synchronous Buck, Voltage Mode Switching Regulator



Additional Resources

- AnDAPT AmP Platform B datasheet

Revision History

Date	Revision
06/03/2022	Updated Input Shutdown current (PV_{IN}) and Input Quiescent current (V_{IN})
01/20/2021	Removed 125 °C OTP and added: See: Recommended Operating Conditions in AnDAPT_AmP_Platform_B Datasheet
10/20/2020	Added I220 with I2C communication for dynamic voltage scaling
07/13/2020	Platform B, Revision B
06/11/2019	Update PVin min from 4.5V to 3V and PVin max from 17V to 14V Removed Vin from Recommended Operating Conditions Added Version C220_A_1_1: Improved soft start monotonicity, Enhanced pre bias startup
02/12/2019	Preliminary release

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