

Power Component: C420

Product Description

The 420 Power Component is a customizable sequencer designed to be used in the AmP™ platform. Combine the C420 component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management device.

Features

- Adjustable, programmable sequencer
- Power Good based sequencing
- Delay based sequencing (0.2 ms to 160 s)
- Grouping multiple rails
- Up to eight independent input and output controls
- Capable of sequencing external power rails
- Connect any signals to GPIOs for monitoring

Block Diagram

Figure 1 provides a block diagram of the C420 component which can be integrated with system power rails on the same AmP device or on another AmP device, if required, for a complete system sequence solution. Signal names alternate in color on Group boundaries.

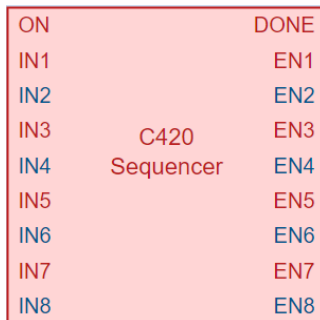


Figure 1. C420 block diagram

Description

The C420 component provides a customizable number of sequencer inputs and outputs with custom dependencies and programmable delays between each sequence step. The range of delay setting is from 0.2 ms to 160 s. The inputs and outputs connect to various status outputs and control inputs of the regulators and switches in the application. For systems with more than 1 AmP device or external power rail, the system sequencing dependencies are set by connecting the corresponding sequencers of the AmP devices via GPIOs. All parameters in Table 2 are customizable through AnDAPT's cloud-based WebAmp™ development software.

Sequencer Parameters
Enable input (ON)
Number of trigger inputs
Number of outputs
Groups
POLs
Sequencer dependency
Delay on each output
Sequence complete output (DONE)

Table 1. C420 parameters

System Characteristics

Parameter	Min	Max	Units
Sequencing delay	0.20	160000	ms
Number of POLs	2	8	-
Groups	2	Number of POLs	-

Table 2. C420 parameters

Sequencer Parameter Entry

The C420 outputs (called Enables or ENs) are sequenced from EN1, EN2... to ENn (where n denotes the number of sequence groups which can be set between 2 and 8). The target delay between rails can be independently set for each group in the configuration dialog box (Figure 2). The delay for the first output, EN1, is measured from the time ON goes high. The delays for the subsequent outputs (EN2 to EN8) are measured from the time the respective previous IN input (IN1 to IN7) goes high (see Application Example). If multiple ENs are part of a group, all the ENs of the group are pulled high at the same time. The delay is measured from the time when all of the INs in the previous group become high.

Sequencer

POL Specification

Number of POLs

Number of Seq. Groups

Time Specification

Time Step ms

Number of Steps

Maximum Delay ms

Delays			
	Channels	Target Delay ms	Actual Delay ms
Group 1	<input style="width: 30px;" type="text" value="1"/>	<input style="width: 30px;" type="text" value="3"/>	<input style="width: 30px;" type="text" value="3"/>
Group 2	<input style="width: 30px;" type="text" value="2"/>	<input style="width: 30px;" type="text" value="7"/>	<input style="width: 30px;" type="text" value="7"/>
Group 3	<input style="width: 30px;" type="text" value="1"/>	<input style="width: 30px;" type="text" value="4"/>	<input style="width: 30px;" type="text" value="4"/>

Figure 2. Sequencer parameter settings on WebAmp

Depending on the resolution of the delay step (time step) and the maximum delay (number of steps), the actual delay offered by the sequencer might be different from the set target delay. The actual achievable delays are seen under “Actual Delay” column in Figure 2. The available time step range is from 0.2 ms to 160,000 ms, and the number of steps can be selected to be any value among 2, 4, 8, 16, and 32. The use of minimal possible value for “number of steps” is recommended to economize device resources.

Application Example

Figure 2, Figure 3 and **Error! Reference source not found.** collectively depict a C420 sequencing example. The WebAMP design in Figure 4 consists of 4 power rails and the sequencer component. Grouping and rail startup sequencing is setup as shown in Figure 2. Number of steps is chosen to be 8 as it will provide all the time-step values as required in this design. In reference to Figure 3 when ON pin 24 is asserted high (event a), the C420 sequencer asserts EN1 high (event b) after waiting for a specified delay (set to 3ms through the parameter entry tab in Figure 2). When IN1 is signaled high (event c), from PGood1, it acts as the input, IN1, to the sequencer. Time between IN1 high and EN2 and EN3 high (event d and event e) is specified as 7ms. In a similar fashion, once both IN2 and IN3 signal high (event f), by PGood2 AND PGood3 respectively, rail-4 EN4 is pulled high after a delay of 4ms. Rail-2 and rail-3 startup at the same time as they belong to the same group.

IN4 high (event h) is followed by the Done going high (event i) indicating that the startup sequence is finished.

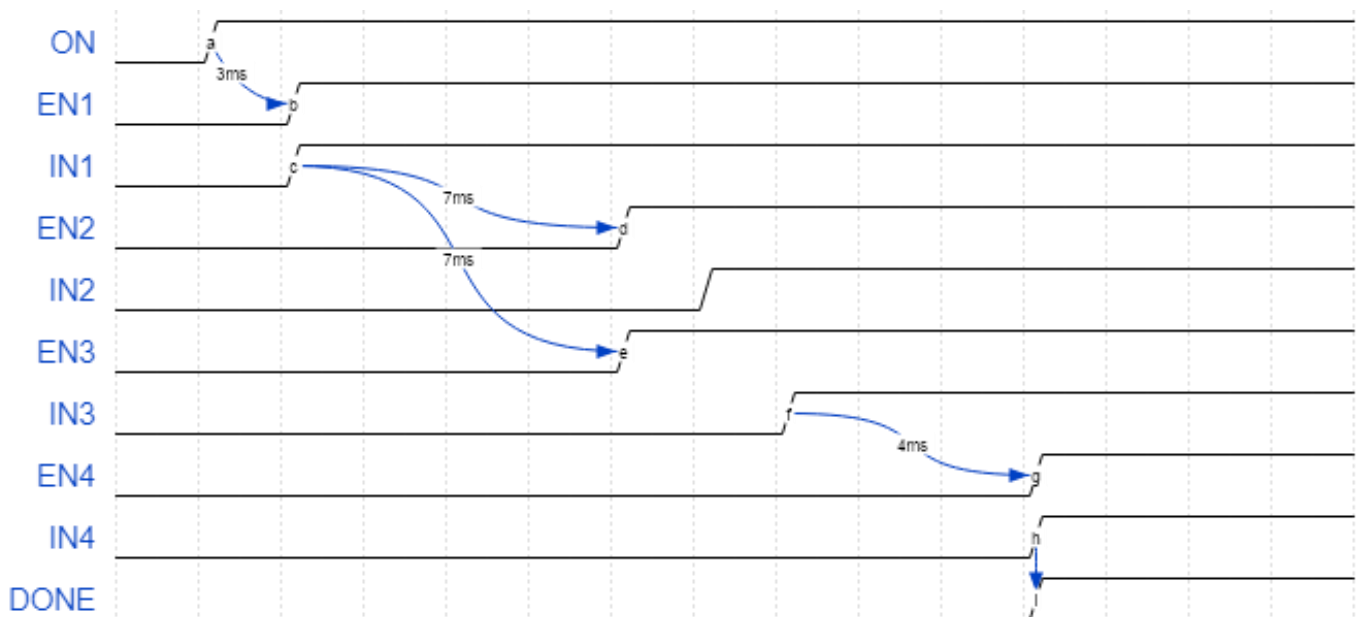


Figure 3. Sequencer application example