C431 Clock Source

Digital Component: C431

Product Description

The C431 Digital Component is a Clock Source function customizable to select one of eight clocks with Global Buffer inverting option. Combine the C431 component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management device.

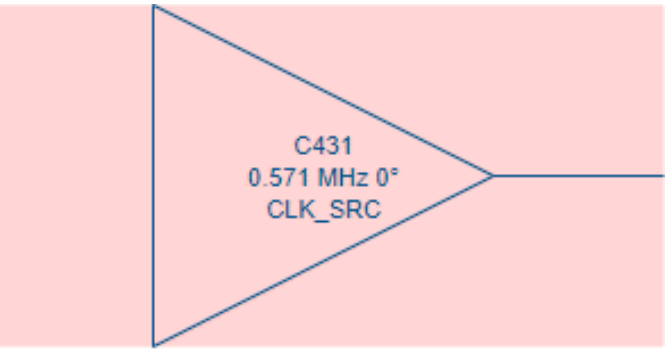
Features

- Select one of eight clocks
- Inverting option
- Drives Global Buffer

Block Diagram

Figure 1 provides a block diagram of the C431 component which can be integrated with system power rails on the AmP device for additional logic and state machine solutions.

Figure 1. C431 block diagram configured for 0.571 MHz



Product Detail

The C431 component provides customizable features described in detailed functionality Verilog Code below.

Verilog Code

```
module C431_Clock_Source(input CLK, output F);

parameter OUT_INV = 1'b0; // 0=no_bubble, 1=bubble

assign F = OUT_INV ^ CLK;

endmodule
```