

Product Description

The C432 Digital Component is a customizable Synchronous 4-bit register designed to be used in the AmP™ platform. Combine the C432 component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management device. The four flip-flops of the C432 are edge-triggered D-type flip-flops with a common clock. On the positive transition of the clock, the Q outputs are set to the logic states as directed by the inputs including Enable EN, Data D[3:0], Count-Up-Down/Shift-Left-Right UPLT, Load LD, and Carry-In/Shift-In CIN.

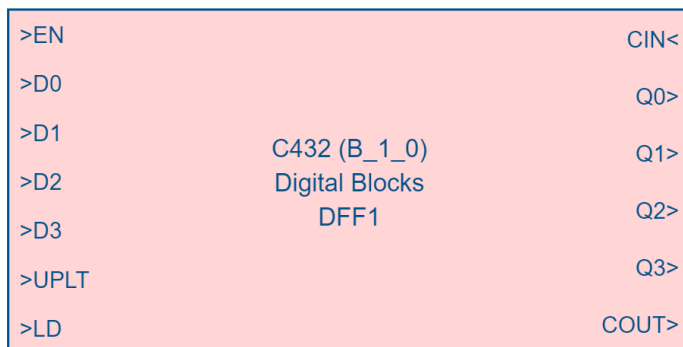
Features

- 4-bit Loadable Register
- Up-Down Counter expandable, Carry-In/Carry-Out
- Shift Left/Right Register expandable, Left-In/Right-In

Block Diagram

Figure 1 provides a block diagram of the C432 component which can be integrated with system power rails on the AmP device for additional logic and state machine solutions.

Figure 1. C432 block diagram



Pin Function and Description Table

Port Name	I/O	Description
EN	I	Synchronous Enable Load, Count, Shift on Clock
D[3:0]	I	Data In for Load Q[3:0]
UPLT	I	Count Up = H, Count Down = L Shift Left = H, Shift Right = L
LD	I	Q[3:0] = D[3:0] overrides Count/Shift
CIN	I	Carry_In or Shift_In
Q[3:0]	O	Register Out
COUT	O	Carry-Out

Product Detail

The C432 component provides customizable features described in the Pin Function and Description Table. The Counter/Shift-Register parameter specifies operation as outlined in the Function Tables below. Also, for detailed functionality see the Verilog Code below.

The C432 counter may be extended to multiple instances for 8, 12 16, 20, ... 32-bit Counter/Shift-Register functions.

Function Table, Parameter = Counter

Function	EN	D	UPLT	LD	CIN	Q	COUT
NOP, Hold	L	X	X	X	X	Q ₀	X
Load	H	D	X	H	X	D ₀	X
Count Up	H	X	H	L	L	Q ₀	Cout
Count Up	H	X	H	L	H	Q ₀ +1	Cout
Count Dn	H	X	L	L	L	Q ₀	Cout
Count Dn	H	X	L	L	H	Q ₀ -1	Cout

Function Table, Parameter = Shift Register

Function	EN	D	UPLT	LD	CIN	Q	COUT
NOP, Hold	L	X	X	X	X	Q ₀	X
Load	H	D	X	H	X	D ₀	X
Shift Left	H	X	H	L	Li	Lt Q ₀	Cout
Shift Right	H	X	L	L	Ri	Rt Q ₀	Cout

Verilog Code

```

module C432_DFF4(input CK0, EN, LD, UPLT, D0, D1, D2, D3, CIN,
output Q0, Q1, Q2, Q3, COUT);

parameter CNT = 1'b1; // 1 = Counter, 0 = Shift Register
wire CK0, CIN, EN, LD, UPLT, D0, D1, D2, D3;
reg [3:0] Q;
assign Q0=Q[0]; assign Q1=Q[1];
assign Q2=Q[2]; assign Q3=Q[3];
assign COUT = UPLT & CIN & Q[0] & Q[1] & Q[2] & Q[3]
| !UPLT & CIN & !Q[0] & !Q[1] & !Q[2] & !Q[3];

always @ (posedge CK0 ) begin
    if (EN&LD) Q<={D3,D2,D1,D0}; // Load
    else if (EN& CNT& UPLT) Q<=Q + CIN; // Count UP
    else if (EN& CNT&!UPLT) Q<=Q - CIN; // Count DOWN
    else if (EN&!CNT& UPLT) Q<={Q[2:0],CIN}; // Shift LFT
    else if (EN&!CNT&!UPLT) Q<={CIN,Q[3:1]}; // Shift RT
    else Q <= Q; // Hold
end

endmodule

```

Timing Characteristics

$PV_{IN} = V_{IN} = 12V$, $T_A = 25^\circ C$, $C_{vdd} = 10\mu F$, $C_{vcc} = 1\mu F$, unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Fmax	Clock Frequency			16†		MHz

† Programmable clock frequency

Clock Settings



The four flip-flops of the C432 are edge-triggered D-type flip-flops that change on the positive transition of the clock as selected from the Project Settings menu shown below.

Project Settings

Clock

Platform BoM

Verilog Library Versions

☐ Super Mode

Configure Clock A

Source

4 MHz

Ext Name

ClockA

Ext Frequency

1

MHz

Mode

7 Phases

Configure Clock B

Source

2 MHz

Ext Name

ClockB

Ext Frequency

1

MHz

Mode

Binary

Clock A		Clock B			
A Freq	A Phase	B Freq	B Phase	Select	Name
0.571 MHz	0°	0.008 MHz	0°	A	CK0
0.571 MHz	51°	0.016 MHz	0°	A	CK1
0.571 MHz	103°	0.031 MHz	0°	A	CK2
0.571 MHz	154°	0.063 MHz	0°	A	CK3
0.571 MHz	206°	0.125 MHz	0°	A	CK4
0.571 MHz	257°	0.25 MHz	0°	A	CK5
0.571 MHz	309°	0.5 MHz	0°	A	CK6
		1 MHz	0°	B	CK7

Oscillator A Select

none

Divide Clock A by

none

Ok

Parameter Settings

The C432 Counter/Shift-Register parameter specifies operation Register Type as a Counter or a Shift-Register. The clock is selected from CK0, CK1, ... CK7 in the Clock pull-down selector.

Counter Configuration

DFF4

Clock

CK0 0.571 MHz 0° ▼

Register Type

Counter ▼

Shift Register Configuration

DFF4

Clock

CK0 0.571 MHz 0° ▼

Register Type

Shift Register ▼

Power Component Version Table

Power Component Name	Description
C432_B_1_0	First Version B

C450_B Resource Usage

Counter

Resource Usage...

Number of AnD_DFF	4
io	13 used (Capacity 24)
clb	3 used (Capacity 64)
ptg	1 used (Capacity 2)
uLogic	20 used (Capacity 512)

Shift Register

Resource Usage...

Number of AnD_DFF	4
io	13 used (Capacity 24)
clb	3 used (Capacity 64)
ptg	1 used (Capacity 2)
uLogic	18 used (Capacity 512)

Additional Resources

[AnDAPT AmP Platform B datasheet](#)

Revision History

Date	Revision
11/13/2020	Preliminary release



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