Reset Generator

Power Component: C450_B

Product Description

The C450_B Reset Generator provides circuit initialization and timing supervision, primarily for processor-based systems. Combine the C450_B component with other Power Components to create a custom-defined, AnDAPT AmP on-demand power management device.

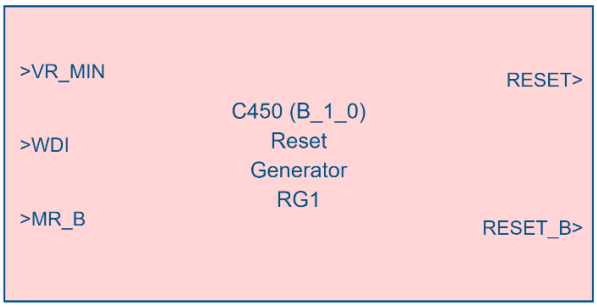
Features

- Power-On reset generator delay time: 1 ms to 5905 ms
- Watchdog timeout: 1 ms to 755,840 sec
- Supply voltage supervision range:
  adjustable from 0.6 V to 4.5 V
- Manual reset input
- Reset output available in active-low or active-high
- Open-Drain, Push-Pull option programmable using GPIO
- Temperature range: –40°C to +125°C operating junction temperature
- Power supply glitch immunity

Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing
- Programmable controls
- FPGA, processor, SSD, subsystem power control & sequencing
- DSPs, microcontrollers, or microprocessors
- Industrial equipment
- Automotive systems
- Portable and battery-powered equipment
- Intelligent instruments

- Figure 1: C450_B application schematic

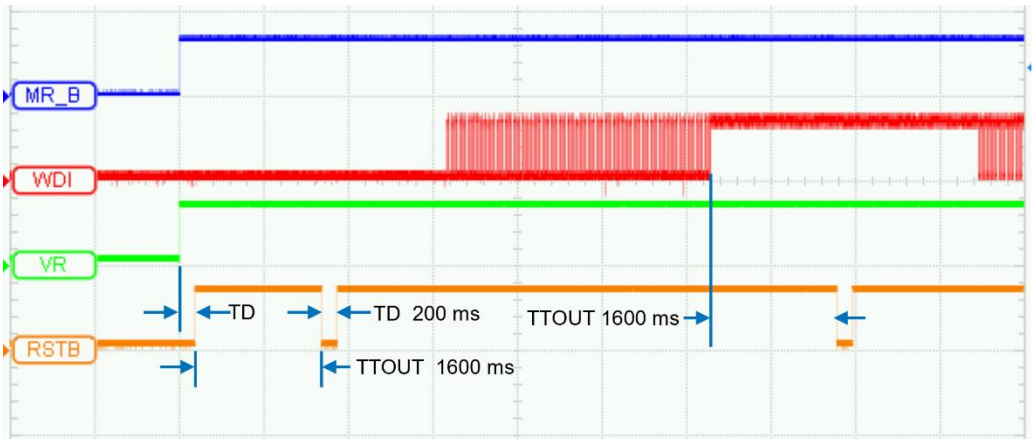


Product Detail

During power on, RESET asserts when the supply voltage input, VR is less than specified threshold. The VR input continuously monitors the voltage and asserts RESET whenever the voltage is less than the specified threshold. An internal timer delays the return of the RESET output to the inactive state (un-asserted) to ensure proper system reset. The delay time, TD, starts after VR is greater than specified threshold. After delay of TD, then RESET is un-asserted.

When watchdog timer input, WDI, when remaining high or low longer than the timeout period, TTOUT, asserts RESET. The timer clears when RESET is asserted or when WDI sees a rising edge or a falling edge.

Timing Diagram



Voltage = 5 V / div Time = 1 s / div

Pin Function and Description Table

Port Name	I/O	Description
MR_B*	I	Manual-reset input. Pull low to force a reset. RESET remains low as long as MR_B is low and for the time-out period after MR_B goes high. Connect to high when unused.
RESET	O	Active-high reset output. May be push-pull or open-drain at GPIO pin.
RESET_B	O	Active-low reset output. May be push-pull or open-drain at GPIO pin.
VR	I	Supply Voltage input. Analog input. When below specified threshold, holds RESET to low. On going above threshold, delays TD, then sets RESET low.
WDI*	I	Watchdog timer input. If WDI remains high or low longer than the timeout period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge. Connect to high or low when unused.

*Polarity is programmable

Timing Characteristics

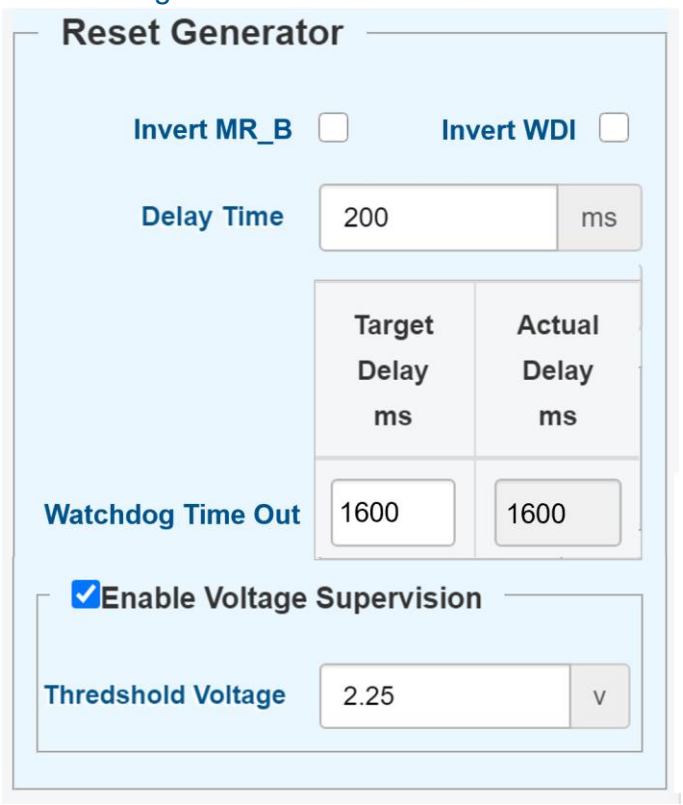
PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
TTOUT	Watchdog Time Out	CK0 = 0.571 MHz	1.44	1.6†	1.76	s
TD	Delay Time	CK0 = 0.571 MHz	180	200†	220	ms

† Programmable delay times

Parameter Settings

Basic Configuration



Power Component Version Table

Power Component Name	Description
C450_B_1_0	First Version B

C450_B Resource Usage

TD = 200 ms, TTOUT = 200 ms

Resource Usage...

io	5 used (Capacity	24)
clb	2 used (Capacity	64)
pmt	1 used (Capacity	16)
atc	1 used (Capacity	6)
corner	1 used (Capacity	4)
ptg	1 used (Capacity	2)
uLogic	15 used (Capacity	512)

TD = 200 ms, TTOUT = 1600 ms

Resource Usage...

io	5 used (Capacity	24)
clb	3 used (Capacity	64)
pmt	1 used (Capacity	16)
atc	1 used (Capacity	6)
corner	1 used (Capacity	4)
ptg	1 used (Capacity	2)
uLogic	23 used (Capacity	512)

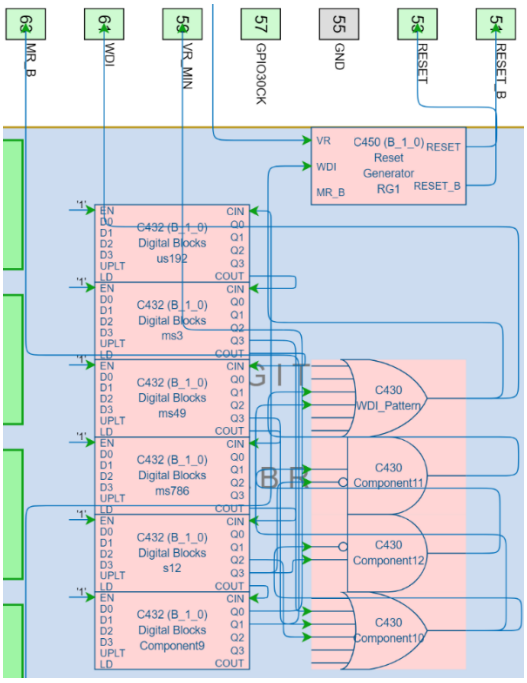
TD = 200 ms, TTOUT = 25600 ms

Resource Usage...

io	5 used (Capacity	24)
clb	4 used (Capacity	64)
pmt	1 used (Capacity	16)
atc	1 used (Capacity	6)
corner	1 used (Capacity	4)
ptg	1 used (Capacity	2)
uLogic	26 used (Capacity	512)

Test Circuit

The circuit used to generate timing signals in the Typical Characteristics is show below.

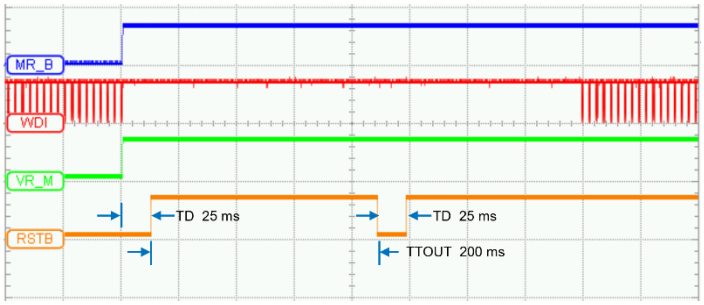


Typical Characteristics

Unless otherwise specified: TA = 25°C

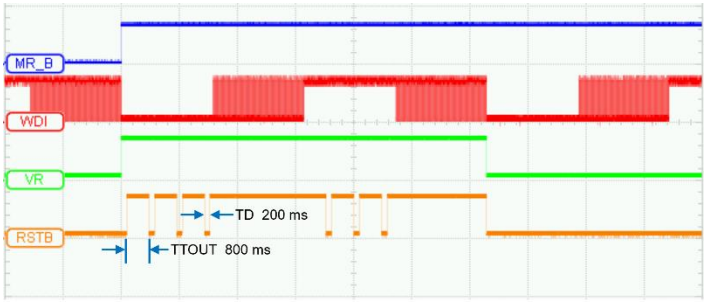
Delay Time and Watchdog Timeout

TD = 25 ms TTOUT = 200 ms



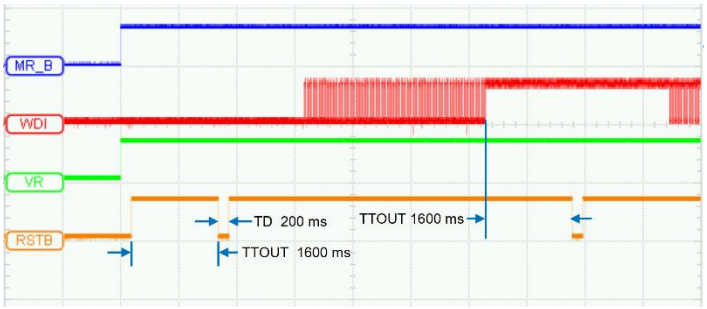
Time = 0.05 s / div

TD = 200 ms TTOUT = 800 ms



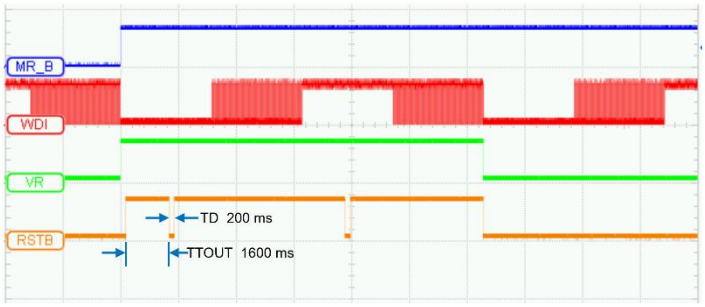
Time = 2 s / div

TD = 200 ms TTOUT = 1600 ms



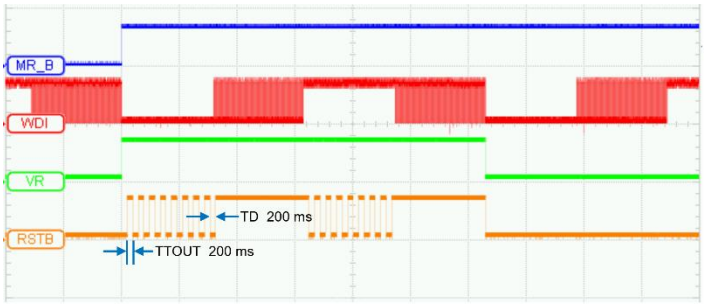
Time = 1 s / div

TD = 200 ms TTOUT = 1600 ms



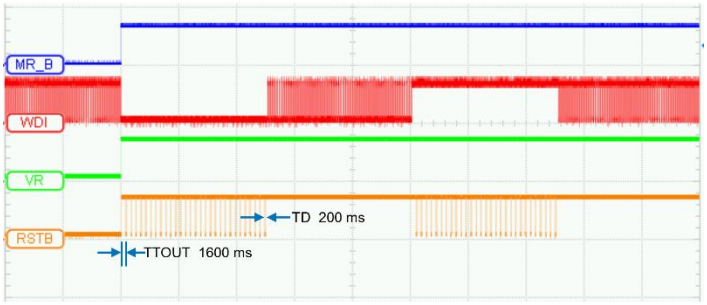
Time = 2 s / div

TD = 200 ms TTOUT = 200 ms



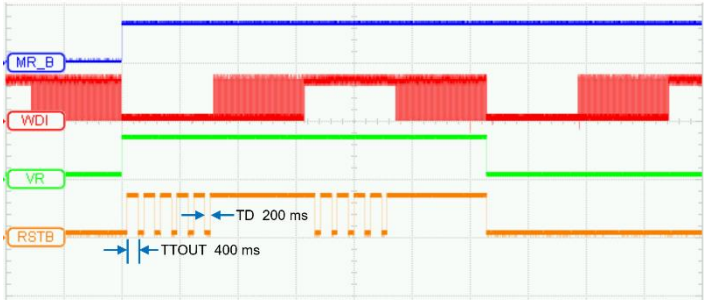
Time = 2 s / div

TD = 200 ms TTOUT = 1600 ms



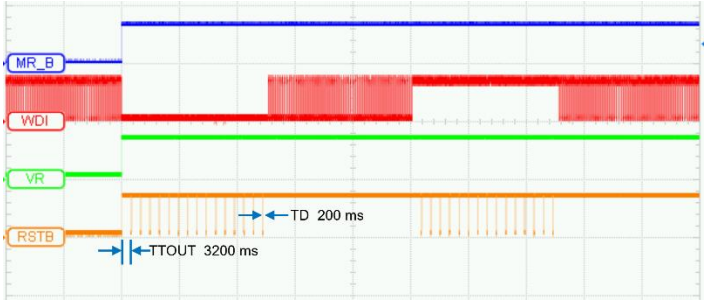
Time = 20 s / div

TD = 200 ms TTOUT = 400 ms



Time = 2 s / div

TD = 200 ms TTOUT = 3200 ms



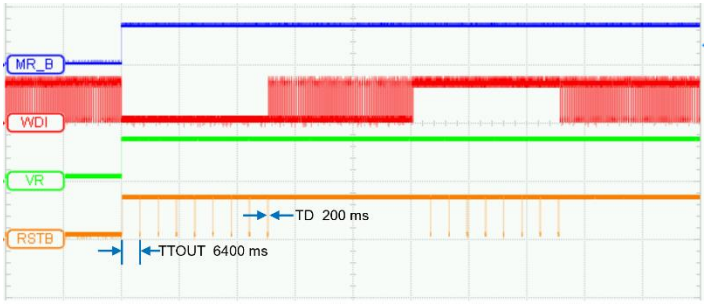
Time = 20 s / div

Typical Characteristics

Unless otherwise specified: TA = 25°C

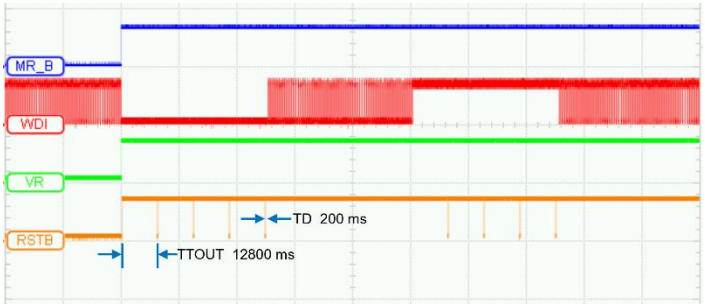
Delay Time and Watchdog Timeout

TD = 200 ms TTOUT = 6400 ms



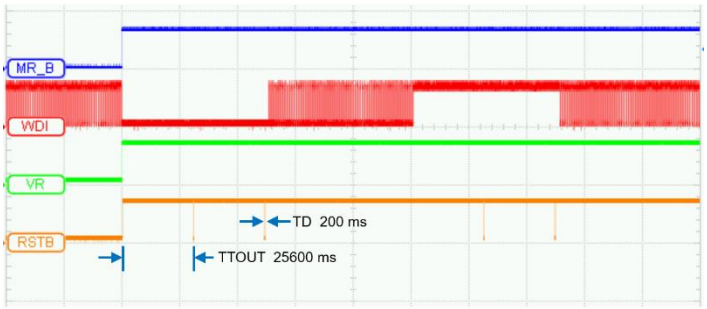
Time = 20 s / div

TD = 200 ms TTOUT = 12800 ms



Time = 20 s / div

TD = 200 ms TTOUT = 25600 ms



Time = 20 s / div

Additional Resources

- AnDAPT AmP Platform datasheet

Revision History

Date	Revision
09/28/2020	Preliminary release

AnDAPT

On-Demand Power Management

www.AnDAPT.com

Trademarks