Low-Dropout (LDO) Regulator

Power Component: C710_B, C711_B

Product Description

The C710_B/C711_B Power Component is a customizable Low-Dropout Voltage Regulator with standard source-side regulation. Combine the C710_B/C711_B component with other Power Components to create a highly integrated, custom-defined, AnDAPT AmP™ on-demand power management device.

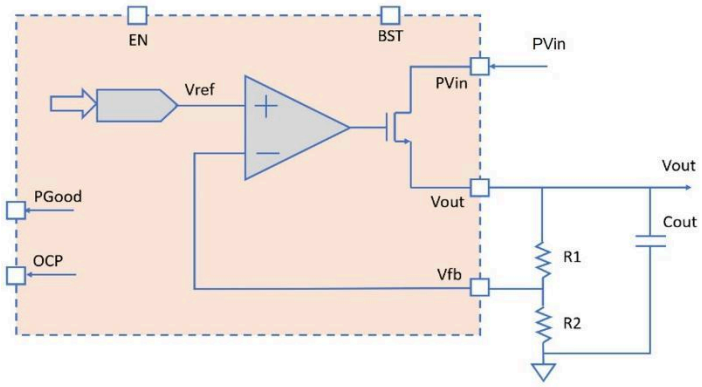
Features

- Linear, constant voltage, low-dropout regulator
- Adjustable V_{OUT}
  - C710_B: From 0.6V to 3.3V
  - C711_B: From 0.6V to 1.8V
- Maximum output current: 1A with “Internal” feedback and 3A with “External” feedback
- 1% typical line and load regulation
- Very low dropout :100 mV dropout @ 0.1A
- Short-circuit protection (SCP)
- Protection: Overcurrent (OCP), and Over Temperature (OTP)
- Power-good and OCP flag outputs and Enable input
- Soft-Start
  - C710_B: CC soft-start with programmable soft-start current
  - C711_B: CV soft-start with programmable soft-start time
- –40°C to +125°C operating junction temperature
- Utilizes one SIM element of an AmP Platform

Applications

- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing
- Imaging: CMOS Sensors, Video ASICs
- Test and Measurement
- Regulated power noise sensitive, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and PLLs with integrated VCOs

External Feedback with resistor divider (C710_B only)

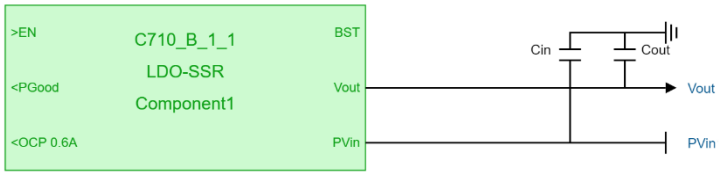


C710_B vs C711_B Comparison Table

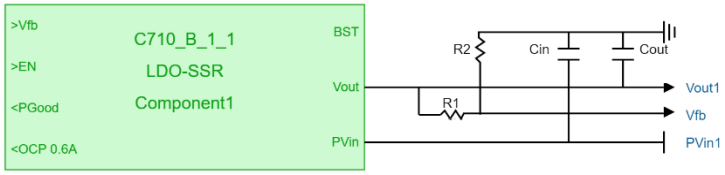
	C710_B	C711_B
Soft-Start	Constant-Current * **Soft-start current programmable*	Constant-Voltage* **Soft-start time programmable*
Vout Range	Internal F/B: 0.6V – 3.3V External F/B: 0.6V – 3.3V	Internal F/B: 0.6V – 1.8V External F/B: 0.6V – 1.8V

Figure 1: C710_B, C711_B application schematic

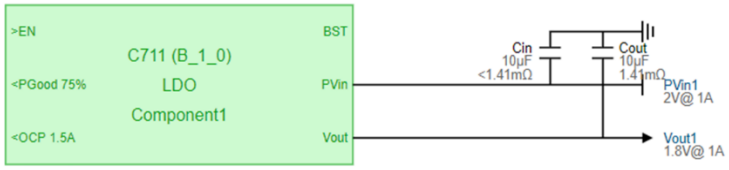
C710 Internal Feedback



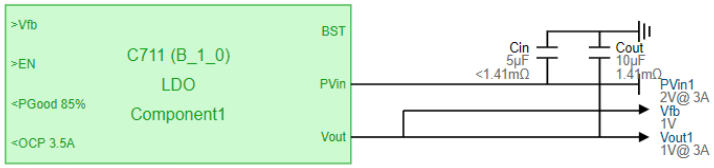
C710 External Feedback



C711 “Internal” Feedback



C711 “External” Feedback



Product Details

The C710_B/C711_B is a 3A general purpose low-dropout (LDO) regulator. The maximum current is defined by the AmP device selected. The integrated current sense provides overcurrent protection (OCP) and short circuit protection.

The C710_B is designed to cover the voltage range (0.6V to 3.3V) while the C711_B covers the voltage range from 0.6V to 1.8V

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmP™ development software. The C710_B/C711_B component has customizable control and status pins including an enable input, an optional power-good output, and optional output flag to signal when the system triggers an overcurrent (OCP) condition.

The C710_B/C711_B also incorporates a soft start feature to mitigate against inrush current. However, the C710_B implements a CC based soft-start with programmable soft-start current while the C711_B implements a CV based soft-start with a programmable soft-start time (from 0.5ms to 8.0ms). Sequencing options are available when used in conjunction with the C420 customizable Sequencer, by interconnecting signals EN, PGood to provide dependencies and delays between each sequence step.

The C710_B/C711_B has a minimum load requirement of 200uA.

VIN Headroom Requirements

The C710_B/C711_B is an NMOS based LDO with PV_{IN} requirements (LDO input voltage) as shown in Table2. In addition there is a VIN headroom requirement (AMP chip supply voltage) above Vout for correct operation. This is typically 3V for LDO Vout values up to 2.5V and 5.5V for Vout values above 2.5V. This means, for example, for 5V VIN applications (i.e. 5V +/- 10%) the largest C710_B/C711_B Vout that can be used is 1.5V. However there are applications solutions which may be applied to address this e.g. charge-pump approaches to boost the VIN voltage. For further information please also refer to Application Note 210202 ("*LDOs and Load-Switches Implementation in 5V input applications on AmP8DB6 - Platform-B*") on the Resource Center page .

Maximum Current, I_{OUT}

Part number	AmP Platform	IOUT Max	VOUT Max
C710 (Internal f/b)	AmPxDB6	1A	3.3V
C710 (External f/b)	AmPxDB6	3A	3.3V
C711 (Internal f/b)	AmPxDB6	1A	1.8V
C711 (External f/b)	AmPxDB6	3A	1.8V

Recommended Capacitance

Product	Cout	Cin
C710/C711 Internal (0-1A)	>=10uF	>=Cout
C710/C711 External f/b (0-1A)	>=22uF	>=Cout
C710/C711 External f/b (1-3A)	>=47uF	>=Cout

Note: Output capacitor of previous converter (if used) counts as part of Cin for LDO. If that capacitor is far from the optimum location of Cin, then add 1µF local capacitor close to the PV_{IN} pin of LDO.

Customizable Options

Table 1 lists the various customizable options available for for the C710 Power Component.

These options are set in the WebAmp development software.

Table 1: C710 Customizable Options

Option	Units
Input voltage	V
Output voltage	V
Output Current	A
Enable OCP output to signal when overcurrent protection is triggered	On/Off
Use optional PGood output to signal “power good”	On/Off
Soft-Start Current (C710 only)	A
Soft-Start Time (C711 only)	ms

System Characteristics

Table 2 lists the system characteristics for the C710_B/C711_B Power Component when implemented in an AnDAPT AmP device.

Table 2: C710_B, C711_B System Characteristics

Parameters	Min	Typ	Max	Units
Input Drain Voltage (PV_{IN}) *	V_{OUT}+ V_{DO}		17	V
VIN Headroom ** Vout ≤ 2.5V Vout > 2.5V		 3V 5.5V		
Output Voltage (V_{OUT}) C710	0.6		3.3	V
Output Voltage (Vout) C711	0.6		1.8	V
Output Current (I_{OUT}) Internal f/b External f/b			 1 3	 A A
Dropout Voltage (V_{DO}) C710/C711 Internal f/b I_{out} = 0.1A Internal f/b I_{out} = 1A External f/b I_{out} = 0.1A External f/b I_{out} = 1A External f/b I_{out} = 3A		 50 100 50 100 250	 100 200 100 200 400	 mV mV mV mV mV
O/P Accuracy Iout = 0.2mA* **			1%	
Load regulation – Internal f/b		16		mV/A
Load regulation – External f/b		4		mV/A
Line regulation (ΔVout/ΔPVin)		0.5		%
Current Limit – OCP	1			A

*Note: The maximum power dissipation for the C710_B,/C711_B, $(PV_{IN}-V_{OUT})*I_{OUT}$, is limited to 1.5W

**: Please refer to the datasheet section “VIN Headroom Requirements” on pg.2

*** For Vout > 2.5V Accuracy will fall to 2%

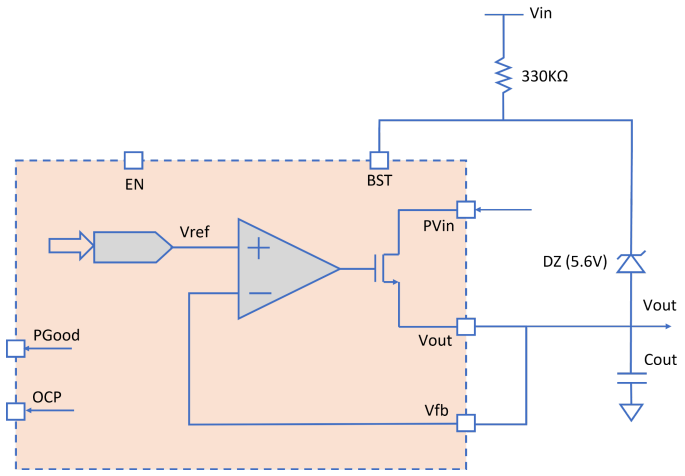
Pre-bias Start Up

C710_B/C711_B can start with a pre-bias voltage on the output. Table 3 lists the limit for startup with an output pre-bias.

Table 3: C710_B, C711_B pre-bias limits

Parameter	Min	Typ	Max	Units
Permitted output pre-bias	0		V_{OUT}	V

For V_{OUT} > 2 V, if the pre-bias functionality is necessary, additional circuitry including a Zener diode between BST pin and V_{OUT} and a 330kΩ resistor to V_{IN} is required, as shown in Figure below.



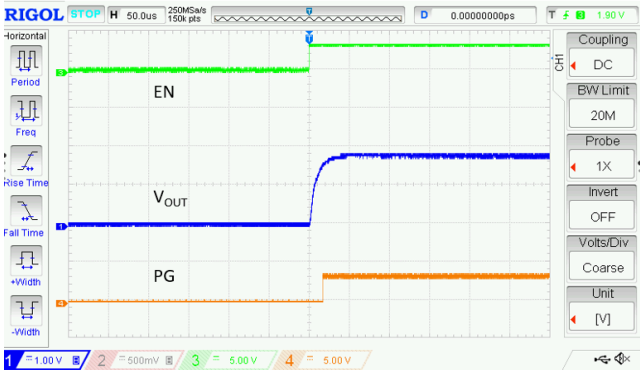
Port Name Table

Port Name	Analog/ Digital	Input/ Output	Description
PV_{IN}	Analog	I/P	LDO Analog I/P
V_{OUT}	Analog	O/P	LDO O/P
Vfb	Analog	I/P	Feedback I/P from O/P resistor divider
BST	Analog	I/P	Bootstrap I/P. This pin should be left floating. [+refer to Figure 1]
EN	Digital	I/P	Enable I/P. HIGH => LDO Enabled LOW => LDO Disabled
Pgood	Digital	O/P	Power Good indicator. HIGH => Vout > Pgood level
OCP	Digital	O/P	Over Current Indicator HIGH => O/P Current exceeds OCP level

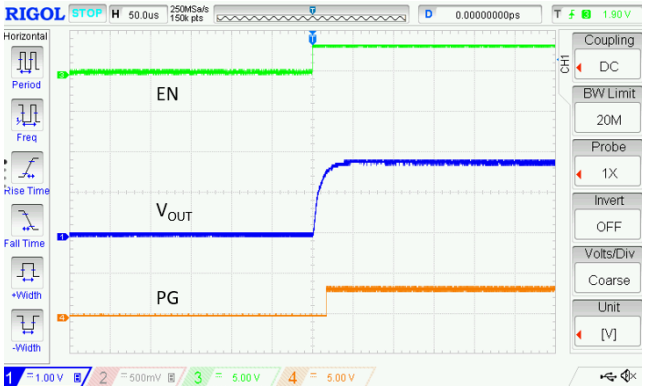
Typical Characteristics

Unless otherwise specified: VIN=12V; TA = 25°C

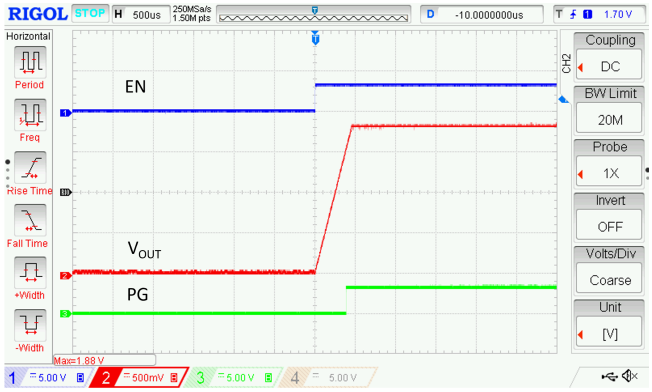
Soft Start C710 PV_{IN} = 2V, V_{OUT} = 1.8V No load



Soft Start C710 PV_{IN} = 2V, V_{OUT} = 1.8V, 2 Ohm



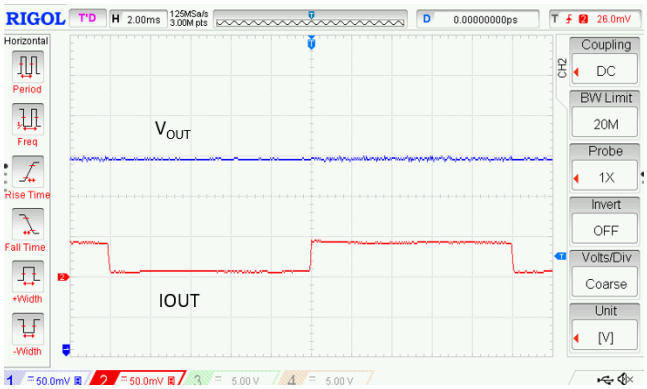
Soft Start C711 0.5ms Soft-Start Time



Soft Start C711 7.0ms Soft-Start Time

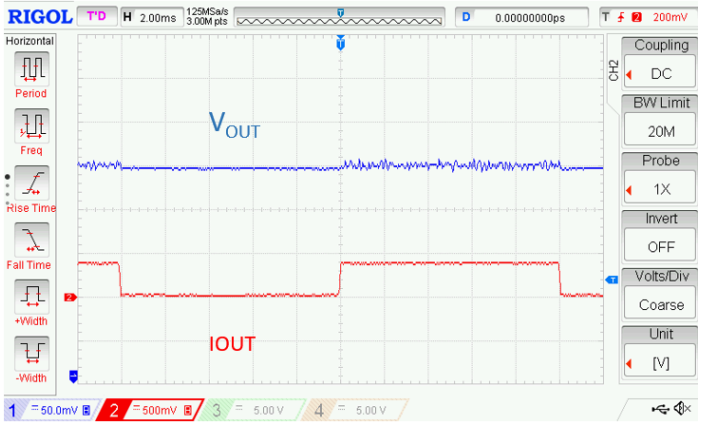
Transient Response C710_B, C711_B

PV_{IN} = 1.8V, V_{OUT} = 1.5V I_{OUT} = 0 to 100 mA Load step



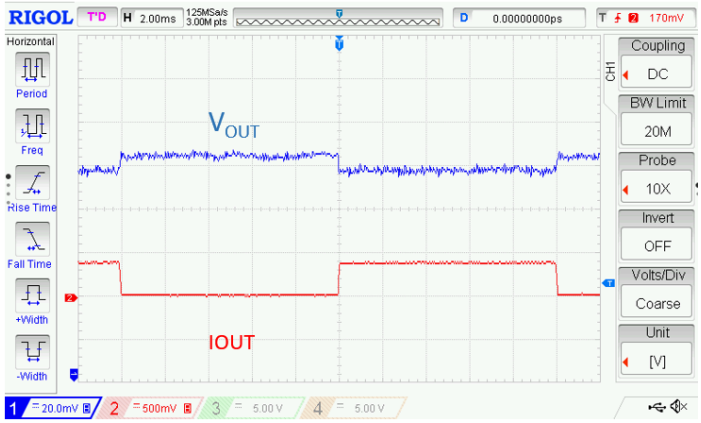
Transient Response C710_B, C711_B

PV_{IN} = 1.8V, V_{OUT} = 1.5V I_{OUT} = 0 to 0.5A Load step



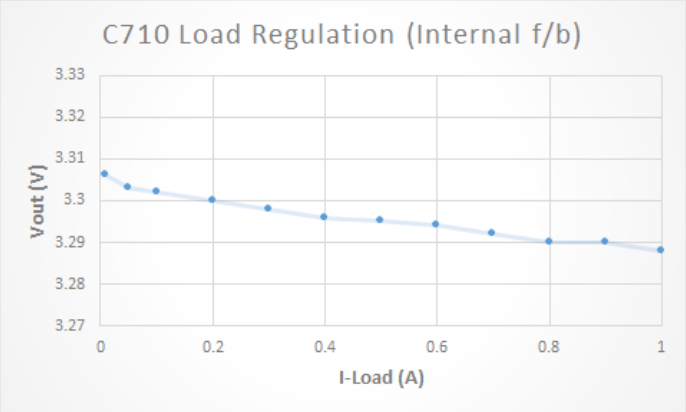
Transient Response C710_B, C711_B

PV_{IN} = 1.8V, V_{OUT} = 1.5V I_{OUT} = 0 to 1A Load step



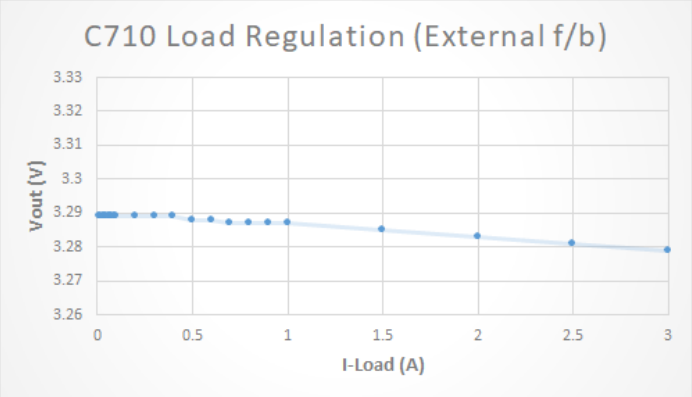
Load Regulation C710_B

V_{OUT} = 3.3V, Cout = 10µF



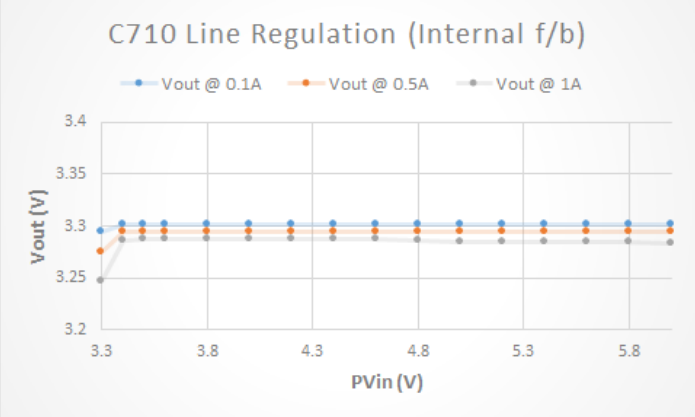
Load Regulation C710_B

V_{OUT} = 3.3V, Cout = 47µF



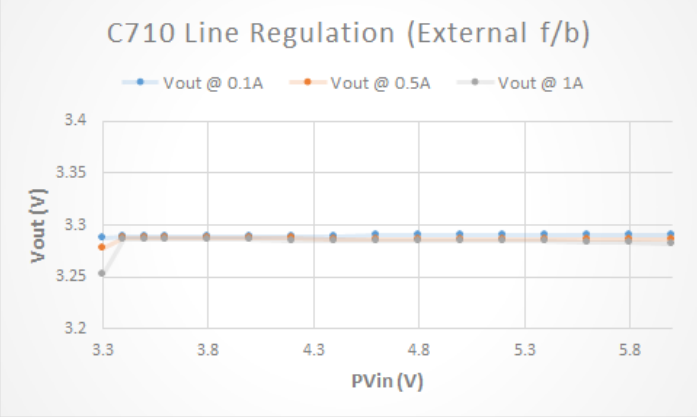
Line Regulation C710_B

V_{OUT} = 3.3V, Cout = 10µF



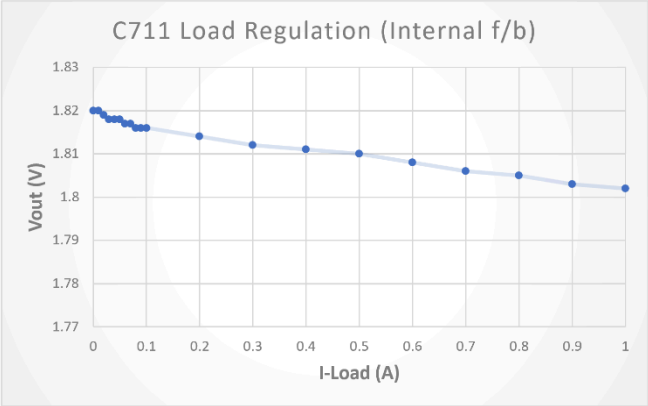
Line Regulation C710_B

V_{OUT} = 3.3V, Cout = 47µF



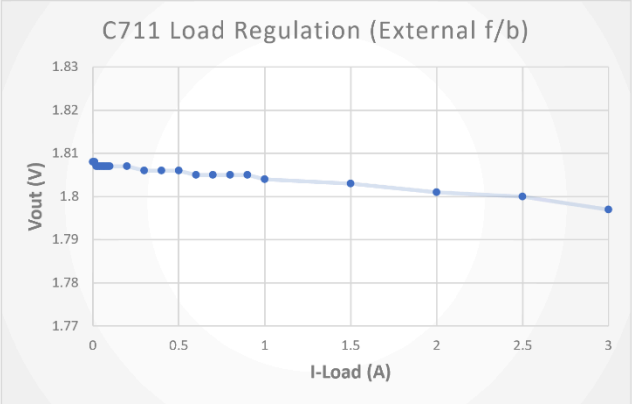
Load Regulation C711_B

V_{OUT} = 1.8V, Cout = 10µF



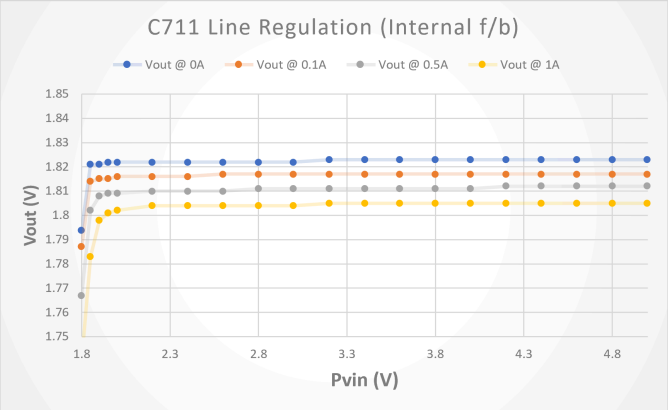
Load Regulation C711_B

V_{OUT} = 1.8V, Cout = 47µF



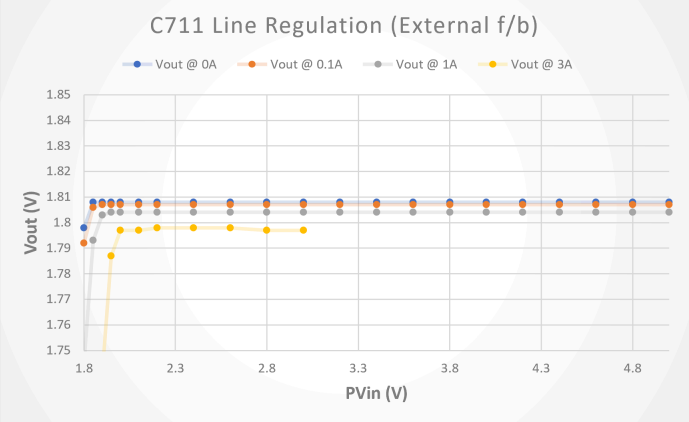
Line Regulation C711_B

V_{OUT} = 1.8V, Cout = 10µF



Line Regulation C711_B

V_{OUT} = 1.8V, Cout = 47µF

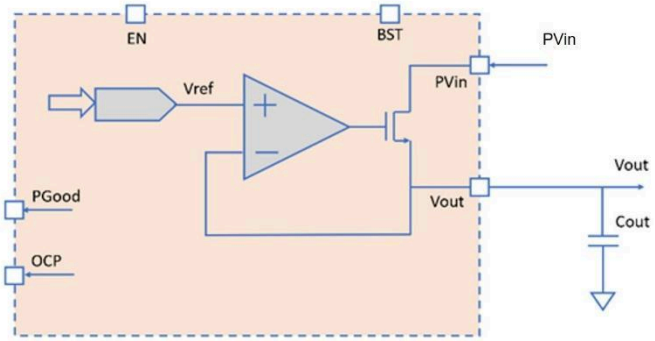


Theory of Operation

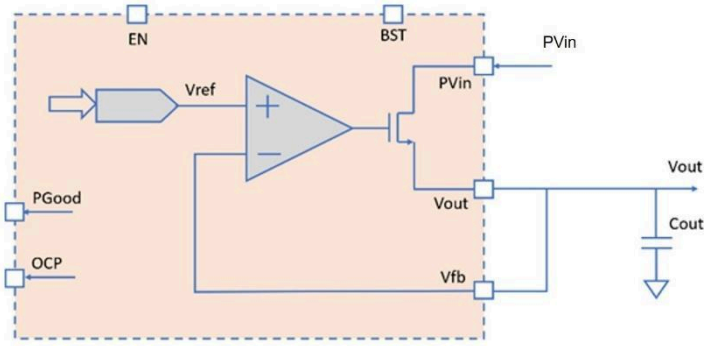
The C710_B/C711_B is a linear voltage regulator. It consists of a reference voltage, a feedback path for the output voltage (which may use a resistor divider) to compare it to the reference, a feedback amplifier, and a series pass transistor (NMOS in the case of the C710_B/C711_B), whose voltage drop is controlled by the amplifier to maintain the output at the required value.

The C710_B/C711_B offers two configurations, Internal feedback and External feedback. External feedback configuration requires the use of a Vfb pin to sense the Vout voltage and offers the best load regulation performance at ~4mV/A as well as operating up to 3A output current while the Internal feedback configuration eliminates the need for a Vfb pin but provides lower load regulation at ~16mV/A and operates up to 1A output current. Block diagrams are shown below:

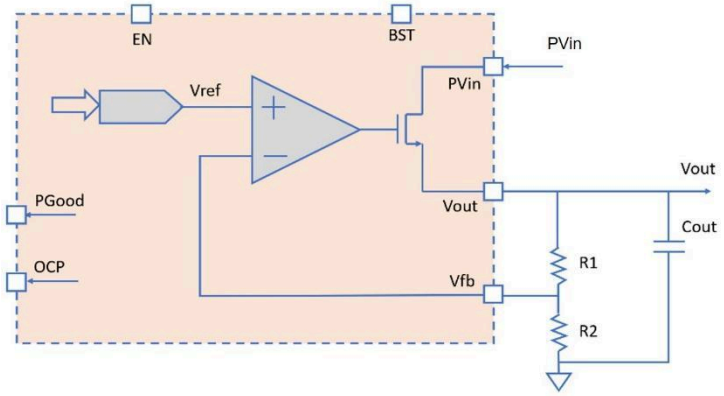
C710_B/C711_B Internal Feedback



C710_B/C711_B External Feedback



External Feedback with resistor divider (C710_B only)



If the load current increases causing the output to drop the error voltage will increase and the amplifier output will fall. This in turn causes the voltage across the pass transistor to decrease and the output will return to its original value. Note that a linear regulator efficiency depends on the voltage difference between input and output and is nominally given by:

100 x (V_{OUT} x I_{OUT})/(V_{IN} x I_{IN})

= 100 x V_{OUT} / V_{IN} assuming I_{OUT} = I_{IN}

with the power loss being (V_{IN} - V_{OUT}) x I_{OUT}.

The maximum power dissipation for the C710_B, C711_B is limited to 1.5W.

Protection Features

The C710_B/C711_B provides protection features including OCP and OTP. OCP can be enabled or disabled using the WebAmp interface.

Over Current Protection

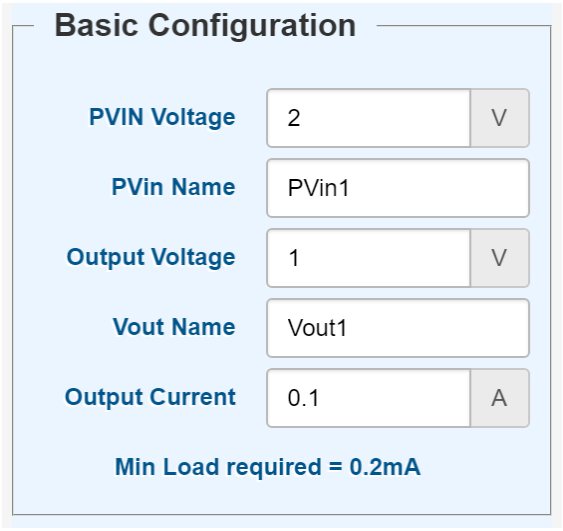
The Over Current Protection (OCP) digital port may be connected to a GPIO pin or a control component such as the C430 Digital Block Gate to indicate the output over current status. OCP goes high when output current, I_{OUT}, is greater than the OCP threshold. OCP goes low when output current, I_{OUT}, is less than the OCP threshold. On detection of OCP, the C710_B/C711_B will shut down. If OCP is triggered, the C710_B/C711_B will power down and PGood will go low. In that case, an EN cycling low-to-high, will restart the C710_B/C711_B with a new Soft Start cycle.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C710_B/C711_B will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C710_B/C711_B with a new Soft Start cycle.

Feature Description

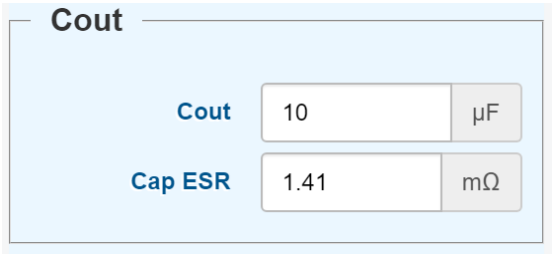
Basic Configuration

Default parameters may be changed per user requirement.



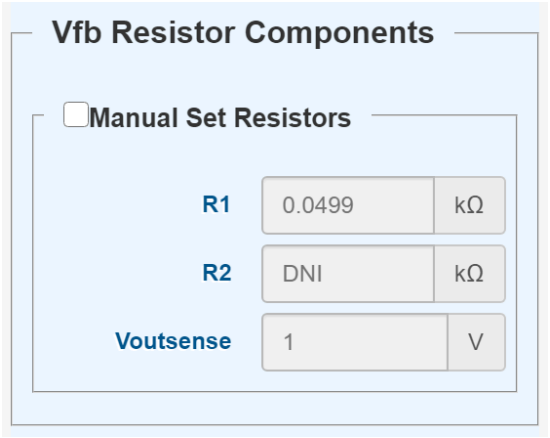
C_{OUT} Component Selection

The minimum output capacitance for stability is 10 µF. for internal feedback and 47µF for external feedback.



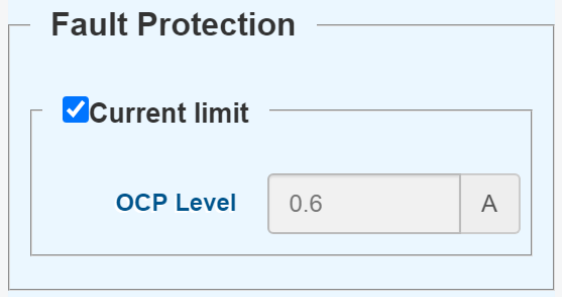
Vfb Resistor Components

C710: Resistor divider R1 and R2 default to 49.9 Ω and open (infinity) for direct feedback of the output to the Vfb pin.



Fault Protection

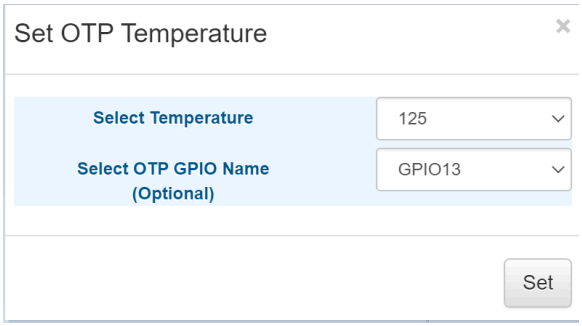
Over Current Protection, OCP, indicates the output over current greater or less than OCP.



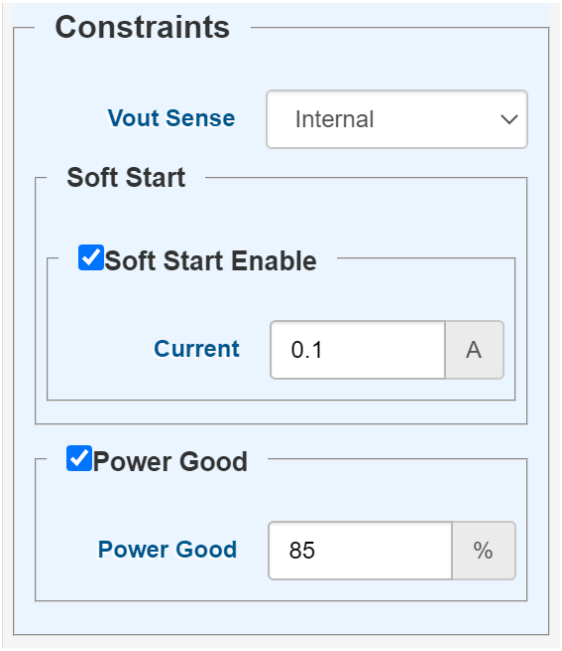
Over Temperature Protection (OTP):

Over Temperature Protection, OTP, indicates thermal shutdown has occurred. The OTP is set by default at 125 Deg C at the device level, routable to a GPIO.

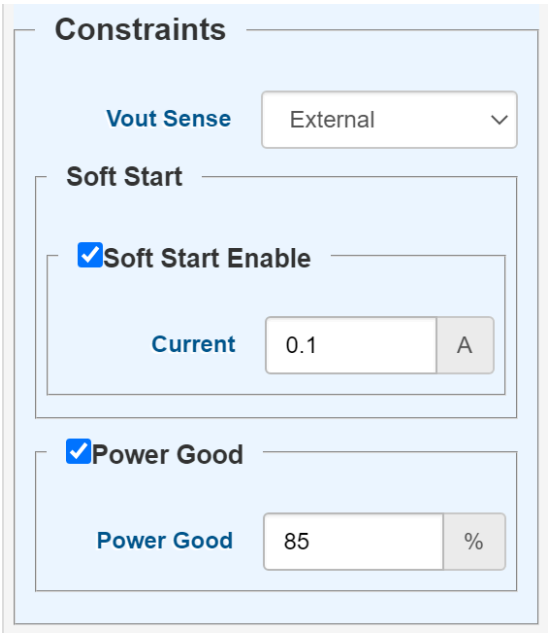
OTP
125°C



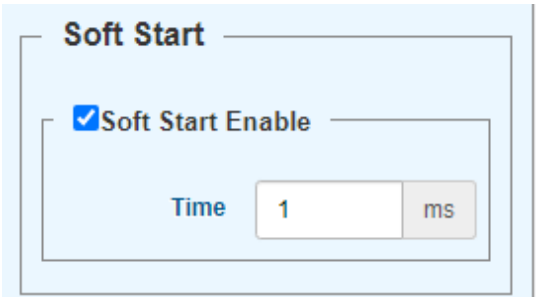
Constraints, Internal Feedback



Constraints, External Feedback



Constraints (C711 Soft-Start)



Power Component Version Table

Power Component Name	Description
C710_B_1_2	Fixes issue in External mode when using a resistor divider
C710_B_1_1	Added “internal” configuration for low current (<1A) applications
C711_B_1_1	Fix timing issue in startup ramp counter
C710_B_1_0, C711_B_1_0	First Release on Platform B

C710_B Internal F/B Resource Usage

Circuit Stats...
- Number of AnD_Temp_Sensor 1
- Number of AnD_SIM_Linear 1
- Number of AnD_SIM_Protect 1
- Number of AnD_SIM_Sense 1
- Number of AnD_Analog_IO 6
- Number of AnD_ATC_IO 3
- Number of AnD_ATC_Comp 3
- Number of AnD_Nref_fix 4
- Number of AnD_PTG_Phase_Count 1
- Number of AnD_PTG_GBUF 1
- Number of AnD_PTG_OSC 1
- Number of AnD_DFFN 7
- Number of AnD_DFF 3
- Number of LUT4 25

Resource Usage...
- io 3 used (Capacity 24)
- clb 6 used (Capacity 64)
- sim 1 used (Capacity 8)
- atc 2 used (Capacity 6)
- corner 3 used (Capacity 4)
- ptg 1 used (Capacity 2)
- uLogic 25 used (Capacity 512)

Components Stats...
- $techmap\otp_fuse_module
  - AnD_DFF 3
  - AnD_DFFN 7
- component_1
  - AnD_ATC_Comp 2
  - AnD_Nref_fix 3
  - AnD_SIM_Linear 1
  - AnD_SIM_Protect 1
  - AnD_SIM_Sense 1
- otp_fuse_module
  - AnD_ATC_Comp 1
  - AnD_Nref_fix 1

C710_B External F/B Resource Usage

Circuit Stats...
- Number of AnD_Temp_Sensor 1
- Number of AnD_SIM_Linear 1
- Number of AnD_SIM_Protect 1
- Number of AnD_SIM_Sense 1
- Number of AnD_Analog_IO 6
- Number of AnD_ATC_IO 4
- Number of AnD_ATC_Comp 3
- Number of AnD_ATC_Summer 1
- Number of AnD_Nref_fix 4
- Number of AnD_PTG_Phase_Count 1
- Number of AnD_PTG_GBUF 1
- Number of AnD_PTG_OSC 1
- Number of AnD_DFFN 7
- Number of AnD_DFF 3
- Number of LUT4 26

Resource Usage...
- io 4 used (Capacity 24)
- clb 6 used (Capacity 64)
- sim 1 used (Capacity 8)
- atc 2 used (Capacity 6)
- corner 3 used (Capacity 4)
- ptg 1 used (Capacity 2)
- uLogic 26 used (Capacity 512)

Components Stats...
- $techmap\otp_fuse_module
  - AnD_DFF 3
  - AnD_DFFN 7
- component_1
  - AnD_ATC_Comp 2
  - AnD_ATC_Summer 1
  - AnD_Nref_fix 3
  - AnD_SIM_Linear 1
  - AnD_SIM_Protect 1
  - AnD_SIM_Sense 1
- otp_fuse_module
  - AnD_ATC_Comp 1
  - AnD_Nref_fix 1

C711_B Internal F/B Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_SIM_Linear	1
Number of AnD_SIM_Protect	1
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	6
Number of AnD_ATC_IO	3
Number of AnD_ATC_Comp	3
Number of AnD_PMT	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	7
Number of AnD_DFF	10
Number of LUT4	39

Resource Usage...

io	3 used	(Capacity 24)
clb	8 used	(Capacity 64)
pmt	1 used	(Capacity 16)
sim	1 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	3 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	39 used	(Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	7

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_ATC_Comp	2
AnD_Nref_fix	3
AnD_PMT	1
AnD_SIM_Linear	1
AnD_SIM_Protect	1
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

C711_B External F/B Resource Usage

Circuit Stats...

Number of AnD_Temp_Sensor	1
Number of AnD_SIM_Linear	1
Number of AnD_SIM_Protect	1
Number of AnD_SIM_Sense	1
Number of AnD_Analog_IO	6
Number of AnD_ATC_IO	4
Number of AnD_ATC_Comp	3
Number of AnD_ATC_Summer	1
Number of AnD_PMT	1
Number of AnD_Nref_fix	4
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFFN	7
Number of AnD_DFF	10
Number of LUT4	40

Resource Usage...

io	4 used	(Capacity 24)
clb	8 used	(Capacity 64)
pmt	1 used	(Capacity 16)
sim	1 used	(Capacity 8)
atc	2 used	(Capacity 6)
corner	3 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	40 used	(Capacity 512)

Components Stats...

$techmap\component_1

AnD_DFF	7

$techmap\otp_fuse_module

AnD_DFF	3
AnD_DFFN	7

component_1

AnD_ATC_Comp	2
AnD_ATC_Summer	1
AnD_Nref_fix	3
AnD_PMT	1
AnD_SIM_Linear	1
AnD_SIM_Protect	1
AnD_SIM_Sense	1

otp_fuse_module

AnD_ATC_Comp	1
AnD_Nref_fix	1

Additional Resources

- AnDAPT AmP Platform datasheet

Revision History

Date	Revision
1/16/2024	Added pre-bias startup requirements
10/20/2022	Updated headroom requirements
05/24/2022	Added Recommended Capacitance, page 2 and updated Version Table Added dropout, V_{IN} headroom and load regulation to Specifications
07/12/2021	Updated COUT Component Selection
10/13/2020	Added Block Diagram to page 1
08/17/2020	Added C711_B
06/19/2020	Platform B, revision B release
07/05/2019	Added C710_A_2_0 conditions for Load Regulation and Constraints
11/27/2018	Preliminary release

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