PWM Single-Phase DrMOS Controller

Power Component: C860

Product Description

The C860 Power Component is a customizable, single-phase, voltage-mode DrMOS controller designed for point-of-load (POL) applications. Combine the C860 with other Power Components to create a custom-defined, AnDAPT AmP on-demand PMIC.

Power components are software components, accessible through WebAmP™, allowing users to create their own PMIC. The C860 has been developed to interface with industry-standard DrMOS devices such as the Vishay SiC645A compatible with 3.3 V SiC645A or the Intersil/Renesas ISL99227 with 3.3V compatible tri-state PWM input. The DrMOS is a fully integrated power stage that integrates a high side and low side MOSFET and a high-performance driver with integrated bootstrap FET. Maximum output current will be based on the selected external DrMOS and on the thermal design of the specific application.

Features

- PWM, voltage mode, DrMOS controller
- Adjustable output voltage with down to 2.4 mV resolution
- 1% voltage accuracy
- Efficiency up to 94%
- Adjustable switching frequency 533 to 1000 kHz
- Adaptable bandwidth, gain & phase margin
- Adjustable protections:
  Input Undervoltage Lockout (ViUVLO), Output Undervoltage Lockout (VoUVLO), Overcurrent Protection (OCP), Overvoltage Protection (OVP), Over temperature Protection (OTP), Short-circuit Protection (SCP)
- Power-good flag output and Enable input
- Controller junction temperature range –40°C to +125°C
- Component included in the WebAmP™ development tool

Applications

- On-demand power management, multi-rail power integration
- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing

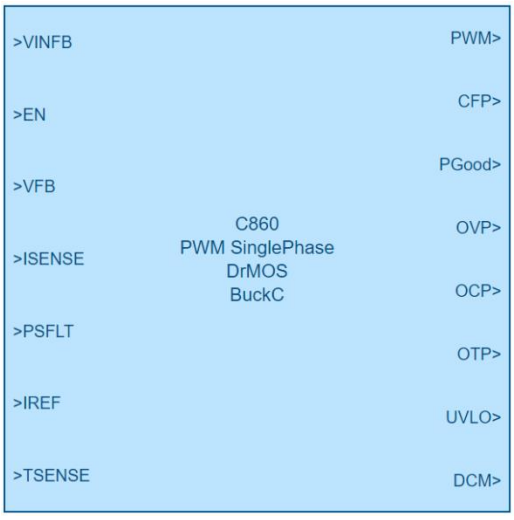


Figure 1. C860 Power Component

Product Detail

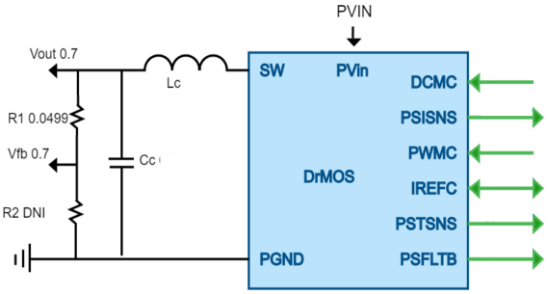
The C860 Synchronous Buck controller power component symbol is shown in Figure 1. The controller drives a DrMOS integrated power stage with connections as shown in Figure 2 and described in the Pin Function and Description Table. A typical application diagram is shown in Figure 3.

Output voltage feedback is compared against an internal reference using a high-performance voltage-error digitizer that provides tight voltage regulation accuracy under transient conditions. Pulse-width modulated (PWM), voltage-mode regulation is implemented with PID compensation. The switching frequency is either generated internally via an oscillator with selectable frequencies or provided via an external pin.

The customizable output voltage is specified by the power engineer during customization using AnDAPT's cloud-based WebAmp development software. The C860 component has customizable control and status pins including enable input, an optional power-good output, and optional output flags to signal when the system triggers an overvoltage (OVP), overcurrent (OCP), undervoltage lockout (UVLO), catastrophic DrMOS failure (CFP) or over temperature (OTP) condition. The threshold values are specified by the power engineer using the WebAmp tool.

Customizable soft-start and soft-stop slew rates are also specified by the power engineer using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 Sequencer, by interconnecting signals EN and PGood to provide customizable dependencies and customizable delays between each sequence step.

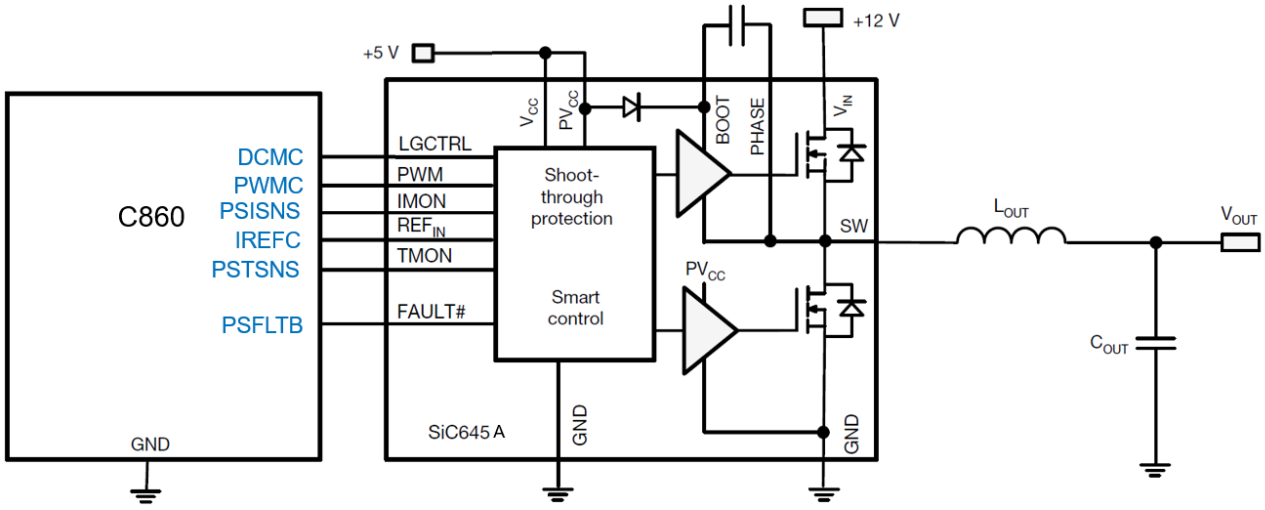
Figure 2: DrMOS Interface



Pin Function and Description Table

Port Name	GPIO Name	SiC645 Name	I/O	Description
OVP			O	Over Voltage Protection fault flag for internal connection to AmP fault manager
OCP			O	Over Current Protection fault flag for internal connection to AmP fault manager
OTP			O	Over Temperature Protection fault flag for internal connection to AmP fault manager
UVLO			O	Input Under Voltage Lock Out fault flag for internal connection to AmP fault manager
PGood			O	Controller Power Good signal
CFP			O	Catastrophic Fault Protection fault flag for internal connection to AmP fault manager.
VINFB			I	Internal - Input voltage measurement for ViUVLO protection
TSENSE	PSTSNS	TMON	I	Temperature monitor input from DrMOS Power Stage to C860 controller
PSFLT	PSFLTB	FAULT#	I	Open drain fault input pin from DrMOS Power Stage to C860 controller.
ISENSE	PSISNS	IMON	I	Current monitor input from DrMOS Power Stage to C860 controller.
IREF	IREFC	REFIN	I	Reference voltage connected to DrMOS power stage REFIN signal and to C860 controller. Recommend using AmP auxiliary 1.2V LDO to drive the signal.
DCM	DCMC	LGCTRL	O	DrMOS power stage lower gate control signal output from DrMOS controller. Used for Discontinuous current mode operation for light load efficiency when available on the DrMOS.
EN			I	Enable DrMOS controller
PWM	PWMC	PWM	O	DrMOS power stage gate driver control signal output from DrMOS controller
VFB	Vfb		I	VOUT feedback for DrMOS controller

Figure 3: Typical Application Diagram



Electrical Characteristics

PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT})		0.7		5.0	V
Output Voltage Regulation (V_{OUT})	Including load regulation and temperature variation V_{IN} range: 4.5V to 6V V_{IN} range: 6V to 14V	 -2 -1		 +1 +1	 % %
Switching frequency (F_{SW})		533		1000	kHz
Switching frequency accuracy		-5		+5	%
Efficiency	V_{IN}=12V, V_{OUT}=1.8V, F_{SW}=571kHz, I_{OUT}=10A		94		%
PROTECTION					
ViUVLO, input Undervoltage Lockout		4		10	V
OCP, Over Current Protection (% I_{OUT})			150		%
OTP, Over Temperature Protection for AmP device	Shutdown (Power Good goes low) Hysteresis		125		°C
OVP, Overvoltage Protection trip point range (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration	+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration	-100		-432	mV
Power Good threshold (relative to Vout Setting)	No resister divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ration	-100		-432	mV

* Parameters shaded in green are user customizable as set in WebAmP development software

Digital GPIO Electrical Characteristics

V_{IN}=12V and T_A=25°C

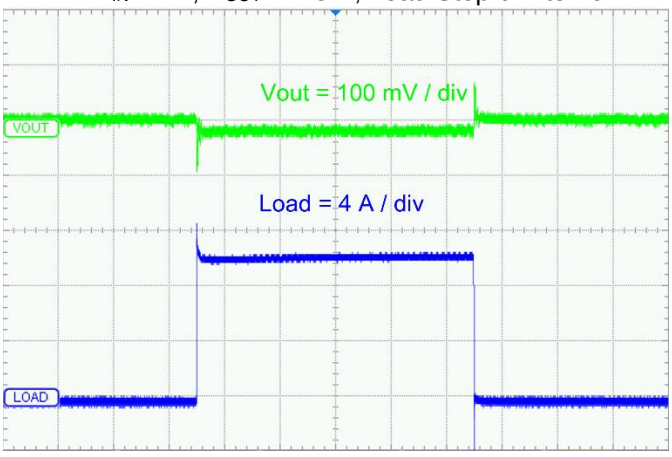
I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	2	-2

Typical Characteristics

Unless otherwise specified: TA = 25°C

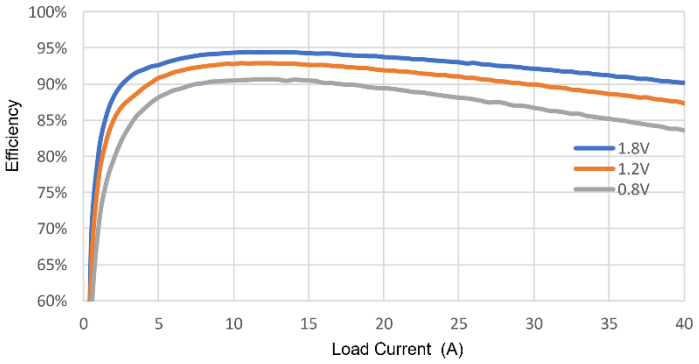
Transient Response

PV_{IN}=12V, V_{OUT} = 1.5 V, Load Step 0 A to 10 A



Time = 200 µs / div F_{SW}=571 kHz

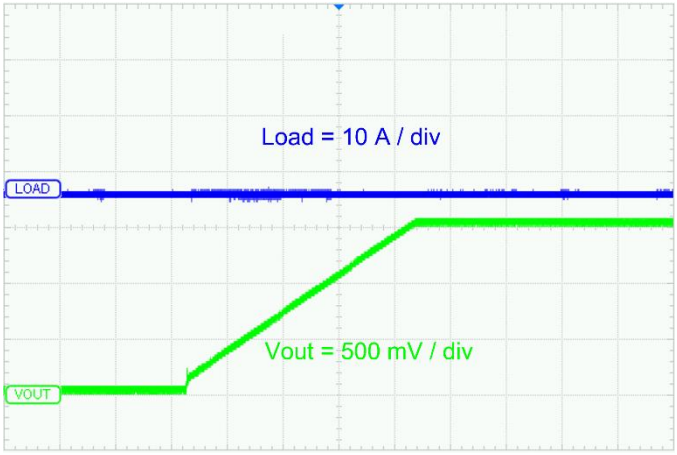
Efficiency



PVin=12V, inductor=250nH, capacitor=564uF F_{SW}=571kHz

Soft Start No Load

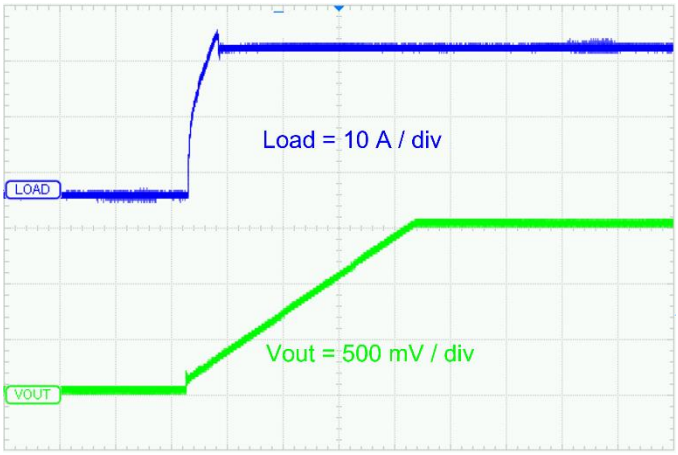
PV_{IN}=12V, V_{OUT} = 1.5 V



Time = 2 ms / div FSW=571 kHz

Soft Start with Load

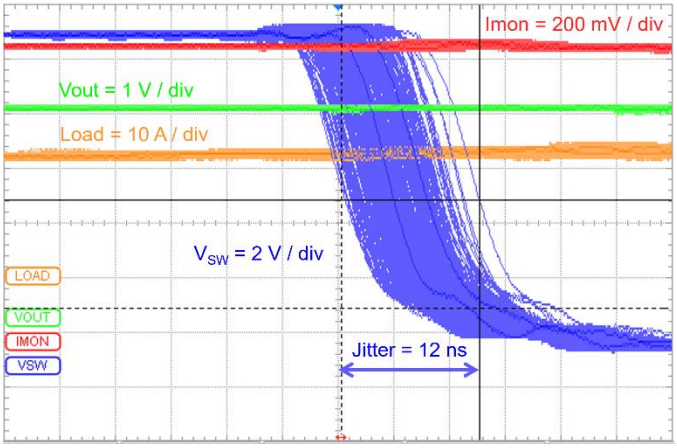
PV_{IN}=12V, V_{OUT} = 1.5 V



Time = 2 ms / div FSW=571 kHz

Jitter

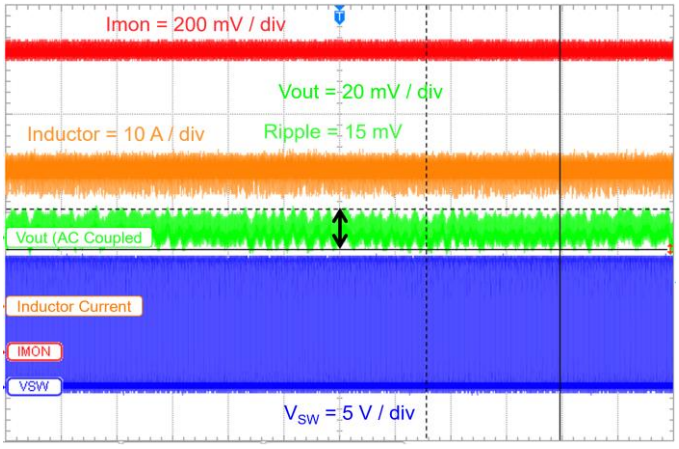
PV_{IN} = 12V, V_{OUT} = 3.8V, I_{LOAD} = 25A



Time = 2 ms / div FSW=571 kHz

Ripple

PV_{IN} = 12V, V_{OUT} = 0.8V, I_{LOAD} = 30A



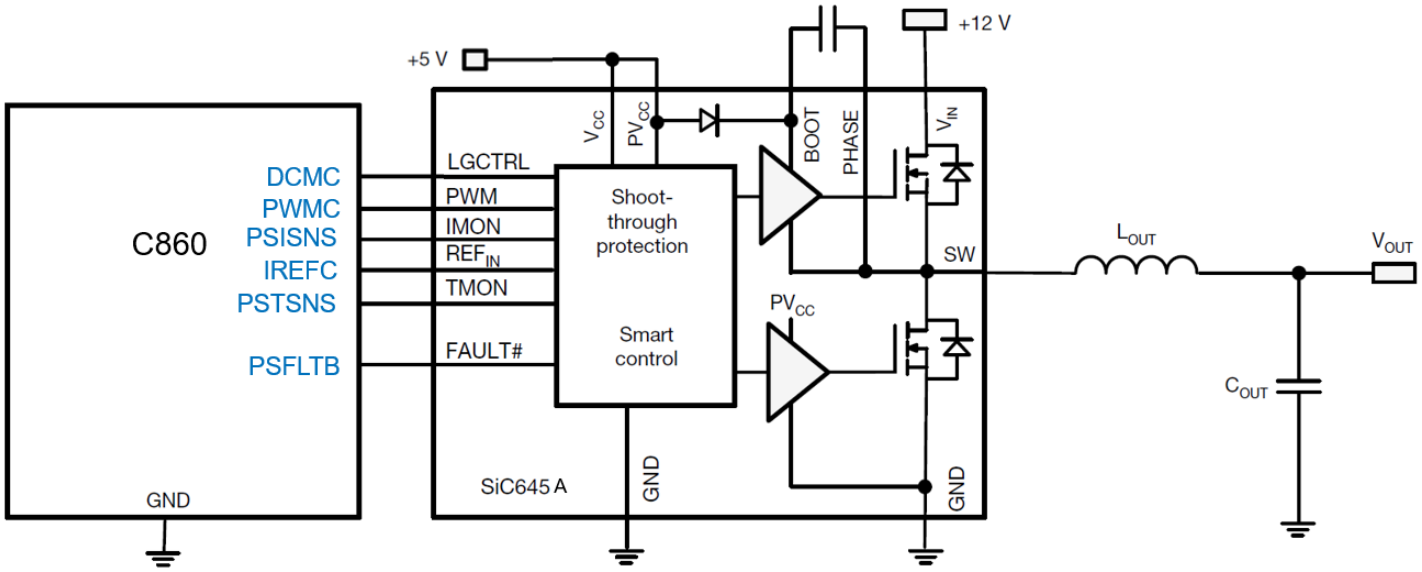
Time = 200 µs / div FSW=571 kHz

Theory of Operation

The C860 Synchronous Buck Regulator with integrated MOSFETs operates in voltage mode by comparing the V_{OUT} feedback voltage, Vfb, with a programmable reference, Vref to direct the PID (Proportional Integral Derivative) controller to produce a PWM (Pulse Width Modulation) input to the Hi-side and Lo-side MOSFET switches as shown in Figure 4.

In CCM (Continuous Conduction Mode), the PWM driver goes high turning the Hi-side switch "ON" to provide PV_{IN} to the LX side of an inductor, L, where $V_L = V_{LX} - V_{OUT}$. When the PWM driver goes low, the Hi-side switch turns "OFF", and after a shoot through delay, the Lo-side switch turns "ON" providing a path for the inductor current to decrease with $V_L = - V_{OUT}$, until the next PWM turns back "ON". As this cycle repeats, the PID algorithm regulates V_{OUT} by continuously updating the PWM cycle to optimize ripple, regulation, and transient response over changing load conditions.

Figure 4: Functional Block Diagram



Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port which may be connected to a GPIO pin or a control component such as the C420 Sequencer. When EN goes high, the output voltage, V_{OUT}, will ramp up according to the Soft Start programmable preset ramp time in Parameter Settings. When EN goes low, the output voltage, V_{OUT}, will ramp down according to the Soft Start programmable preset ramp time in Parameter Settings.

PGood

The power-good, PGood, digital port may be connected to a GPIO pin or a control component such as the C420 Sequencer to indicate the output voltage regulation status. PGOOD goes high on power-up after completion of all the Soft Start time (Figure 5) and when all Faults are cleared. PGOOD will go low for faults such as ViUVLO, VoUVLO, OVP over voltage, OCP current limit, or OTP thermal shutdown. PGOOD will also go low if EN goes low.

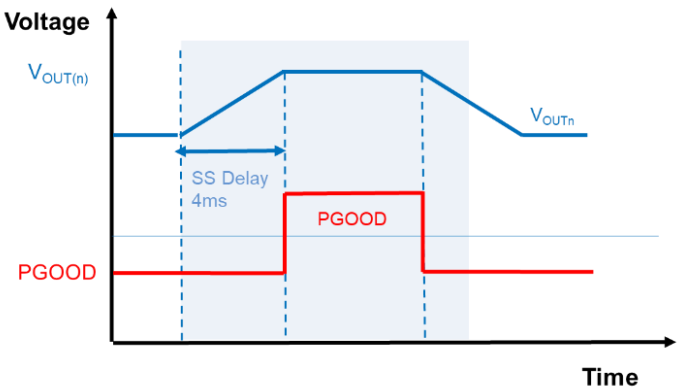


Figure 5

Protection Features

The C860 provides many protection features including ViUVLO, OVP, OCP and OTP.

ViUVLO

The PV_{IN} voltage Under Voltage Lockout, ViUVLO, digital port may be connected to a GPIO pin or a control component such as Digital Logic Block to indicate the PV_{IN} voltage status. ViUVLO flag stays low when PV_{IN} voltage is higher than the programmable preset condition in Parameter Settings. ViUVLO goes high when PV_{IN} voltage is less than the programmable preset condition in Parameter Settings. PVIN may be sensed on the GPIO pin connected to the PVINFB analog port which is resistor divided by a fixed 1/6 ratio of PVIN. On detection of ViUVLO, the C860 will power down and PGood will go low. On ViUVLO returning low, the C860 will restart with a new Soft Start cycle.

ViUVLO from Power Stage (DrMOS)

In addition to the standard protections which are implemented at the device level using other power components, the C860 also includes other protection depending on the DrMOS used. When Hiccup options are selected, then the controller will shut down and automatically power up when the power stage fault has cleared.

OVP

The Over Voltage Protection, OVP, digital port may be connected to a GPIO pin or control component logic blocks to indicate the output voltage over voltage status. OVP goes high when output voltage, V_{OUT}, is higher than the programmable preset condition in Parameter Settings. OVP goes low when output voltage, V_{OUT}, is less than the programmable preset condition in Parameter Settings. On detection of OVP, the C860 will skip Hi-side switch pulses until OVP returns low.

OCP

The Over Current Protection, OCP, digital port may be connected to a GPIO pin or control component logic blocks to indicate the output over current status. When I_{OUT}, is greater than 150% of the Output Current setting, the C860 will limit the Hi-side switch pulse width and OCP will go high.

OCP from Power Stage (DrMOS)

In addition to the standard protections which are implemented at the device level using other power components, the C860 also includes other protection depending on the DrMOS used. When Hiccup options are selected, then the controller will shut down and automatically power up when the power stage fault has cleared.

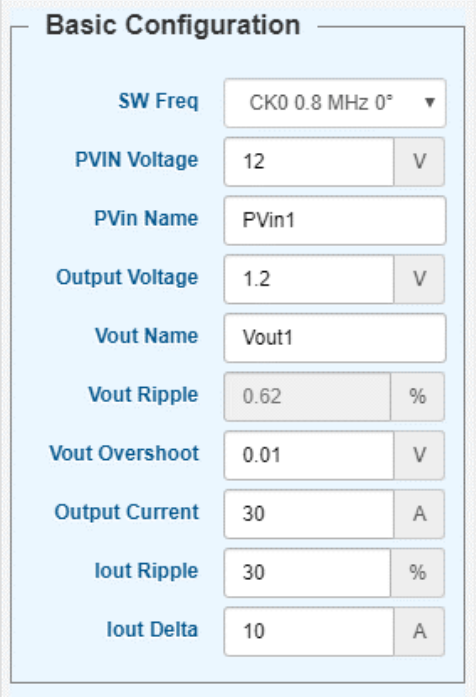
OTP

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches 125°C the device shuts down. On detection of OTP, the C860 will power down and PGood will go low. On OTP returning low, an EN cycling low-to-high, will restart the C860 with a new Soft Start cycle.

Parameter Settings

Basic Configuration

Default parameters may be changed per user requirement.



$V_{OUT\ ripple}$ is computed as follows:

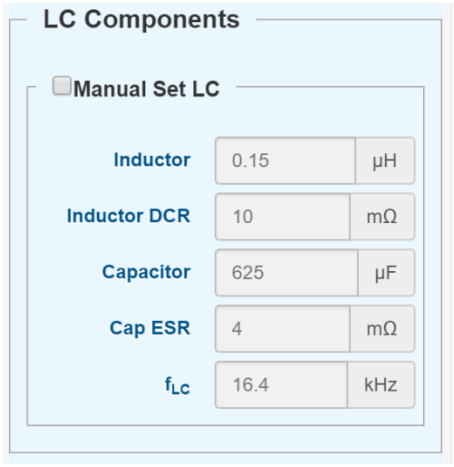
$$V_{OUT\ ripple} = Iripple/(8*C_{OUT}*Fsw)$$

LC Component Selection

Default values for Inductance, L, and output capacitance, Cout, are computed as follows:

$$L = (V_{IN}-V_{OUT})* V_{OUT} / (V_{IN} *Fsw*Iripple)$$

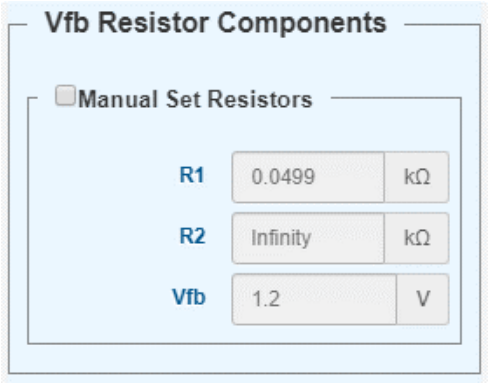
$$C_{OUT} = I_{OUT}delta\text{^}2*L / (2* V_{OUT} *Vos)$$



Inductor and Capacitor values may be changed by checking Manual Set LC or selecting the BoM tab where manufacturers part numbers may be selected.

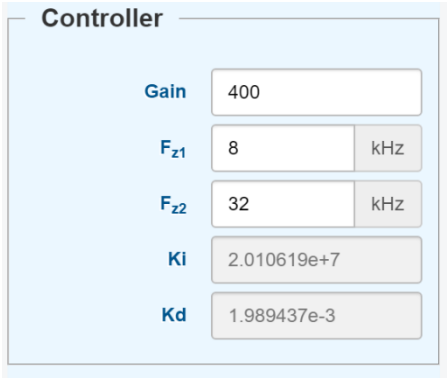
Vfb Resistor Components

Feedback divider resistors R1 and R2 default to 49.9 Ω and open (infinity). When V_{OUT} is larger than 2.3V, a resistor divider ratio is computed to select 1% resistor values for both R1 and R2.

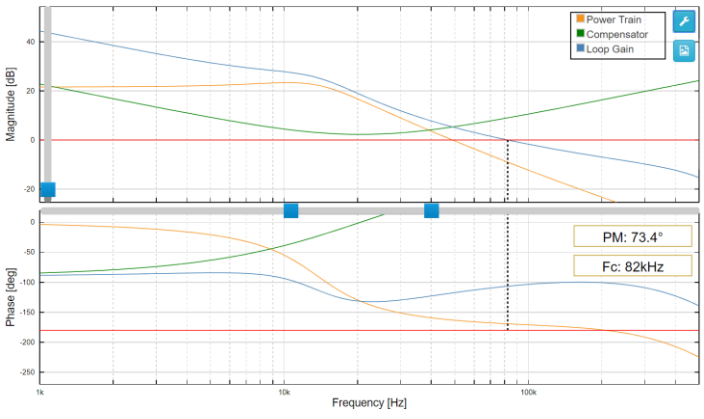


Controller

The controller compensation memory block provides PID compensation of error signals using the integrated compensation logic without external passives or an arithmetic unit. The user can adjust a bandwidth, a gain, and a phase margin of the compensation logic. For example, a user can interactively adjust the proportional gain Kp and the gains Fz1 and Fz2 shown below to effectively adjust the derivative and integral gains Kd and Ki as well as the bandwidth and the phase margin.

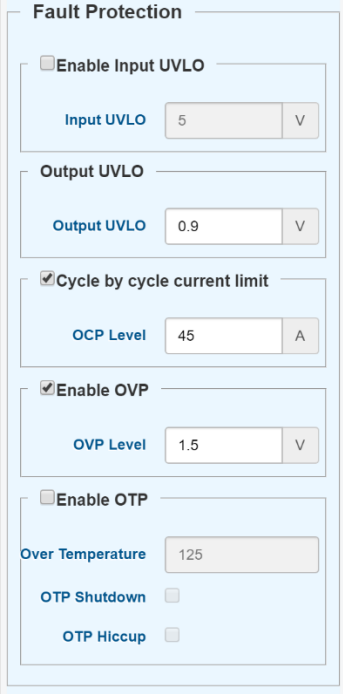


Gain, Fz1 and Fz2 are chosen to provide best Phase Margin and Crossover Frequency, Fc, as adjusted in the Bode Plot shown below:



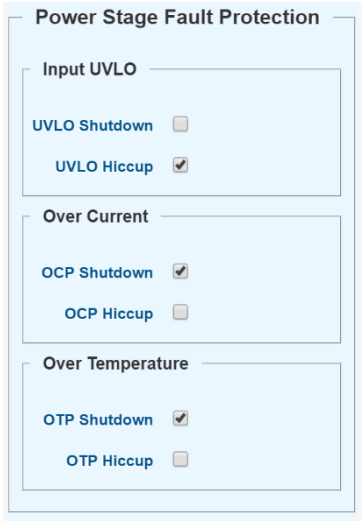
Fault Protection

Input voltage Under Voltage Lockout, ViUVLO, indicates the input voltage status greater or less than programmable preset condition (default 4.5V). Output voltage Under Voltage Lockout, VoUVLO, indicates the output voltage status greater or less than programmable preset condition (default 75% of VOUT). Over Voltage Protection, OVP, indicates output voltage status greater or less than the programmable preset condition (default 25% above Vout). Over Current Protection, OCP, indicates the output over current greater or less than the programmable preset condition. Over Temperature Protection, OTP, indicates thermal shutdown has occurred. (set to 125°C)..



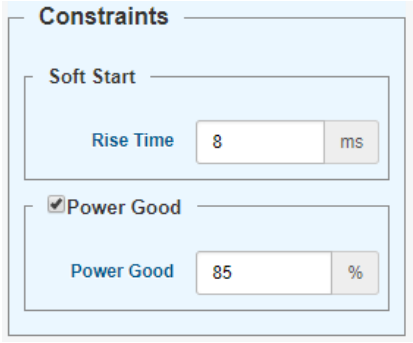
Fault Protection Power Stage

In addition to the standard protection which are implemented at the device level using other power components, the C860 also includes other protection depending on the DrMOS used. When Hiccup options are selected, then the controller will shut down and automatically power up when the power stage fault has cleared.



Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good ranges 59% to 100% and default is 85%.



Additional Information DrMOS

For additional information see DrMOS supplier datasheets such as the SiC645A DrMOS recommended for use with C860.

Pin Name	I/O	Description
LGCTRL	I	Lower gate control signal input. LO = GL LO (LFET off). HI = normal operation (GL and GH strictly obey PWM). This pin should be driven with a logic signal, or externally tied high if not required; it should not be left floating
FAULT#	O	Open drain output pin. Any fault (over-current, over-temperature, shorted HFET, or POR / UVLO) will pull this pin to ground. This pin may be connected to the controller enable pin or used to signal a fault at the system level.
PWM	I	PWM input of gate driver, compatible with 3.3 V and 5 V tri-state PWM signal.
REFIN	I	Input for external reference voltage for IMON signal. This voltage should be between 0.8 V and 1.6 V. Connect REFIN to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to GND.
IMON	O	Current monitor output referenced to REFIN. IMON will be pulled high (to REFIN +1.2 V) to indicate an HFET shorted or over-current fault. Connect the IMON output to the appropriate current sense input of the controller. No more than 56 pF capacitance can be directly connected across IMON and REFIN pins. With a 100 Ohm series resistor, up to 470 pF may be used.
TMON	O	Temperature monitor output. TMON will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across TMON and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kohm for 100 nF load.

C860 Resource Usage

```
Circuit Stats...
      Number of AnD_Temp_Sensor      1
      Number of AnD_ADi_dual         1
      Number of AnD_ATC_IO           12
      Number of AnD_ATC_Comp         4
      Number of AnD_ATC_Summer       1
      Number of AnD_PMT              3
      Number of AnD_CM_PID           1
      Number of AnD_Nref_dyn         1
      Number of AnD_Nref_fix         4
      Number of AnD_PTG_Phase_Count  1
      Number of AnD_PTG_GBUF         1
      Number of AnD_PTG_OSC          1
      Number of AnD_DFFN             21
      Number of AnD_DFF              31
      Number of AnD_ADCR             10
      Number of LUT4                 114
```

```
Resource Usage...
      io      12 used (Capacity   24)
      clb     18 used (Capacity   64)
      cm       1 used (Capacity    8)
      pmt      3 used (Capacity   16)
      atc      1 used (Capacity    6)
      corner   4 used (Capacity    4)
      ptg      2 used (Capacity    2)
      uLogic 124 used (Capacity  512)

Components Stats...
      $techmap\buck_c
            AnD_DFF           28
            AnD_DFFN          14

      buck_c
            AnD_ADCR          10
            AnD_ADi_dual      1
            AnD_ATC_Comp      3
            AnD_ATC_Summer    1
            AnD_CM_PID        1
            AnD_Nref_dyn      1
            AnD_Nref_fix      3
            AnD_PMT           3
```

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C860 power components. An example application is shown in Figure 6.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages to analog GPIOs, Adaptive Digitizers, Threshold Comparators, In Amp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Lowers bias current, system freq.

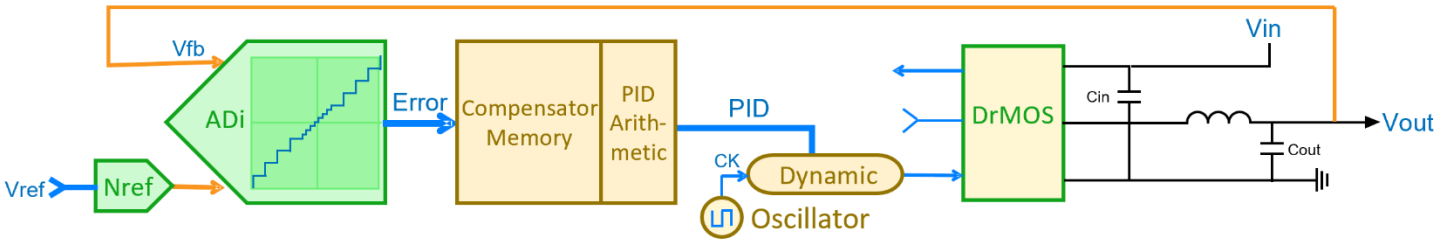
The PMT provides precision delays for Pulse Width Modulation (PWM), MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with resolution less than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

Figure 6: AmP Blocks and Resources driving DrMOS Example - Buck Regulator



Additional Resources

- AnDAPT AmP Platform datasheet

Revision History

Date	Revision
05/15/2019	Preliminary release
03/26/20**20**	Clarified DrMOS part numbers for 3.3V compatible tri-state PWM input

AnDAPT

On-Demand Power Management

www.AnDAPT.com

Trademarks