Current-Mode Two-Phase DrMOS Controller

Power Component: C870_B

Product Description

The C870_B Power Component is a customizable, two-phase, current-mode DrMOS controller designed for point-of-load (POL) applications. Combine with other Power Components to create a custom-defined, AnDAPT AmP on-demand PMIC. Power Components are software components, accessible through the WebAmP™ cloud-based development tool, allowing users to create their own PMIC. The C870_B has been developed to interface with industry-standard DrMOS devices such as Vishay SiC645A or Intersil/Renesas ISL99227 with 3.3V compatible tri-state PWM input. The DrMOS is a fully integrated power stage that integrates high and low side MOSFETs and a high-performance driver with integrated bootstrap diode. Maximum output current is based on selected external DrMOS and on thermal design of specific application.

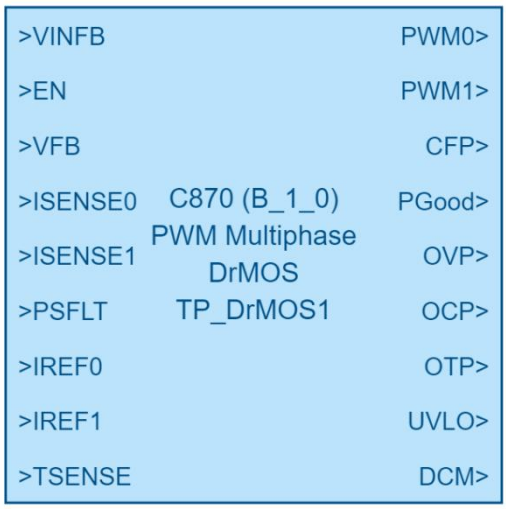
Features

- Constant frequency, emulated peak current mode, two-phase DrMOS controller with built-in slope compensation
- Adjustable output voltage with down to 2.5 mV resolution
- 1% voltage accuracy
- Efficiency up to 94%
- Adjustable switching clock 500-1000 kHz (each phase switches at half of the clock frequency)
- Adjustable bandwidth, gain & phase margin
- Adjustable protections:
  Input Undervoltage Lockout (ViUVLO), Output Undervoltage Lockout (VoUVLO), Cycle-by-cycle Overcurrent Protection (OCP), Output Overvoltage Protection (OVP)
- Power-good flag output and Enable input
- Component included in the WebAmP™ development tool

Applications

- FPGA/SoC, processor power management
- Telecom servers, networking equipment
- Industrial equipment and medical systems

Figure 1. C870_B Power Component

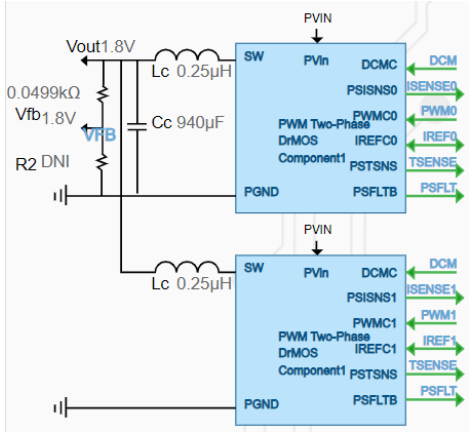


Product Details

The C870_B 2-phase Synchronous Buck DrMOS controller power component symbol is shown in Figure 1. The controller drives two DrMOS integrated power stages 180° out-of-phase with connections as shown in Figure 2 and described in the Pin Function and Description Table. A typical application diagram is shown in Figure 3. Output voltage feedback is fed back into a high-performance voltage error digitizer that provides tight voltage regulation accuracy even under transient conditions. The digital compensator's PID gain parameters are user adjustable. The switching frequency is user-selectable with the option to sync to an external clock connected to a GPIO pin.

The output voltage and maximum current are specified by the power engineer during customization using AnDAPT's cloud based WebAmp development software. The C870_B component has customizable control and status pins including an enable input, an optional power-good output, and optional output flags to signal when the system senses an overvoltage (OVP), overcurrent (OCP), undervoltage lockout (UVLO), catastrophic DrMOS failure (CFP) or over-temperature (OTP) condition. The threshold values are configured in the WebAmp tool.

Figure 2: DrMOS Interface

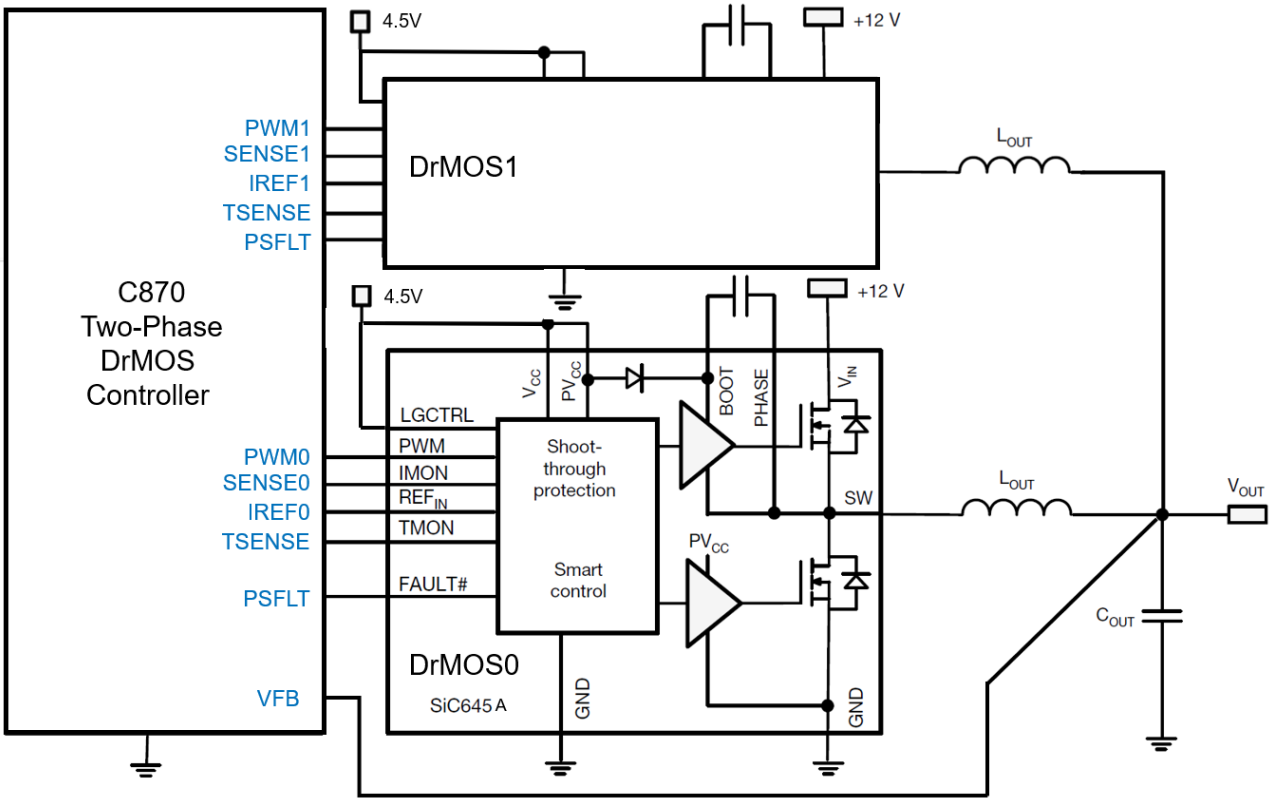


Soft-start and soft-stop ramp times are also specified using the WebAmp tool. Additional sequencing options are available when used in conjunction with the C420 Sequencer, by interconnecting signals EN and PGOOD to provide customizable dependencies and customizable delays between each sequence step.

Pin Function and Description Table

Port Name	SiC645 Name	I/O	Description
OVP		O	Over-Voltage Protection fault flag that can be routed to internal logic and/or a GPIO
OCP		O	Over-Current Protection fault flag that can be routed to internal logic and/or a GPIO
OTP		O	DrMOS Over-Temperature Protection fault flag that can be routed to additional internal logic and/or a GPIO pin
UVLO		O	Output Under-Voltage Lock-Out fault flag that can be routed to internal logic and/or a GPIO
PGood		O	Controller Power Good signal
CFP		O	Catastrophic Fault Protection fault flag that can be routed to internal logic and/or a GPIO
VINFB		I	Input voltage (PVIN) measurement for ViUVLO protection
TSENSE	TMON	I	Analog temperature signal from DrMOS Power Stage to C870_B controller
PSFLT	FAULT#	I	Open-drain fault signal from DrMOS Power Stage to C870_B controller
ISENSE0 ISENSE1	IMON	I	Analog current monitor signal from DrMOS Power Stage to C870_B controller. In the PCB, these signals should be routed as a sensitive differential pair with their respective IREF signals.
IREF0 IREF1	REFIN	I	Reference voltage for DrMOS IMON signal and C870_B ISENSE differential input amplifiers. Route these as differential pairs with their respective ISENSE lines from the AmP device to the DrMOS. Run a separate trace from the AmP device 1.2V *VCC* pin to the DrMOS pins.
DCM	LGCTRL	O	Reserved for future DCM (discontinuous mode) control. In Webamp leave the DCM signal unconnected, and in the PCB, connect LGCTRL to the DrMOS VCC pin.
EN		I	Enable DrMOS controller
PWM0 PWM1	PWM	O	DrMOS power stage gate driver control signal output from DrMOS controller
VFB		I	VOUT feedback for DrMOS controller

Figure 3: Typical Application Diagram. Note 4.5V is powered from AmP device VDD pin



Electrical Characteristics

PV_{IN}= V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, unless otherwise specified

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage (V_{OUT}) (subject to max duty cycle limits and input voltage)		0.7		The lesser of: 5.0 or max duty cycle * PV_{IN}	V
Output Voltage Regulation (V_{OUT})	Including load regulation and temperature variation V_{IN} range: 4.5V to 6V V_{IN} range: 6V to 14V	 -2 -1		 +1 +1	 % %
Switching frequency (F_{SW}) per phase		250		500	kHz
Switching frequency accuracy		-5		+5	%
Efficiency	V_{IN}=12V, V_{OUT}=0.72V, F_{SW}=500kHz, I_{OUT}=22A		88		%
Maximum Duty Cycle	(Dictated by 250 ns Minimum Off-Time of SiC645)		The lesser of: 85% or 1-250ns*$F_{SW\_per\_phase}$		%
PROTECTION					
ViUVLO, input Undervoltage Lockout		4		10	V
OCP, Over Current Protection (% of I_{OUT})			150		%
OTP, Over Temperature Protection for AmP device	Shutdown (Power Good goes low) Hysteresis	125			°C
OVP, Overvoltage Protection trip point range (relative to Vout Setting)	No resistor divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ratio	+100		+432	mV
VoUVLO, output Undervoltage Lockout threshold range (relative to Vout Setting)	No resistor divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ratio	-100		-432	mV
Power Good threshold (relative to Vout Setting)	No resistor divider on voltage feedback. If a resistor divider is used, these values will increase by a factor equal to the divider ratio	-100		-432	mV

* Parameters shaded in green are user customizable as set in WebAmP development software

Digital GPIO Electrical Characteristics

V_{IN}=12V and T_A=25°C

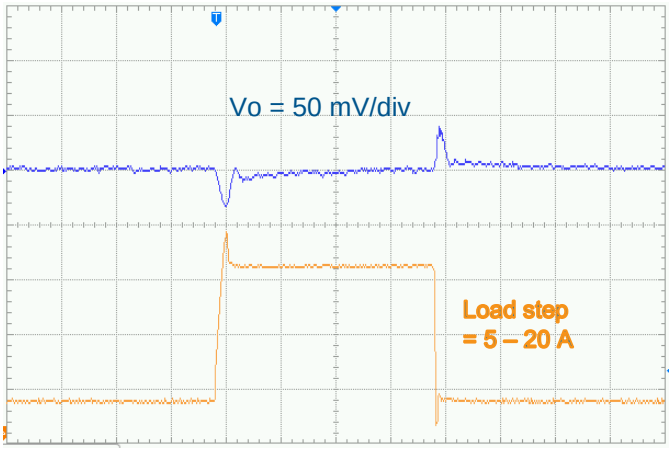
I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	2	-2

Typical Performance

Unless otherwise specified: TA = 25°C, F_{SW} = 500kHz per phase, PVIN = 12 V, Vout = 1.8V,; L=250 nHx2; C=20x 47µF MLCC + 2x 470 uF/ 3mΩ polymer

Transient Response

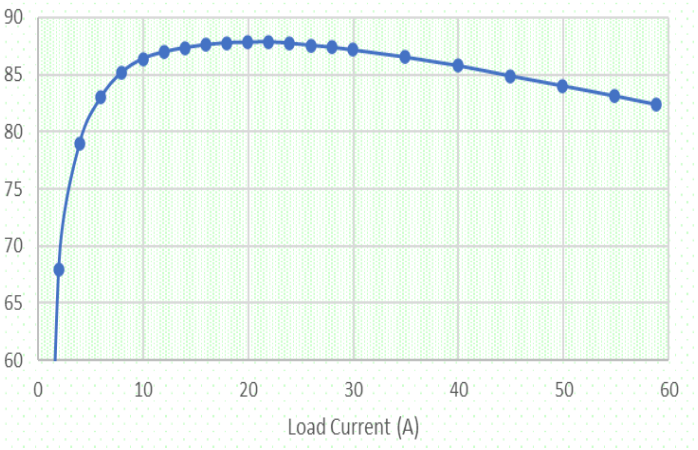
Load Step 0 A to 10 A



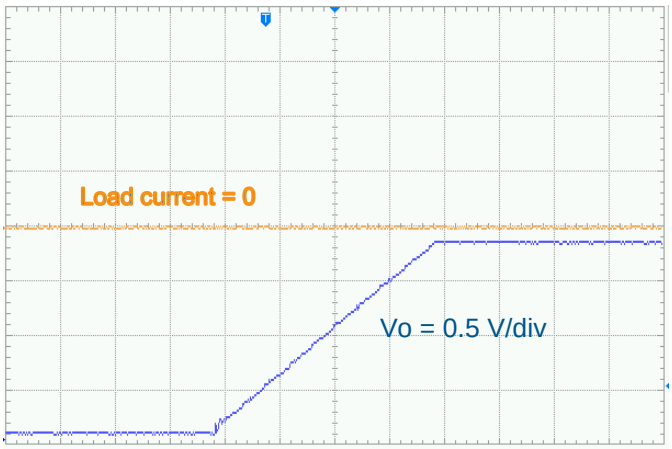
50 µs/div;

Efficiency

Vo=0.72 V

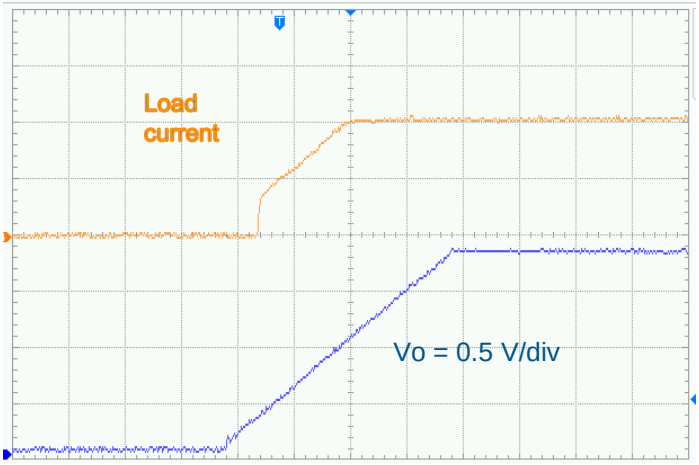


Soft Start No Load



2 ms/div

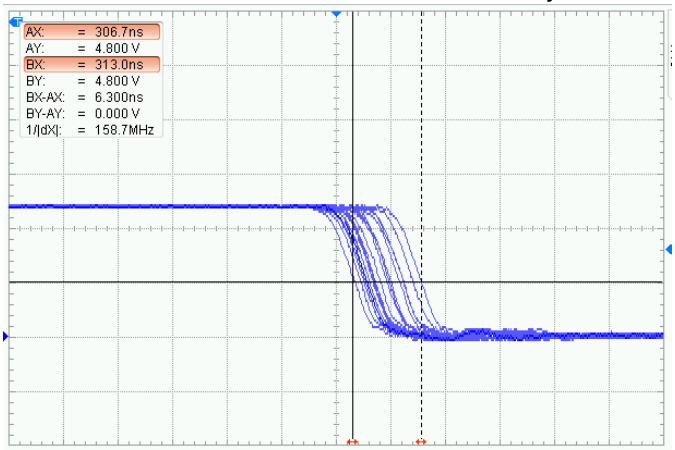
Soft Start with Load



2 ms/div; load=50 A

Jitter

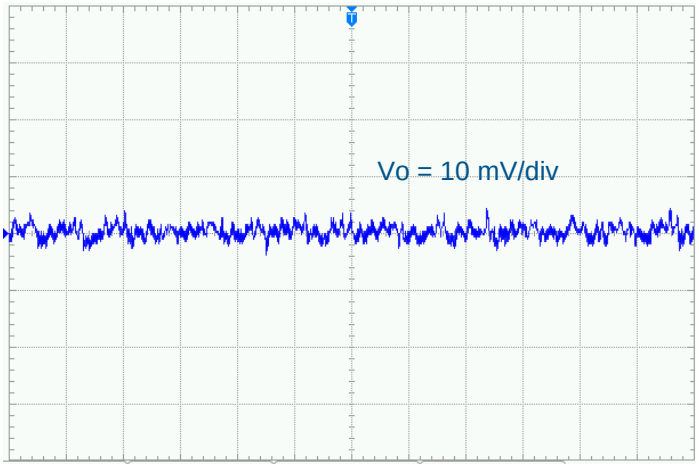
I_{LOAD} = 25A, Jitter Reduction set to “Best jitter”



5 ns/div; Jitter = 6.3 ns

Ripple

V_{OUT} = 0.72 V, I_{LOAD} = 30A

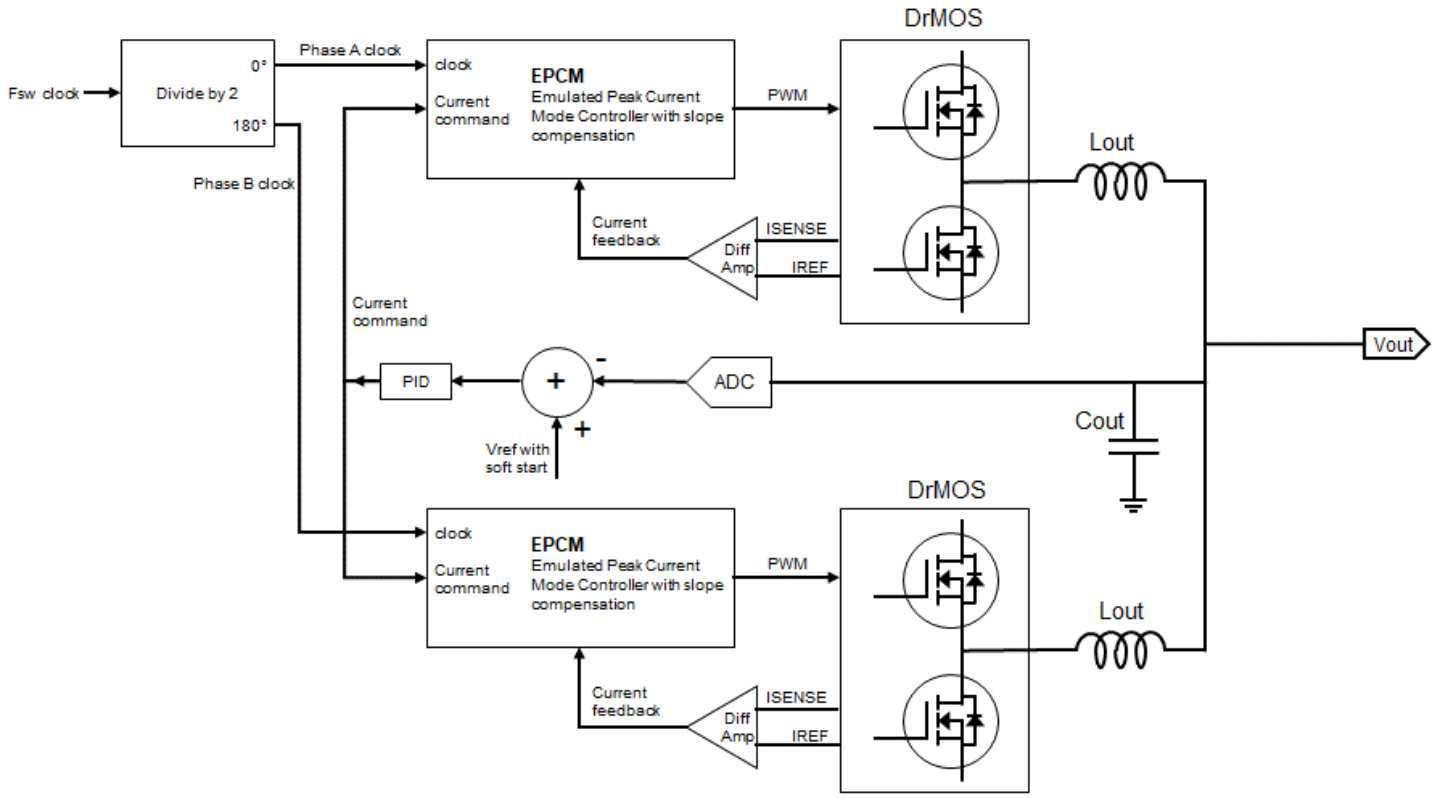


100 µs/div;

Theory of Operation

The C870_B 2-phase DrMOS Synchronous Buck Controller operates in emulated peak current mode wherein the PID (proportional, integral, derivative) voltage error amplifier does not control the duty cycle directly but instead controls the peak current command into the Emulated Peak Current Mode (EPCM) modulator as shown in Figure 4. The EPCM modulator controls the on-time on a cycle-by-cycle basis such that the inductor peak current equals the commanded value (plus slope compensation for stability) from the voltage error amplifier. EPCM uses a sample-and-hold version of the inductor current at the end of the off period, which is provided by the DrMOS controller. A slope compensation signal is generated, whose slope is pre-calculated by WebAmP from the inductance, and the input and output voltages entered by the user.

Figure 4: Functional Block Diagram



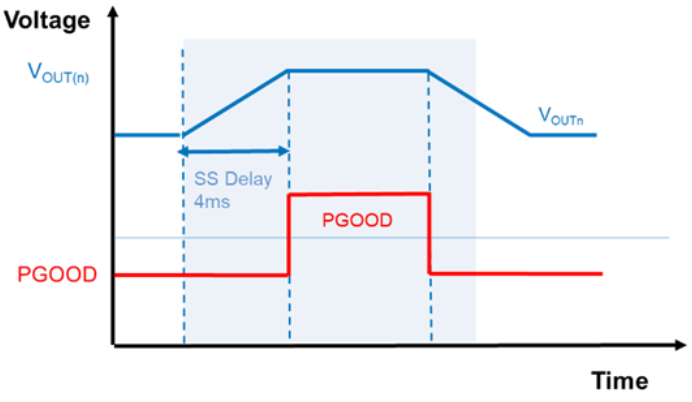
Start-up and Shutdown

Start-up and shutdown are controlled by the EN digital port which may be connected to a GPIO pin or an internal control component such as the C420 Sequencer. When EN goes high, the output voltage, will ramp up according to the programmable Soft Start ramp time in Parameter Settings. When EN goes low, the output voltage, V_{OUT}, will ramp down over the same time.

PGood

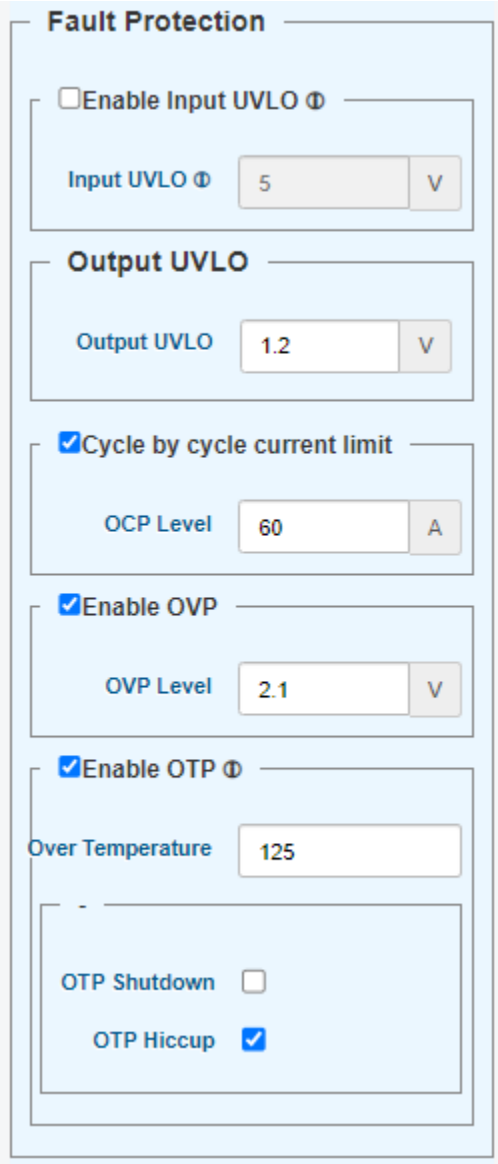
The power-good, PGOOD, digital port may be connected to a GPIO pin or a control component such as the C420 Sequencer to indicate the output voltage regulation status. PGOOD goes high on power-up after the user-specified soft-start (Figure 5) and if there are no Faults. It goes low at the beginning of power-down. PGOOD will also go low if any faults are triggered - ViUVLO, VoUVLO, OVP, OCP, or OTP. PGOOD will also go low if the EN input goes low.

Figure 5 Soft Start PGOOD waveforms



Protection Features

The C870_B provides many protection features including ViUVLO, OVP, OCP and OTP. These can be enabled as desired.



Pulse-by-pulse OCP

OCP, Over Current Protection, is a digital output port which may be connected to a GPIO pin or a control component logic block to indicate the output over-current status. When the inductor “valley” current is greater than the OCP value entered into WebAmp, the C870_B will skip the next cycle, and the OCP port will go high for one switching cycle. This is separate from the DrMOS internal OCP which is a much higher value than the user-specified C870_B OCP value.

OVP

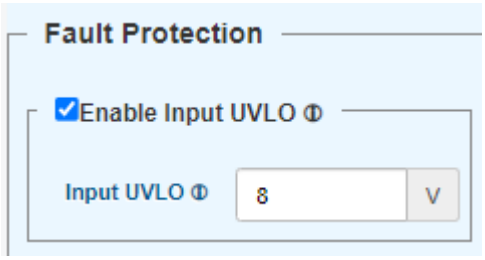
OVP, Over Voltage Protection, is a digital output port which may be connected to a GPIO pin or control component logic block to indicate the output voltage over voltage status. OVP goes high when output voltage, V_{OUT}, is higher than the programmable preset condition in WebAmp Parameter Settings, and is low otherwise. On detection of OVP, the C870_B will skip Hi-side switch pulses until OVP returns low.

ViUVLO

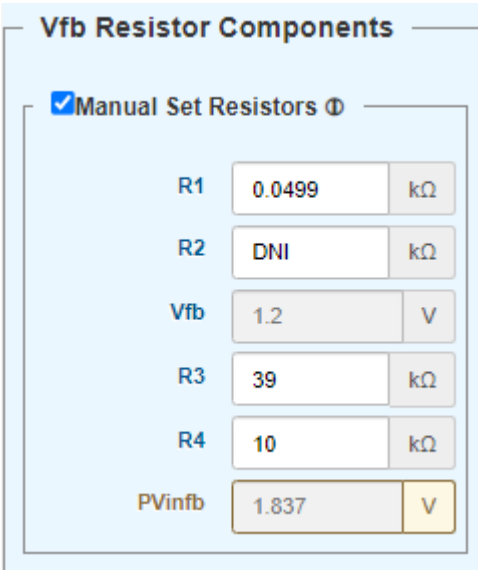
ViUVLO is the PV_{IN} (powertrain input) voltage Under Voltage Lockout. It shuts down the C870 when the PVIN voltage is lower than this threshold, and the ViUVLO output goes high. It is a digital output port which may be connected to a GPIO pin or a control component such as a Digital Logic Block. When PVIN rises above the threshold, the C870_B will go through its normal soft-start sequence.

To use:

1) Check the box as per below and enter the desired threshold voltage



2) In the schematic of the WebAmp Design tab, route a wire from the PVINFB input pin to a GPIO pin
3) In the PCB, connect the above GPIO pin to a divide by ~5 resistor divider (e.g. 10k and 39k) connected to the PVIN (high current) supply.
4) Enter the above resistor values in WebAmp under R3 and R4:



DrMOS Power Stage Fault Protection

In addition to the C870_B P*rotection Features*, the C870_B also monitors the DrMOS Fault# signal. The DrMOS asserts the Fault# signal when its internal OCP or OTP is asserted. See its datasheet for details.

When the *Hiccup* option *under Power Stage Fault Protection* in WebAmp is selected, the controller will shut down when the Fault# signal goes low and automatically powers up with a new soft-start cycle when the power stage fault has cleared. Otherwise, the EN signal needs to be cycled to restart the C870_B. This also applies to the DrMOS OTP below.

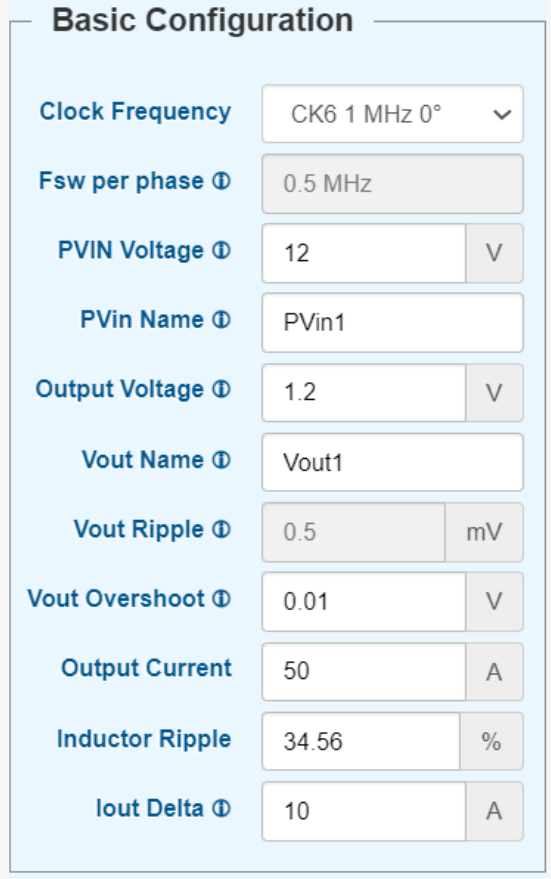
OTP

The DrMOS has a Tmax (maximum temperature) above which it will shut down and pull its FAULT# pin low. Additionally, it has a TMON (temperature monitor) analog output pin. The C870B monitors this voltage and shuts down if the user-specified temperature is exceeded.

Parameter Settings

Basic Configuration

Default parameters may be changed per user requirements.



The *Clock Frequency* can be adjusted between 500 kHz and 1 MHz (per phase switching frequency 250-500 kHz) Several phase settings relative to the other converters are available.

PVIN Voltage is the nominal input voltage into the converter.

Enter a name for the input rail *PVin Name,* and for the output rail in *Vout Name* to be used in the circuit diagram in the *Design* tab.

Vout Ripple is the calculated output voltage ripple from the switching frequency, input and output voltages, and the L and C values in the output filter. It is computed as follows:

c=1/(8*Cc*Fclock);
b=1/(8*Cb*Fclock);
$V_{OUT\ ripple}$ = delta_I*c*(Rb + b)/(Rb+b+c)

where:
Fclock = Clock Frequency
Cc = Cout(Ceramic)
Cb = Cout(Bulk)
Rb = Cout ESR(Bulk)
delta_I = inductor p-p ripple current of each inductor in Amps

Vout Overshoot is the allowable overshoot during the specified load release transient entered into *Iout Delta* . The output capacitor value is calculated from this and the inductors' value. If the box "*Manual Set L C*" is checked, it will be grayed out and its value will be calculated from the L and C values.

Output Current is the rated load current.

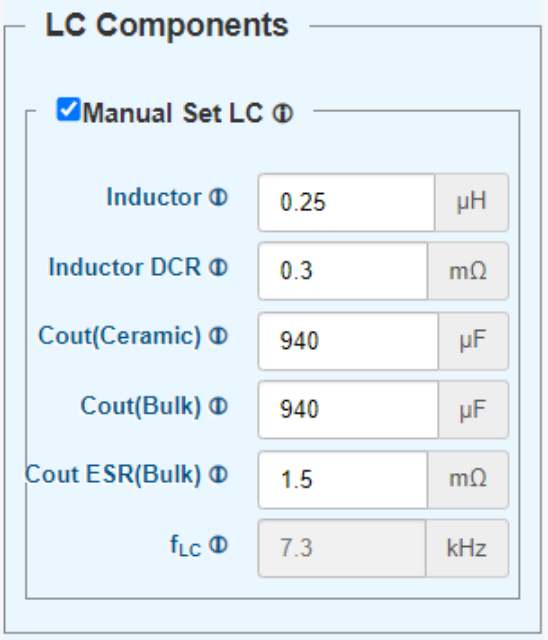
Inductor Ripple, the inductor peak-peak ripple current as a percentage of rated load current, calculates the inductor value. It is grayed out when the box "*Manual Set LC*" is checked and is calculated from the inductor value.

LC Component Selection

Default values for the inductors' inductance value, L, and output capacitance, Cout, are computed as follows:

$L = (V_{IN}-V_{OUT})* V_{OUT} / (V_{IN} *Fsw*Iripple)$

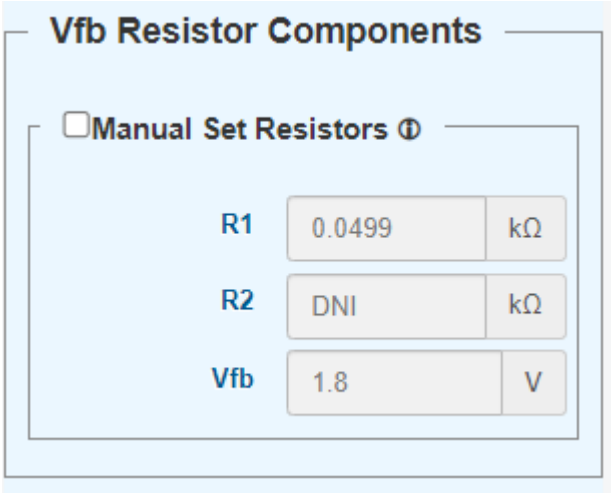
$C_{OUT} = I_{OUT}delta\text{^}2*L / (2* V_{OUT} *Vout\_overshoot)$



Inductor and Capacitor values may be changed by checking the box *Manual Set LC* or selecting the BoM tab where manufacturer part numbers may be selected.

Vfb Resistor Components

Feedback divider resistors R1 and R2 default to 49.9 Ω and open (infinity), respectively. When V_{OUT} is larger than 2.25V, a resistor divider ratio is computed to select 1% resistor values for both R1 and R2. If "Manual Set Resistors" is selected, the values for R1 and R2 are over-ridden and the new feedback sense voltage Vfb is calculated. For output voltages > 2.25V, the recommended value for Vfb is 2.25V for best load transient response.



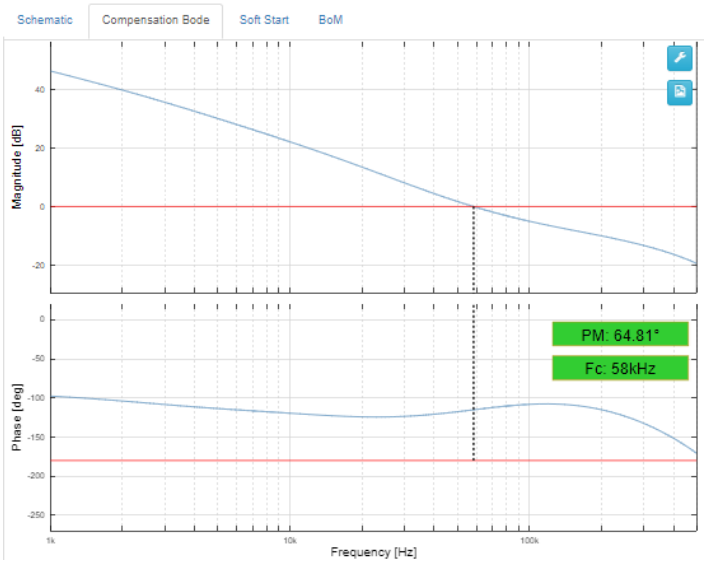
PID Controller

The controller compensation memory block provides PID compensation of the error using the integrated compensation logic without external passive components. The user can adjust the bandwidth, gain, and phase margin of the design by interactively adjusting the proportional (midband) gain Kp and the zero frequencies Fz1 and Fz2 shown below.

The dropdown box “Jitter Reduction” allows the selection of “Best jitter”, “Good jitter and transient”, and “Best transient” which balances the duty cycle jitter vs. transient performance. “Best transient” is useful for designs which require a very small output voltage excursion with fast load transients.

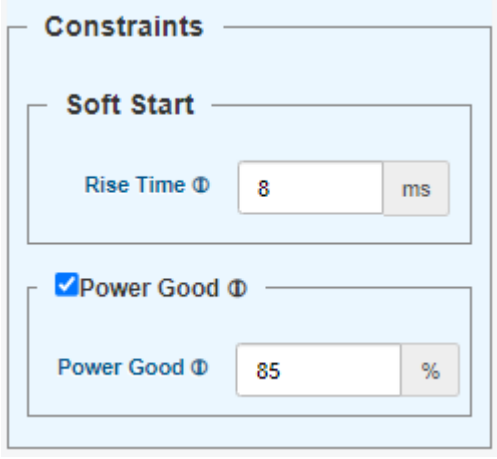
Gain, Fz1 and Fz2 are chosen to provide best Phase Margin and Crossover Frequency, Fc

WebAmp then calculates the derivative and integral gains Kd and Ki, and plots the Bode response. The Bode response is visible by clicking the Compensation Bode tab under the Design tab:



Constraints

Soft Start times of 1 to 16 milliseconds are programmable by the user as a parameter selection. The default is 8 milliseconds as shown. Power Good is adjustable from ranges 59% to 100% and default is 85%.



Additional Information on DrMOS

For additional information see the DrMOS supplier datasheets such as the SiC645A DrMOS recommended for use with C870_B.

Pin Name	I/O	Description
LGCTRL	I	Lower gate control signal input. LO = GL LO (LFET off). HI = normal operation (GL and GH strictly obey PWM). This pin should be driven with a logic signal, or externally tied high if not required; it should not be left floating
FAULT#	O	Open drain output pin. Any fault (over-current, over-temperature, shorted HFET, or POR / UVLO) will pull this pin to ground. This pin may be connected to the controller enable pin or used to signal a fault at the system level.
PWM	I	PWM input of gate driver, compatible with 3.3 V tri-state PWM signal.
REFIN	I	Input for external reference voltage for IMON signal. This voltage should be between 0.8 V and 1.6 V. Connect REFIN to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to GND.
IMON	O	Current monitor output referenced to REFIN. IMON will be pulled high (to REFIN +1.2 V) to indicate an HFET shorted or over-current fault. Connect the IMON output to the appropriate current sense input of the controller. No more than 56 pF capacitance can be directly connected across IMON and REFIN pins. With a 100 Ohm series resistor, up to 470 pF may be used.
TMON	O	Temperature monitor output. TMON will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across TMON and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kohm for 100 nF load.

C870_B Resource Usage

```
Circuit Stats...
      Number of AnD_Temp_Sensor     1
      Number of AnD_ADi_dual        1
      Number of AnD_SIM_Sense       1
      Number of AnD_ATC_IO          9
      Number of AnD_ATC_Comp        8
      Number of AnD_ATC_Summer      2
      Number of AnD_PMT             4
      Number of AnD_CM_PID          2
      Number of AnD_Nref_dyn        1
      Number of AnD_Nref_fix        5
      Number of AnD_PTG_Phase_Count 1
      Number of AnD_PTG_GBUF        1
      Number of AnD_PTG_OSC         1
      Number of AnD_DFFN            11
      Number of AnD_DFF             58
      Number of LUT4                137

Resource Usage...
      io       9 used (Capacity   24)
      clb     21 used (Capacity   64)
      cm       2 used (Capacity    8)
      pmt      4 used (Capacity   16)
      sim      1 used (Capacity    8)
      atc      4 used (Capacity    6)
      corner   4 used (Capacity    4)
      ptg      1 used (Capacity    2)
      uLogic 137 used (Capacity  512)
Components Stats...
      $techmap\component_1
            AnD_DFF           55
            AnD_DFFN          4

      $techmap\otp_fuse_module
            AnD_DFF           3
            AnD_DFFN          7

      component_1
            AnD_ADi_dual      1
            AnD_ATC_Comp      7
            AnD_ATC_Summer    2
            AnD_CM_PID        2
            AnD_Nref_dyn      1
            AnD_Nref_fix      4
            AnD_PMT           4
            AnD_SIM_Sense     1

      otp_fuse_module
            AnD_ATC_Comp      1
            AnD_Nref_fix      1
```

Internal PMIC Blocks and Resources

Each Power Component uses several blocks and resources that are available as part of the AmP platform. Listed below is a description of blocks and resources that are used to create C870_B power components. An example application is shown in Figure 6.

Noise-immune references - Nrefs

- 10 bit, 0.1% resolution for <0.5% regulation
- Curvature compensated band-gap trim
- Precision across process, temperature

Nrefs provide reference voltages that can be routed to analog GPIOs, Adaptive Digitizers, Threshold Comparators, In Amp, SIM linear LDO and SIM protect. On power-up, Nrefs are configured to voltages specified by the user.

Compensator Memory – CRAM

- Flexible, high bandwidth PID
- Adjust gain/phase margin, bandwidth
- Symmetric, binary scaling cuts memory by four
- Adaptive, dual regulation, 1 or 2 pole

The CRAM provides digital compensation to integrated MOSFETs implementing switching regulator functions including buck, boost and multi-phase regulators. The CRAM implements the Proportional Integral Derivative algorithm, PID, as in the following equation:

P[n] = P[n-1]*a1 + P[n-2]*a2 + E[n]*a + E[n-1]*b + E[n-2]*c
1 pole: a1 = 1, a2 = 0 2 pole: a1 = 0.5, a2 = 0.5
E[n] = Vref-Vout[n]

Precision Modulation Timers - PMTs

- 11-bit, 1.25 ns resolution
- Static, dynamic or stopwatch
- Reduces bias current, system freq.

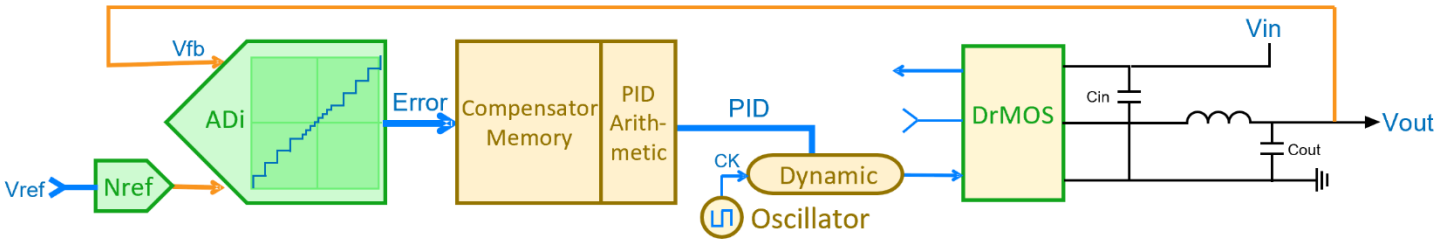
The PMT provides precision delays for, MOSFET turn-on, turn-off timing and sensor sample timing. Delays may be fixed or dynamic ranging from nanoseconds, milliseconds, microseconds to seconds with a resolution or better than one nanosecond.

Adaptive Digitizer – ADi

- Digitize feedback Error
- Highest precision at reference point
- Low cost & fast sampling

The ADi converts differential analog signals from GPIOs or Nrefs and deliver up to 10-bits digital signed magnitude numbers to the digital fabric. Each ADi consists of two digitizers to provide highest speed and precision.

Figure 6: AmP Blocks and Resources driving DrMOS Example - Buck Regulator



Additional Resources

- AnDAPT AmP Platform_B datasheet

Revision History

Date	Revision
01/09/2023	Added description of jitter/transient optimization drop down box
12/17/2022	Adjustable output voltage with down to 2.4 mV resolution changed to 2.5 mV resolution
08/26/2022	Initial release

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On-Demand Power Management

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Trademarks