Source Selector

Power Component: I470

Product Description

The I470 Component is a customizable 2 channel source selector targeted at DC power with battery backup or dual battery applications.

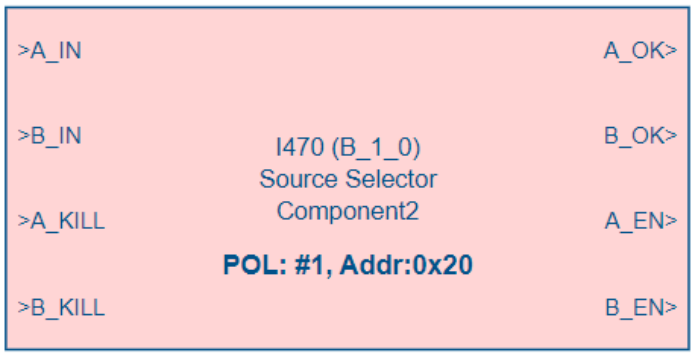
Features

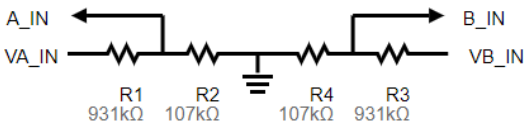
- Two independent window comparators
- Parameterized UVLO and OVP thresholds
- Parameterized rising/falling hysteresis on thresholds
- Independent “OK” outputs
- “EN”able outputs with priority encoding of A Over B
- I2C readable status register
- I2C adjustable UVLO thresholds

Applications

- Dual Power Sources
- Dual battery source selection
- DC / Battery pack backup source selection

Figure 1: I470 component





Product Detail

The I470 Source Selector enables priority selection of two external high voltage sources based on programmable UVLO and OVP threshold parameter settings. Thresholds are set in WebAMP parameter settings and can be updated over I2C.The following describes the Source Selector operation.

Operations

- Independent UVLO thresholds are available for A_IN and B_IN
- UVLO falling thresholds are parameters and can also be modified via I2C
- UVLO Hyst is a parameter
- UVLO rising thresholds are generated from UVLO falling + UVLO Hyst
- Both inputs use same OVP rising and OVP falling threshold parameters
- An input is OK if it sits between its UVLO and OVP thresholds
- Selection Logic will prioritize A_ENABLE over B_ENABLE
- Both sources can be disabled using the A_KILL and B_KILL inputs

Pin Function and Description Table

Port Name	I/O	Description
A_IN	I	source A input voltage
B_IN	I	source B input voltage
A_KILL	I	Source A kill input. Causes A_EN to be de-asserted. If B is OK, B_EN will be asserted
B_KILL	I	Source B kill input. Causes B_EN to be de-asserted
A_OK	O	Indicator that A_IN is between its UVLO and OVP thresholds
B_OK	O	Indicator that B_IN is between its UVLO and OVP thresholds
A_EN	O	Signal to enable Source A
B_EN	O	Signal to enable Source B

Figure 2: I470 Block Diagram

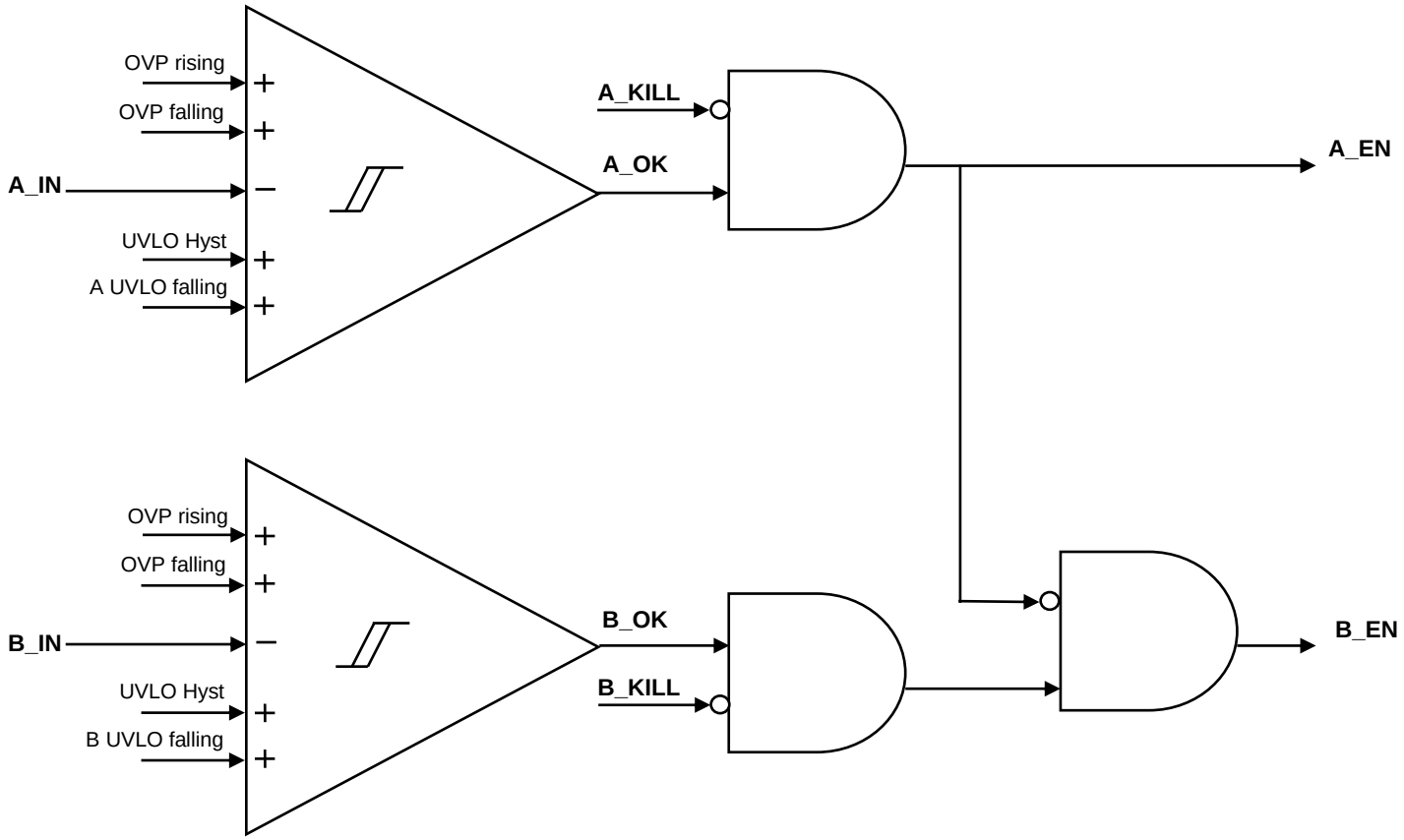
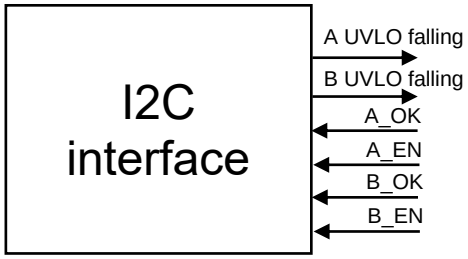


Fig.1 I470 Logic diagram



Electrical Characteristics

VIN=12V, TA=25°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Voltages below are voltages at the pins of the i.c.					
V_{A_IN}	source A divided input voltage	0.5		2.5	V
V_{B_IN}	source B divided input voltage	0.5		2.5	V
Threshold accuracy	V_{IN} = 0.8v	-8		+8	mV
	0.75v > V_{IN} > 2.0v	-10		+10	mV
	0.5 > V_{IN} > 2.5v	-15		+15	mV
Threshold variation over temperature	$0^0C<T_A<85^oC$	-0.4		+0.4	%
	$-40^0C<T_A<150^oC$	-0.8		+0.8	%

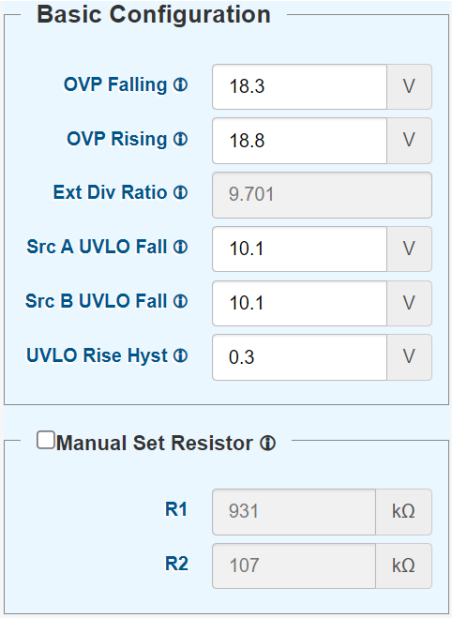
Recommended Operating Conditions

over operating free-air temperature range

Symbol	Paramaeter	Min	Typ	Max	Units
Voltages below are specified before an external voltage divider The voltage divider should ensure that the Vin limits above are not exceeded					
Src A UVLO fall	UVLO falling threshold for source A		10.1		V
Src B UVLO fall	UVLO falling threshold for source B		10.1		V
UVLO rise Hyst	hysteresis from UVLO falling to UVLO rising for both sources		0.3		V
OVP falling	OVP falling threshold for both sources		18.3		V
OVP rising	OVP rising threshold for both sources		18.8		V

Parameter Settings

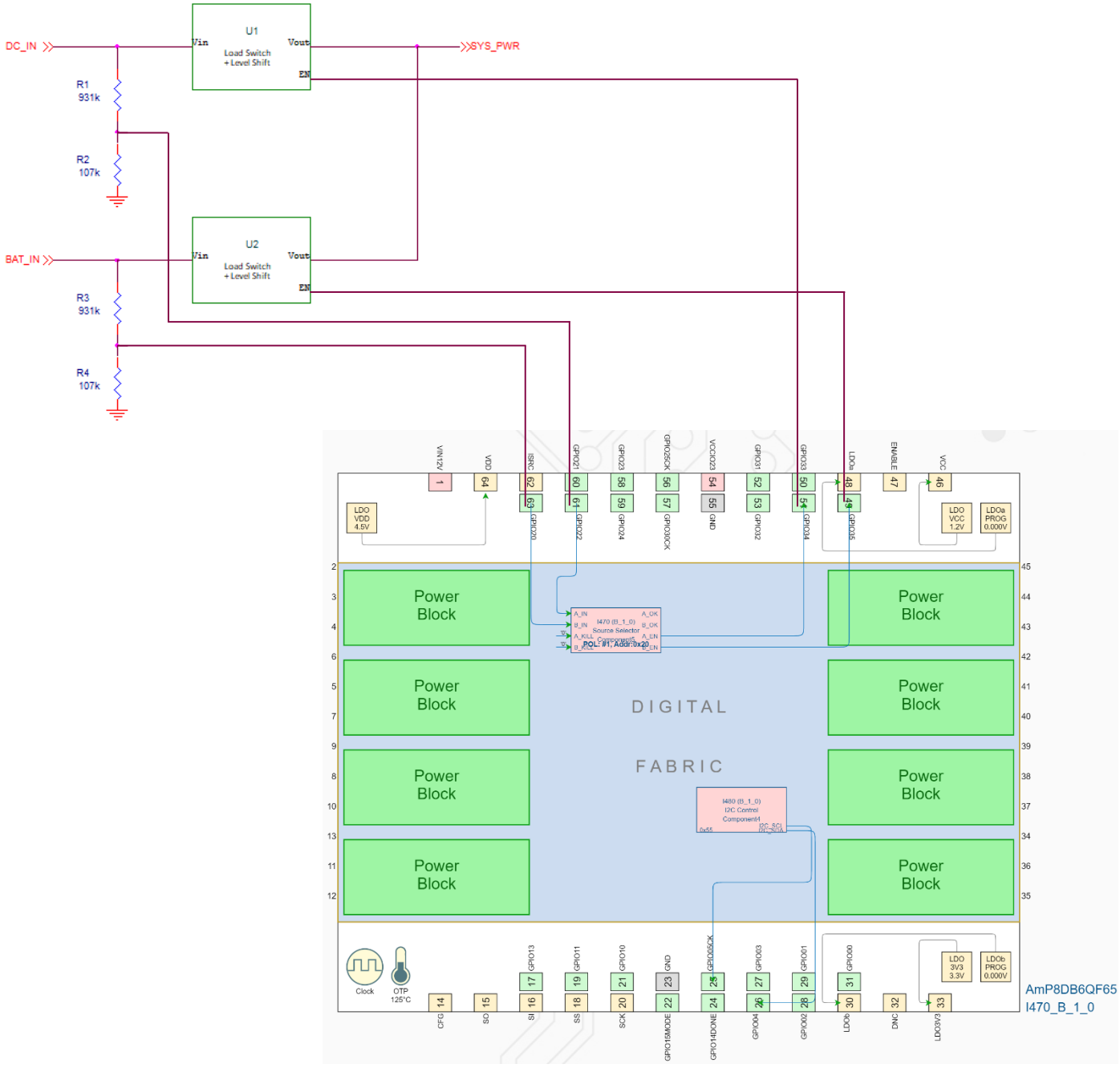
Default parameters may be changed per user requirement.



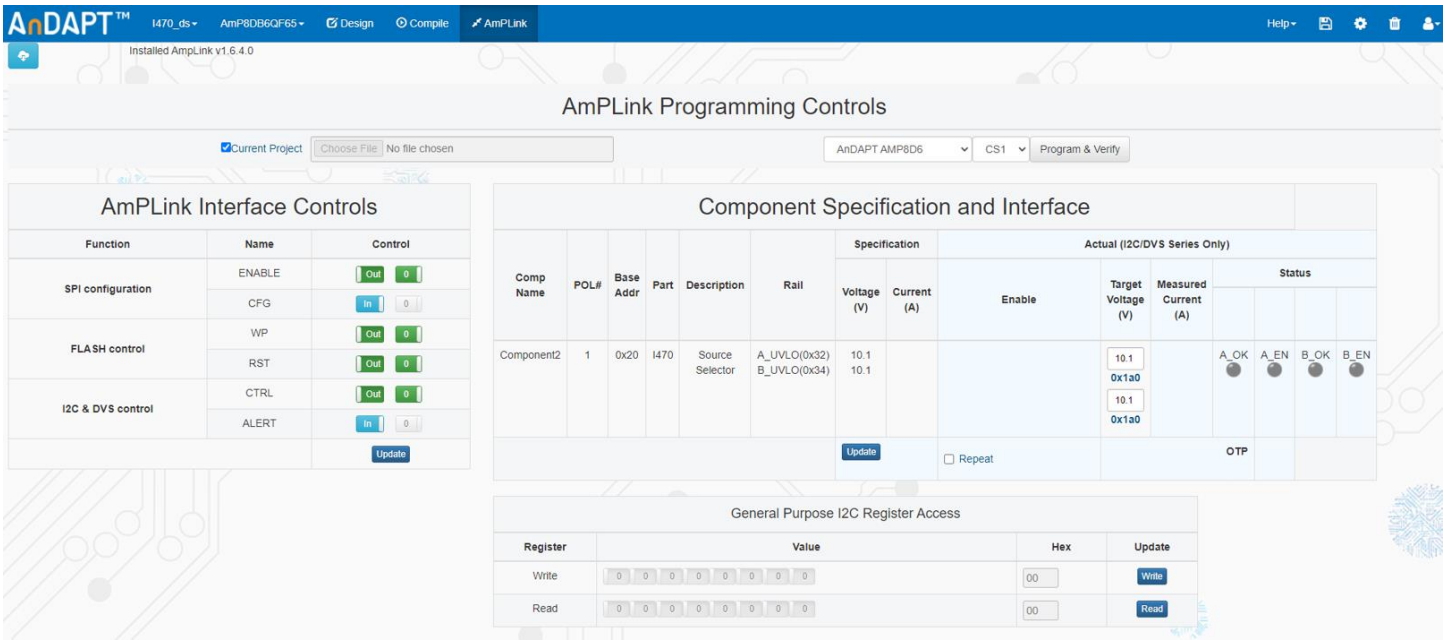
Basic Design

Below shows part of a design using this component

Figure 3 I470 example schematic diagram



I2C Interface



The I2C registers are summarized Table 1.

Note that the first I2C series Power Component will automatically insert one I480 I2C Controller Power Component with additional SDA and SCL signal pins. Additional I2C series Power Components will not insert an I480 as one I480 supports multiple I2C series Power Components.

The I2C Interface provides a user interface to read and write the I2C commands for all the I2C series Power Components contained in the AmP device. When I2C enabled component is present in the design, users will be able to read several device and design parameters. Refer to “I2C Design and Usage Guide” for details on I2C register architecture and accessing I2C registers. The registers used for I470 component are shown in Table 1.

Table 1: I2C Register Map

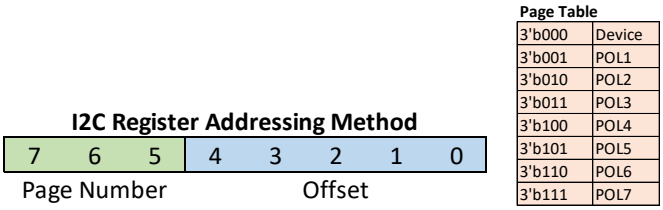
Address	Register / bit	R/W	7	6	5	4	3	2	1	0
0x28	STATUS	R	B_EN	B_OK	A_EN	A_OK	unused reads 1	unused reads 1	unused reads 1	unused reads 1
0x32	Source A UVLO lo	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Source A UVLO hi	R/W	unused	unused	unused	unused	unused	unused	Bit9	Bit8
0x34	Source B UVLO lo	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Source B UVLO hi	R/W	unused	unused	unused	unused	unused	unused	Bit9	Bit8

* Address page+offset methodology as in Figure 4.
** Slave Address can be set in I480 Module

Register Address Format

The register address format for the AmP device is shown in Figure 4. The register address is an 8-bit number which can take on any value from 0x00 to 0xFF. The register space is divided into eight pages, with page 0 dedicated to device-wide registers and pages 1 through 7 to support up to 7 POLs.

Figure 4 Amp I2C register address format



Page Table

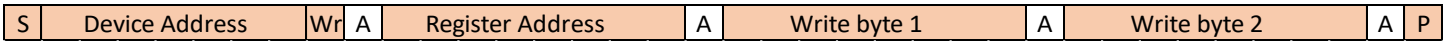
3'b000	Device
3'b001	POL1
3'b010	POL2
3'b011	POL3
3'b100	POL4
3'b101	POL5
3'b110	POL6
3'b111	POL7

I2C Write/Read Protocol

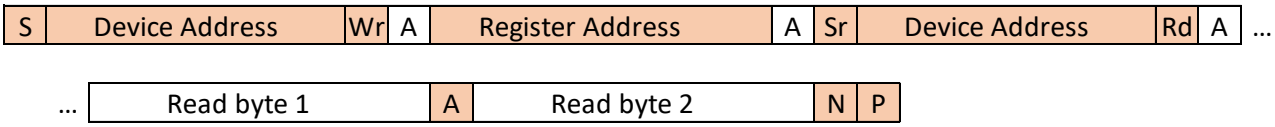
An Amp device is addressed by its pre-defined 7-bit device physical address (default address is 0x55). Along with the 7-bit address, an 8th bit is added to the LSB position to identify whether the following transaction is a read or write, making it an 8-bit address byte. If the least significant bit of the address byte is zero, it is a write transaction whereas a 1 is a read transaction. The Amp device parameters as well as the read/write parameters of the different POLs in the device are accessed through 256 8-bit registers. Every I2C transaction to the Amp device therefore needs another 8-bit register address. The general format of I2C-Amp device write/read protocol is shown in Figure 5. Note that the Amp device is always the slave. In the figure, the shaded portion is sent by the master and the unshaded portion by the slave.

Figure 5 I2C read/write protocol

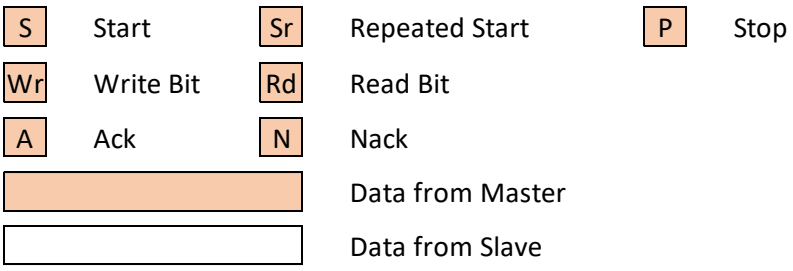
I2C write to the device



I2C read from the device



Details of the bit notation



Both write and read transactions can be either a one byte or a multi-byte transfer. Accordingly, the register address is either the address of the register that is being accessed or the starting address of a sequence of registers that is being accessed. For a write transaction, the device updates write data to successive registers until it receives an I2C stop signal. For read transactions, the master first writes the starting address into the device and starts accepting read from the device after a repeated start signal. The device sends successive register data until the master issues a NACK for the last byte read.

I470_B Resource Usage

```
Circuit Stats...

      Number of AnD_I2C_Phy          1
      Number of AnD_ADi_dual         1
      Number of AnD_ATC_IO           10
      Number of AnD_CM_RAM_256x18    1
      Number of AnD_Nref_dyn         2
      Number of AnD_PTG_Phase        1
      Number of AnD_PTG_GBUF         1
      Number of AnD_PTG_OSC          1
      Number of AnD_DFFN             2
      Number of AnD_DFF              73
      Number of AnD_ADCR             20
      Number of LUT4                 154


Resource Usage...

      io       6 used (Capacity   24)
      clb     22 used (Capacity   64)
      cm       1 used (Capacity    8)
      corner   2 used (Capacity    4)
      ptg      1 used (Capacity    2)
      uLogic 174 used (Capacity  512)
```

Revision History

Date	Revision
03/30/2022	Initial version

AnDAPT

On-Demand Power Management

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Trademarks