Power Component: I483

Product Description

The I483 Component is a customizable 1 or 2 channel PWM generator targeted at DC motor or stepper motor driving.

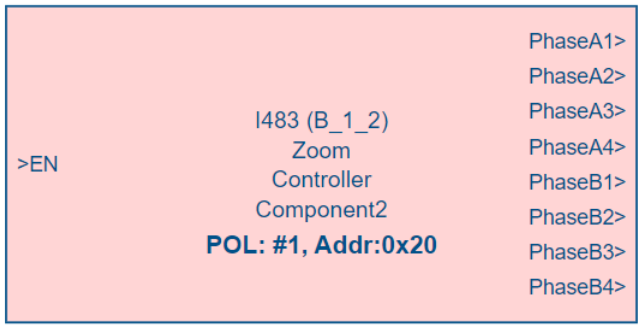
Features

- Two independent PWM channels
- Selectable pulse rates 100pps to 1000pps
- I2C controlled sequencer 1- 511 pulses
- I2C controlled Low Power mode
- I2C controlled CW / CCW direction
- Autonomous accelerate & decelerate phases

Applications

- Stepper motor driving

Figure 1: I483 component symbol



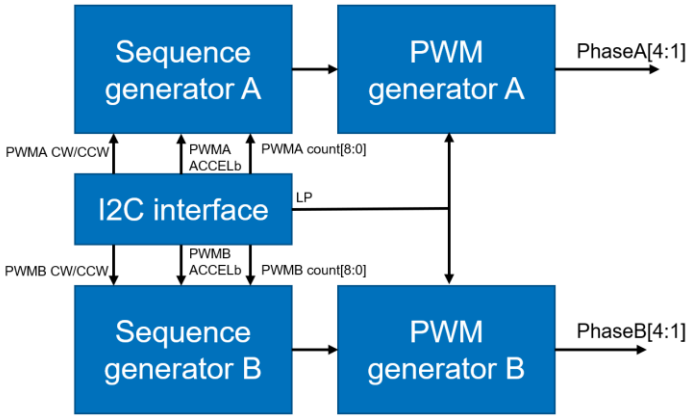
Pin Function and Description Table

Port Name	I/O	Description
PhaseA[4:1]	O	PWM A output phases
PhaseB[4:1]	O	PWM B output phases
EN	I	Currently no connection, possible future expansion

Theory of operation

Each of the two independent PWM generators produces quadrature output phases. The min. and max. rate of these phases is parameterized from 100pps to 1000pps. The outputs can be set to a low power state where all phases are logic 0, exiting from low power returns the outputs to the same state as when low power was entered.
An I2C controlled sequencer commands the PWM generators to accelerate from min to max rate, run for up to 2048 cycles at max rate and then decelerate from max to min rate. This sequence is autonomous and begins once the I2C transaction is complete. The accelerate and decelerate sequence can optionally be disabled and the PWM will run at the min rate for the entire sequence. The outputs can follow a P1->P2->P3->P4 or P4->P3->P2->P1 direction also under I2C control. There is an I2C register which can be read to determine if the PWM is running or stopped.

Block Diagram



Electrical Characteristics

VIN=12V, TA=25°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Pulse rate		100		1000	Hz
Pulse rate accuracy	Vin=12V, T_A=25°C	-7		+7	%
	-40°C<T_A<150°C	-9		+9	%

Recommended Operating Conditions

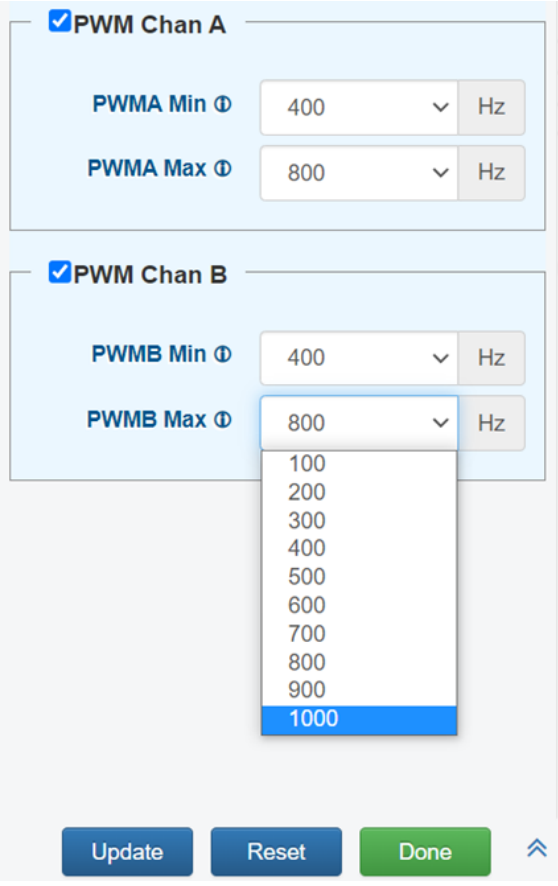
over operating free-air temperature range

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage	4.5		14	V
Fout	Output pulse rate.	100		1000	Hz

Parameter Settings

Basic Configuration

Default parameters may be changed per user requirement.



Basic Design

Figure 2 below shows a simple WebAmP design using this component.

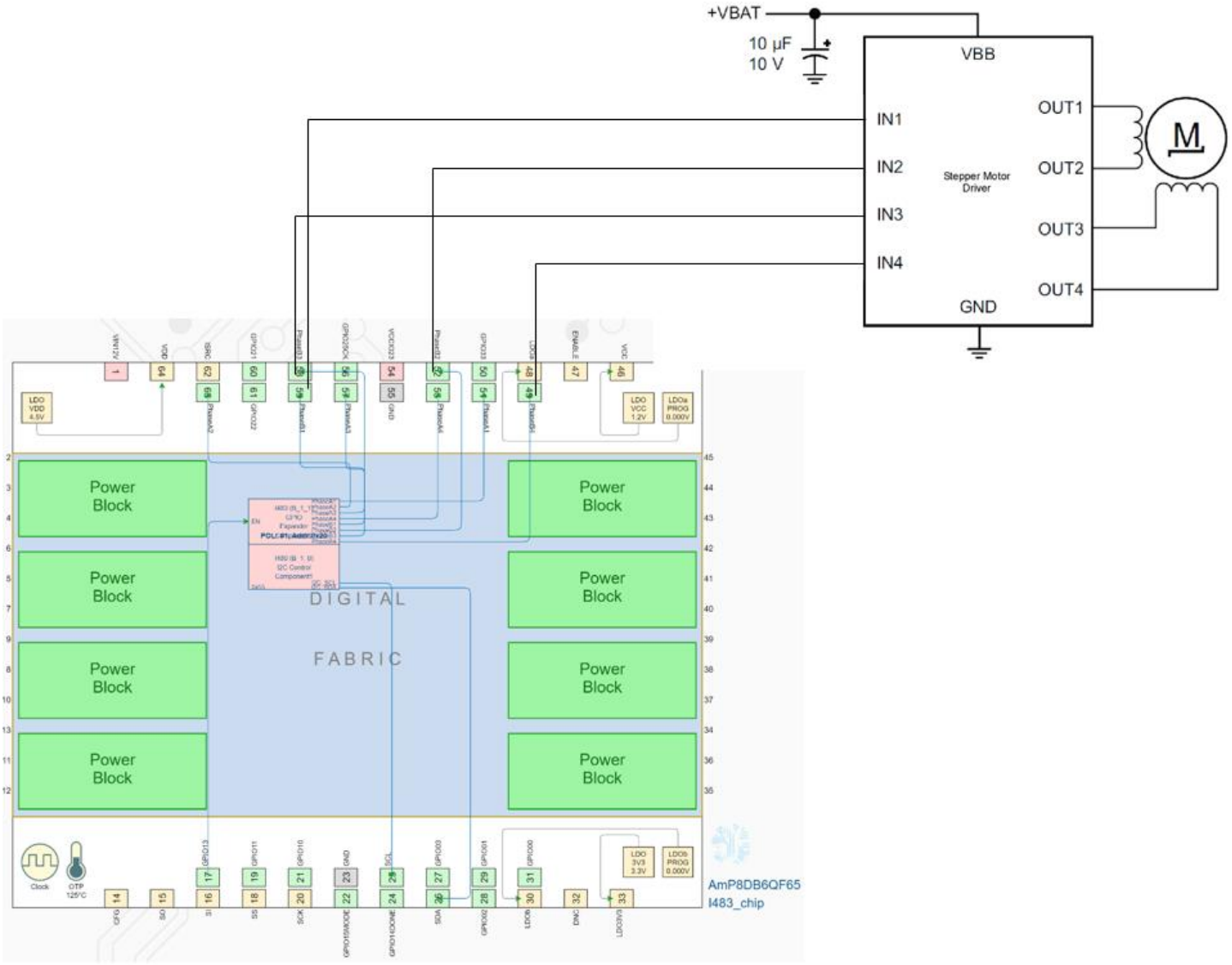
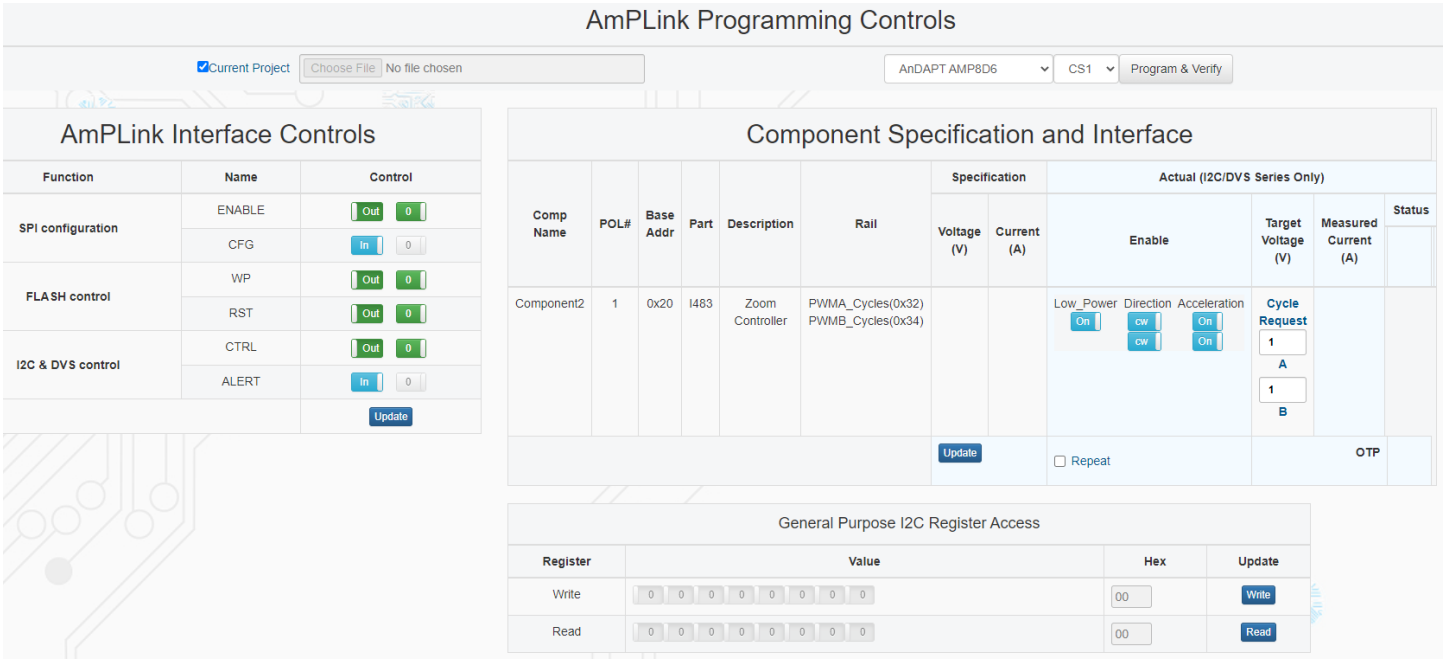


Figure 2: I483 WebAmP design

I2C Interface



The I2C AmPScope Interface provides a user interface to read and write the I2C commands for all the I2C series Power Components contained in the AmP device. When I2C enabled component is present in the design, users will be able to read several device and design parameters. Refer to “I2C Design and Usage Guide” for details on I2C registers architecture and accessing I2C registers.

Writing to a PWM sequence register starts the requested sequence immediately after the i2c write is completed. Unless requested not to, the sequencer will go through accelerate –> run –> decelerate steps.

I2C sequence writes will only be accepted & acknowledged when the PWM being written to is not running. The user should ensure sufficient time for a sequence to complete before sending additional i2c register writes.

Note that the first I2C series Power Component will automatically insert one I480 I2C Controller Power Component with additional SDA and SCL signal pins. Additional I2C series Power Components will not insert an I480 as one I480 supports multiple I2C series Power Components.

The I2C registers are summarized in Table 1.

Table 1a: I2C Register Map

Address	Register	R/W	7	6	5	4	3	2	1	0
0x28	Status	R	A_Run	B_Run	0	0	1	1	1	1
0x30	Low Power Enable	W	unused	unused	unused	unused	unused	unused	unused	LP
0x32	PWMA Sequence [7:0]	W	B7	B6	B5	B4	B3	B2	B1	B0
	[15:8]	W	CCW	ACCELb	unused	unused	unused	B10	B9	B8
0x34	PWMB Sequence [7:0]	W	B7	B6	B5	B4	B3	B2	B1	B0
	[15:8]	W	CCW	ACCELb	unused	unused	unused	B10	B9	B8

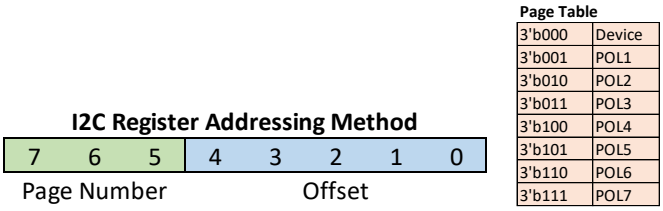
Table 1b: I2C Register Description

Register Bit	Description
A_Run **B_Run**	1: Channel A/B is currently running a sequence 0: Channel A/B is stopped
[B10..B0]	Phase count request 0x001 – 0x7FF
LP	Low Power Enable When set output phases are low – low – low – low When clear output phases are high – low – high – low Applies to both PWMA & PWMB simultaneously Should only be changed when PWM is in stop condition
CCW	When set commands PWM phase sequence: P1 -> P2 -> P3 -> P4 When clear commands PWM phase sequence: P4 -> P3 -> P2 -> P1
ACCELb	When set, the PWM will skip the accelerate / decelerate steps giving the sequence: • Stop • Run for the requested number of phases at min. rate • Stop When clear, the PWM will go through the sequence: • Stop • Accelerate from min. to max. rate, 1 phase per rate • Run for the requested number of phases at max. rate • Decelerate from max. to min. rate, 1 phase per rate • Stop Note: The total number of phases output when ACCELb = 0 is given by: **((max. rate – min. rate) / 100) + Phase count request + ((max. rate – min. rate) / 100)** Example: ((800 – 400) / 100) + 8 + ((800 – 400) / 100) = 16 phases

Register Address Format

The register address format for the Amp device is shown in Figure 3. The register address is an 8-bit number which can take on any value from 0x00 to 0xFF. The register space is divided into eight pages, with page 0 dedicated to device-wide registers and pages 1 through 7 to support up to 7 POLs.

Figure 3 Amp I2C register address format

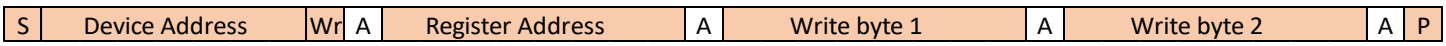


I2C Write/Read Protocol

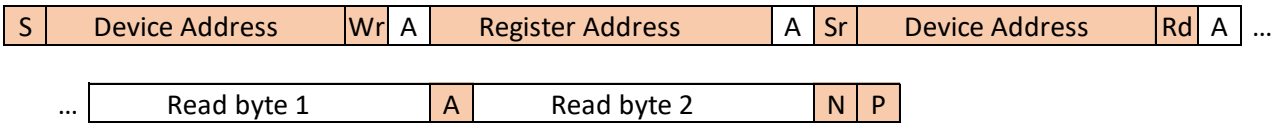
An Amp device is addressed by its pre-defined 7-bit device physical address (default address is 0x55). Along with the 7-bit address, an 8th bit is added to the LSB position to identify whether the following transaction is a read or write, making it an 8-bit address byte. If the least significant bit of the address byte is zero, it is a write transaction whereas a 1 is a read transaction. The Amp device parameters as well as the read/write parameters of the different POLs in the device are accessed through 256 8-bit registers. Every I2C transaction to the Amp device therefore needs another 8-bit register address. The general format of I2C-Amp device write/read protocol is shown in Figure 4. Note that the Amp device is always the slave. In the figure, the shaded portion is sent by the master and the unshaded portion by the slave.

Figure 4 I2C read/write protocol

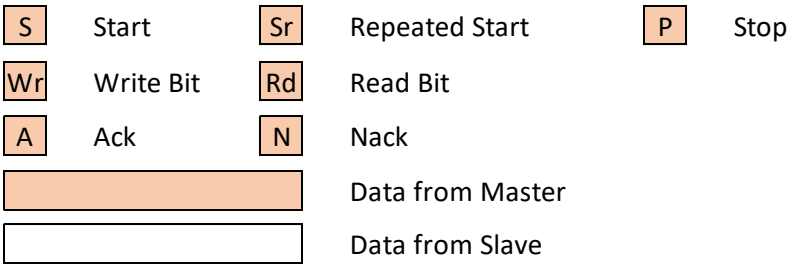
I2C write to the device



I2C read from the device



Details of the bit notation



Both write and read transactions can be either a one byte or a multi-byte transfer. Accordingly, the register address is either the address of the register that is being accessed or the starting address of a sequence of registers that is being accessed. For a write transaction, the device updates write data to successive registers until it receives an I2C stop signal. For read transactions, the master first writes the starting address into the device and starts accepting read from the device after a repeated start signal. The device sends successive register data until the master issues a NACK for the last byte read.

I2C AmPLink Interface

The AnDAPT AmPLink Interface can be used to exercise I2C commands of the I483 design.

Figure 5a: I2C transaction: 0x55 32 03 40 <- request 3 pulses with ACCELb bit set on PWMA

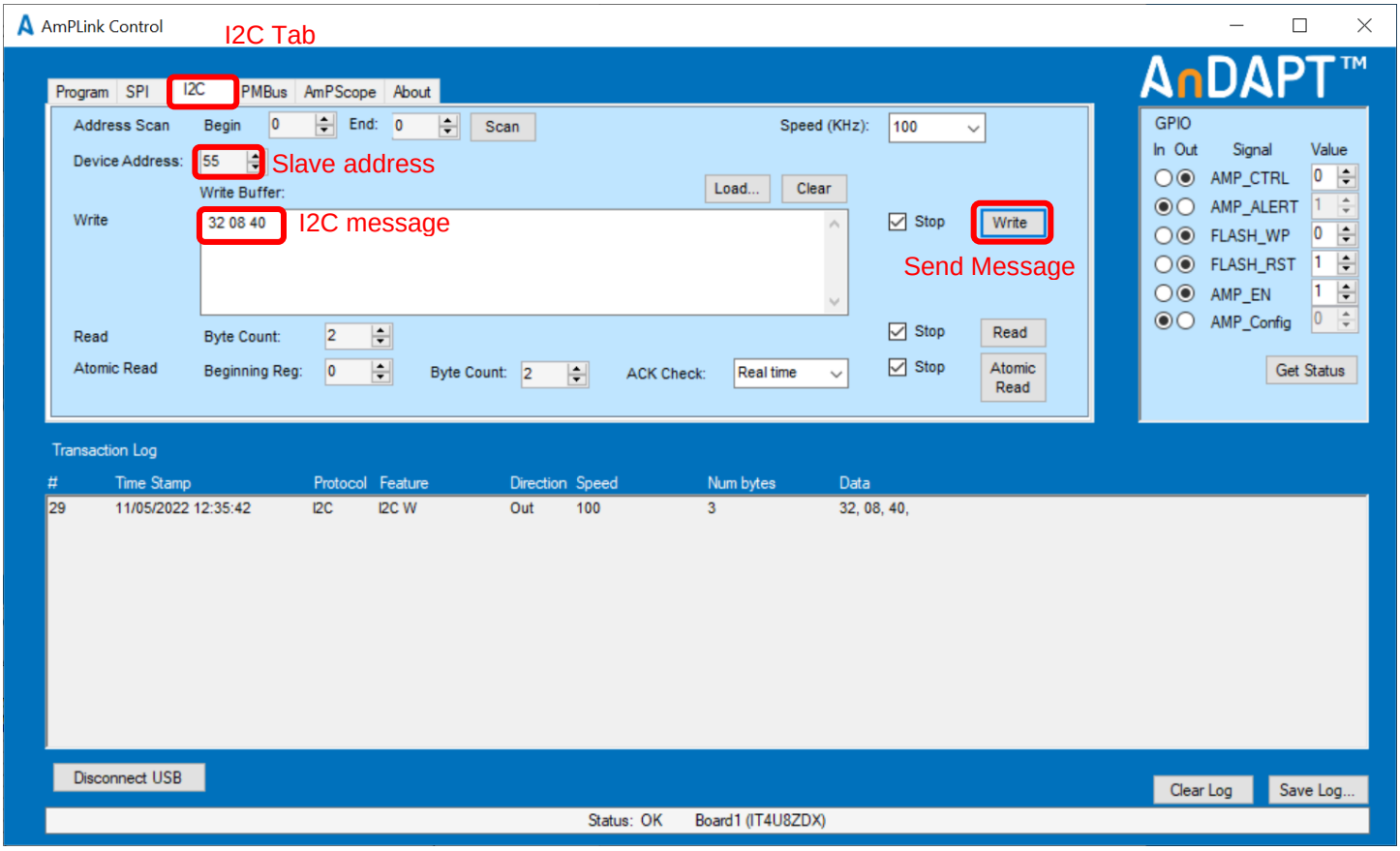


Figure 5b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4

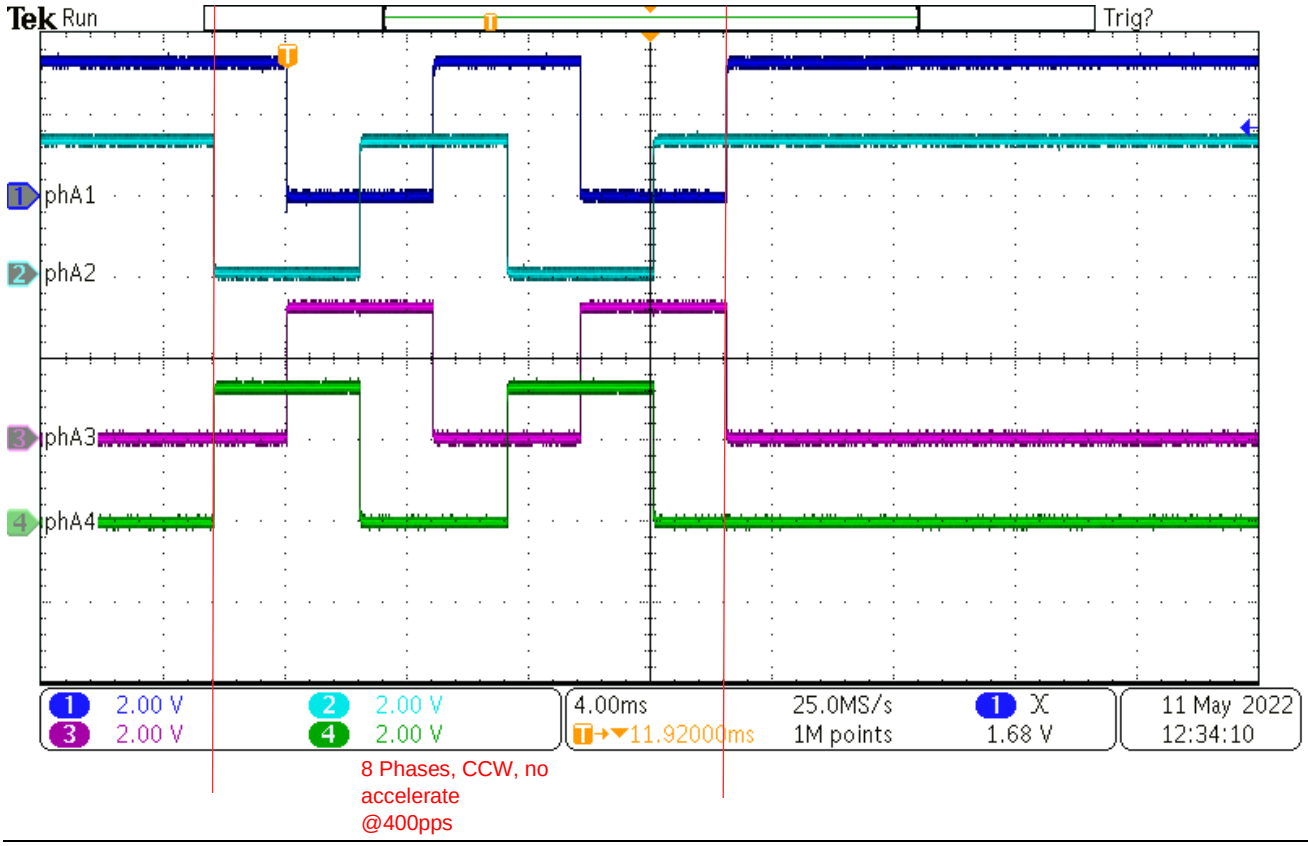


*Figure 6a: I2C transaction: 0x55 32 08 80 <- request 8 phases **with** acceleration & deceleration, CCW, PWMA*

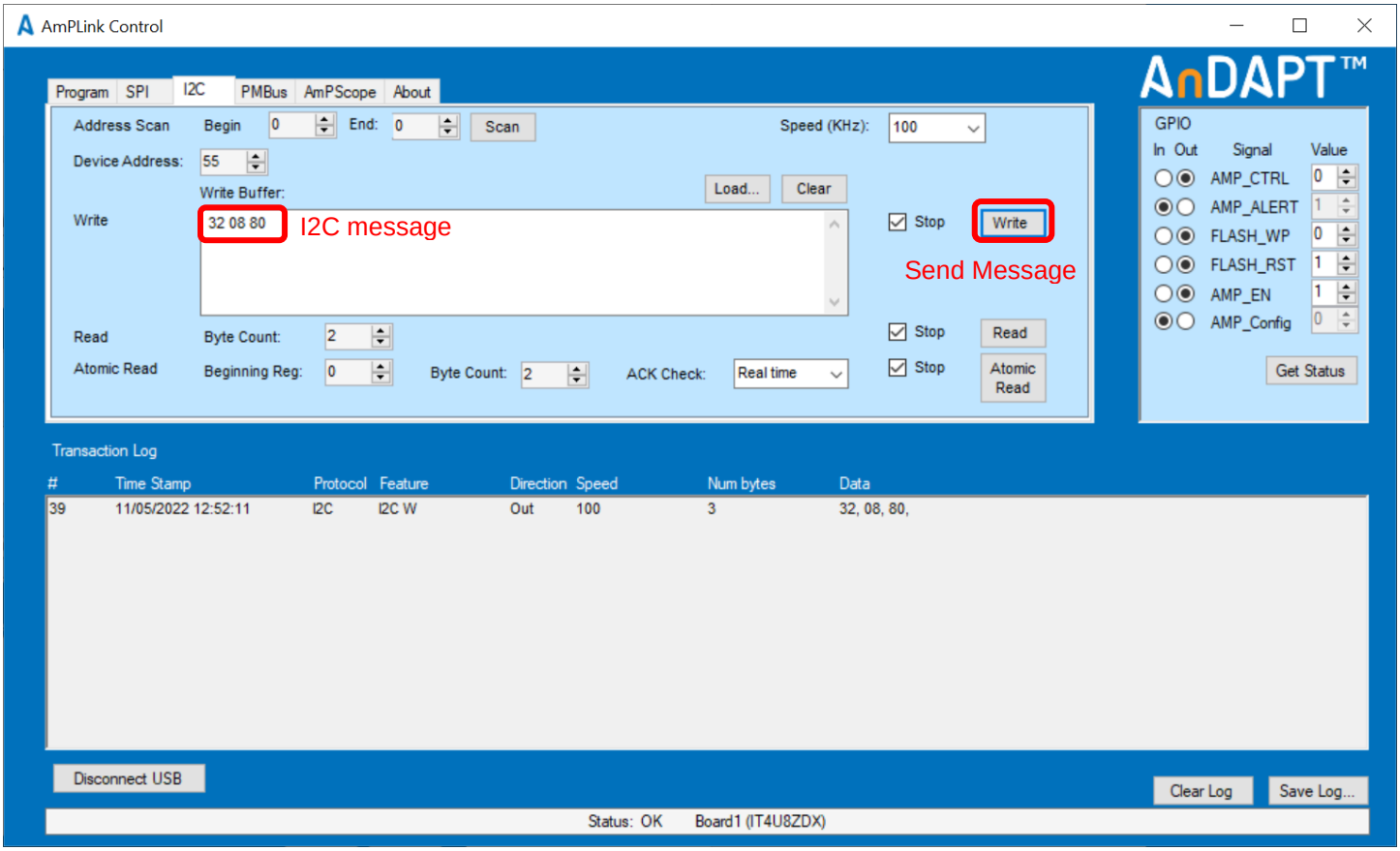


Figure 6b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4

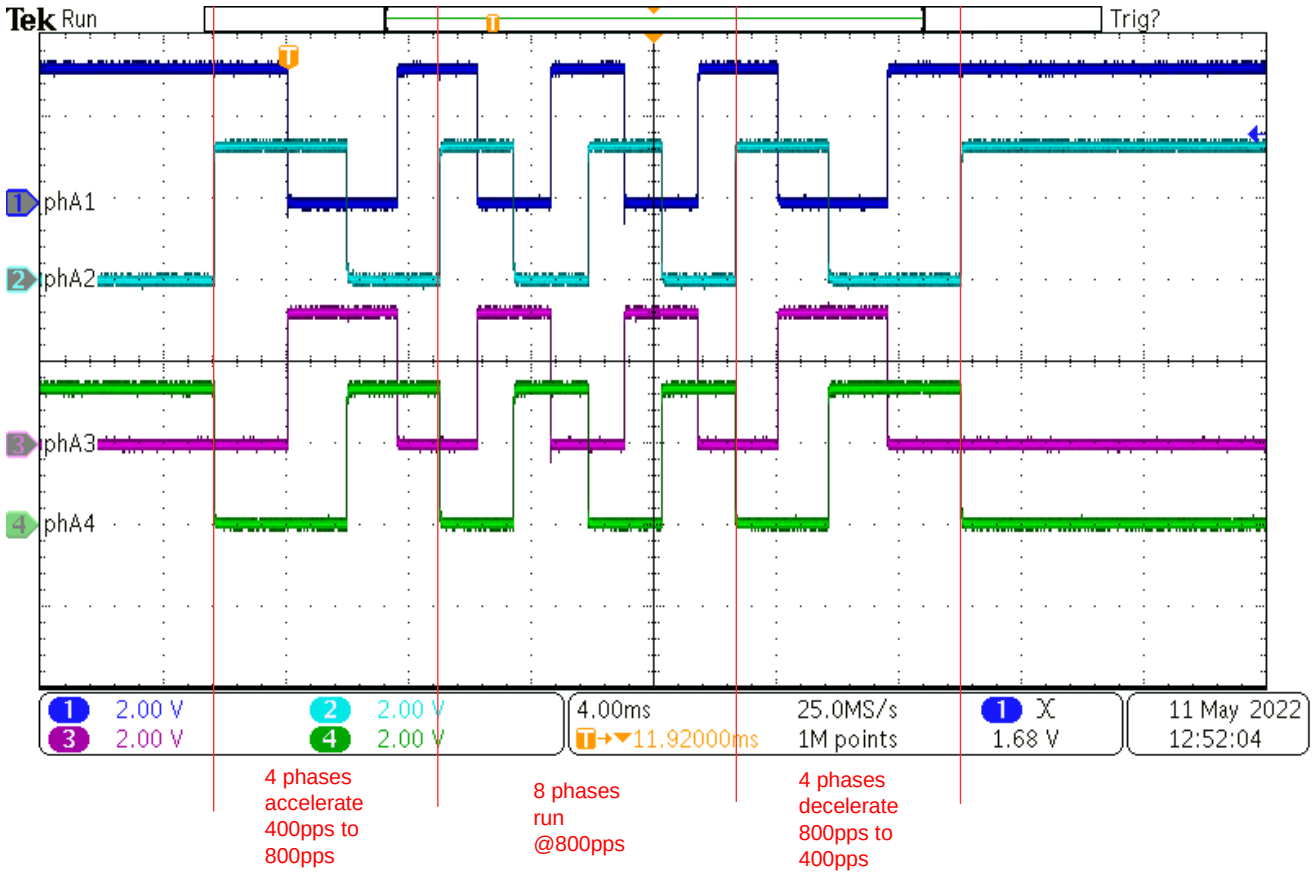


Figure 7a: Long phase sequence with repeated read of status register.

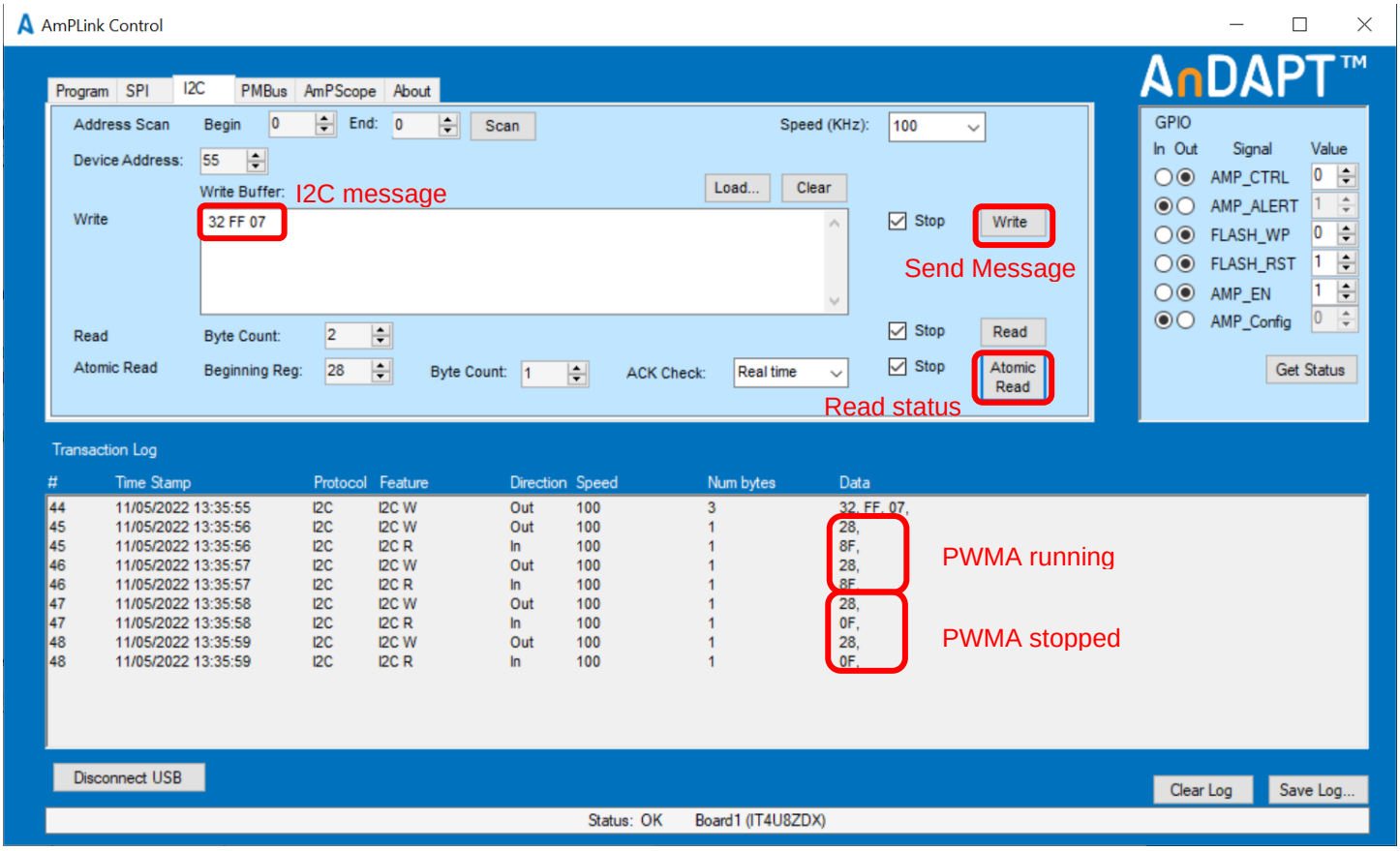


Figure 7b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4

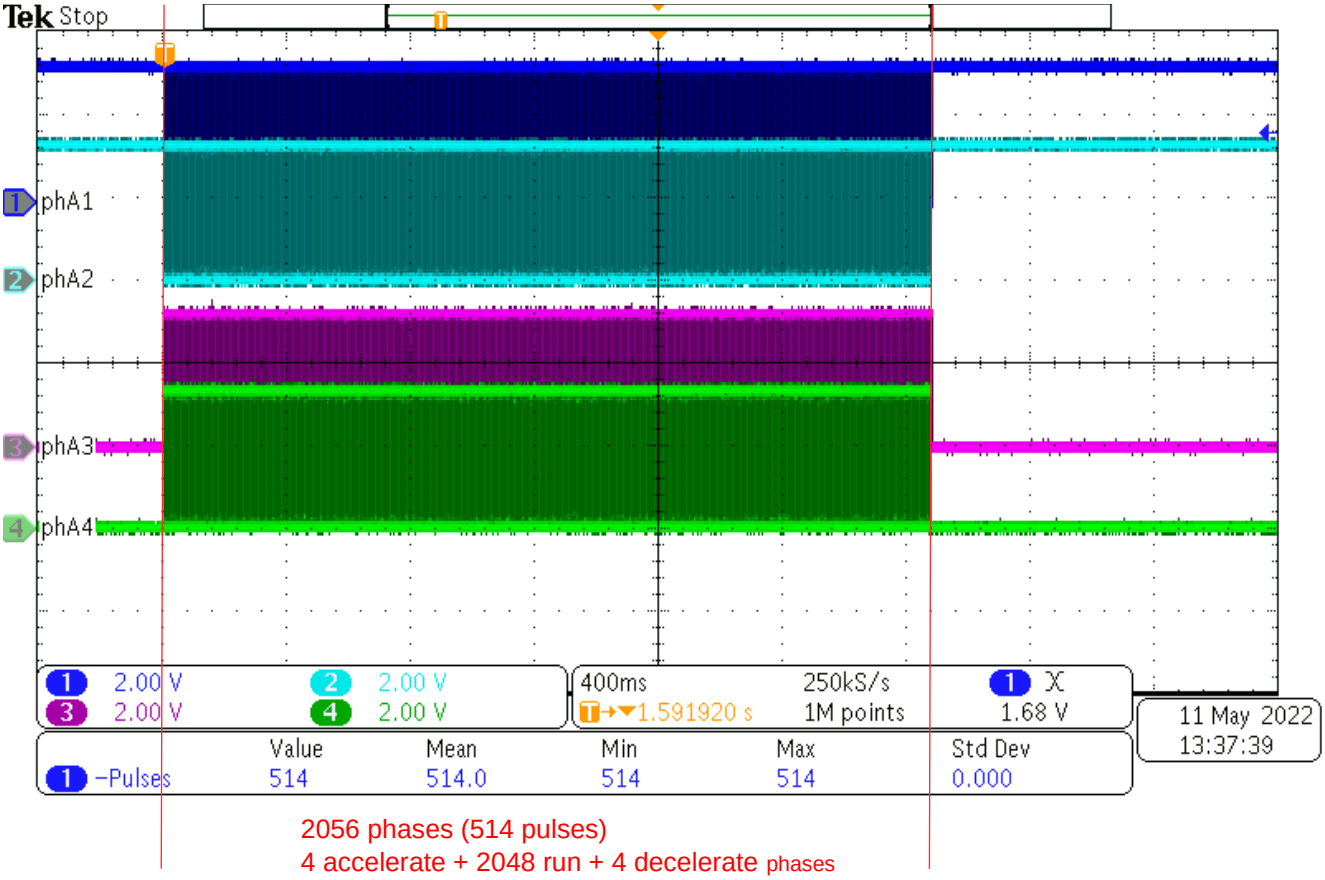
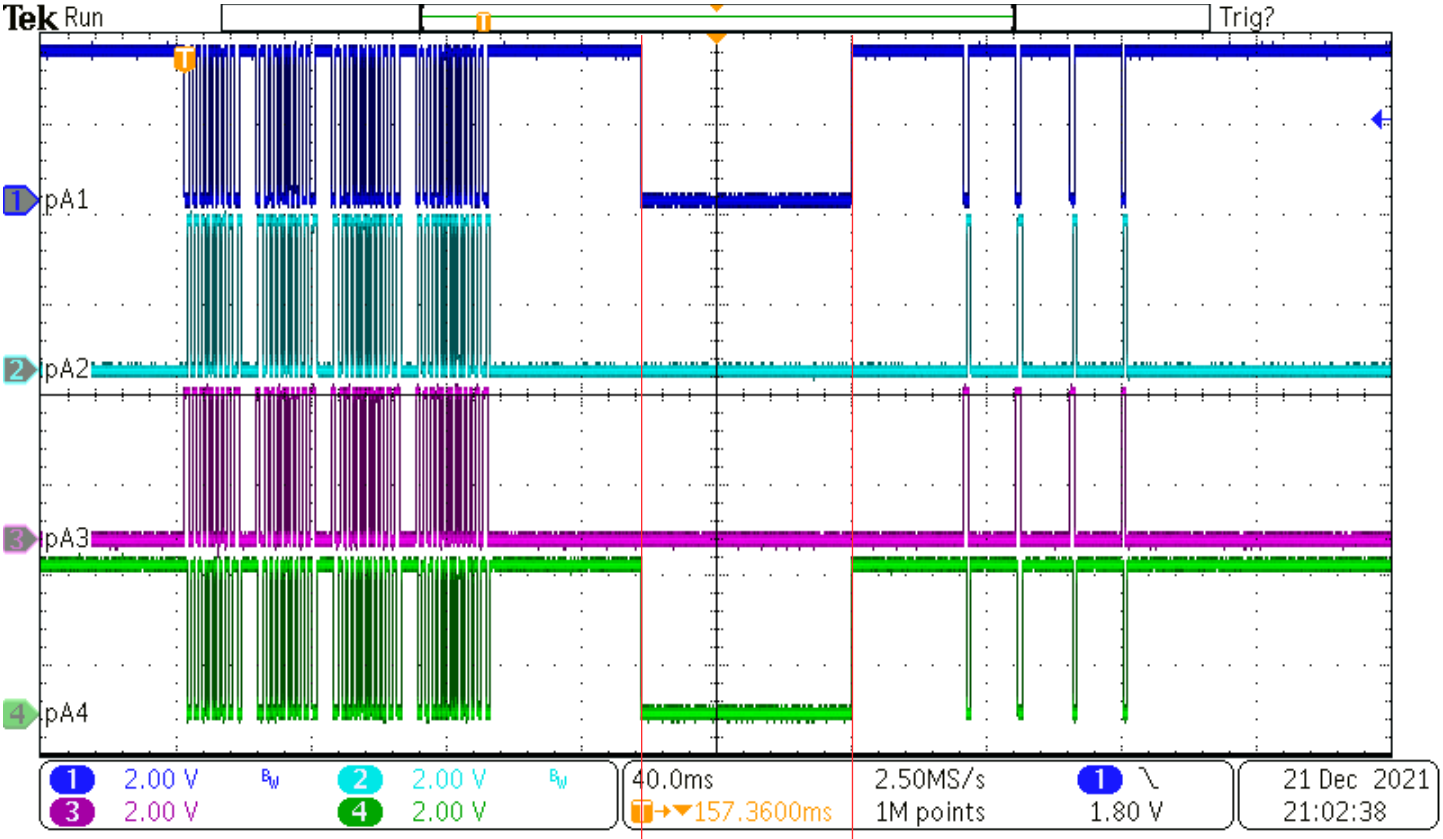


Figure 8: More complex example. Multiple i2c transactions using uController



I483 Resource Usage

Circuit Stats.

Number of AnD_I2C_Phy	1
Number of AnD_ATC_IO	10
Number of AnD_PMT	1
Number of AnD_CM_RAM_256x18	2
Number of AnD_PTG_Phase_Count	1
Number of AnD_PTG_GBUF	1
Number of AnD_PTG_OSC	1
Number of AnD_DFF	68
Number of LUT4	205

Resource Usage...

io	10 used	(Capacity 24)
clb	26 used	(Capacity 64)
cm	2 used	(Capacity 8)
pmt	1 used	(Capacity 16)
corner	1 used	(Capacity 4)
ptg	1 used	(Capacity 2)
uLogic	205 used	(Capacity 512)

Components Stats...

$techmap\component_1
- AnD_DFF 18

$techmap\component_2
- AnD_DFF 50

component_1
- AnD_CM_RAM_256x18 1

component_2
- AnD_CM_RAM_256x18 1
- AnD_PMT 1..

Additional Resources

AnDAPT AmP Platform datasheet

Revision History

Date	Revision
05/20/2022	Initial datasheet release

AnDAPT

On-Demand Power Management

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