Zoom Controller Power Component: 1483

Product Description

The I483 Component is a customizable 1 or 2 channel PWM generator targeted at DC motor or stepper motor driving.

Features

- Two independent PWM channels
- Selectable pulse rates 100pps to 1000pps
- I2C controlled sequencer 1- 511 pulses
- I2C controlled Low Power mode
- I2C controlled CW / CCW direction
- Autonomous accelerate & decelerate phases

Applications

• Stepper motor driving

Figure 1: I483 component symbol

I483 (B_1_2) Zoom Controller Component2 POL: #1, Addr:0x20	PhaseA1> PhaseA2> PhaseA3> PhaseA4> PhaseB1> PhaseB2> PhaseB3> PhaseB4>
---	--

Pin Function and Description Table

Port Name	I/O	Description
PhaseA[4:1]	0	PWM A output phases
PhaseB[4:1]	0	PWM B output phases
EN	I	Currently no connection, possible future expansion

Theory of operation

Each of the two independent PWM generators produces quadrature output phases. The min. and max. rate of these phases is parameterized from 100pps to 1000pps. The outputs can be set to a low power state where all phases are logic 0, exiting from low power returns the outputs to the same state as when low power was entered. An I2C controlled sequencer commands the PWM generators to accelerate from min to max rate, run for up to 2048 cycles at max rate and then decelerate from max to min rate. This sequence is autonomous and begins once the I2C transaction is complete. The accelerate and decelerate sequence can optionally be disabled and the PWM will run at the min rate for the entire sequence. The outputs can follow a P1->P2->P3->P4 or P4->P3->P2->P1 direction also under I2C control. There is an I2C register which can be read to determine if the PWM is running or stopped.

Block Diagram



Electrical Characteristics

VIN=12V, TA=25°C unless otherwise specified

Parameter	Condition	Min	Тур	Max	Units
Pulse rate		100		1000	Hz
Pulse rate accuracy	Vin=12V, T _A =25°C	-7		+7	%
	-40°C <t<sub>A<150°C</t<sub>	-9		+9	%

Recommended Operating Conditions

over operating free-air temperature range

Symbol	Parameter	Min	Тур	Мах	Unit
VIN	Input Voltage	4.5		14	V
Fout	Output pulse rate.	100		1000	Hz

Parameter Settings

Basic Configuration

Default parameters may be changed per user requirement.

──			
PWMA Min Φ	400	~	Hz
PWMA Max O	800	~	Hz
─			
PWMB Min Φ	400	~	Hz
PWMB Max O	800	~	Hz
	100 200 300 400 500 600 700 800 900 1000		
Update	Reset	Done	1



Basic Design

Figure 2 below shows a simple WebAmP design using this component.



Figure 2: I483 WebAmP design

I2C Interface

AnDAPT

AndAPT AMP8DG CS1 Program & Verry AndAPT AMP8DG CS1 Program & Verry AmPLink Interface Controls Component Specification and Interface Function Name Control ENABLE Comp PoL# Base Addr Part Description Rail Specification Actual (I2C/DVS Series Only- Voitage Target Measured Voitage Target Mea							ols	ming Contro	rogrami	k Pi	Lin	AmP	1			
Component Specification and Interface Function Name Control ENABLE Out O Base Addr Part Addr Description Rail Specification and Interface SPI configuration CFG Image Out O Base Addr Part Addr Description Rail Specification and Interface				Program & Verify	CS1	D6 •	APT AMP8	AnDA						Choose File No file chosen	Current Project	
Selection in the second secon																
Function Name Control Specific Specific Specific Specific Actual (12C/JC/SC/SC/SC/SC/SC/SC/SC/SC/SC/SC/SC/SC/SC				nterface	and Ir	ation	ecifica	ponent Spe	Com					ontrols	Interface C	AmPLink
SPI configuration ENABLE Image: Configuration Comp Name Pot Addr Base Addr Part Description Rail Voltage (V) Current (A) Enable Part Base Voltage (V) Part Part<		iy)	Series Onl	Actual (I2C/DVS		fication	Specif							Control	Name	Function
CFG In 0 Name Addr Voltage Current (V) (A) Enable Voltage Current (V) (A)	Status	Measured	Target					Rail	Description	Part	Base	POL#	Comp	Out 0	ENABLE	SPI configuration
		Current (A)	Voltage (V)	Enable		(A)	Voltage (V)				Addr		Name	in 0	CFG	arreoniguration
														Out	WP	ELA SH control
RST Out 0 Component2 1 0x20 1483 Zoom PWIMA_Cycles(0x32) Low_Power Direction Acceleration Cycle RST Out 0 0 0 0 0 0 Request			Cycle Request	ver Direction Acceleration	Low_Pow			PWMA_Cycles(0x32) PWMB_Cycles(0x34)	Zoom Controller	1483	0x20	1	Component2	Out	RST	PERSHCONTON
			1	cw On										Out 0	CTRL	12C & DVS control
ALERT IN 0														In 0	ALERT	
Update			в											Update		
UpdaleRepeat OTP		OTP		at	🗌 Repea		Update									
General Purpose I2C Register Access						Access	Register	eneral Purpose I2C	Ge							
Register Value Hex Update			pdate	Hex U				Value				r	Register			
Write 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			Write	00				0 0 0	0 0	0 0	0		Write			
Read 0 0 0 0 0 0 0 0 0 0 Read			Read	00				0 0 0	0 0	0 0	0		Read			

The I2C AmPScope Interface provides a user interface to read and write the I2C commands for all the I2C series Power Components contained in the AmP device. When I2C enabled component is present in the design, users will be able to read several device and design parameters. Refer to "I2C Design and Usage Guide" for details on I2C registers architecture and accessing I2C registers.

Writing to a PWM sequence register starts the requested sequence immediately after the i2c write is completed. Unless requested not to, the sequencer will go through accelerate -> run -> decelerate steps.

I2C sequence writes will only be accepted & acknowledged when the PWM being written to is not running. The user should ensure sufficient time for a sequence to complete before sending additional i2c register writes.

Note that the first I2C series Power Component will automatically insert one I480 I2C Controller Power Component with additional SDA and SCL signal pins. Additional I2C series Power Components will not insert an I480 as one I480 supports multiple I2C series Power Components.

The I2C registers are summarized in Table 1.

Table 1a: I2C	Fable 1a: I2C Register Map									
Address	Register	R/W	7	6	5	4	3	2	1	0
0x28	Status	R	A_Run	B_Run	0	0	1	1	1	1
0x30	Low Power Enable	W	unused	LP						
0x32	PWMA Sequence [7:0]	W	B7	B6	B5	B4	B3	B2	B1	B0
	[15:8]	W	CCW	ACCELb	unused	unused	unused	B10	B9	B8
0x34	PWMB Sequence [7:0]	W	B7	B6	B5	B4	B3	B2	B1	B0
	[15:8]	W	CCW	ACCELb	unused	unused	unused	B10	B9	B8

Table 1b: I2C Register Description

Register Bit	Description
A_Run B_Run	1: Channel A/B is currently running a sequence 0: Channel A/B is stopped
[B10B0]	Phase count request 0x001 – 0x7FF
LP	Low Power Enable When set output phases are low – low – low When clear output phases are high – low – high – low Applies to both PWMA & PWMB simultaneously Should only be changed when PWM is in stop condition
CCW	When set commands PWM phase sequence: P1 -> P2 -> P3 -> P4 When clear commands PWM phase sequence: P4 -> P3 -> P2 -> P1
ACCELb	When set, the PWM will skip the accelerate / decelerate steps giving the sequence: Stop Run for the requested number of phases at min. rate Stop When clear, the PWM will go through the sequence: Stop Accelerate from min. to max. rate, 1 phase per rate Run for the requested number of phases at max. rate Decelerate from max. to min. rate, 1 phase per rate Stop Note: The total number of phases output when ACCELb = 0 is given by: ((max. rate - min. rate) / 100) + Phase count request + ((max. rate - min. rate) / 100) Example: ((800 - 400) / 100) + 8 + ((800 - 400) / 100) = 16 phases

Register Address Format

The register address format for the Amp device is shown in Figure 3. The register address is an 8-bit number which can take on any value from 0x00 to 0xFF. The register space is divided into eight pages, with page 0 dedicated to device-wide registers and pages 1 through 7 to support up to 7 POLs.

Figure 3 Amp I2C register address format

								Page Tal	ole
								3'b000	Device
								3'b001	POL1
								3'b010	POL2
		• •						3'b011	POL3
	12C R	egiste	er Add	ressi	ng Me	thod		3'b100	POL4
7	6	5	4	ч	2	1	0	3'b101	POL5
'	0	5	-	5	2	-	0	3'b110	POL6
Pag	e Num	ıber			Offset	t		3'b111	POL7

I2C Write/Read Protocol

An Amp device is addressed by its pre-defined 7-bit device physical address (default address is 0x55). Along with the 7bit address, an 8th bit is added to the LSB position to identify whether the following transaction is a read or write, making it an 8-bit address byte. If the least significant bit of the address byte is zero, it is a write transaction whereas a 1 is a read transaction. The Amp device parameters as well as the read/write parameters of the different POLs in the device are accessed through 256 8-bit registers. Every I2C transaction to the Amp device therefore needs another 8-bit register address. The general format of I2C-Amp device write/read protocol is shown in Figure 4. Note that the Amp device is always the slave. In the figure, the shaded portion is sent by the master and the unshaded portion by the slave.

Figure 4 I2C read/write protocol

I2C write to the device

S	Device Address	Wr A	Reg	ister Address	A	V	/rite	byte 1	Α	Write byte 2	A P
I2C	read from the devic	е									
S	Device Address	W	r A	Register Add	ress	A	Sr	Device A	Address	Rd A	
	Read byte	e 1	Α	Read b	yte 2		Ν	Ρ			
Deta	ails of the bit notatio	n									
S	Start	r Re	peated	Start	Ρ	Stop					
Wr	Write Bit	<mark>d</mark> Re	ad Bit								
Α	Ack	Na Na	ick								
		Da	ita from	n Master							
		Da	ita from	n Slave							

Both write and read transactions can be either a one byte or a multi-byte transfer. Accordingly, the register address is either the address of the register that is being accessed or the starting address of a sequence of registers that is being accessed. For a write transaction, the device updates write data to successive registers until it receives an I2C stop signal. For read transactions, the master first writes the starting address into the device and starts accepting read from the device after a repeated start signal. The device sends successive register data until the master issues a NACK for the last byte read.

I2C AmPLink Interface

The AnDAPT AmPLink Interface can be used to exercise I2C commands of the I483 design.

Figure 5a: I2C transaction: 0x55 32 03 40 <- request 3 pulses with ACCELb bit set on PWMA

A AmPLink Control I2C Tab	– 🗆 X
Program SPI I2C PMBus AmPScope About	AnDAPT [™]
Address Scan Begin Image: Clear indication in	GPIO In Out Signal Value ● AMP_CTRL ● AMP_ALERT 1 ÷ ● FLASH_WP ● FLASH_RST ● AMP_EN ● AMP_Config ● Get Status
Transaction Log	
# Time Stamp Protocol Feature Direction Speed Num bytes Data 29 11/05/2022 12:35:42 I2C I2C W Out 100 3 32, 08, 40,	
Disconnect USB	Clear Log Save Log
Chatras OK Depart (ITALIOZDV)	

Figure 5b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4



Copyright © 2022 AnDAPT

7

Figure 6a: I2C transaction: 0x55 32 08 80 <- request 8 phases with acceleration & deceleration, CCW, PWMA

A AmPLink Control	- 🗆 X
Program SPI 12C PMBus AmPScope About	
Address Stall Begin 0 • End. 0 • Stall Speed (K12). Device Address: 55 • Write 32 08 80 I2C message Read Byte Count: Atomic Read Beginning Reg: 0 • Byte Count: 2 • ACK Check: Real time •	00 ↓ 00 ↓ In Out Signal Value ○ ○ AMP_CTRL ○ AMP_ALERT 1 ↓ ○ FLASH_WP ○ FLASH_RST ○ AMP_EN ○ AMP_Config ○ AMP_Config ○ Get Status
Transaction Log # Time Stamp Protocol Feature Direction Speed Num bytes Data 39 11/05/2022 12:52:11 I2C I2C W Out 100 3 32, 08, 8),
Disconnect USB Status: OK Board 1 (IT4U8ZDX)	Clear Log Save Log

Figure 6b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4



Figure	7a [·] I ond	nhase	sequence	with	repeated	read	of	status	reaister
riguie	ra. Long	priase	Sequence	VVILII	repeated	reau	UI	Siaius	register.

jule Ta. Long phase seque	nce with tepeated read o	status register.		
AmPLink Control				- 🗆 X
Program SPI I2C PMBus	AmPScope About			AnDAPT™
Address Scan Begin 0 Device Address: 55 Write Buffer: Write 32 FF 07 Read Byte Count: Atomic Read Beginning Reg: 	End: 0 Scan 2C message	Speed (KHz): Load Clear	100 VIIIE Stop Write Send Message Stop Read Stop Read Atomic Read	GPIO In Out Signal Value ○ AMP_CTRL 0 ↓ ○ AMP_ALERT 1 ↓ ○ FLASH_WP 0 ↓ ○ FLASH_RST 1 ↓ ○ AMP_EN 1 ↓ ○ AMP_Config 0 ↓ Get Status
Transaction Log				
# Time Stamp 44 11/05/2022 13:35:55 45 11/05/2022 13:35:56 45 11/05/2022 13:35:56 46 11/05/2022 13:35:57 46 11/05/2022 13:35:57 47 11/05/2022 13:35:58 48 11/05/2022 13:35:59 48 11/05/2022 13:35:59	Protocol Feature Direction I2C I2C W Out I2C I2C R In	Speed Num bytes Data 100 3 32, FI 100 1 28, 100 1 8F, 100 1 28, 100 1 28, 100 1 28, 100 1 28, 100 1 28, 100 1 28, 100 1 0F, 100 1 0F,	PWMA running PWMA stopped	
Disconnect USB				Clear Log Save Log
		Status: OK Board1 (IT4U8ZDX)		

Figure 7b: Result on scope PhaseA1, PhaseA2, PhaseA3, PhaseA4



9



I483

I483 Resource Usage

Circuit Stats.

Nu Nu Nu Nu Nu Nu Nu	mber of AnD_I2C_Phy mber of AnD_ATC_IO mber of AnD_PMT mber of AnD_CM_RAM_256x18 mber of AnD_PTG_Phase_Count mber of AnD_PTG_GBUF mber of AnD_PTG_OSC mber of AnD_DFF mber of LUT4	1 10 1 2 1 1 1 68 205
Resource L	Jsage	
io	10 used (Capacity 24)	
clb	26 used (Capacity 64)	
cm	2 used (Capacity 8)	
pm	t 1 used (Capacity 16)	
cor	mer 1 used (Capacity 4)	
ptg	1 used (Capacity 2)	
ULC	bgic 205 used (Capacity 512)	
Componen	is Stats	
φιe		
	AIID_DFF 16	
\$te	chmap\component 2	
+	AnD_DFF 50	
cor	nponent_1	
	AnD_CM_RAM_256x181	
cor	nponent_2 AnD_CM_RAM_256x181 AnD_PMT 1	

Additional Resources

AnDAPT AmP Platform datasheet

Revision History

Date	Revision
05/20/2022	Initial datasheet release



www.AnDAPT.com

Trademarks

© 2022 AnDAPT, the AnDAPT logo, AmP, WebAmP, AmPLink, AmPScope and other designated brands included herein are trademarks of AnDAPT in the United States and other countries. All other trademarks are the property of their respective owners.