Integrated Low-Dropout (LDO) Regulators

Power Component: LDOa, LDOb

Product Description

The Amp Platforms B and C have 4 integrated LDOs of which two are fixed output voltages (3.3V and 1.2V) and two are user programmable. The user programmable LDOa and LDOb are described here and can be customized by using WebAmP Tools. The user programmable LDOs can be dynamically enabled/disabled from the digital fabric, allowing sequencing and external control. Combine these LDO components with other Power Components to create a highly integrated, custom-defined, AnDAPT AmP™ on-demand power management device.

Features

- Linear, constant voltage, low-dropout regulators
- Adjustable V_{OUT} LDOa. LDOb, 0.6 V to 4.5 V
- V_{OUT} ± 3% accuracy
- Maximum output current: 200 mA
- 10% typical line and load regulation
- Very low dropout :100 mV dropout
- Enable input allowing sequencing and external control
- –40°C to +125°C operating junction temperature

Applications

- Powering server, processor, memory, storage, network switcher and router platforms
- FPGA, processor, SSD, subsystem power control & sequencing
- Imaging: CMOS Sensors, Video ASICs
- Test and Measurement
- Regulated power noise sensitive, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and PLLs with integrated VCOs

Figure 1: LDOa application schematic

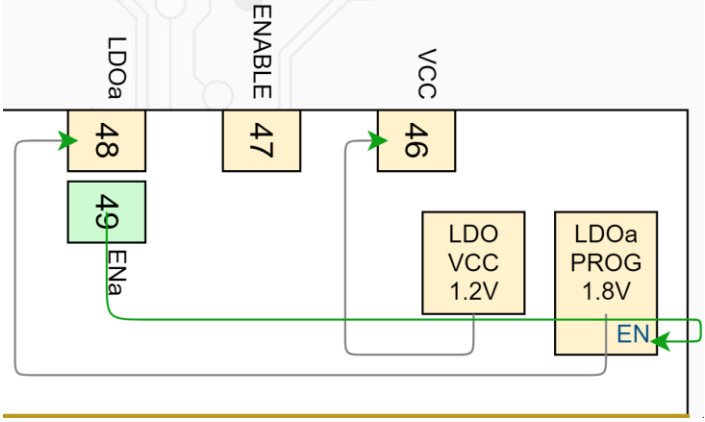
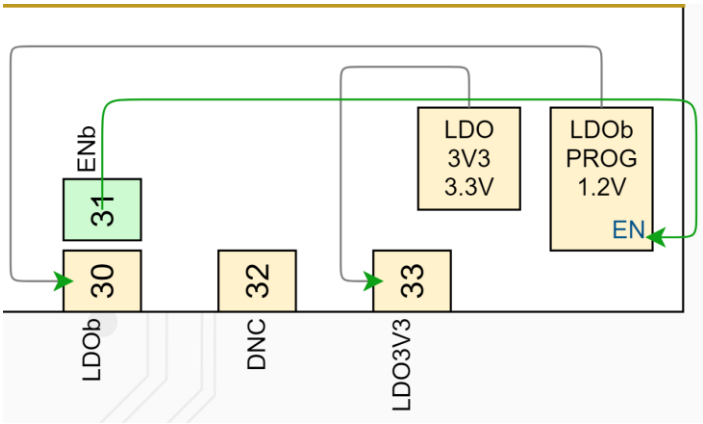


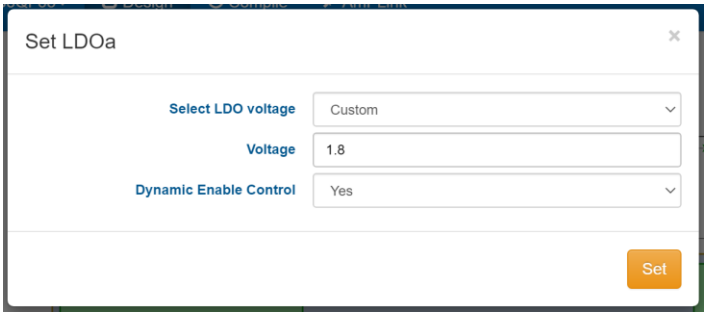
Figure 2: LDOb application schematic



Product Detail

The input voltage to LDOa and LDOb is from the internal 4.5V bias voltage. The pin locations of these integrated LDOs, are fixed and cannot be modified by WebAmP Tools. The two programable outputs are on pins 17/30 and 70/48 respectively in QF74 and QF65 package.

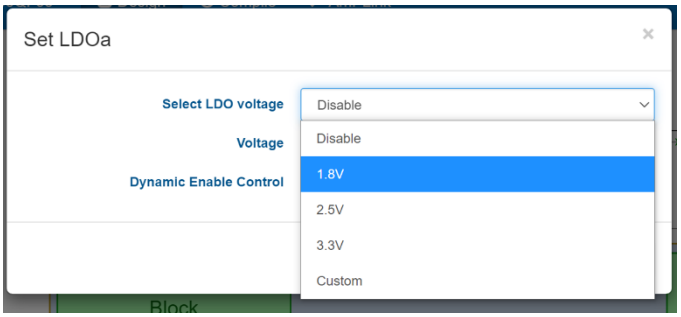
Sequencing and external control of the user programmable LDOa and LDOb can be dynamically enabled/disabled from the digital fabric, when “Yes” is selected in the WebAmP menu as shown below:



Simply double-click the LDOa or LDOb symbol to select voltage, then drag a wire from any GPIO pin or power component to the EN port of LDOa or LDOb as shown in Figures 1 and 2.

Product Detail (continued)

The user programmable LDOa and LDOb can be set to standard voltages of 1.8,V, 2.5 V, or 3.3V by selecting in the WebAmP menu as shown below:



These standard voltage selections save Nref resources as shown in the Resource Usage reports below:

LDOa, LDOb Resource Usage with Enable

Circuit Stats...

Number of AnD_Prog_LDOB	1
Number of AnD_Prog_LDOA	1
Number of AnD_Analog_IO	2
Number of AnD_ATC_IO	2
Number of AnD_Nref_fix	2
Number of LUT4	2

LDOa, LDOb Resource Usage without Enable

Circuit Stats...

Number of AnD_Prog_LDOB	1
Number of AnD_Prog_LDOA	1
Number of AnD_Analog_IO	2
Number of LUT4	2

Electrical Characteristics

V_{IN}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, Cldo3v3=1µF, Cldoa=1µF and Cldob=1µF unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LDOa	LDOa Programmable range		0		V_{DD}	V
	LDOa load regulation	Ia=200mA, V_{IN}=4.5V		Vnom-0.1		V
	LDOa tolerance	Ia=0mA, V_{IN}=4.5V	-3		+3	%Vnom
Ia	LDOa output current**				200	mA
LDOb	LDOb Programmable range		0		V_{DD}	V
	LDOb load regulation	Ib=200mA, V_{IN}=4.5V		Vnom-0.1		V
	LDOb tolerance	Ib=0mA, V_{IN}=4.5V	-3		+3	%Vnom
Ib	LDOb output current**				200	mA

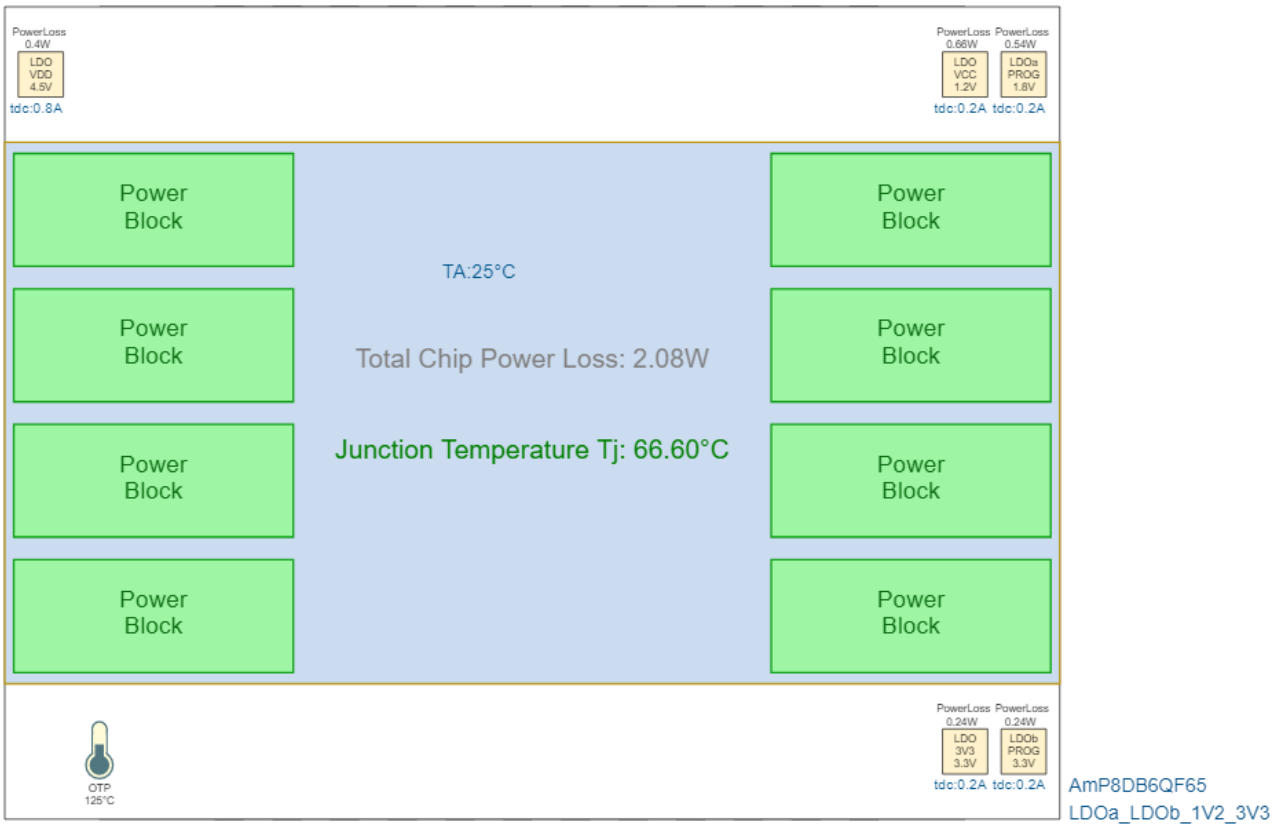
. **Total LDO power dissipation must not exceed Package Dissipation Ratings. VIN supplies VDD LDO which supplies sub LDOs VCC, LDO3V3, LDOa and LDOb. VDD pin requires >10µF external decoupling and is for internal use only.

Thermal Example

The WebAmP Thermal view below calculates Total Chip Power Loss and Junction Temperature.
For this example, Vin = 5V, Ia = Ib = I1V2 = I3V3 = 200 mA. $\theta_{JA(effective)}$ = 20°C/W

Total Chip Power Loss = (5-4.5)*0.8 + (4.5–1.2)*0.2 + (4.5–1.8)*0.2 + (4.5–3.3)*0.2 + (4.5–3.3)*0.2
= 0.4 + 0.66 + 0.54 + 0.24 + 0.24
= 2.08 W

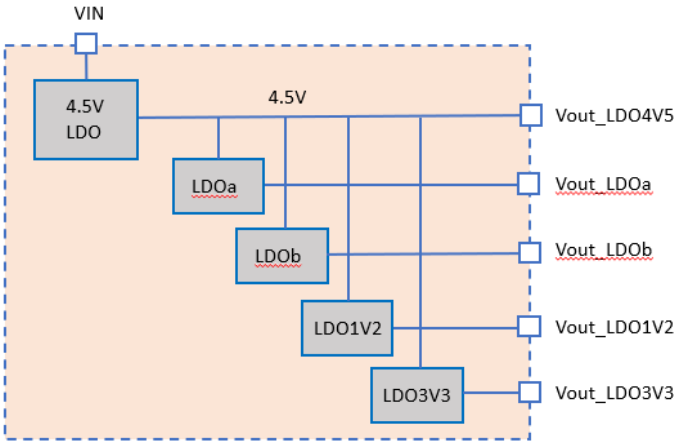
Junction Temperature = 25°C + 20°C/W * 2.08W = 66.60 °C



Theory of Operation

The LDOa and LDOb are linear voltage regulators which consist of a reference voltage, a feedback path for the output voltage to compare it to the reference, a feedback amplifier, and a series pass transistor (PMOS in this case), whose voltage drop is controlled by the amplifier to maintain the output at the required value.

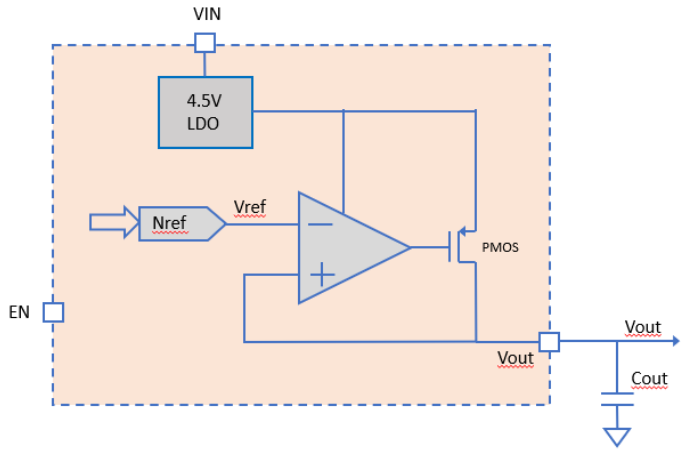
The power rail for LDOa and LDOb comes from the output of an additional on-chip 4.5V LDO which in turn has VIN as it's supply rail. This is illustrated below:



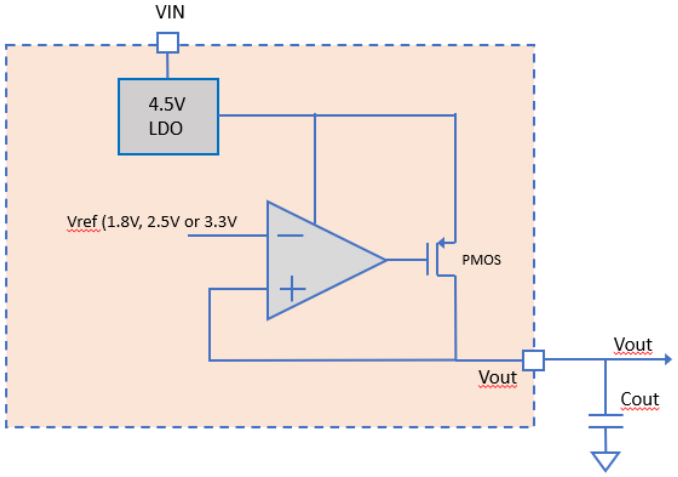
The feedback paths for LDOa and LDOb are internal to the device and the LDOs offer load regulation performance at ~40mV/100mA as well as operating up to 200mA output current.

Block diagrams for LDOa and LDOb are shown below. Note that in "Custom" programming mode an Nref resource is required while in fixed programming (1.8V, 2.5V or 3.3V) the Nref is not required.

LDOa/b in "Custom" programming mode



LDOa/b in fixed programming mode



If the load current increases causing the output to drop the error voltage will increase and the amplifier output will fall. This in turn causes the voltage across the pass transistor to decrease and the output will return to its original value.Note that a linear regulator efficiency depends on the voltage difference between input and output and is nominally given by:

$100 \times (V_{OUT} \times I_{OUT})/(V_{IN} \times I_{IN})$

$= 100 \times V_{OUT} / V_{IN}$ assuming $I_{OUT} = I_{IN}$

with the power loss being $(V_{IN} - V_{OUT}) \times I_{OUT}$.

Additional Resources

- AnDAPT AmP Platform B datasheet

Revision History

Date	Revision
12/04/2020	Preliminary release

AnDAPT

On-Demand Power Management

www.AnDAPT.com

Trademarks