Considerations on voltage bias requirements for C710/C715 LDO and C750/C755 Load Switch power components

Application Note 200130

Description

Careful design considerations must be used when selecting and designing linear power components. While PVin (power fet drain) Voltage range is explicitly specified in the datasheets of these power components, the chip bias voltage Vin must respect specific conditions in order to obtain the desired operation.

Specifically:

- For C710/C715 LDO Power Component, Vin must be 2.3V higher than the desired output voltage.
- For C750/C755 Load Switch Power Component, Vin must be 2.0V higher than the desired output voltage.

If these conditions are not met, the application might still be possible with the addition of small external passive components. Please contact AnDAPT factory for application support and example schematics.

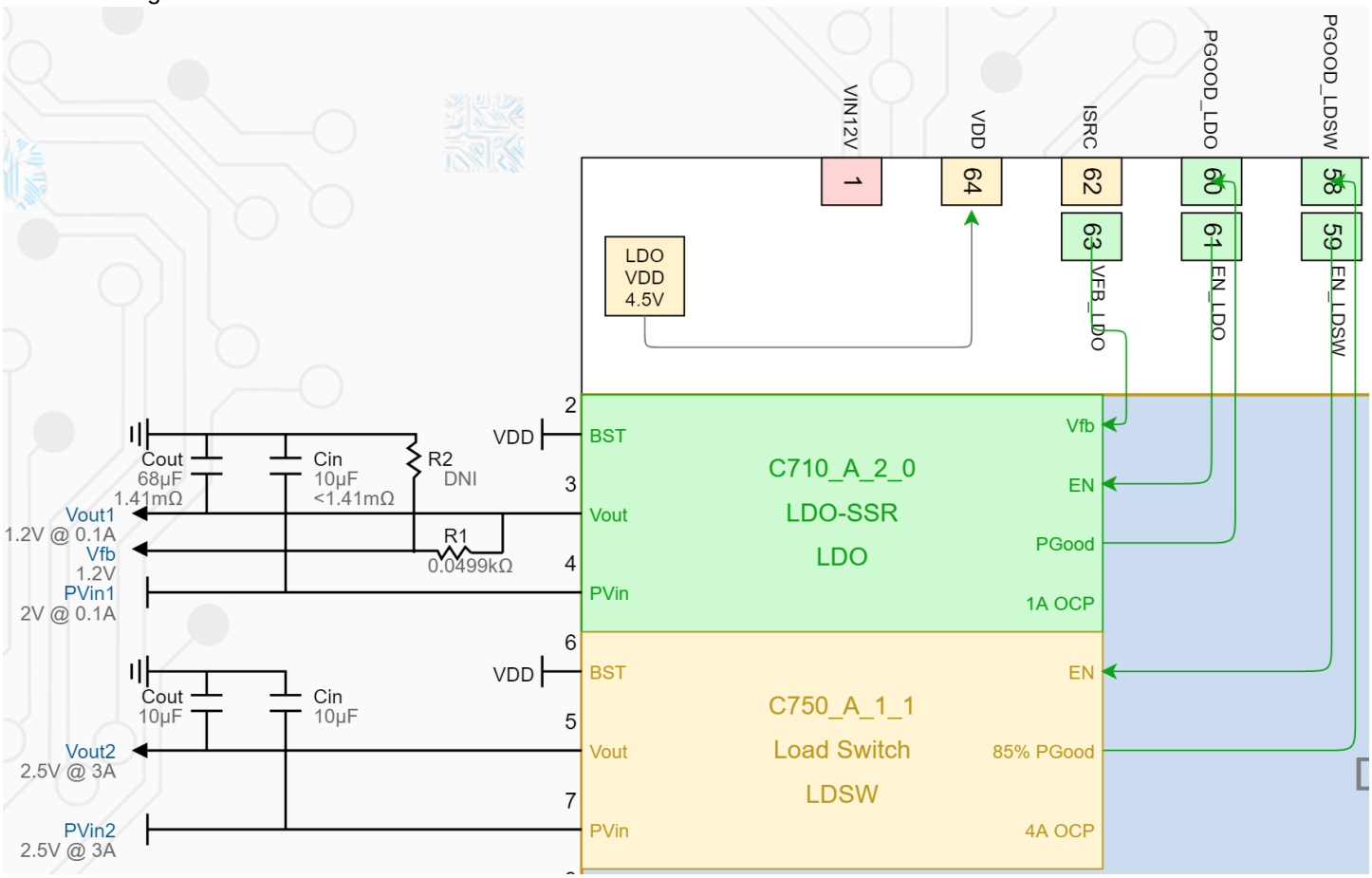

Figure 1. LDO and LDSW example WebAmP Design View showing Vin = 12V, PVin1 = 2V and PVin2 = 2.5V

Revision History

Date	Revision
01/30/2020	Initial release

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Trademarks