# C200/C210 PCB Layout Guidelines

## Application Note 220602

## Introduction

The C200_B and C210_B Power Components are synchronous buck converters. Like all switching power converters, care must be taken in the design of the PCB layout to prevent unpredictable problems that are difficult to troubleshoot.

## Ground Plane Selection

Layer two in the PCB is best used as a ground plane. This minimizes the length of ground vias from the top layer, minimizing stray resistance and inductance. The ground plane will also act as a Faraday shield between switching nodes on the top layer and any traces that carry susceptible signals in layer 3. Likewise, the 2nd to the last layer is also best used as a ground plane, for boards with 6 or more layers. In general, all component pins connected to ground should have ground vias near or underneath them, most especially for bypass capacitors. Lastly, "ground stitch" vias should be added all over the board to connect the ground layers together. These are important in areas close to components and less important in blank areas of the board with no components.

## LX Connection Resistive Losses

The LX node is pointed to by the arrow in Figure 1, and labeled "LX" in Figure 2. It connects the half-bridge output to the inductor. Because it carries high current, the trace needs to be wide to minimize resistive losses that reduce system efficiency. A quick rule of thumb to calculate the full load efficiency loss in percent due to resistive losses, $\%_{LOSS}$:

$\%_{LOSS} = V_{LOSS} / V_O$, where $V_O$ is the output voltage
$V_{LOSS} = I_O * R_{TRACE}$ where $I_O$ is the full load current
$R_{TRACE}$ = Number of squares x Ohms per square

The method of quickly estimating copper trace resistance $R_{TRACE}$ using "Ohms per square" and "number of squares" is described here: https://www.edn.com/resistance-of-a-copper-trace-rule-of-thumb-14/
(*EDN magazine: "Resistance of a copper trace: Rule of Thumb #14")*

## dv/dt Noise Coupling

The LX node is the half-bridge switching node, with fast dv/dt at the switching edges. And because the trace is wide, it has a strong capacity to couple dv/dt noise into susceptible traces. Susceptible signals are those which have high impedance and low voltage. Stray capacitance between a node with large dv/dt, and a susceptible trace, will cause noise from the former to couple into the latter signal.

Ensure that any PCB traces that carry a susceptible signal do not run in a layer immediately under the LX trace without a ground or power plane between them to act as a Faraday shield. Otherwise, the stray capacitance between them will inject dv/dt noise.

The high-side BST (gate drive bootstrap) pin (pin 42 / BST2 in Figure 2), and components attached to it (C561, R741, and the cathode of D211), have the same dv/dt as the LX node. Ensure that these components, and their traces, likewise do not couple dv/dt noise into susceptible traces.

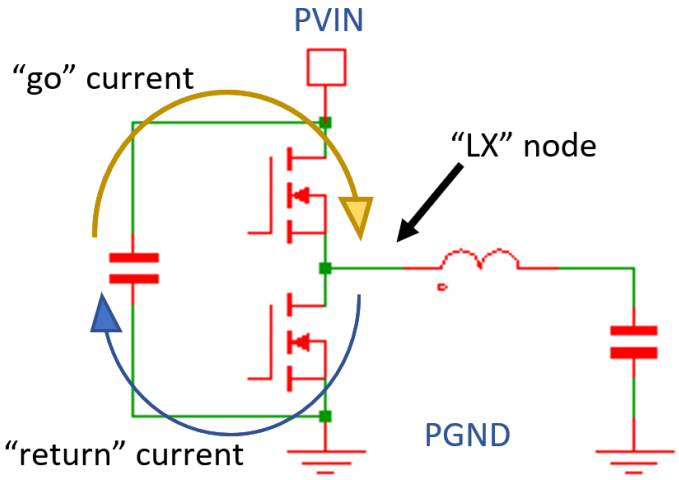


*Figure 1: Synchronous Buck Converter: main switching loop and high dv/dt node*

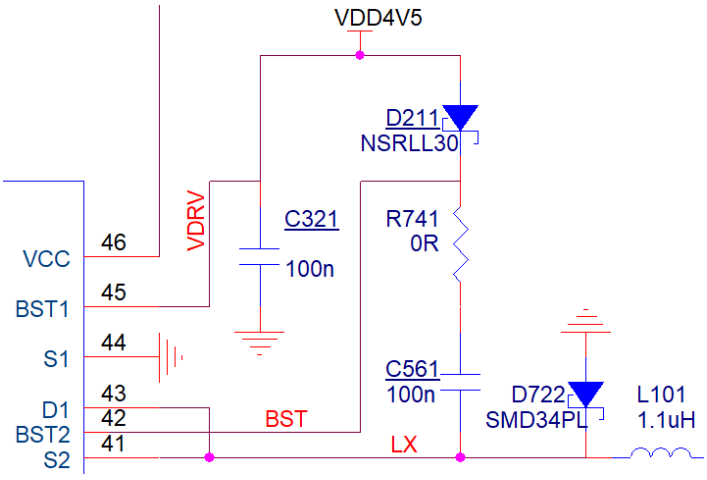


*Figure 2: Schematic showing bootstrap components C561, optional R741, and D211; and optional freewheeling diode D722.*

## Main Switching Loop

Currents flow in loops. The main switching loop in a synchronous buck converter *with high di/dt* is shown in Figure 1. This is formed by the half-bridge main MOSFETs, and the connections to the closest PVIN bypass capacitor. The yellow curved arrow represents the "go" current, and the blue curved arrow represents the "return" current. Together they form a loop, whose area needs to be minimized.

Note that current does not actually flow in this loop at any given time (except during a very short period when the high-side turn-on edge charges the low-side MOSFET $C_{OSS}$ and drives its body diode reverse recovery current). Instead, all the current branches in this loop have large di/dt. They have fast current edges during the switching transitions, and these branches' *di/dt* arrow directions (not absolute current directions) form a complete loop. If this loop area is large, it will radiate di/dt noise, and form a large stray inductance in series with the bypass capacitor. This inductance will cause ringing at the AmP half-bridge – i.e. across the PVin and PGND terminals as seen in Figure 3. If severe, this ringing can cause unpredictable behavior.

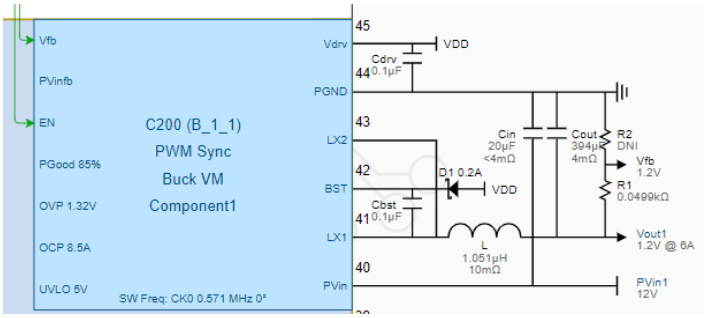


*Figure 3: WebAmP schematic of C200*

This loop area is minimized in a PCB layout when the go and return conductors are one on top of the other in adjacent layers. This means that the "go" current branches on the top layer have a corresponding unbroken return current path directly underneath in the ground plane on layer 2. This is best achieved when the closest PVIN bypass capacitor, usually the smallest, is close to and on the same layer as the AmP device, and the next copper layer is a ground plane. (See Figure 4 and Figure 5) Other larger bypass capacitors can be a little further away, such as on the opposite side of board, connected with vias. All PVIN bypass capacitors should use wide traces to connect the PVIN terminals between them and to the PVIN pins of the AmP device. If a power plane is used for convenience, the PVIN terminal should have vias close by.

## Source Pin of Low-side MOSFET

The Source pin of the low-side MOSFET, labeled as "PGND" in Figure 3, does not have an internal connection to ground. It requires a low inductance connection to the ground plane. Two vias-in-pad are recommended. Via-in-pads with 6 mil or 0.15 mm drill diameters will work. (Figure 4). If vias-in-pad are not preferred, refer to Figure 7.

Note that vias-in-pad should be filled and planarized by the PCB manufacturer to ensure reliable solder joints.

The copper pour for the thermal pad (ground) should encompass the Source pin. (Figure 4)

## Via resistance estimation

The "Ohms per square" method can also be used to estimate via resistance where:

$$Number\ of\ squares = via\_length\ /\ (\pi\ *\ via\_diameter)$$

If the via connects the top layer to the 2nd layer, the typical length will only be 10 mils for a 6 layer board. The number of squares for a 6 mil diameter via will thus be 0.5 squares. However, the plating inside a via is typically only ½ oz thick (18 µm) unless specified to be thicker. So compared to a 1 oz top layer, it has the same resistance as 1 square on the top layer, or 2 squares of a 2 oz top layer. If instead the ground plane is the 5th of 6 layers, then the resistance of the via will be 4-5x larger. This shows the advantage of having the 2nd layer as a ground plane for high current connections.

PCB manufacturers can fill small vias with thermally and electrically conductive material. This improves electrical and heat conduction – an advantage for the AmP device's thermal pad. Consult your PCB manufacturer for their conductivity constants to enable calculating their thermal and electrical resistance. Also note that for thermally demanding applications, the MOSFET Source and Drain pins (S1/S2 and D1/D2 in Figure 2) also provide a heat path out of the device, in addition to the thermal pad. The vias and copper traces connected to these pins will help carry heat away.

# Layout Examples

## Single layer LX connection to inductor

Figure 4 illustrates the 4 important points discussed. Note that the AmP device thermal pad copper pour connects to the low-side MOSFET Source pin.

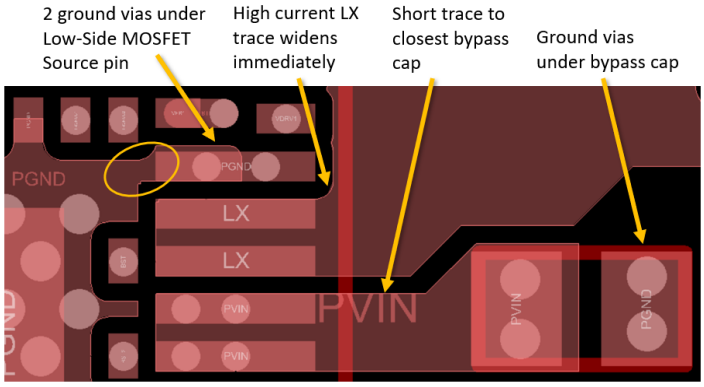


*Figure 4: Example layout using 1 layer for LX trace. Inductor (not visible) is to the upper right. Circle shows grounded thermal pad copper pour connection to low-side MOSFET Source pin.*

Figure 5 shows the current loop path. The ground plane is displayed as a white shadow. The “go” current is shown with the yellow arrows, and “return” current is shown with the blue arrows. Note that the high frequency return currents flow in a manner that minimizes the loop area that is physically possible. In this example, the ground plane underneath the go current is unbroken as shown by the blue arrows. If the ground plane is in the next layer, this makes for the smallest possible loop area. Any breaks in the ground plane where the blue arrows lie will increase the loop area and should be avoided.

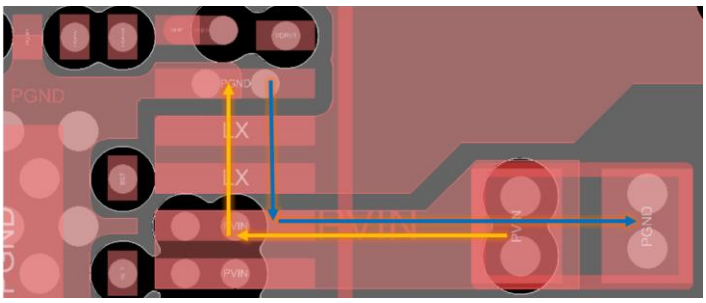


*Figure 5: Same layout as Figure 4, showing ground plane (white shadow) and high frequency current loop from Figure 1*

## Dual layer LX

Sometimes a wide LX trace in the top layer is not feasible yet efficiency must be maximized. In this case, layer 2 (nominally the ground plane) is used to help share the current with a parallel connection to the inductor. Figure 6 shows an example. Use as little of the ground plane as possible as needed to reduce resistive losses. Note that for proper current sharing, the layer 2 copper island should also have vias to the top layer near the inductor.

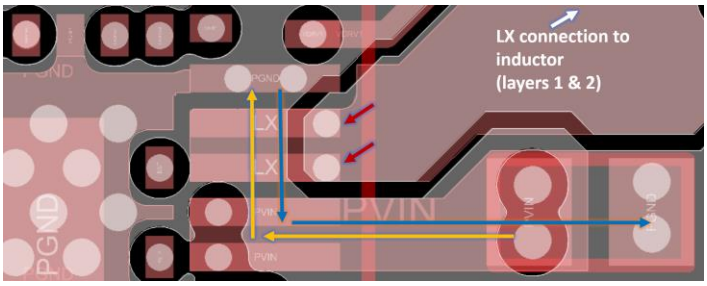


*Figure 6: Layout example using layer 2 in parallel with top layer for the LX connection to the inductor (not shown, to upper right)*

Care must be taken to maintain an unbroken return current path (blue arrows) that is as close as possible to the “go current” path (yellow arrows). To this end, note the location of the vias at the LX pins of the AmP device which connect to layer 2 (small red arrows). They are placed as close to the outside (right) as possible, so that the vertical blue arrow is uninterrupted.

## Layout with no vias-in-pad

Figure 7 shows an example layout for a PCB design without vias-in-pad.

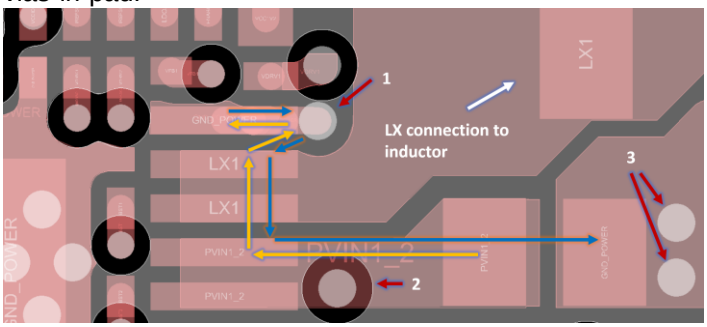


*Figure 7: Same layout as Figure 5 but without vias-in-pad*

The ground via for the Source pin of the C200 should be very close to the pin (red arrow “1”). The closest bypass capacitor has ground vias very close to its ground pin (red arrows “3”). The via, red arrow “2”, connects the PVIN node to a wide trace in an inner layer (not shown). It is positioned low so that it will not interrupt the go current from the capacitor (long horizontal yellow arrow). Without vias-in-pad, the LX connection to the inductor becomes somewhat narrower, and this may have a slight impact on efficiency.

## Other components which require low inductance connections

There are a few more component connections which require attention. These components need to have a small loop area formed between them and the AmP device pins they connect to. That is, they need to be relatively close to the AmP device, and have short traces connecting them. The components which have a terminal connected to ground should have a via to the ground plane nearby. The components which have neither terminal grounded, ideally will have their respective go and return traces side by side, or one on top of the other on separate layers. These components are the following, visible in Figure 2:

- High side drive bootstrap Schottky (D211)
- Gate drive bypass capacitors
  - High side: connections are to the BST2/3/6/7 pin (BST pin in Figure 3) to LX
  - Low side: connections are to the BST1/4/5/8 pin (Vdrv pin in Figure 3) to the ground plane
- The optional low-side FET anti-parallel Schottky (D722 in Figure 2)
  - This Schottky can improve efficiency by up to 2% and a high inductance connection will reduce this improvement. This is optional and depends on board area availability.

## Output capacitor and feedback sensing

The output capacitor(s) must have low inductance connections to the output connector or the load. Significant inductance between them will degrade the transient response during fast load di/dt.

The voltage feedback sense connection from the output VOUT to the C200 feedback input (bottom of R1 in Figure 3) must be at the output capacitor closest to the load. Connecting it closer to the inductor will degrade the load transient performance. In the schematic and PCB layout, the voltage feedback trace is the same net as VOUT; care must be taken in routing it to ensure there is only one connection point: to the last output capacitor. Figure 8 shows the use of a separate layer (blue trace) so the single point connection is at a via close to the output capacitor closest to the load. Do not simply connect it to the VOUT copper island at a random point.

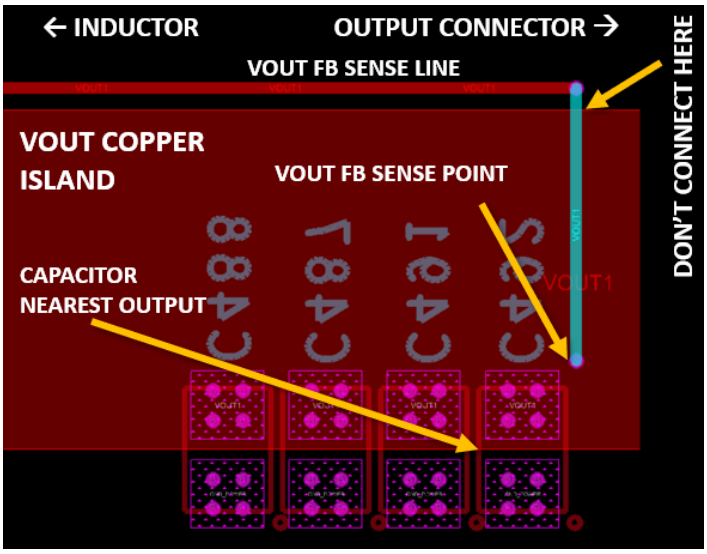


*Figure 8: Multiple output capacitors and single feedback pickup point. Blue trace connection is in another layer and connects to a via close to the last capacitor*

## Summary/checklist

1) Is layer 2 a ground plane?
2) Does the Source/PGND pin of the C210/C200 have 2 vias-in-pad to the ground plane, or is the via that connects it to the ground plane right next to the pin?
3) Is the closest PVIN bypass capacitor connected with a very short wide trace to the PVIN pins of the C200/C210?
4) Does the grounded terminal of the closest PVIN bypass capacitor have vias to the ground plane underneath or nearby?
5) Does the return path from the Source/PGND pin to the bypass capacitor grounded terminal have an uninterrupted path in the ground plane, under the “go currents” as per Figure 5?
6) Is the LX connection to the inductor wide enough to reduce resistive losses?
7) If using a layer 2 copper island in parallel with the LX connection to the inductor, is there an uninterrupted path in the ground plane for the return currents under the go currents as per Figure 6?
8) Is there problematic stray capacitance between the sensitive traces and the LX or BST nodes?
9) Do the following connections have low loop inductance to the AmP device pins?
    a. High side drive bootstrap Schottky
    b. Gate drive bypass capacitors
        i. High side BST pins
        ii. Low side BST pins
    c. The optional low-side FET anti-parallel Schottky
10) Do the connections from the output capacitors to the load have low inductance?
11) Is the feedback sense point at the last output capacitor?

## Revision History

| Date | Revision |
|---|---|
| 06/02/2022 | Initial Release |

**On-Demand Power Management**

www.AnDAPT.com

## Trademarks