# **AnDAPT** Configuration and Control using – AmPLink

AmP8D

# **AmP Configuration**

The AmP platform supports two modes of configuration through the SPI compliant serial interface. In master mode, the AmP device loads its configuration bitfile (.HEX) from an external non-volatile memory. In slave mode, the AmP device is loaded with its configuration bitfile (.HAX) by an external controller/AmPLink.

## AmP SPI Master Configuration Interface

The AmP device simply receives valid input power and takes control of the external FLASH memory to load its configuration. The AmP device acts as the SPI master and controls the external FLASH memory as a slave. Master mode is ideally suited for applications where the AmP device is independently providing FLASH power.

#### AmP SPI Slave Configuration Interface

An external controller/AmPLink acts as the SPI bus master and drives the AmP device as a slave. Configuration data for the device is provided over a sequence of SPI commands. Slave mode is ideally suited for applications where the AmP device is configured by a processor (also AmPLink).

### AmPLink and WebAmP

The AmPLink<sup>™</sup> USB Adapter provides the interface between the AmPDB1 Demonstration Board and the WebAmP design tool to program and control AmP and FLASH memory devices using SPI, I<sup>2</sup>C and GPIO interfaces. The I<sup>2</sup>C bus provides control and monitoring of the power supply functions of the AmP device, independent of configuration method.





AmPLink Pin Out		AmPLink Pin Functional Description			
			٨mD	ENABLE	High(float): AmP power on, Low: AmP power off
				CFG	High: config reset, High-to-Low: start config
GND - 1 SCLK - 3 SI - 5 SS/CS CS3 - 7 CFG - 9 SO - 11 SO - 11 GND - 1 CFLASH_RST 10 - FLASH_RST 12 - GND 10 - FLASH_RST 12 - GND 14 - SCL FLASH_WP - 15 ALERT - 17 ENABLE - 19 C - CS1 SS/CS 8 - CS4 SS/CS 10 - FLASH_RST 12 - GND 14 - SCL 16 - SDA 18 - CTRL 20 - VBUS	FLASH Program	AmP Configuration	SPI	SCLK	Clock output, Hi-Z when not in use
				SI	MOSI output when connecting to AmP devices
					MISO input when programming flash devices
					Hi-Z when not in use
				SO	MISO input when connecting to AmP devices
					MOSI output when programming flash devices
					Hi-Z when not in use
				SS	Active low chip select enables AmP
			CS	CS1, CS2, CS3, CS4	Active low chip selects connect to AmP SS or
					FLASH CS
			FLASH		HI-Z when not in use
				FLASH_WP	Flash write protect output
				FLASH_RST	Flash reset output
	I <sup>2</sup> C		AmP GPIOs	SCL	Clock output. Open drain with internal 2.2k $\Omega$ pull
					up resistor
				SDA	Bidirectional data line. Open drain with internal
					2.2kO pull up resistor
				ALERI	alert signal input
				CIRL	control signal output
				GND	Connected to USB GND and shield
				VRUS	5V output 0.5A to 0.7A current limiting
			3.3V	3.3V output with 0.5A current limiting	

AmP8D