AmP Multi-device SPI Flash Sharing

Application Note 027

Introduction

This application note details advanced methodologies for sharing a SPI flash memory among multiple devices, specifically AmP devices with either an FPGA/SoC or other AmP devices.

Scope

Provides guidelines for implementing seamless integration, ensuring optimal performance and reliability. This application note describes how to prepare the SPI flash image for FPGA / SoC or AmP device sharing and the connections and additional components needed for multiple AmP devices.

Key Features

- Multi-Device Compatibility: Supports concurrent access for AmP devices, FPGA/SoC, and other AmP devices.
- Optimized Communication Protocols: Ensures efficient data transfer and minimizes latency.
- Space Savings: Eliminates the need for dedicated flash devices, reducing both cost and board space.
- Memory Requirements: Requires a sufficiently large flash memory to accommodate multiple images.
- Additional Components: For multiple AmP devices, an additional Schottky diode per AmP device is necessary to ensure proper operation.

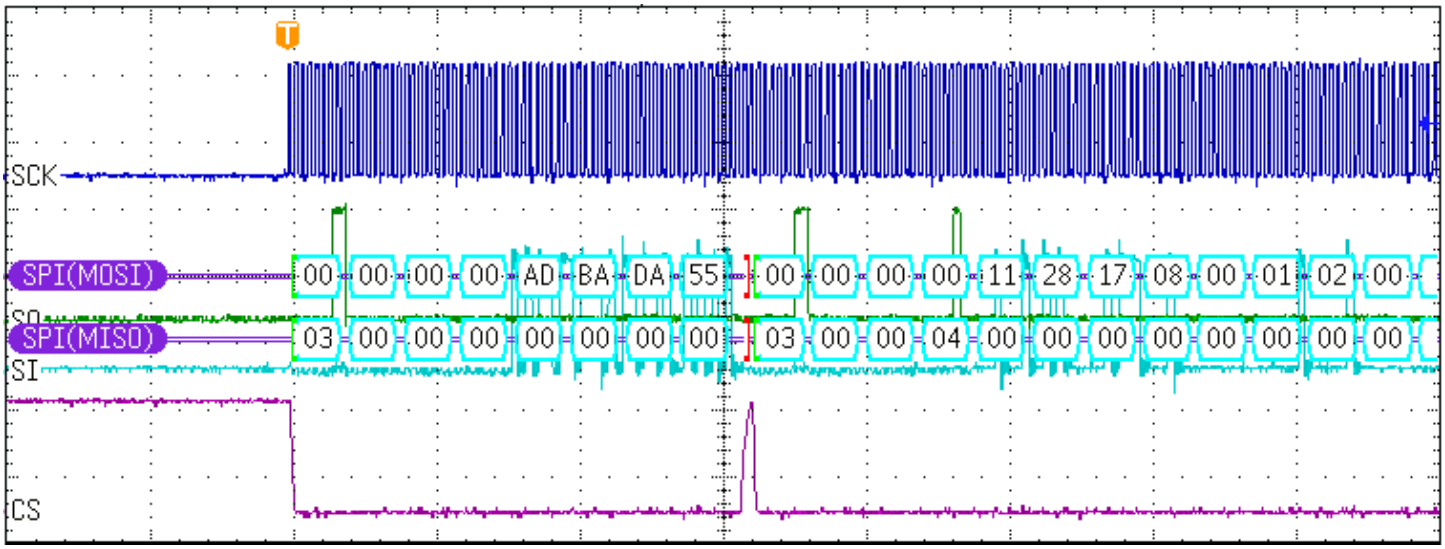
SPI / Configuration Pin Function and Description

Pin	Description
GPIO14DONE	GPIO14 shared with DONE output DONE: Driven high when configuration is complete GPIO14: Connect to any internal signal for monitoring / driving
GPIO15MODE	GPIO15 shared with MODE function Before configuration : Mode function After configuration: GPIO15 Mode function: Host ROM or Flash mode: Connect high through 47kΩ resistor Client AmPLink or external controller: Connect low through 47kΩ resistor Do not leave floating. GPIO15: Connect to any internal signal for monitoring / driving
SCK	SPI clock output when AmP is Host, input clock when AmP is Client
SS	SPI chip select output when AmP is Host, input when AmP is Client
SI	SPI serial input, receives SPI data
SO	SPI serial output, transmits SPI data
CFG	Active high: configuration restart AmP is held in reset while signal is high Reconfiguration is triggered on a negative edge

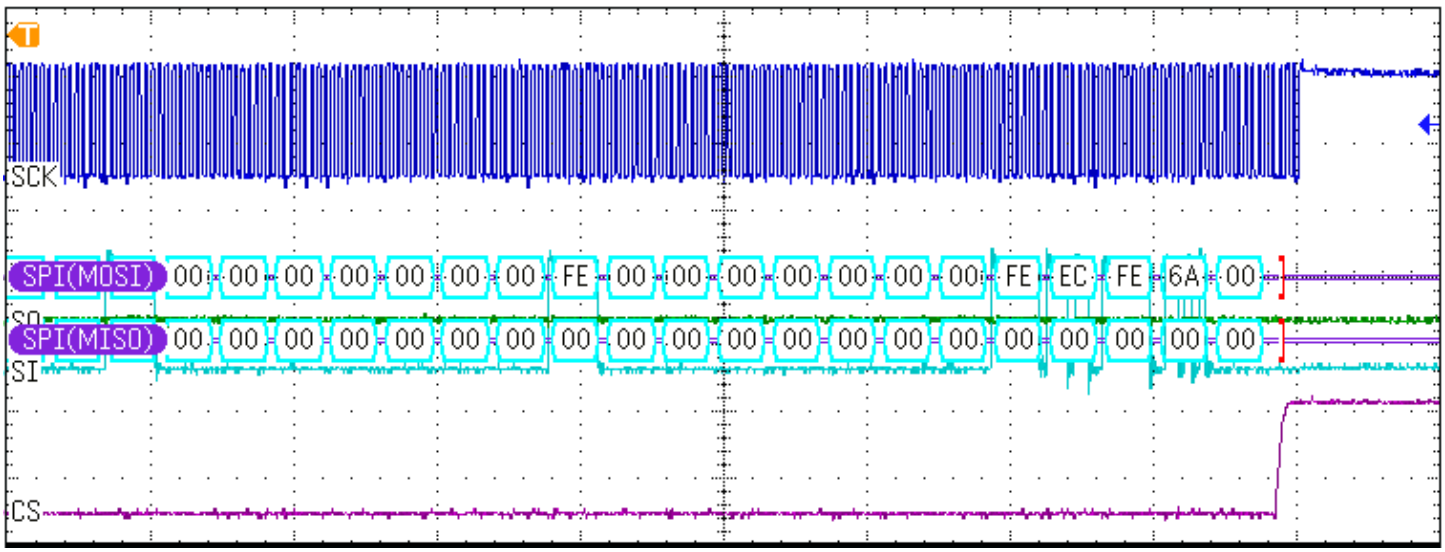
AmP Device Configuration From Flash

An AmP device, when configured as an SPI master, expects to find its image at address 0x0000 in the SPI flash. It first sends the SPI “read array from address 0x0000” command: “03 00 00 00” on MISO and expects to read a header “AD BA DA 55” on MOSI. If the AmP does not read the expected header it will try again from address 0x0000. It will repeat this re-try ~6000 times before stopping and expecting a configuration restart via a CFG pin negative edge.

When it does read the expected header, the AmP device starts again with a SPI “read array from address 0x0004” command “03 00 00 04” and will then read its image on the MOSI in one continuous read transaction.



The final bytes in the image are the checksum command “EC xx yy 00” to the AmP device. When these bytes are read, the AmP device performs a check of the supplied checksum “xx yy” versus that calculated while reading its image. If the checksums match the AmP releases the SPI bus and configures itself. If not matched, the AmP device does not configure and waits for another configuration cycle to be started via a CFG pin negative edge.

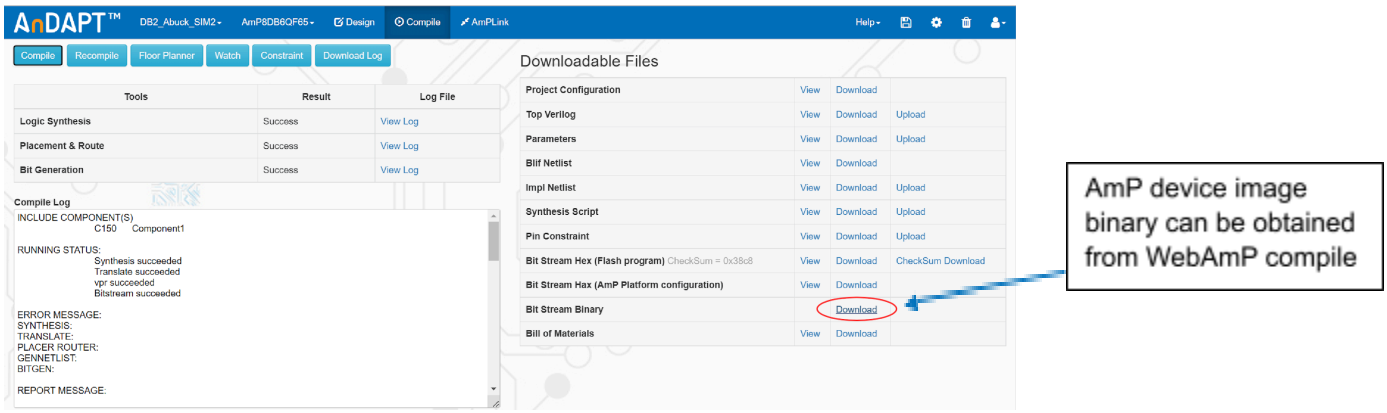


AmP and FPGA Sharing Flash

In the case of sharing a SPI flash with an FPGA / SoC, the AmP device image must be located at the address 0x0000 of the flash memory. The AmP image ends at address 0x73BF. The FPGA image should be located after this address and the FPGA must have the ability to search for its configuration header in flash memory.

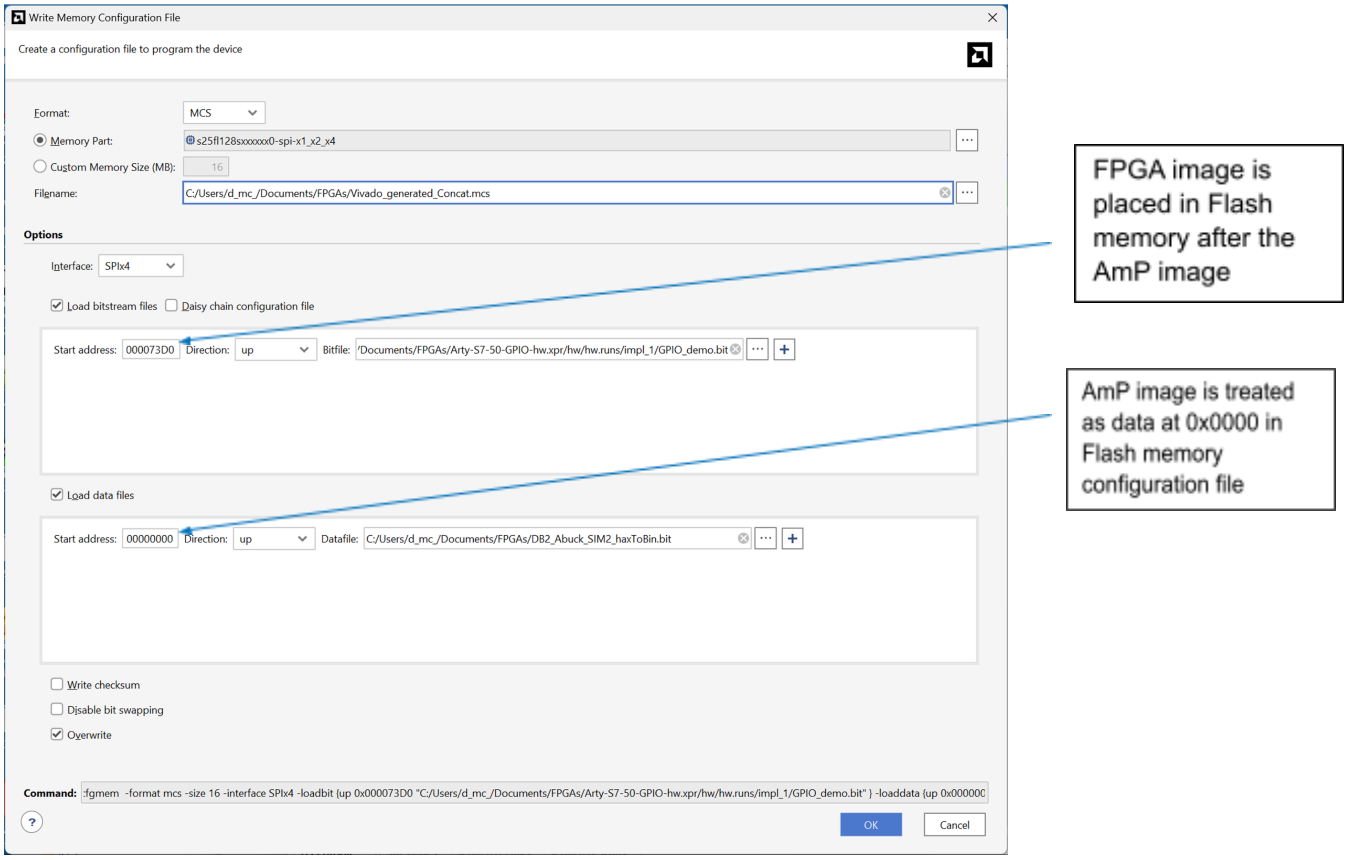
```
Offset(h)  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F

00000000   AD BA DA 55 11 28 17 08 00 01 02 00 00 00 20 00
00000010   00 00 00 00 00 00 00 00 00 00 00 00 00 00 10 00
00000020   00 00 00 00 00 00 00 00 00 00 00 00 00 00 10 00
00000030   24 04 00 04 00 00 00 00 02 40 00 00 00 00 00 00
.....
00007370   00 00 00 00 00 00 00 FE 00 00 00 00 00 00 00 FE
00007380   00 00 00 00 00 00 00 FE 00 00 00 00 00 00 00 FE
00007390   00 00 00 00 00 00 00 FE 00 00 00 00 00 00 00 FE
000073A0   00 00 00 00 00 00 00 FE EC FE 6A 00 1B 00 00 00
000073B0   D7 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

The AmP device image binary can be downloaded from the WebAmP tool following a successful compile in the Compile tab.

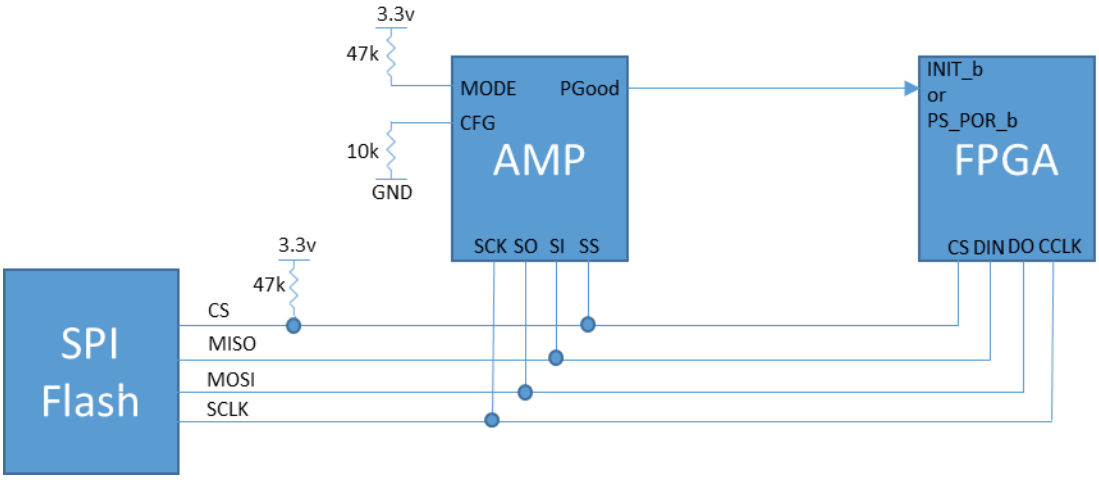


Placement of images can be achieved in the tool used to prepare the FPGA configuration file. An example of the Xilinx Vivado tool is shown below, others will be similar.

The AmP device image is placed at location 0x0000 in Flash memory by assigning it as data.
The FPGA image is then placed at address 0x73C0 or higher.



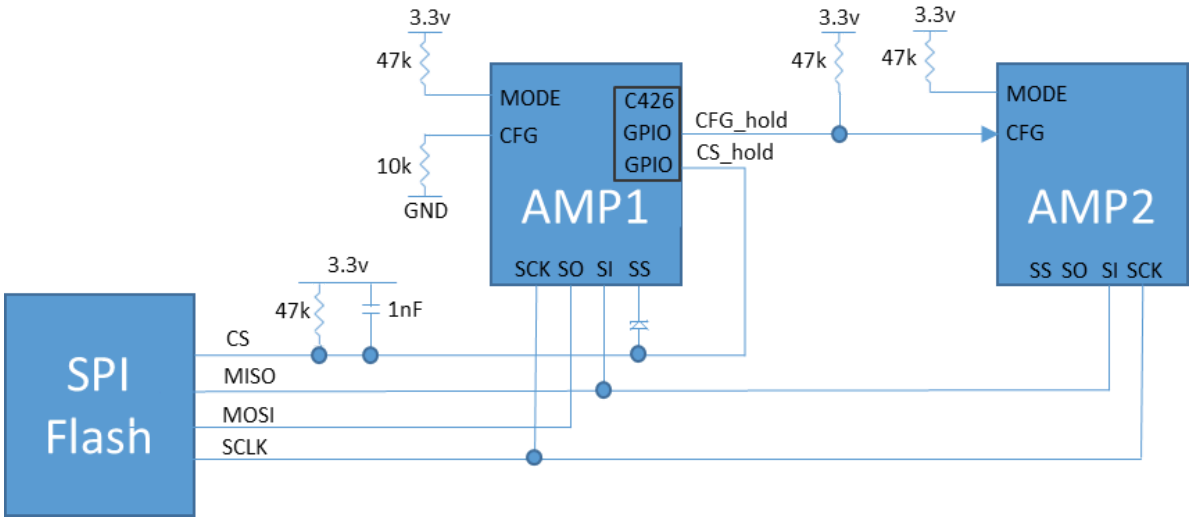
Once the AmP device has configured itself and established the required FPGA power rails, a PGood output from the AmP device can be used to release the FPGA from reset and allow it to be configured from flash memory. The pin used to hold the FPGA or SoC in reset is device dependent but two examples are INIT_b for Xilinx 7-series FPGAs or PS_POR_b for Zynq-7000 SoC devices. When configuration starts, the FPGA will search for its header in the SPI flash starting from address 0x0000. It will skip the AmP image until it finds its expected header and will load its image from the header location onwards.



Multiple AmP Devices Sharing Flash

Multiple AmP devices can share the same SPI flash memory with some additional components & manipulation of the bitstream file to make the configuration for all AmP devices appear as one continuous read from the SPI flash device.

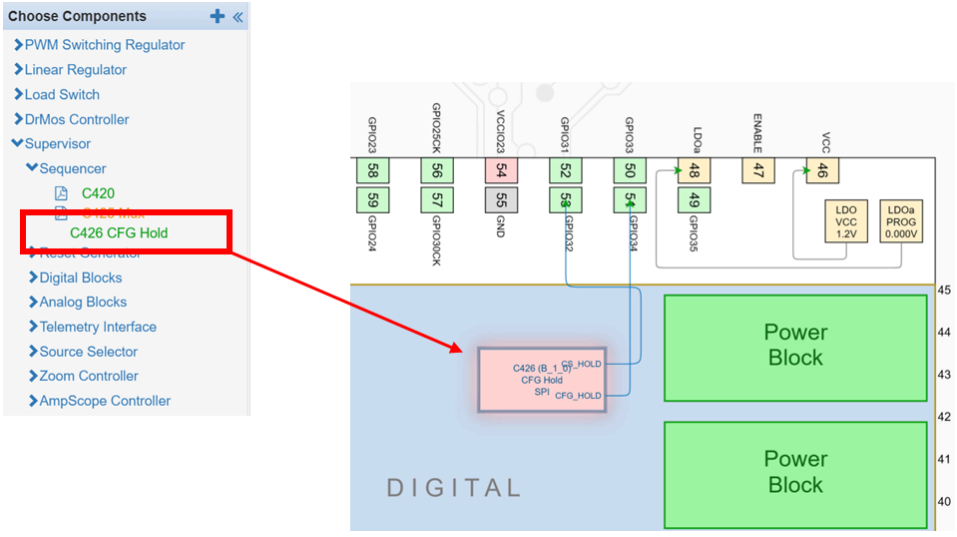
The connection diagram is as follows:



The first AmP device requires a Schottky diode to SS to prevent it driving CS high but still allow it to pull CS low.
The CS line requires an additional 1nF capacitor to slow its rise during handover from one AmP device to the next. The 2nd and subsequent AMP devices do not need to connect to the CS os MOSI lines .

Each AmP device, other than the last in the chain, requires an internal soft component, C426, which controls two GPIOs; one to hold & delay the CFG of the next AmP device and the other to hold CS. Only the 1st AMP device requires the connection to CS.

C426 component in webAMP

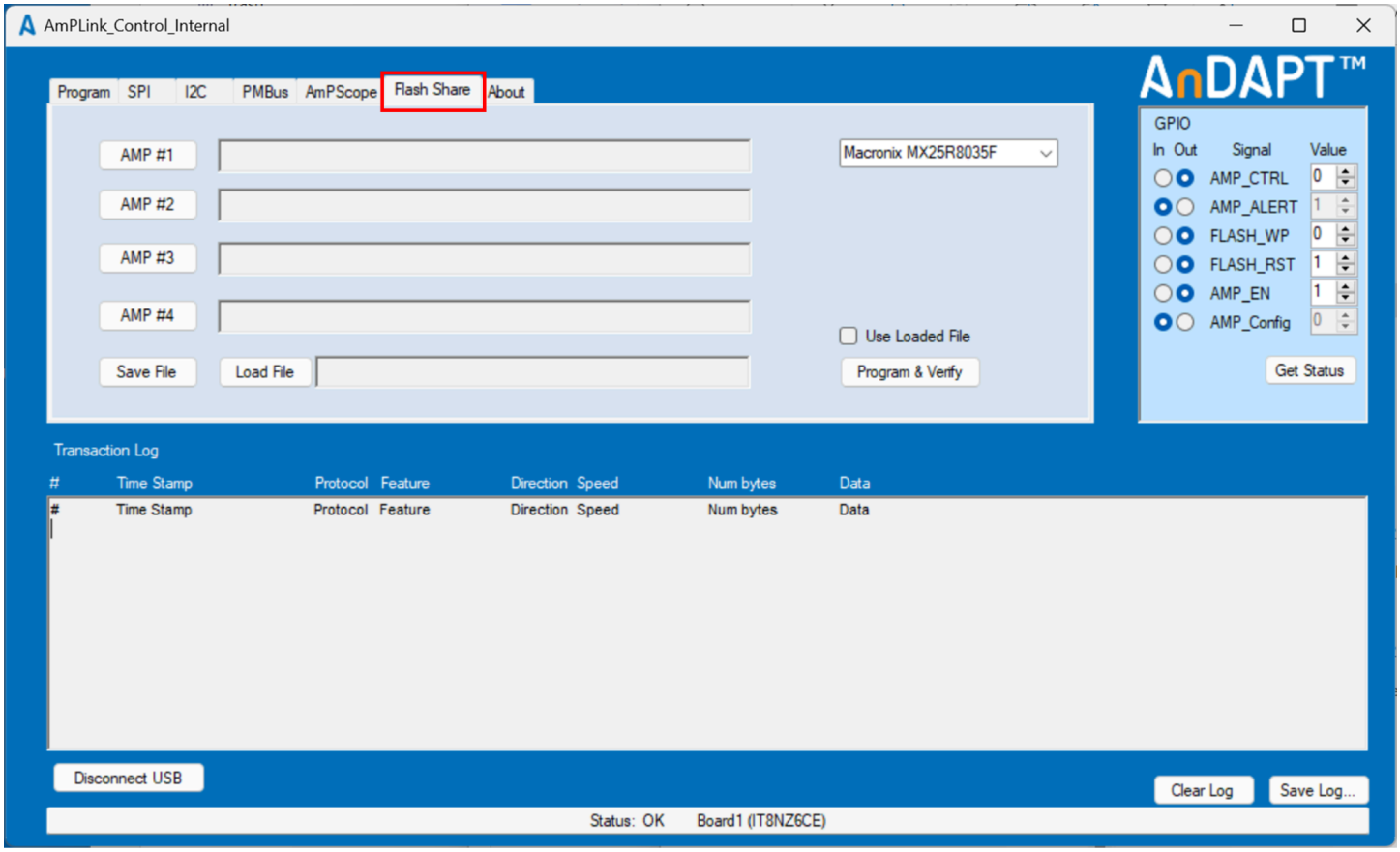


The required concatenation & manipulation of the bitstream file can be done in the AmpLink programming tool. This final bitstream contains the image for each AMP device suitably separated to make the flash read appear as one continuous transaction. See next section for details of this tool.

AmpLink tool Flash Sharing

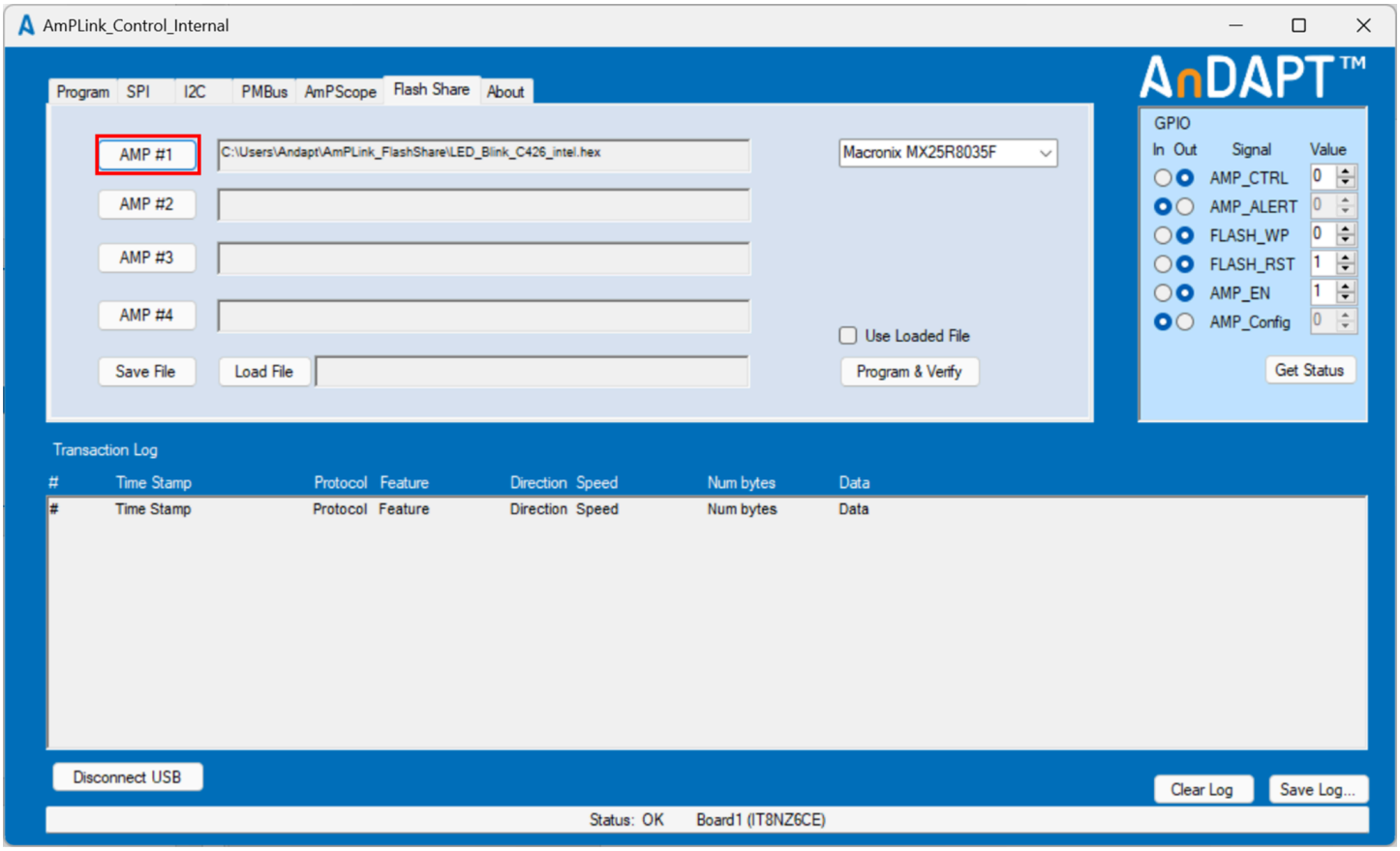
The AmpLink tool has a section for compiling flash sharing images. This allows selected AMP .hex images to be concatenated into a single flash image. The AMP images should be the intex.hex versions downloaded from the webAMP. Individual images should be added in the order that the AMP chips will be configured. Saving and SPI programming of the concatenated image can also be performed from this section.

AmplLink Flash Share tab

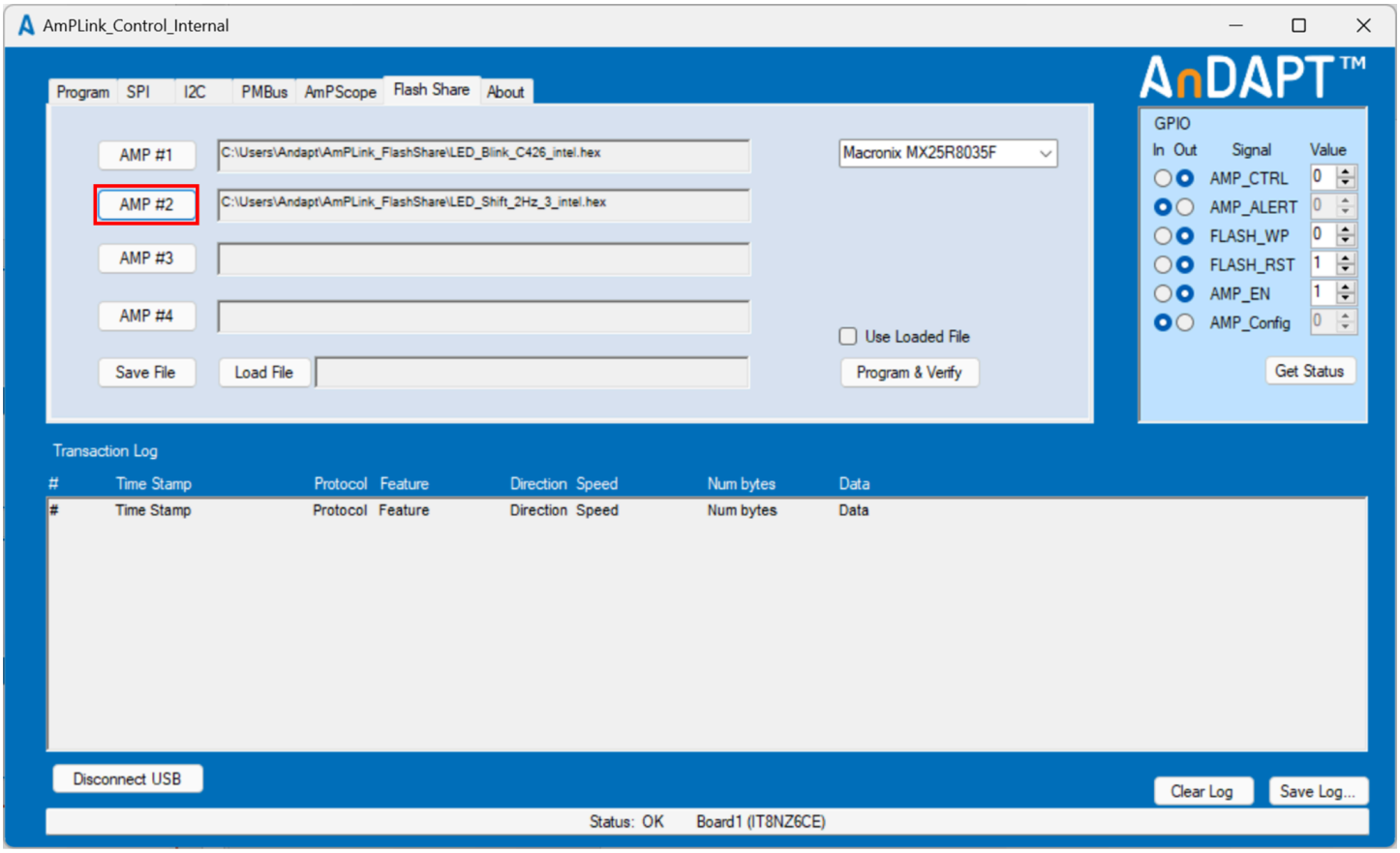


Load & program of the saved concatenated image can also be performed in the normal ‘SPI’ tab of AmpLink tool. The concatenated image is formatted as intex.hex and is compatible with most third party flash programmers.

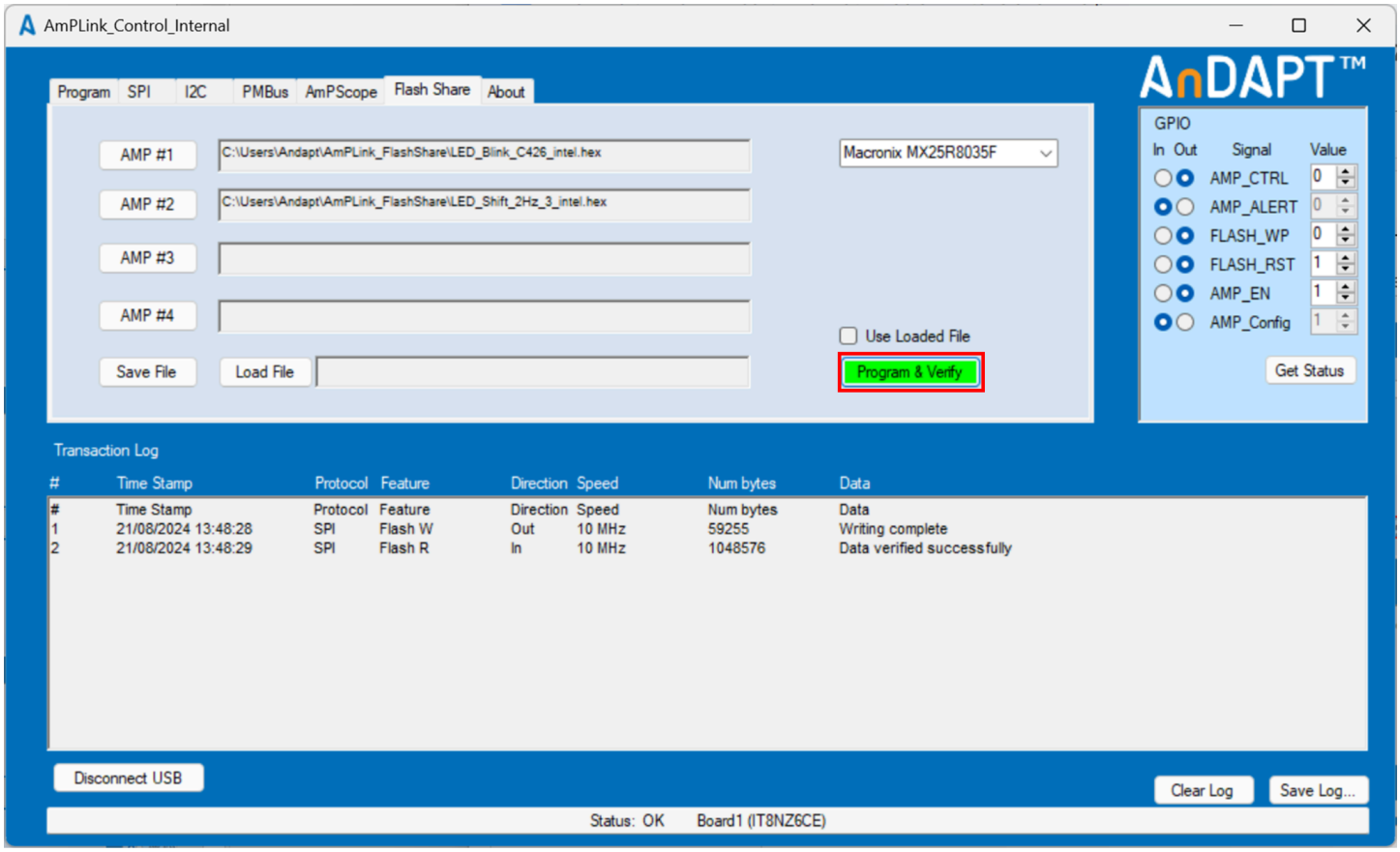
Select first AMP image.



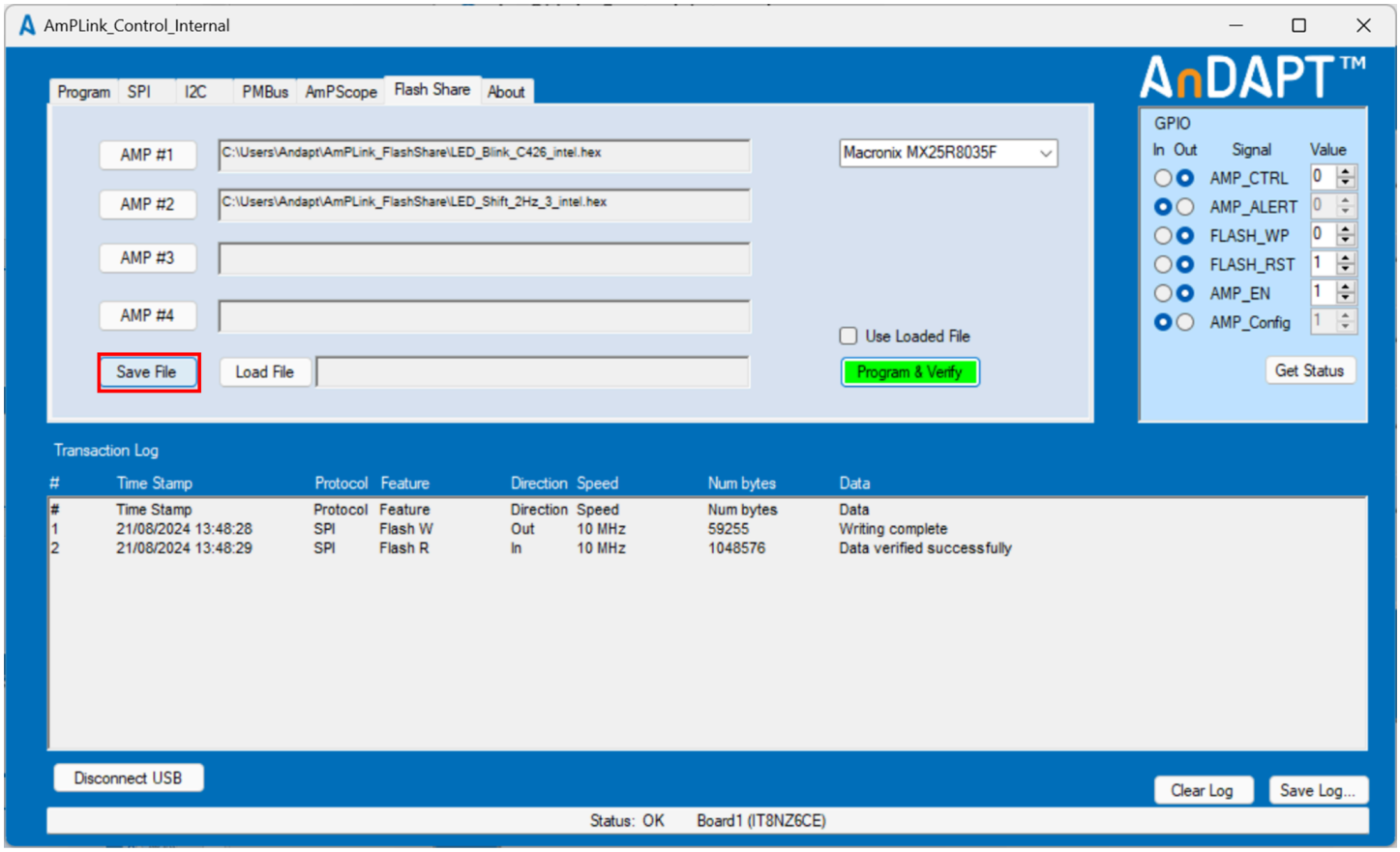
Select second AMP image (Up to 4x AMP images can be added)



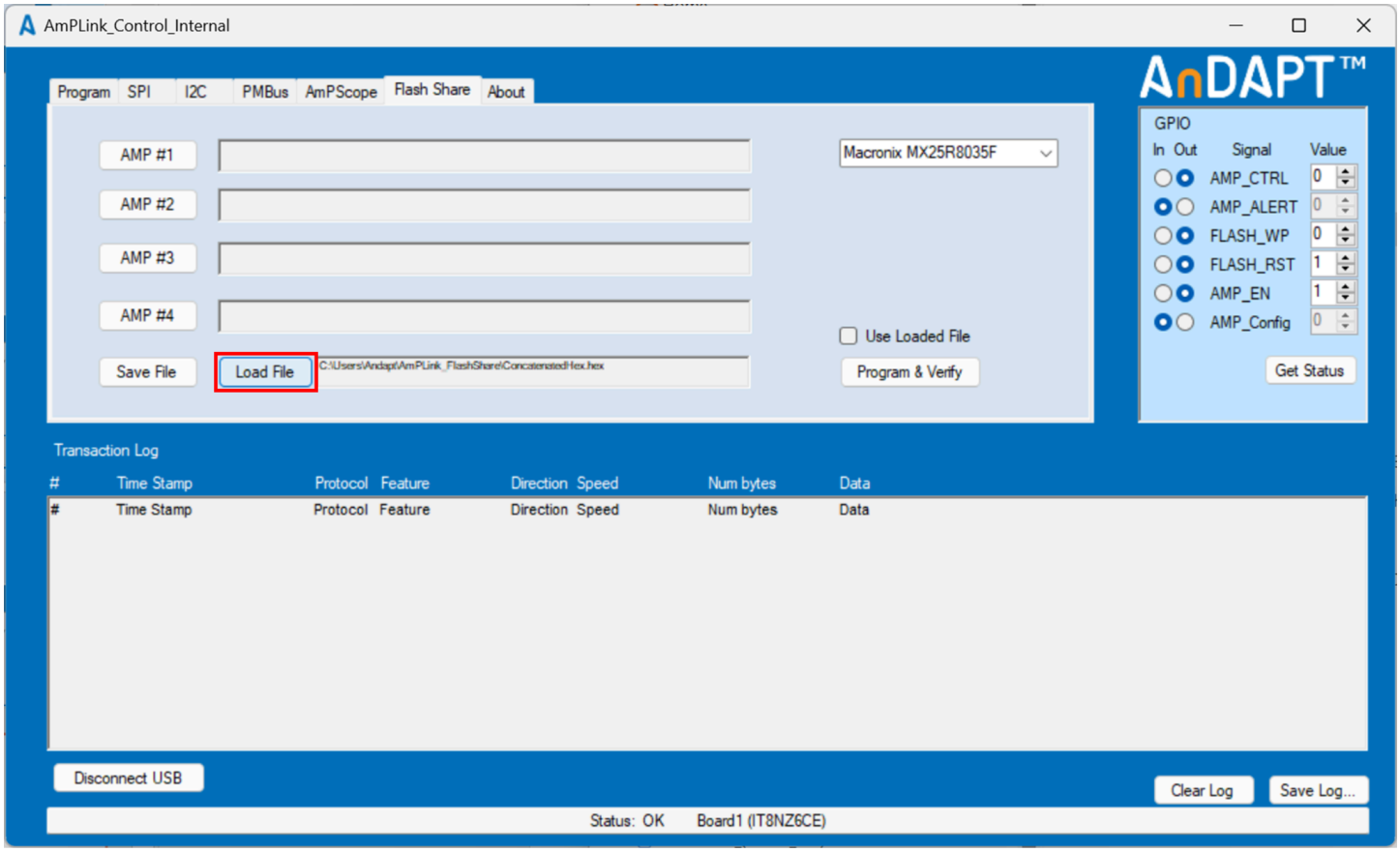
Program the concatenated flash image to a connected SPI flash device



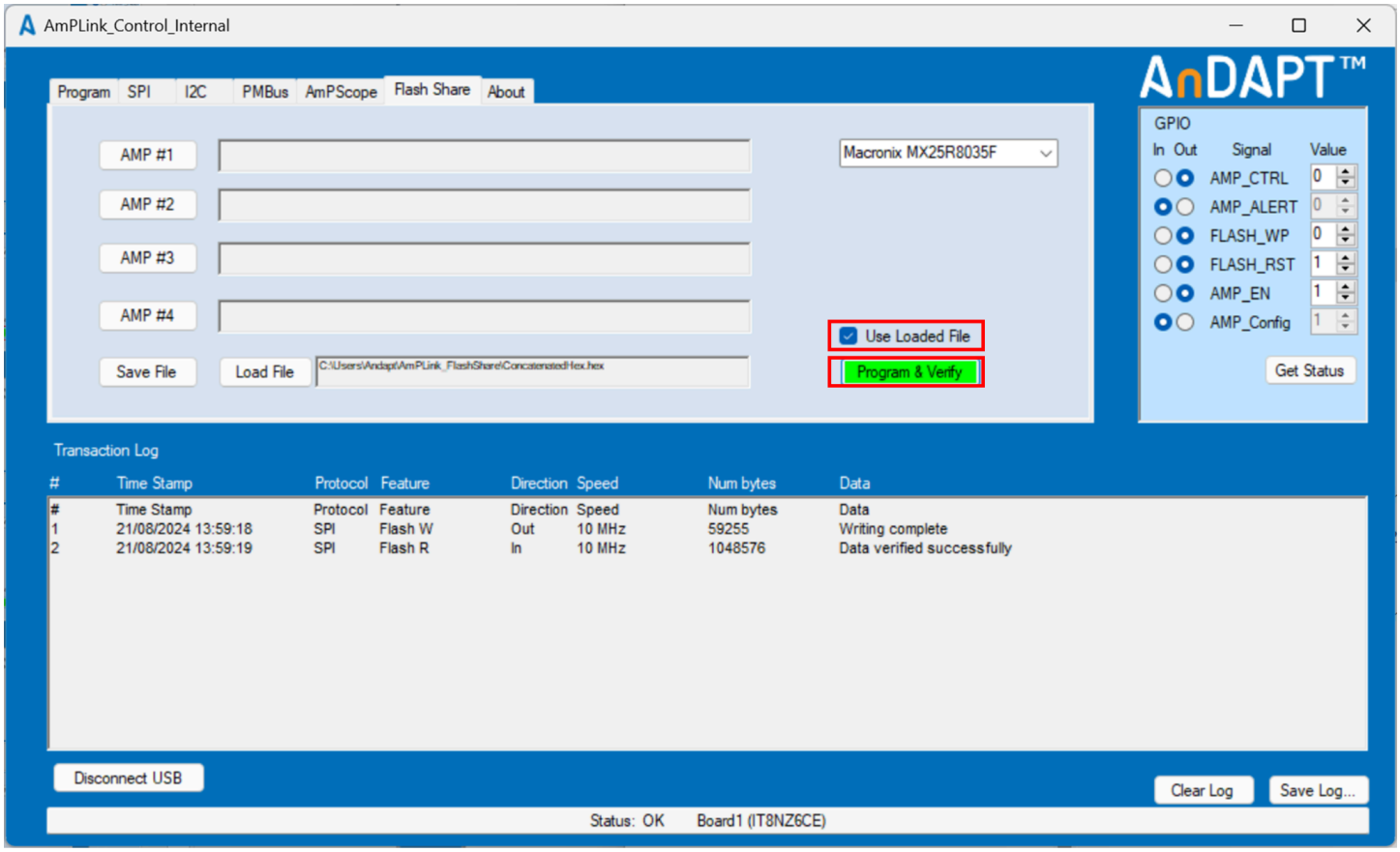
Save the concatenated flash image for programming later to more flash devices



For later programming of other flash devices: Load the flash image saved previously

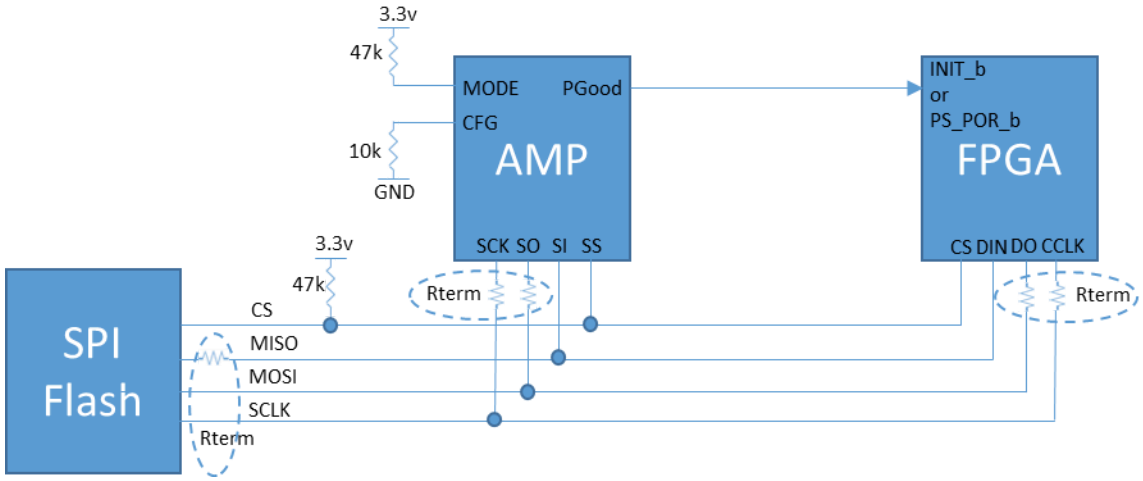


Select “Use Loaded File” and press “Program & Verify”

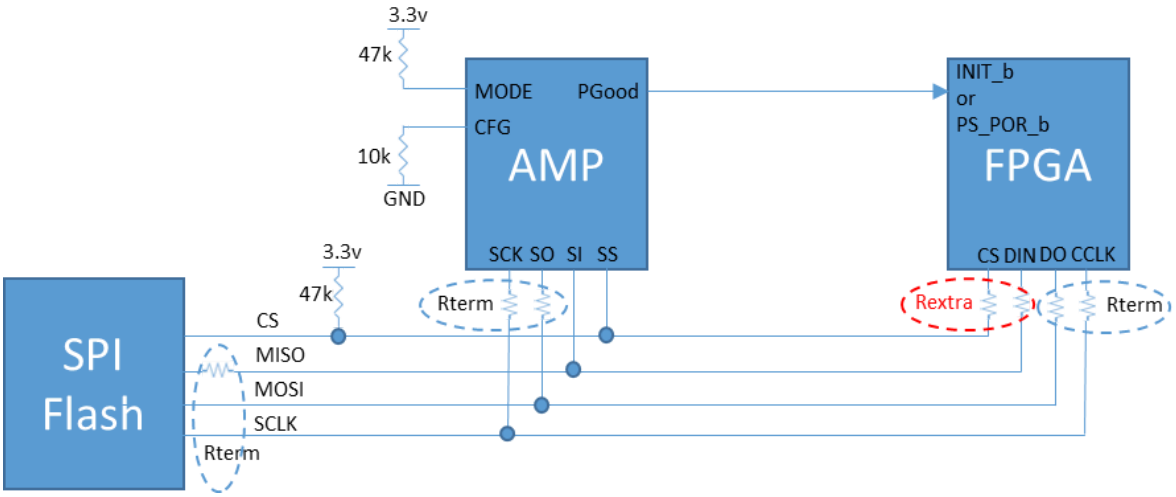


SPI Termination

It is recommended to terminate SPI bus lines to avoid ringing due to transmission line effects. There are several methods to terminate SPI, the most effective is a series resistor termination placed close to the source device. The value of this resistor depends on both the characteristic impedance of the traces and the output impedance of the driver. A typical value is 34ohms, this value may change depending on exact layout & device output drivers but is generally not critical.



Some SOC / FPGA devices can be partly powered up through active SPI lines. If this occurs the effect can be mitigated by placing extra termination resistors on all SPI lines close to the SOC / FPGA. This will ensure that any current drawn from SPI lines will result in the voltage at the pins of the SOC / FPGA being reduced and prevent it partly powering up.



Revision History

Date	Revision
8/19/2024	Added AmPLink concatenation section
8/7/2024	Updated heading, typos
07/23/2024	Updated app note number, front page content
05/16/2024	Initial version
05/30/2024	Modified diagrams with FPGA pin names Added section on termination
07/08/2024	Added C426 component & bit manipulation description

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