General Layout Guidelines

EP connection to low side FET

The package exposed pad, EP, should be directly connected to the low side FET as shown below in the AmP Platform Buck x4 Via-In-Pad (VIP) example. For no Via-In-Pad example (next page) a sufficient number of vias must be used by reducing the use of the corner GPIOs.

Switch node area minimized for high current

The switch node area must be as small as possible to handle current requirement with the, smallest possible loop area.

Trace current density.

Traces must be sufficiently wide enough to handle rated currents for switch nodes, LDOs or Load switches

Via and Via In Pad

QF65 5mm x 5mm package: Via-In-Pad (VIP) or Vias may be used. Note that all the vias being filled have better thermal performance. VIP size requires all VIPs to be filled and planarized. Example layout for a Buck x4 is shown below using using Vias and VIPs.

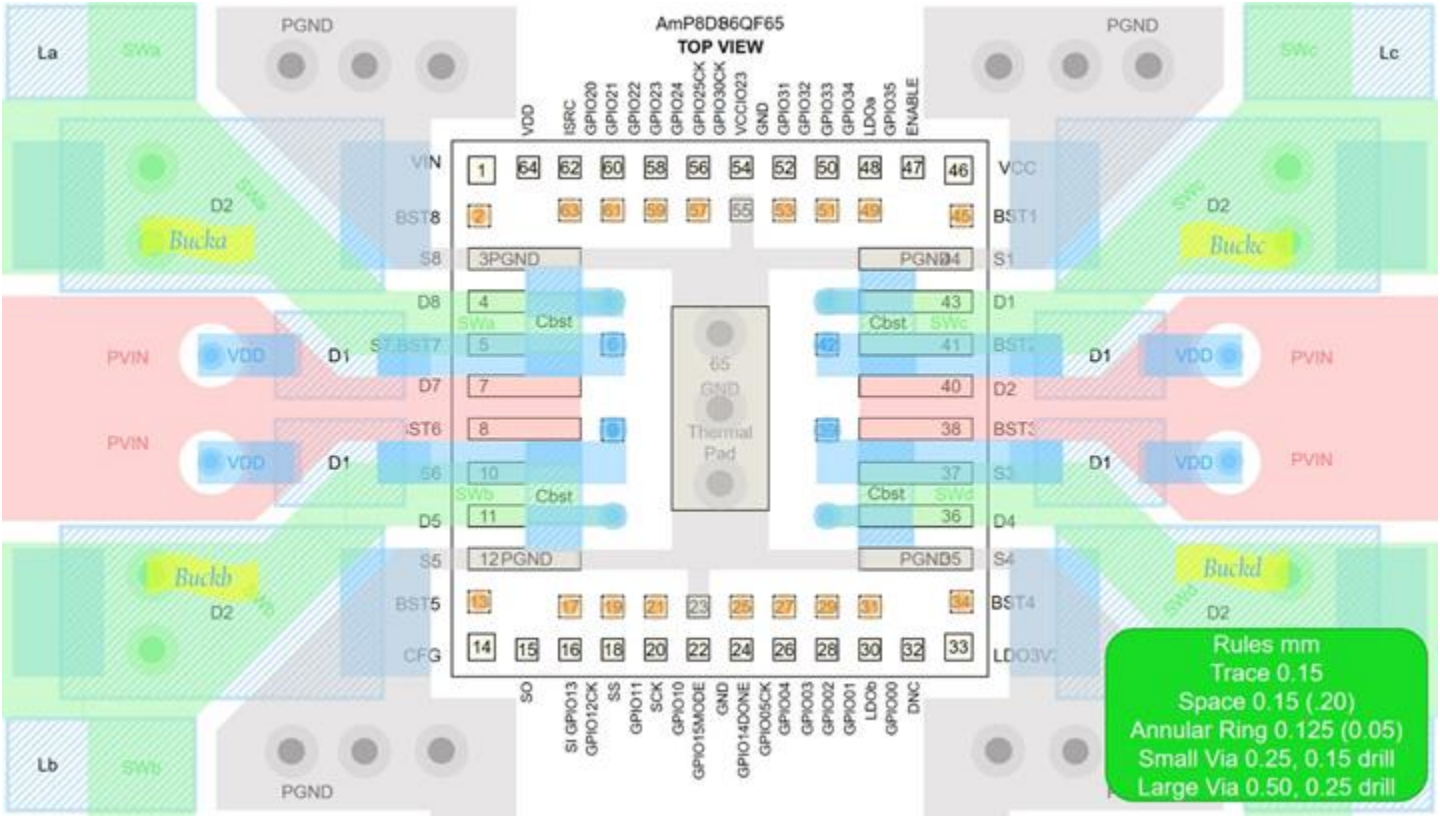
Packages

AnDAPT offers the AmP8DB6 platform in the QF65, 5mm x 5mm as shown below.

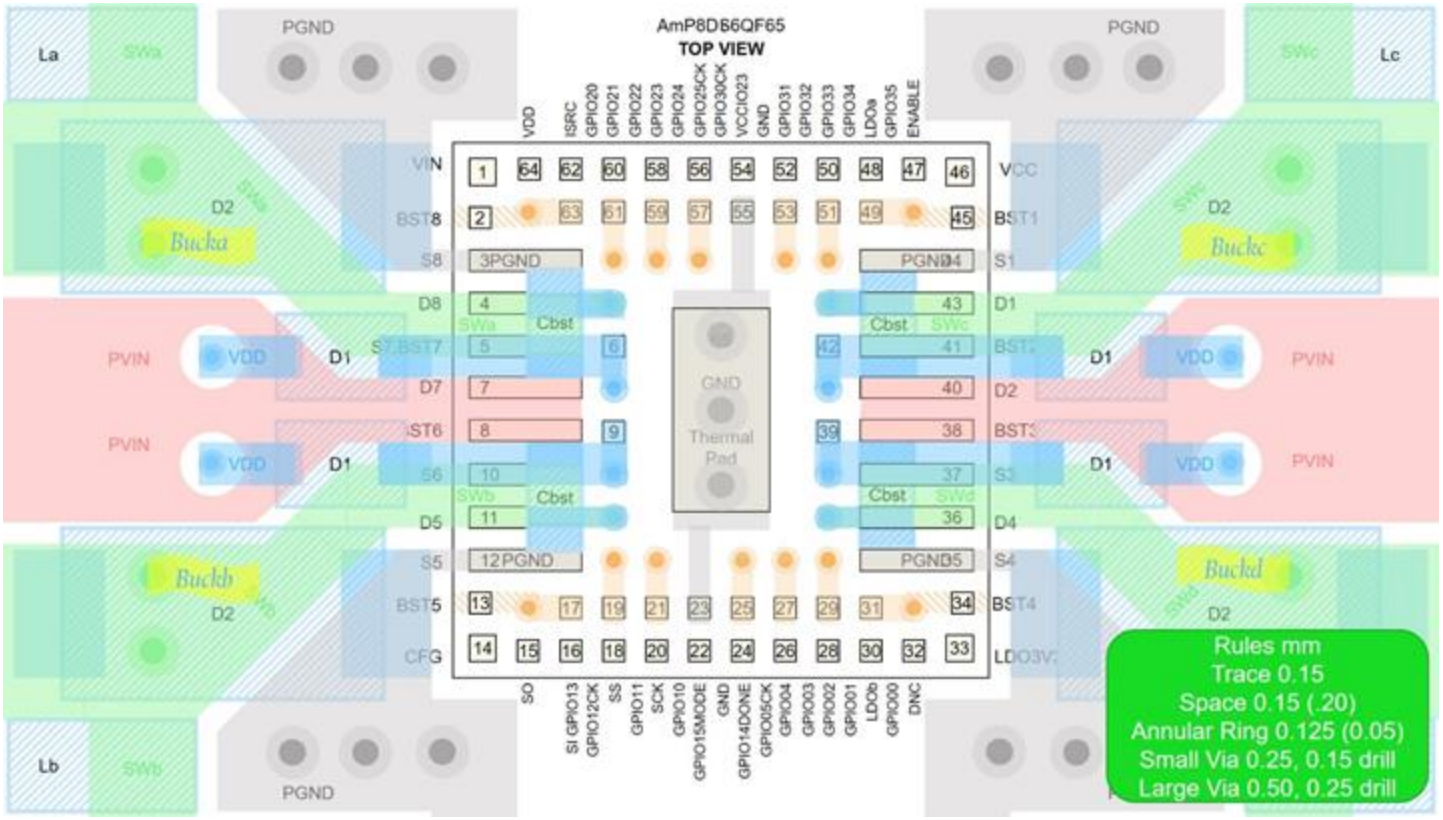
QF65 Package

For package size reduction, the package has a second row pins. The second-row pins may require via's for routing due to pad pitch.

AmP Platform Buck x4 Via-In-Pad (VIP)



AmP Platform Buck x4 no Via-In-Pad (VIP)



PCB Assembly

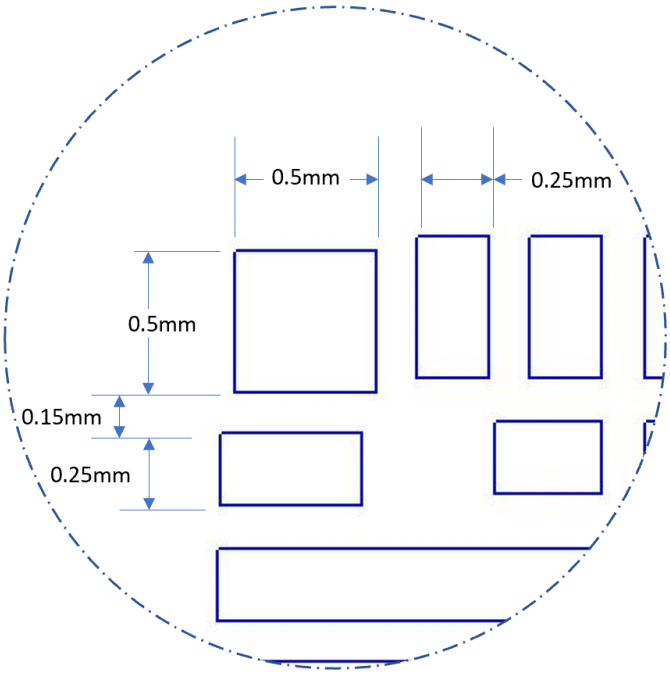
The combination of solder paste, assembly equipment, and stencil thickness is a PCB assembly house expertise and is typically proprietary to each assembly house.

Issues may include too much solder which can cause shorts or not enough solder which can cause opens. Optimizing the correct amount of solder requires adjustment of equipment speed, solder types, thickness of stencil, solder injection pressure, and stencil/PCB alignment. The combination of these parameters, together, are adjusted to maximize assemble yield.

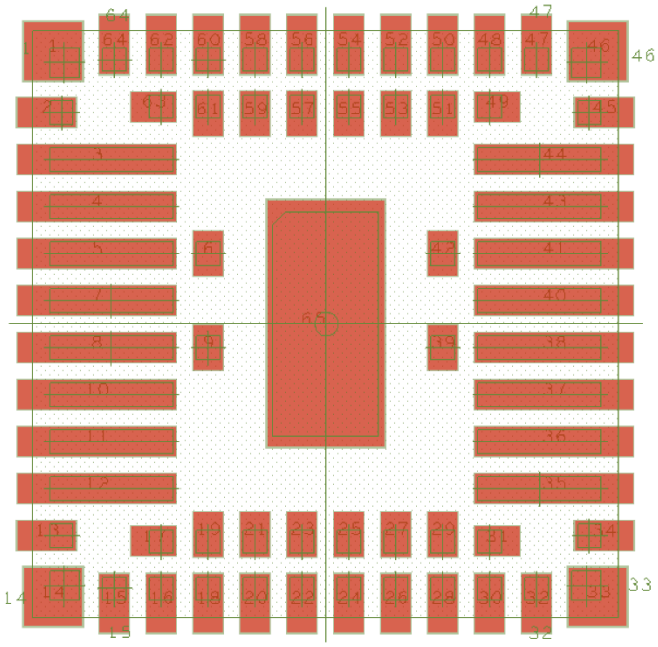
All of these variables are in assembly house control.

Recommended solder stencil design and package footprint files are shown below.

Example PCB stencil pattern detail used to make AnDAPT Evaluation Boards features 0.15 mm space and 0.25 mm trace



Example Solder Stencil Pattern for QF65 package



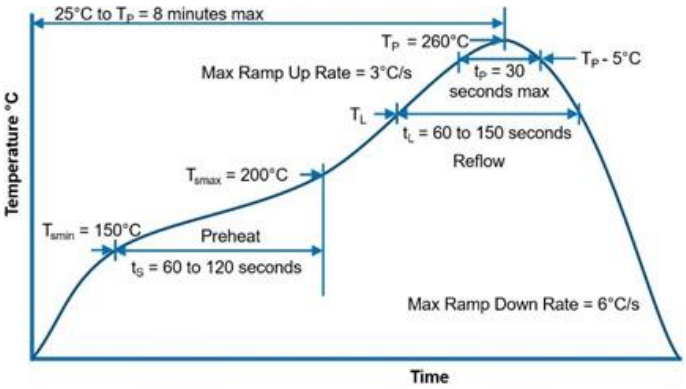
Download files: AmP8DB6QF65footprint.zip

Solder Stencils

The contrast between large thermal pad and small terminal pads of the QFN package can present a challenge in production of an even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow- solder processing. The solder joint thickness for QFN package terminal pads should be 50 – 75 μm. Stencil recommended type is laser cutting stainless steel with thickness of 100 ~ 150 μm (125 μm as a guide). The actual thickness of a stencil is depending on other SMD components on the PCB. Metal blade or polymer with 90-degree hardness squeegee is recommended. Aperture size for terminal pad should have aspect ratio (width / thickness) of greater than 1.5 and area ratio (Area of aperture opening / aperture wall area) of greater than 0.66. The stencil aperture is typically designed to match the pad size on the PCB 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. Oval-shaped opening should be used to get the optimum paste release and rounded corners to minimize clogging. Positive taper walls (5-degree tapering) with bottom opening larger than the top is recommended. The small multiple openings should be used instead of one big opening. 60% ~ 85% solder paste coverage is recommended to reduce the chance of having short connection.

REFLOW SPECIFICATION

AnDAPT products are qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder-reflow attachment phase of PCB assembly. Check solder paste data sheet for any additional or difference instruction. Using forced convection reflow oven with nitrogen is recommended. Also, the reflow oven should have equal or less than ± 5°C temperature uniformity. The reflow profile for lead-free solder paste is shown below for reference only. Solder paste datasheet should be used accordingly.



Pb Free Classification Process Reflow Profile
JEDEC-J-STD-020D.1

Environmental Compliance

AnDAPT products are RoHS and Green compliant.

AnDAPT products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC COMPLIANCE

AnDAPT products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

COMPLIANCE DECLARATION DISCLAIMER

AnDAPT believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. AnDAPT subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by AnDAPT.

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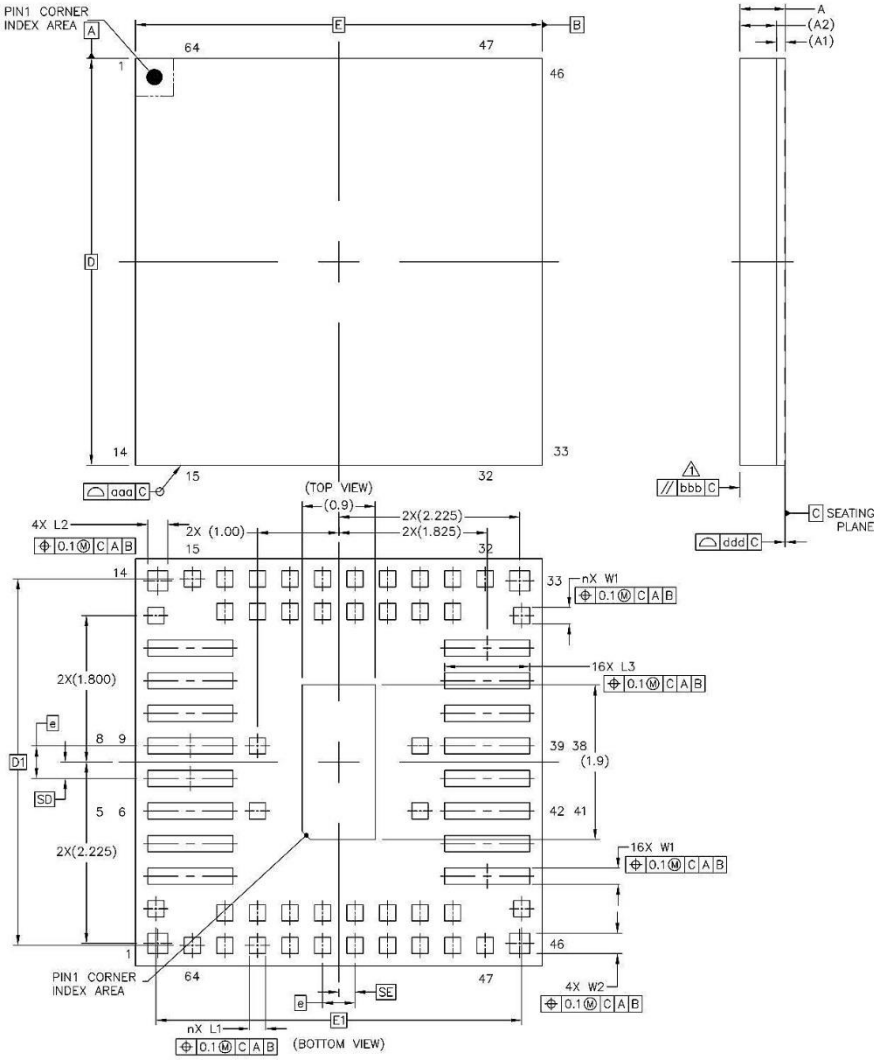
Package Description – QF65 5x5 mm

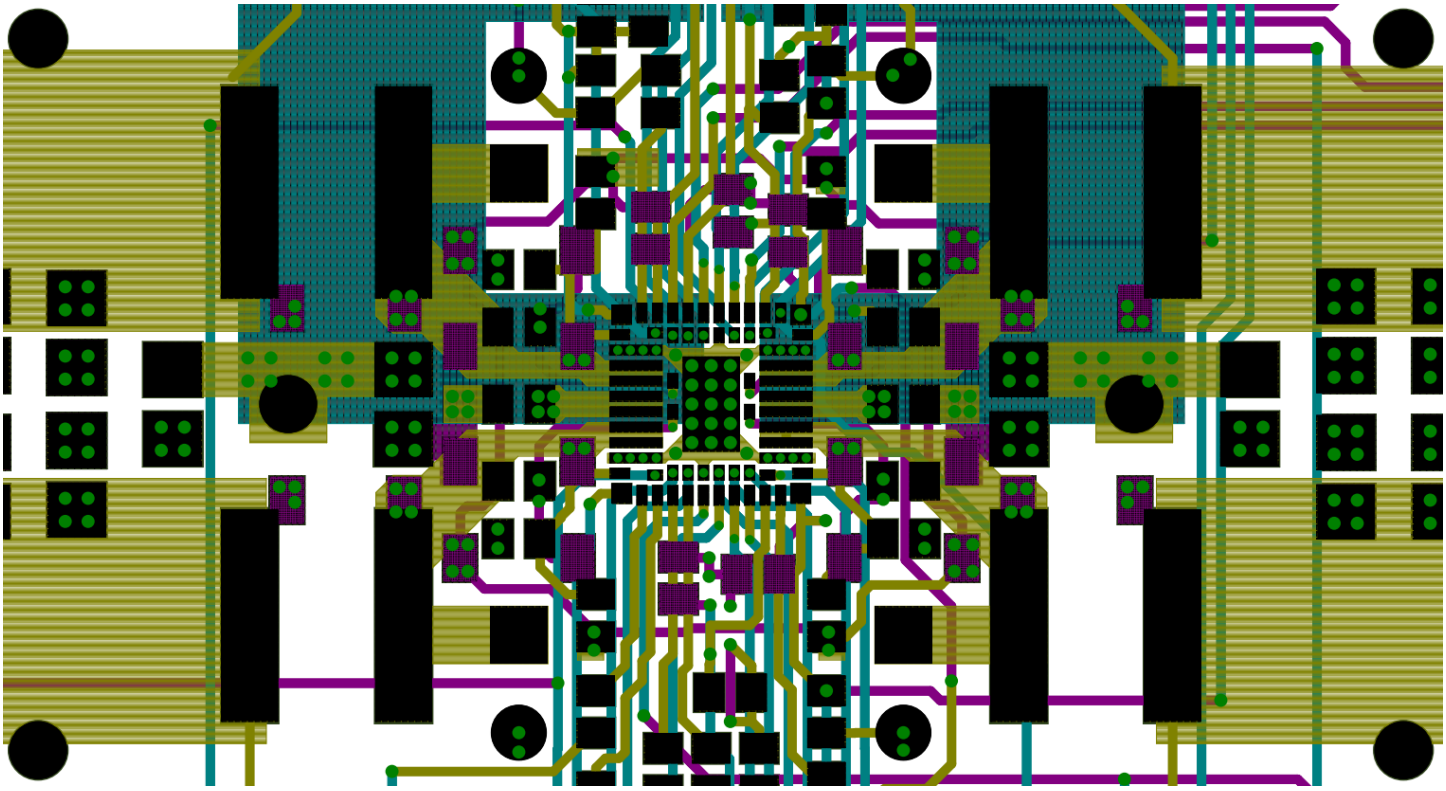


	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.65
SUBSTRATE THICKNESS	A1		0.11	REF
MOLD THICKNESS	A2		0.45	REF
BODY SIZE	D		5	
	E		5	BSC
LEAD WIDTH	W1	0.15	0.2	0.25
LEAD WIDTH	W2	0.2	0.25	0.3
LEAD LENGTH	L1	0.15	0.2	0.25
LEAD LENGTH	L2	0.2	0.25	0.3
LEAD LENGTH	L3	1	1.05	1.1
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		65	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

Download files: AmP8DB6QF65footprint.zip

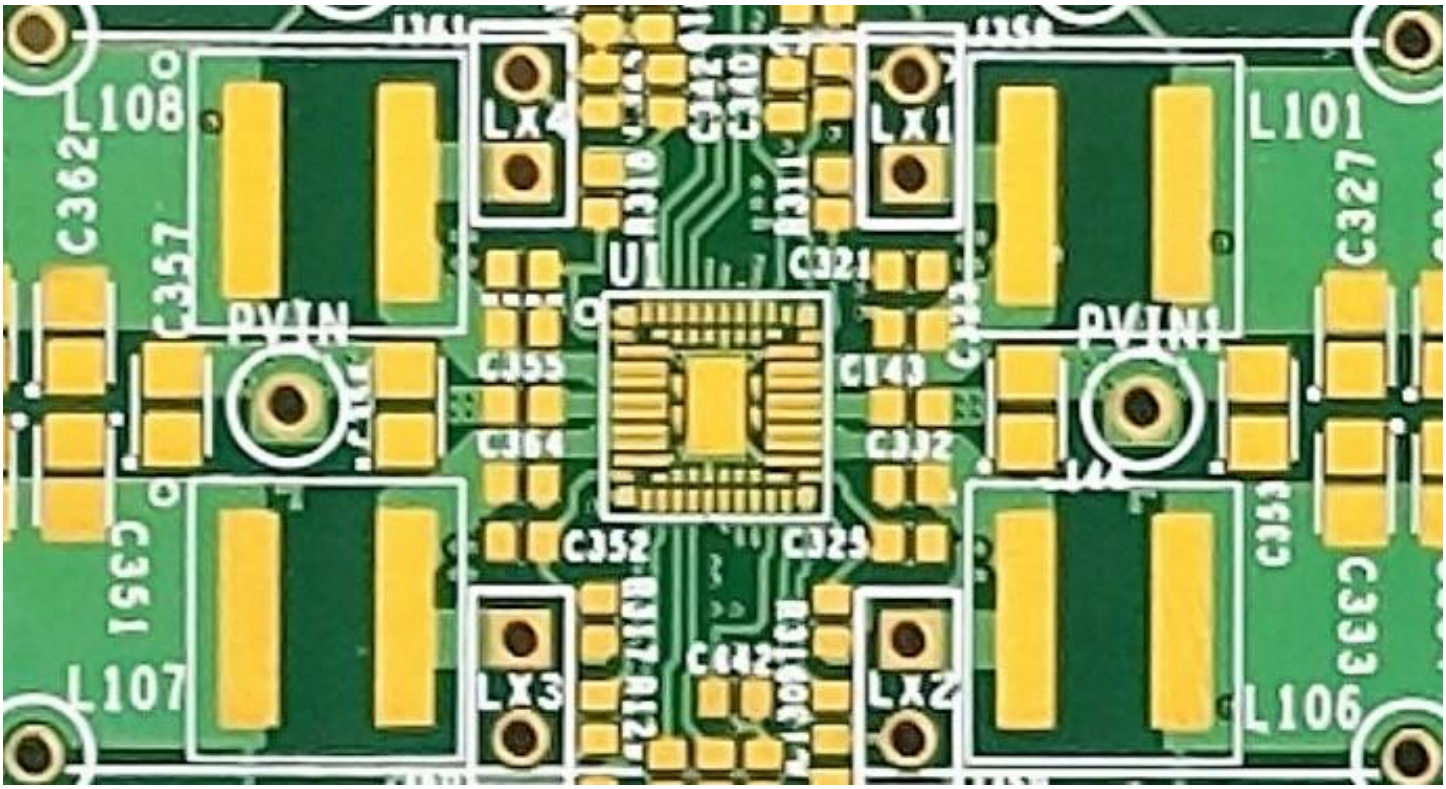
Example Cadence Allegro CAD Layout

Pitch minimum: 0.4mm, 0.25mm trace, 0.15mm space; 4 layers: top 2oz GND 1oz, power/signal 1oz, bottom 2 oz

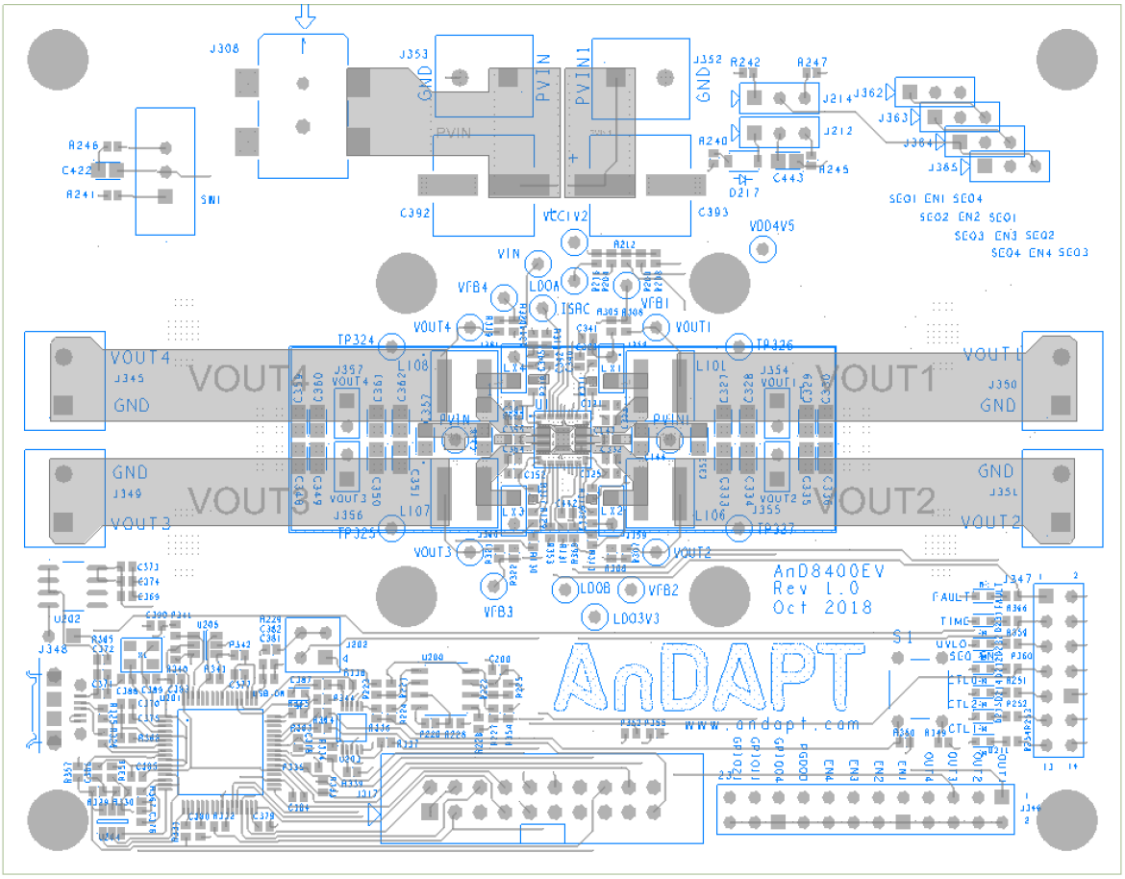


Example PCB Layout

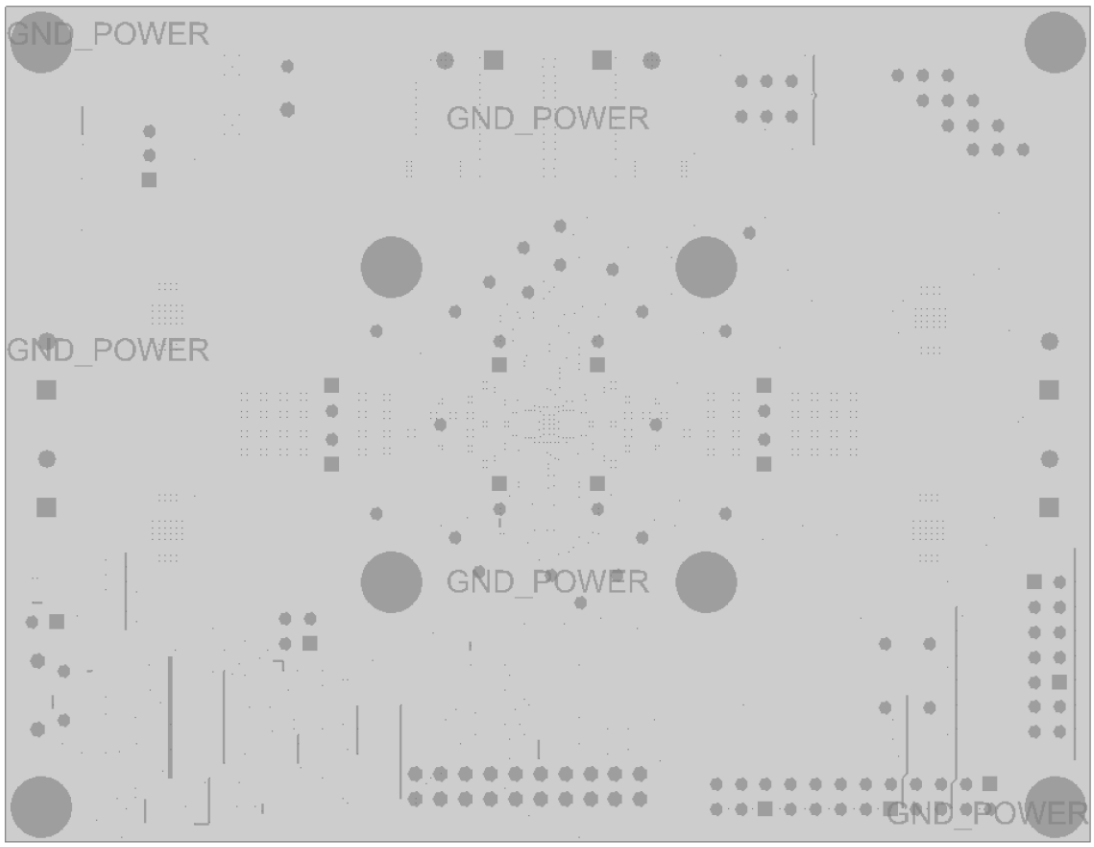
Symmetric layout: One Buck in each quadrant, AnD8400 Adaptable PMIC in center



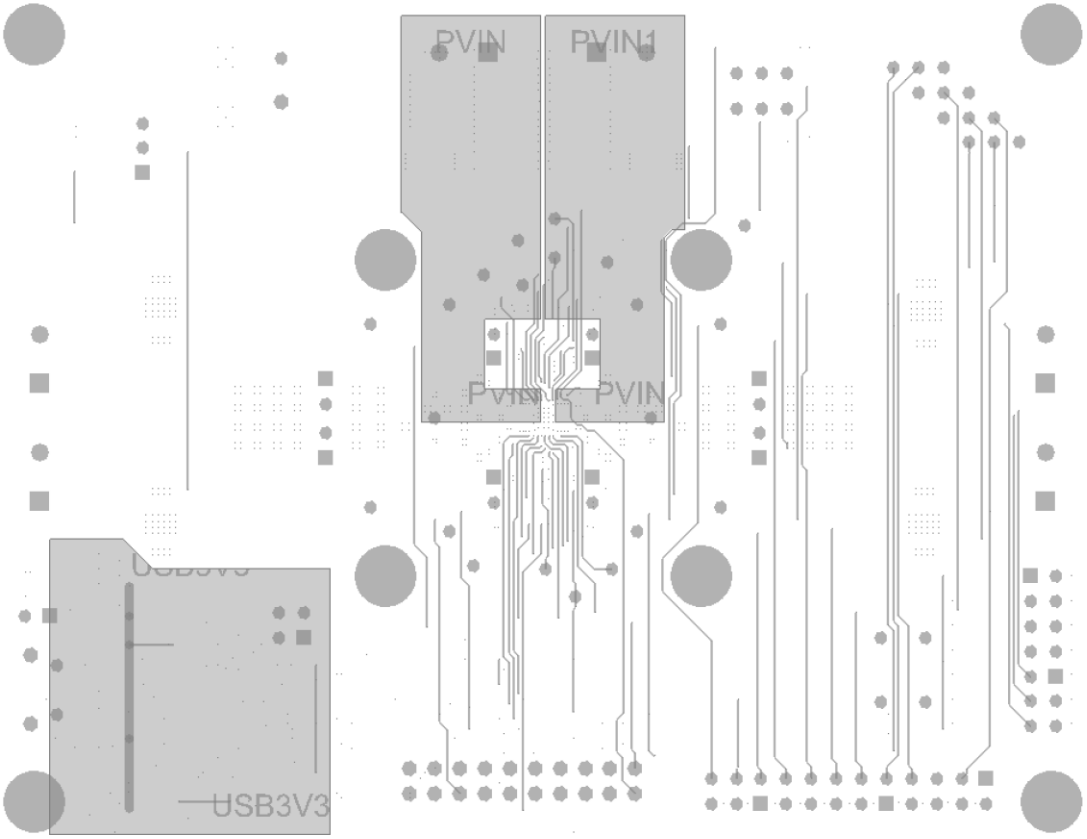
Example PCB Top Layer with Silk Screen



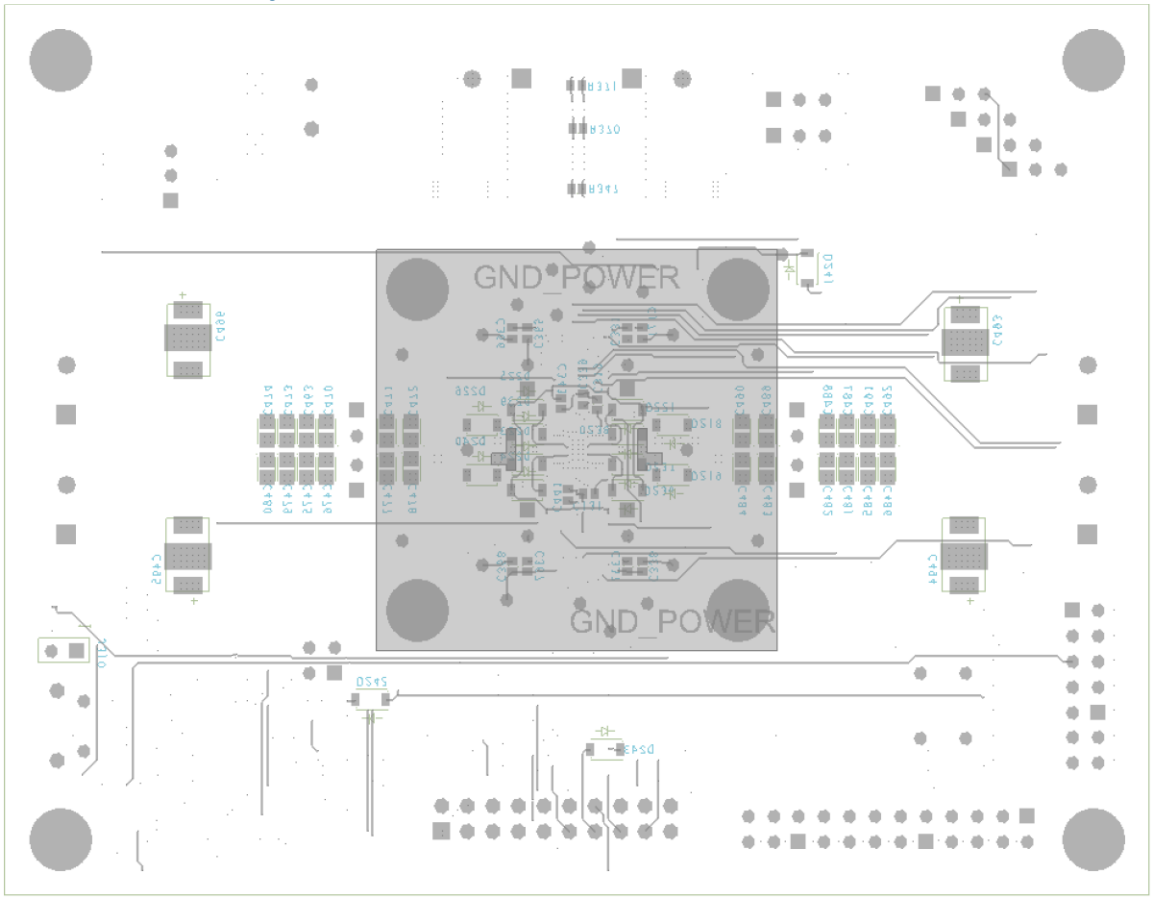
Example PCB Layer 2 GND



Example PCB Layer 3 PVIN



Example PCB Bottom Layer with Silk Screen



Revision History

Date	Revision
09/02/2021	QF74 Package removed
03/17/2021	Updated Pb Free Classification Process Reflow Profile JEDEC-J-STD-020D.1
03/14/2021	Updated QF65 to small Exposed Pad (EP) Package Description in compliance with Platform B datasheet
01/10/2020	Added Via and Via In Pad layout examples Added QF74 8mm x 8 mm layout footprint files
10/21/2019	Initial Release

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